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KSZ8091RNA/RND

10BASE-T/100BASE-TX PHY with RMII and EEE Support

Features

- Single-Chip 10BASE-T/100BASE-TX IEEE 802.3 Compliant Ethernet Transceiver
- RMII V1.2 Interface Support with a 50 MHz Reference Clock Output to MAC, and an Option to Input a 50 MHz Reference Clock
- RMII Back-to-Back Mode Support for a 100 Mbps Copper Repeater
- MDC/MDIO Management Interface for PHY Register Configuration
- Programmable Interrupt Output
- LED Outputs for Link and Activity Status Indication
- On-Chip Termination Resistors for the Differential Pairs
- Baseline Wander Correction
- HP Auto MDI/MDI-X to Reliably Detect and Correct Straight-Through and Crossover Cable Connections with Disable and Enable Option
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100 Mbps) and Duplex (Half/Full)
- Energy Efficient Ethernet (EEE) Support with Low-Power Idle (LPI) Mode for 100BASE-TX and Transmit Amplitude Reduction with 10BASE-TE Option
- Wake-on-LAN (WoL) Support with Either Magic Packet, Link Status Change, or Robust Custom-Packet Detection
- LinkMD® TDR-Based Cable Diagnostics to Identify Faulty Copper Cabling
- HBM ESD Rating (6 kV)
- Parametric NAND Tree Support for Fault Detection Between Chip I/Os and the Board
- Loopback Modes for Diagnostics
- Power-Down and Power-Saving Modes
- Single 3.3V Power Supply with V_{DD} I/O Options for 1.8V, 2.5V, or 3.3V
- Built-In 1.2V Regulator for Core
- Available in 24-Pin (4 mm × 4 mm) QFN Package

Target Applications

- Game Consoles
- IP Phones
- IP Set-Top Boxes
- IP TVs
- LOM
- Printers

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8091RNA is a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8091RNA is a highly integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core, and by offering a flexible 1.8/2.5/3.3V digital I/O interface.

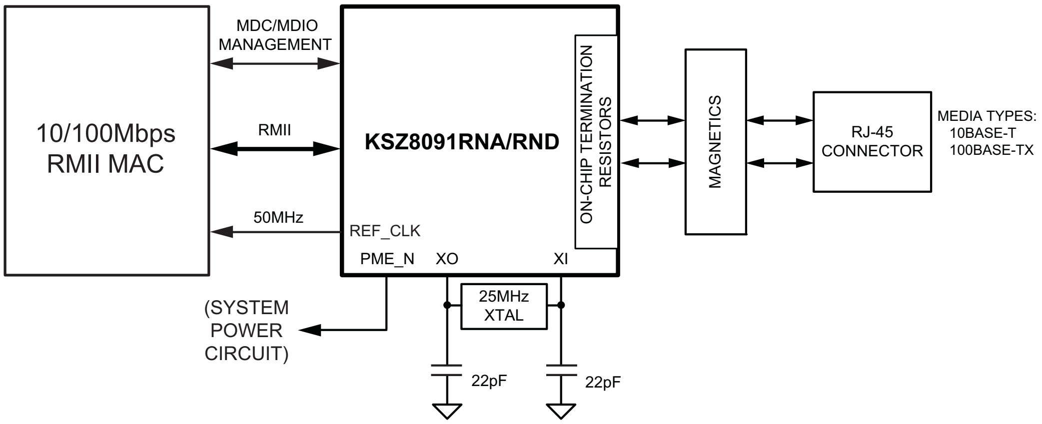
The KSZ8091RNA offers the Reduced Media Independent Interface (RMII) for direct connection with RMII-compliant Ethernet MAC processors and switches.

As the power-up default, the KSZ8091RNA uses a 25 MHz crystal to generate all required clocks, including the 50 MHz RMII reference clock output for the MAC. The KSZ8091RND takes in the 50 MHz RMII reference clock as the power-up default.

Energy Efficient Ethernet (EEE) provides further power saving during idle traffic periods and Wake-On-LAN (WOL) provides a mechanism for the KSZ8091RNA to wake up a system that is in standby power mode.

The KSZ8091RNA and KSZ8091RND are available in 24-pin, lead-free QFN packages.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 24-PIN 4 MM X 4 MM QFN ASSIGNMENT (TOP VIEW)

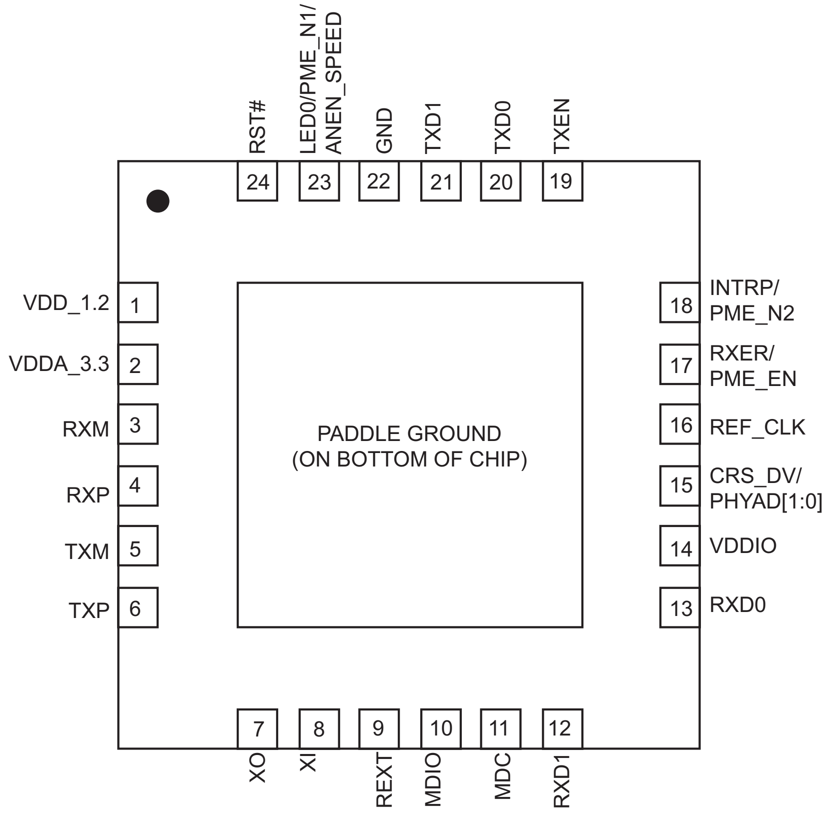


TABLE 2-1: SIGNALS - KSZ8091RNA/RND

Pin Number	Pin Name	Type Note 2-1	Description
1	VDD_1.2	P	1.2V Core V_{DD} (power supplied by KSZ8091RNA/KSZ8091RND). Decouple with 2.2 µF and 0.1 µF capacitors to ground.
2	VDDA_3.3	P	3.3V analog V_{DD}.
3	RXM	I/O	Physical receive or transmit signal (– differential).
4	RXP	I/O	Physical receive or transmit signal (+ differential).
5	TXM	I/O	Physical transmit or receive signal (– differential).
6	TXP	I/O	Physical transmit or receive signal (+ differential).
7	XO	O	Crystal Feedback for 25 MHz Crystal. This pin is a no connect if an oscillator or external clock source is used.
8	XI	I	RMII – 25 MHz Mode: 25 MHz ±50 ppm Crystal/Oscillator/External Clock Input RMII – 50 MHz Mode: 50 MHz ±50 ppm Oscillator/External Clock Input For unmanaged mode (power-up default setting), KSZ8091RNA takes in the 25 MHz crystal/clock on this pin. KSZ8091RND takes in the 50 MHz clock on this pin. After power-up, both the KSZ8091RNA and KSZ8091RND can be programmed to either the 25 MHz mode or 50 MHz mode using PHY Register 1Fh, Bit [7]. See REF_CLK (Pin 16).
9	REXT	I	Set PHY Transmit Output Current Connect a 6.49 kΩ resistor to ground on this pin.
10	MDIO	Ipu/ Opu	Management Interface (MII) Data I/O. This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor.
11	MDC	Ipu	Management Interface (MII) Clock Input. This clock pin is synchronous to the MDIO data pin.
12	RXD1	Ipd/O	RMII Receive Data Output[1] (Note 2-2).
13	RXD0	Ipu/O	RMII Receive Data Output[0] (Note 2-2).
14	VDDIO	P	3.3V, 2.5V, or 1.8V digital V_{DD}.
15	CRS_DV / PHYAD[1:0]	Ipd/O	RMII Mode: Carrier Sense/Receive Data Valid output Config Mode: The pull-up/pull-down value is latched as PHYAD[1:0] at the de-assertion of reset. See the Strap-In Options - KSZ8091RNA/RND section for details.

TABLE 2-1: SIGNALS - KSZ8091RNA/RND (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
16	REF_CLK	Ipd/O	RMII – 25 MHz Mode: This pin provides the 50 MHz RMII reference clock output to the MAC. RMII – 50 MHz Mode: This pin is a no connect. For unmanaged mode (power-up default setting): • KSZ8091RNA is in RMII – 25 MHz mode and outputs the 50 MHz RMII reference clock on this pin. • KSZ8091RND is in RMII – 50 MHz mode and does not use this pin. After power-up, both KSZ8091RNA and KSZ8091RND can be programmed to either 25 MHz mode or 50 MHz mode using PHY Register 1Fh, Bit [7]. See also XI (Pin 8).
17	RXER / PME_EN	Ipd/O	RMII Mode: RMII Receive Error Output Config Mode: The pull-up/pull-down value is latched as PME_EN at the de-assertion of reset. See the Strap-In Options - KSZ8091RNA/RND section for details.
18	INTRP/ PME_N2	Ipu/ Opu	Interrupt Output: Programmable interrupt output, with Register 1Bh as the Interrupt Control/Status register, for programming the interrupt conditions and reading the interrupt status. Register 1Fh, Bit [9] sets the interrupt output to active low (default) or active high. PME_N Output: Programmable PME_N output (pin option 2). When asserted low, this pin signals that a WOL event has occurred. This pin has a weak pull-up and is an open-drain. For Interrupt (when active low) and PME functions, this pin requires an external 1.0 kΩ pull-up resistor to V_{DDIO} (digital V_{DD}).
19	TXEN	I	RMII Transmit Enable Input
20	TXD0	I	RMII Transmit Data Input[0] (Note 2-3)
21	TXD1	I/O	RMII Mode: RMII Transmit Data Input[1] (Note 2-3) NAND Tree Mode: NAND Tree Output
22	GND	GND	Ground

TABLE 2-1: SIGNALS - KSZ8091RNA/RND (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th colspan="3">Description</th></tr>
<tr><td rowspan="12">23</td><td rowspan="12">LED0/
PME_N1/
ANEN_SPEED</td><td rowspan="12">Ipu/O</td><td colspan="3">LED Output: Programmable LED0 output
PME_N Output: Programmable PME_N Output (pin option 1). When asserted low, this pin signals that a WOL event has occurred. In this mode, this pin has a weak pull-up, is an open-drain, and requires an external 1.0 kΩ pull-up resistor to V_{DDIO} (digital V_{DD}).
Config Mode: Latched as Auto-Negotiation enable (Register 0h, Bit [12]) and Speed (Register 0h, Bit [13]) at the de-assertion of reset. See the Strapping Options section for details.
The LED0 pin is programmable using Register 1Fh, Bits [5:4], and is defined as follows:</td></tr>
<tr><td colspan="3">LED Mode = [00]</td></tr>
<tr><td>Link/Activity</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td colspan="3">LED Mode = [01]</td></tr>
<tr><td>Link/Activity</td><td>Pin State</td><td>LED Definition</td></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td colspan="3">LED Mode = [10], [11]‘ Reserved</td></tr>
<tr><td>24</td><td>RST#</td><td>Ipu</td><td colspan="3">Chip Reset (Active Low)</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>GND</td><td colspan="3">Ground</td></tr>
</table>

Note 2-1 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Electrical Characteristics for value).
Ipd = Input with internal pull-down (see Electrical Characteristics for value).
Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) and output with internal pull-up (see Electrical Characteristics for value).

Note 2-2 RMII RX Mode: The RXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.

Note 2-3 RMII TX Mode: The TXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.

2.1 Strap-In Options - KSZ8091RNA/RND

The PHYAD[1:0] and PME_EN strap-in pins are latched at the de-assertion of reset. In some systems, the RMII MAC receive input pins may drive high/low during power-up or reset, and consequently cause the PHYAD[1:0] and PME_EN strap-in pins, shared pin with the RMII CRS_DV and RXER signals respectively, to be latched to the unintended high/low state. In this case, an external pull-up (4.7 kΩ) or pull-down (1.0 kΩ) should be added on the PHYAD[1:0] and PME_EN strap-in pins to ensure that the intended value is strapped-in correctly.

TABLE 2-2: STRAP-IN OPTIONS - KSZ8091RNA/RND

Pin Number	Pin Name	Type Note 2-4	Description
15	PHYAD[1:0]	Ipd/O	The PHY Address is latched at the de-assertion of reset and is configurable to either one of the following two values: Pull-up = PHY Address is set to 00011b (3h) Pull-down (default) = PHY Address is set to 00000b (0h) PHY Address 0 is assigned by default as the broadcast PHY address, but it can be assigned as a unique PHY address after writing a ‘1’ to Register 16h, Bit [9]. PHY Address bits [4:2] are set to 000 by default.
17	PME_EN	Ipd/O	PME Output for Wake-On-LAN Pull-up = Enable Pull-down (default) = Disable At the de-assertion of reset, this pin value is latched into Register 16h, Bit [15].
23	ANEN_SPEED	Ipu/O	Auto-Negotiation Enable and Speed Mode Pull-up (default) = Enable Auto-Negotiation and set 100 Mbps Speed Pull-down = Disable Auto-Negotiation and set 10 Mbps Speed At the de-assertion of reset, this pin value is latched into Register 0h, Bit [12] for Auto-Negotiation enable/disable, Register 0h, Bit [13] for the Speed select, and Register 4h (Auto-Negotiation Advertisement) for the Speed capability support.

Note 2-4 Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8091RNA is an integrated single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8091RNA supports 10BASE-T and 100BASE-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8091RNA offers the Reduced Media Independent Interface (RMII) for direct connection with RMII-compliant Ethernet MAC processors and switches

The MII management bus option gives the MAC processor complete access to the KSZ8091RNA control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

As the power-up default, the KSZ8091RNA uses a 25 MHz crystal to generate all required clocks, including the 50 MHz RMII reference clock output for the MAC. The KSZ8091RND version uses the 50 MHz RMII reference clock as the power-up default.

The KSZ8091RNA/RND is used to refer to both KSZ8091RNA and KSZ8091RND versions in this datasheet.

3.1 10BASE-T/100BASE-TX Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII/RMII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal to NRZ format. This signal is sent through the de-scrambler, then the 4B/5B decoder. Finally, the NRZ serial data is converted to MII/RMII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The scrambler spreads the power spectrum of the transmitted signal to reduce electromagnetic interference (EMI) and baseline wander. The de-scrambler recovers the scrambled signal.

3.1.4 10BASE-T TRANSMIT

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10BASE-T signals with a typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/10BASE-Te signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV, or with short pulse widths, to prevent noise at the RXP and RXM inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8091RNA/RND decodes a data frame. The receive clock is kept active during idle periods between data receptions.

3.1.6 PLL CLOCK SYNTHESIZER

The KSZ8091RNA/RND in RMII – 25 MHz Clock mode generates all internal clocks and all external clocks for system timing from an external 25 MHz crystal, oscillator, or reference clock. For the KSZ8091RNA/RND in RMII – 50 MHz clock mode, these clocks are generated from an external 50 MHz oscillator or system clock.

3.1.7 AUTO-NEGOTIATION

The KSZ8091RNA/RND conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

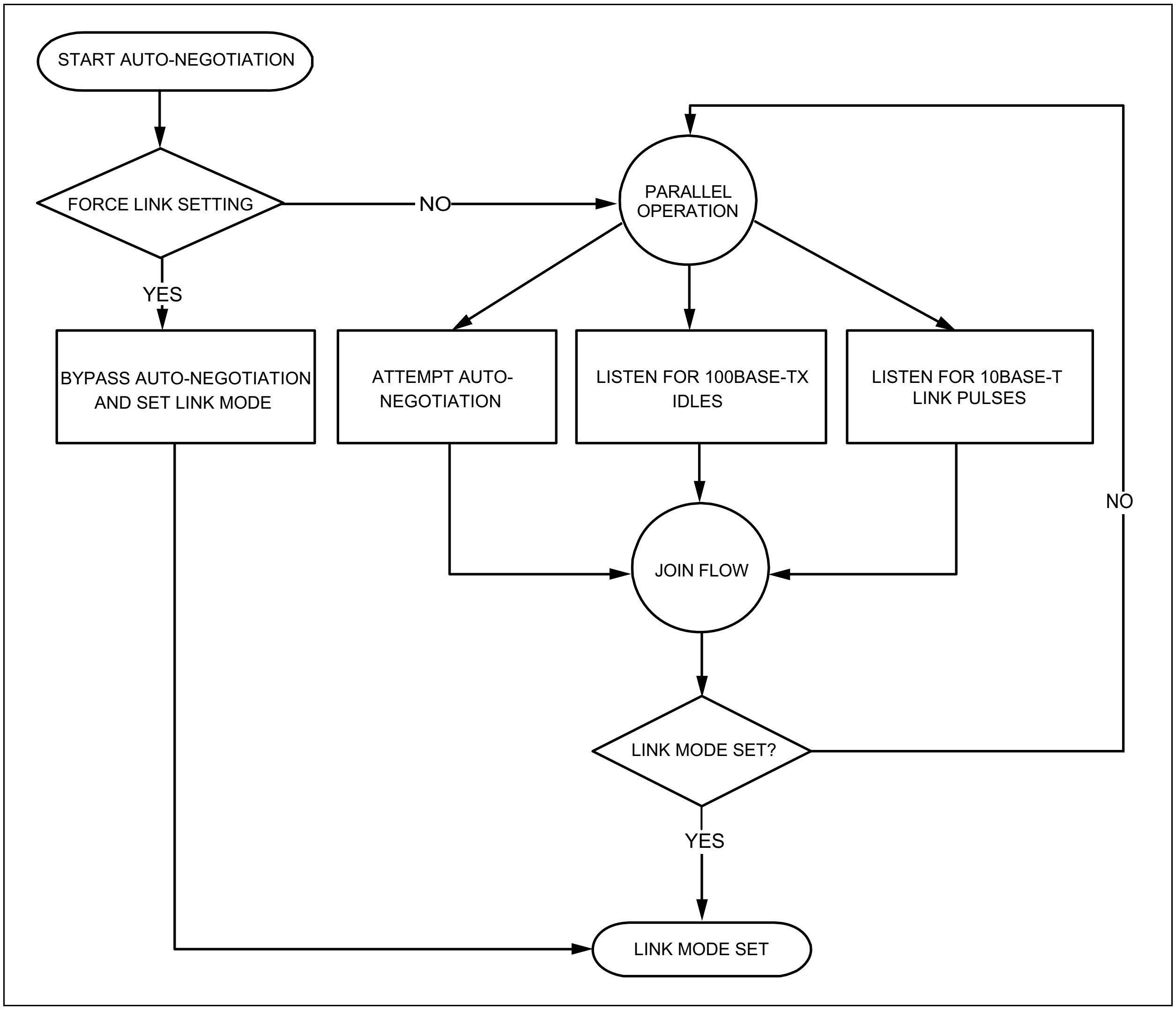
If Auto-Negotiation is not supported or the KSZ8091RNA/RND link partner is forced to bypass Auto-Negotiation, then the KSZ8091RNA/RND sets its operating mode by observing the signal at its receiver. This is known as parallel detection, which allows the KSZ8091RNA/RND to establish a link by listening for a fixed signal protocol in the absence of the Auto-Negotiation advertisement protocol.

Auto-Negotiation is enabled by either hardware pin strapping (ANEN_SPEED, Pin 23) or software (Register 0h, Bit [12]).

By default, Auto-Negotiation is enabled after power-up or hardware reset. After that, Auto-Negotiation can be enabled or disabled by Register 0h, Bit [12]. If Auto-Negotiation is disabled, the speed is set by Register 0h, Bit [13], and the duplex is set by Register 0h, Bit [8].

The auto-negotiation link-up process is shown in Figure 3-1.

FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART



3.2 RMII Data Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, and 1 pin for the 50 MHz reference clock).
- 10 Mbps and 100 Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2 bits wide, a dibit.

3.2.1 RMII SIGNAL DEFINITION

Table 3-1 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

TABLE 3-1: RMII SIGNAL DEFINITION

RMII Signal Name	Direction with Respect to PHY, KSZ8091RNA/RND Signal	Direction with Respect to MAC	Description
REF_CLK	Output (25 MHz clock mode)/ <no connect> (50 MHz clock mode)	Input/ Input or <no connect>	Synchronous 50 MHz reference clock for receive, transmit, and control interface
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data[1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data[1:0]
RXER	Output	Input, or (not required)	Receive Error

3.2.1.1 Reference Clock (REF_CLK)

REF_CLK is a continuous 50MHz clock that provides the timing reference for TXEN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

For RMII – 25 MHz Clock Mode, the KSZ8091RNA/RND generates and outputs the 50 MHz RMII REF_CLK to the MAC at REF_CLK (Pin 16).

For RMII – 50 MHz Clock Mode, the KSZ8091RNA/RND takes in the 50 MHz RMII REF_CLK from the MAC or system board at XI (Pin 8) and leaves the REF_CLK (Pin 16) as no connect.

3.2.1.2 Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting dibits on TXD[1:0] for transmission. It is asserted synchronously with the first dibit of the preamble and remains asserted while all dibits to be transmitted are presented on the RMII. It is negated before the first REF_CLK following the final dibit of a frame.

TXEN transitions synchronously with respect to REF_CLK.

3.2.1.3 Transmit Data[1:0] (TXD[1:0])

When TXEN is asserted, TXD[1:0] are the data dibits presented by the MAC and accepted by the PHY for transmission.

When TXEN is de-asserted, the MAC drives TXD[1:0] to either 00 for the idle state (non-EEE mode) or 01 for the LPI state (EEE mode).

TXD[1:0] transitions synchronously with respect to REF_CLK

3.2.1.4 Carrier Sense/Receive Data Valid (CRS_DV)

The PHY asserts CRS_DV when the receive medium is non-idle. It is asserted asynchronously when a carrier is detected. This happens when squelch is passed in 10 Mbps mode, and when two non-contiguous 0s in 10 bits are detected in 100 Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

While carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered dibit of the frame through the final recovered dibit. It is negated before the first REF_CLK that follows the final dibit. The data on RXD[1:0] is considered valid after CRS_DV is asserted. However, because the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is 00 until receive signals are properly decoded.

3.2.1.5 Receive Data[1:0] (RXD[1:0])

For each clock period in which CRS_DV is asserted, RXD[1:0] transfers a dibit of recovered data from the PHY.

When CRS_DV is de-asserted, the PHY drives RXD[1:0] to either 00 for the idle state (non-EEE mode) or 01 for the LPI state (EEE mode).

RXD[1:0] transitions synchronously with respect to REF_CLK.

3.2.1.6 Receive Error (RXER)

When CRS_DV is asserted, RXER is asserted for one or more REF_CLK periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) is detected somewhere in the frame that is being transferred from the PHY to the MAC.

RXER transitions synchronously with respect to REF_CLK.

3.2.1.7 Collision Detection (COL)

The MAC regenerates the COL signal of the MII from TXEN and CRS_DV.

3.2.2 RMII SIGNAL DIAGRAM – 25/50 MHZ CLOCK MODE

The KSZ8091RNA/RND RMII pin connections to the MAC for 25 MHz clock mode are shown in Figure 3-2. The connections for 50 MHz clock mode are shown in Figure 3-3.

3.2.2.1 RMII – 25 MHz Clock Mode

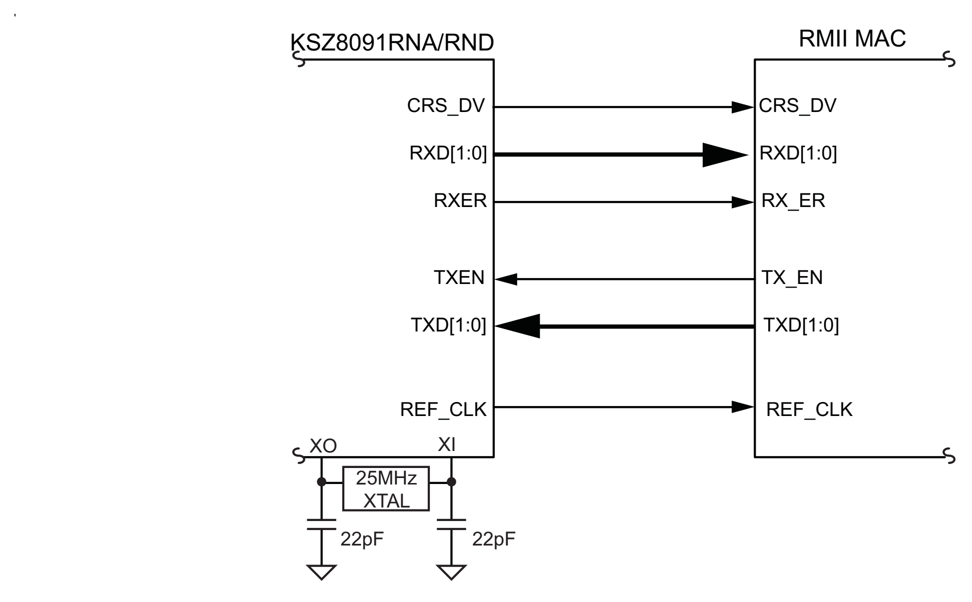
The KSZ8091RNA is configured to RMII – 25 MHz clock mode after it is powered up or hardware reset with the following:

- A 25 MHz crystal connected to XI, XO (Pins 8, 7), or an external 25 MHz clock source (oscillator) connected to XI

The KSZ8091RND can optionally be configured to RMII – 25 MHz clock mode after it is powered up or hardware reset and software programmed with the following:

- A 25 MHz crystal connected to XI, XO (Pins 8, 7), or an external 25 MHz clock source (oscillator) connected to XI
- Register 1Fh, Bit [7] programmed to ‘1’ to select RMII – 25 MHz clock mode

FIGURE 3-2: KSZ8091RNA/RND RMII INTERFACE (RMII – 25 MHZ CLOCK MODE)



3.2.2.2 RMII – 50 MHz Clock Mode

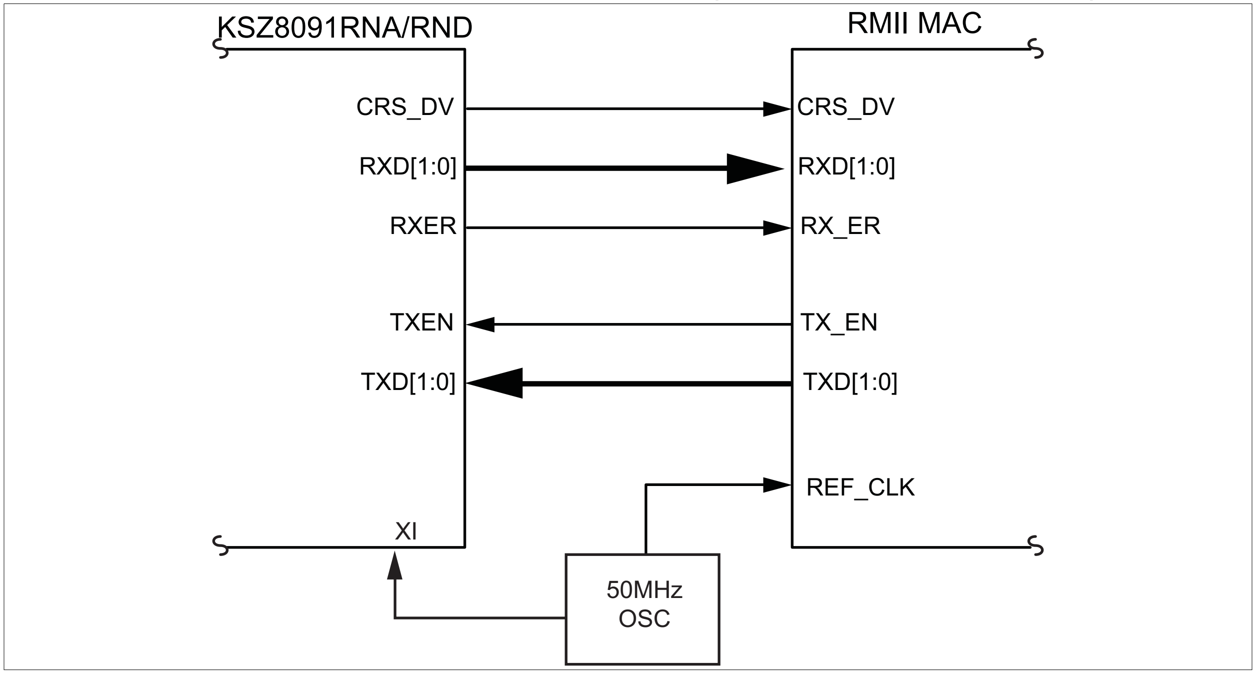
The KSZ8091RND is configured to RMII – 50 MHz clock mode after it is powered up or hardware reset with the following:

- An external 50 MHz clock source (oscillator) connected to XI (Pin 8)

The KSZ8091RNA can optionally be configured to RMII – 50 MHz clock mode after it is powered up or hardware reset and software programmed with the following:

- An external 50 MHz clock source (oscillator) connected to XI (Pin 8)
- Register 1Fh, Bit [7] programmed to ‘1’ to select RMII – 50 MHz clock mode

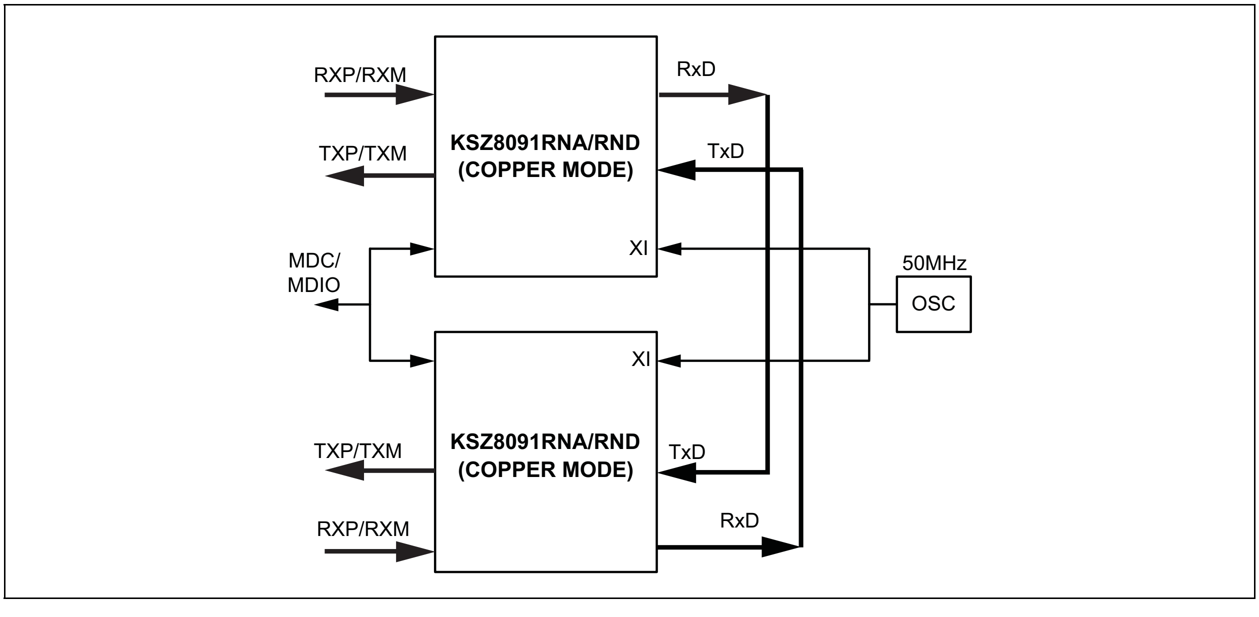
FIGURE 3-3: KSZ8091RNA/RND RMII INTERFACE (RMII – 50 MHZ CLOCK MODE)



3.3 Back-to-Back Mode – 100 Mbps Copper Repeater

Two KSZ8091RNA/RND devices can be connected back-to-back to form a 100BASE-TX copper repeater.

FIGURE 3-4: KSZ8091RNA/RND TO KSZ8091RNA/RND BACK-TO-BACK COPPER REPEATER



3.3.1 RMII BACK-TO-BACK MODE

In RMII back-to-back mode, a KSZ8091RNA/RND interfaces with another KSZ8091RNA/RND to provide a complete 100 Mbps copper repeater solution.

The KSZ8091RNA/RND devices are configured to RMII back-to-back mode after power-up or reset, and software programming, with the following:

- A common 50 MHz reference clock connected to XI (Pin 8) of both KSZ8091RNA/RND devices.
- Register 1Fh, Bit [7] programmed to ‘1’ to select RMII – 50 MHz clock mode for KSZ8091RNA. (KSZ8091RND is set to RMII – 50 MHz clock mode as the default after power up or hardware reset).
- Register 16h, Bits [6] and [1] programmed to ‘1’ and ‘1’, respectively, to enable RMII back-to-back mode.
- RMII signals connected as shown in Table 3-2.

TABLE 3-2: RMII SIGNAL CONNECTION FOR RMII BACK-TO-BACK MODE (100 BASE-TX COPPER REPEATER)

KSZ8091RNA/RND (100BASE-TX Copper) [Device 1]			KSZ8091RNA/RND (100BASE-TX Copper) [Device 2]		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
CRSDV	15	Output	TXEN	19	Input
RXD1	12	Output	TXD1	21	Input
RXD0	13	Output	TXD0	20	Input
TXEN	19	Input	CRSDV	15	Output
TXD1	21	Input	RXD1	12	Output
TXD0	20	Input	RXD0	13	Output

3.4 MII Management (MIIM) Interface

The KSZ8091RNA/RND supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows an upper-layer device, such as a MAC processor, to monitor and control the state of the KSZ8091RNA/RND. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows the external controller to communicate with one or more PHY devices.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers. See the Register Descriptions section.

The KSZ8091RNA/RND supports only two unique PHY addresses. The PHYAD[1:0] strapping pin is used to select either 0h or 3h as the unique PHY address for the KSZ8091RNA/RND device.

PHY Address 0h is defined as the broadcast PHY address according to the IEEE 802.3 Specification, and can be used to read/write to a single PHY device, or write to multiple PHY devices simultaneously. For the KSZ8091RNA/RND, PHY Address 0h defaults to the broadcast PHY address after power-up, but PHY Address 0h can be disabled as the broadcast PHY address using software to assign it as a unique PHY address.

For applications that require two KSZ8091RNA/RND PHYs to share the same MDIO interface with one PHY set to Address 0h and the other PHY set to Address 3h, use PHY Address 0h (defaults to broadcast after power-up) to set both PHYs’ Register 16h, Bit [9] to ‘1’ to assign PHY Address 0h as a unique (non-broadcast) PHY address.

The MIIM interface can operates up to a maximum clock speed of 10 MHz MAC clock.

Table 3-3 shows the MII management frame format for the KSZ8091RNA/RND.

TABLE 3-3: MII MANAGEMENT FRAME FORMAT FOR THE KSZ8091RNA/RND

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	000AA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	000AA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.5 Interrupt (INTRP)

INTRP (Pin 18) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8091RNA/RND PHY register. Bits [15:8] of Register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Bits [7:0] of Register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [9] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8091RNA/RND control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

3.6 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the need to decide whether to use a straight cable or a crossover cable between the KSZ8091RNA/RND and its link partner. This feature allows the KSZ8091RNA/RND to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and assigns transmit and receive pairs to the KSZ8091RNA/RND accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a '1' to Register 1Fh, bit [13]. MDI and MDI-X mode is selected by Register 1Fh, bit [14] if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 3-4 shows how the IEEE 802.3 Standard defines MDI and MDI-X.

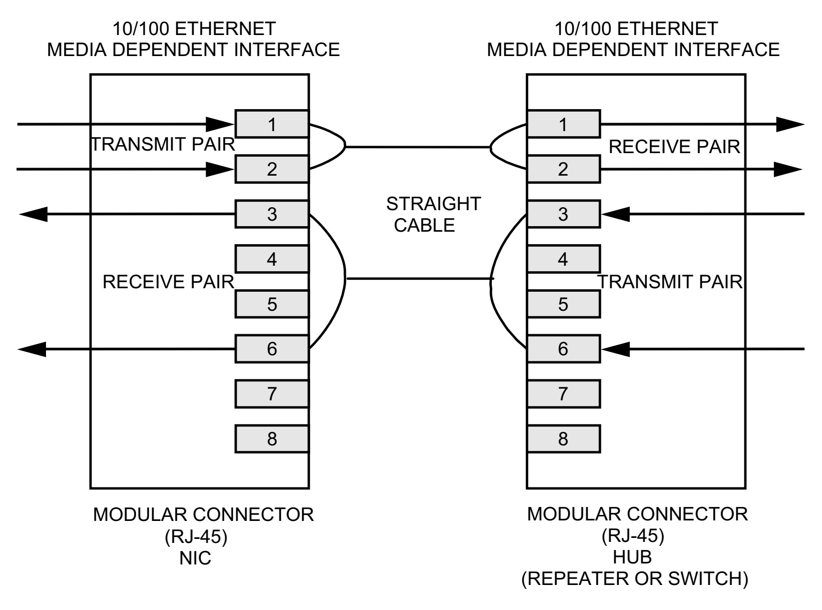
TABLE 3-4: MDI/MDI-X PIN DESCRIPTION

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TX+	1	RX+
2	TX–	2	RX–
3	RX+	3	TX+
6	RX–	6	TX–

3.6.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-5 shows a typical straight cable connection between a NIC card (MDI device) and a switch or hub (MDI-X device).

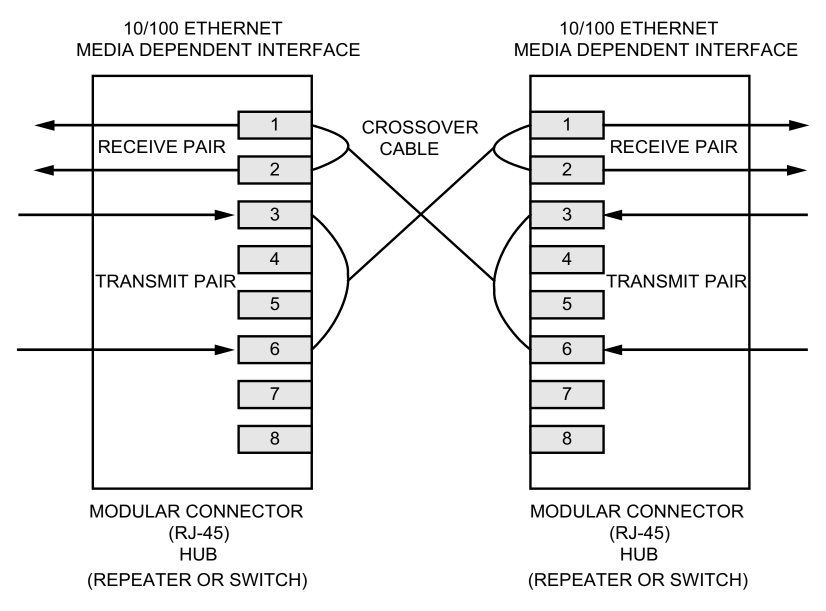
FIGURE 3-5: TYPICAL STRAIGHT CABLE CONNECTION



3.6.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-6 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-6: TYPICAL CROSSOVER CABLE CONNECTION



3.7 Loopback Mode

The KSZ8091RNA/RND supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

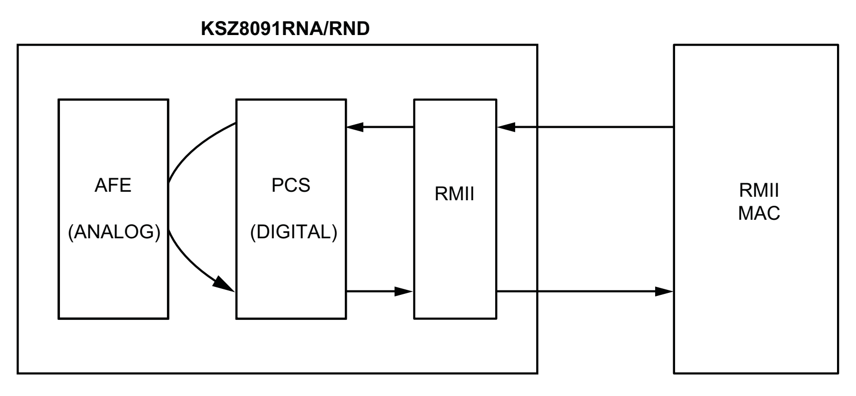
3.7.1 LOCAL (DIGITAL) LOOPBACK

This loopback mode checks the MII/RMII transmit and receive data paths between the KSZ8091RNA/RND and the external MAC, and is supported for both speeds (10/100 Mbps) at full-duplex.

The loopback data path is shown in Figure 3-7.

1. The MII/RMII MAC transmits frames to the KSZ8091RNA/RND.
2. Frames are wrapped around inside the KSZ8091RNA/RND.
3. The KSZ8091RNA/RND transmits frames back to the MII/RMII MAC.
4. Except the frames back to the RMII MAC, the transmit frames also go out from the copper port.

FIGURE 3-7: LOCAL (DIGITAL) LOOPBACK



The following programming action and register settings are used for local loopback mode:

For 10/100 Mbps loopback:

Set Register 0h,

Bit [14] = 1 // Enable local loopback mode

Bit [13] = 0/1 // Select 10 Mbps/100 Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

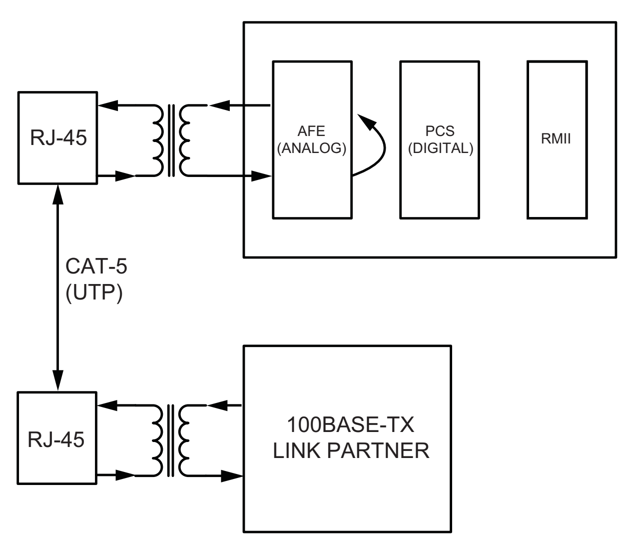
3.7.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ8091RNA/RND and its link partner, and is supported for 100BASE-TX full-duplex mode only.

The loopback data path is shown in Figure 3-8.

1. The Fast Ethernet (100BASE-TX) PHY link partner transmits frames to the KSZ8091RNA/RND.
2. Frames are wrapped around inside the KSZ8091RNA/RND.
3. The KSZ8091RNA/RND transmits frames back to the Fast Ethernet (100BASE-TX) PHY link partner.

FIGURE 3-8: REMOTE (ANALOG) LOOPBACK



The following programming steps and register settings are used for remote loopback mode:

1. Set Register 0h,L

Bits [13] = 1 // Select 100 Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

Orjustauto-negotiateandlinkupat100BASE-TXfull-duplexmodewiththelinkpartner.

2. Set Register 1Fh,

Bit [2] = 1 // Enable remote loopback mode

3.8 LinkMD® Cable Diagnostic

The LinkMD function uses time-domain reflectometry (TDR) to analyze the cabling plant for common cabling problems. These include open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing register 1Dh, the LinkMD Cable Diagnostic register, in conjunction with Register 1Fh, the PHY Control 2 Register. The latter register is used to disable Auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

3.8.1 USAGE

The following is a sample procedure for using LinkMD with Registers 1Dh and 1Fh:

1. Disable auto MDI/MDI-X by writing a ‘1’ to Register 1Fh, bit [13].
2. Start cable diagnostic test by writing a ‘1’ to Register 1Dh, bit [15]. This enable bit is self-clearing.
3. Wait (poll) for Register 1Dh, bit [15] to return a ‘0’, and indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in Register 1Dh, bits [14:13]. The results are as follows:

00 = normal condition (valid test)

01 = open condition detected in cable (valid test)

10 = short condition detected in cable (valid test)

11 = cable diagnostic test failed (invalid test)

The ‘11’ case, invalid test, occurs when the device is unable to shut down the link partner. In this instance, the test is not run because it would be impossible for the device to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating Register 1Dh, bits [8:0] and multiplying the result by a constant of 0.38. The distance to the cable fault can be determined by the following formula:

EQUATION 3-1:

$$D(\text{Distance to cable fault in meters}) = 0.38 \times (\text{Register 1Dh, bits[8:0]})$$

D (distance to cable fault) is expressed in meters.

Concatenated value of Registers 1Dh bits [8:0] should be converted to decimal before multiplying by 0.38.

The constant (0.38) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.9 NAND Tree Support

The KSZ8091RNA/RND provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8091RNA/RND digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the TXD1 pin provides the output for the nested NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving each NAND tree input pin low, sequentially, according to the NAND tree pin order
- Checking the NAND tree output to make sure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 3-5 list the NAND tree pin order for KSZ8091RNA/RND.

TABLE 3-5: NAND TREE TEST PIN ORDER FOR KSZ8091RNA/RND

Pin Number	Pin Name	NAND Tree Description
10	MDIO	Input
11	MDC	Input
12	RXD1	Input
13	RXD0	Input
15	CRS_DV	Input
16	REF_CLK	Input
18	INTRP	Input
19	TXEN	Input
23	LED0	Input
20	TXD0	Input
21	TXD1	Output

3.9.1 NAND TREE I/O TESTING

Use the following procedure to check for faults on the KSZ8091RNA/RND digital I/O pin connections to the board:

1. Enable NAND tree mode by setting Register 16h, Bit [5] to ‘1’.
2. Use board logic to drive all KSZ8091RNA/RND NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, in KSZ8091RNA/RND NAND tree pin order, as follows:
    a) Toggle the first pin (MDIO) from high to low, and verify that the TXD1 pin switches from high to low to indicate that the first pin is connected properly.
    b) Leave the first pin (MDIO) low.
    c) Toggle the second pin (MDC) from high to low, and verify that the TXD1 pin switches from low to high to indicate that the second pin is connected properly.
    d) Leave the first pin (MDIO) and the second pin (MDC) low.
    e) Toggle the third pin (RXD1) from high to low, and verify that the TXD1 pin switches from high to low to indicate that the third pin is connected properly.
    f) Continue with this sequence until all KSZ8091RNA/RND NAND tree input pins have been toggled.

Each KSZ8091RNA/RND NAND tree input pin must cause the TXD1 output pin to toggle high-to-low or low-to-high to indicate a good connection. If the TXD1 pin fails to toggle when the KSZ8091RNA/RND input pin toggles from high to low, the input pin has a fault.

3.10 Power Management

The KSZ8091RNA/RND incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

3.10.1 POWER-SAVING MODE

Power-saving mode is used to reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a ‘1’ to Register 1Fh, Bit [10], and is in effect when Auto-Negotiation mode is enabled and the cable is disconnected (no link).

In this mode, the KSZ8091RNA/RND shuts down all transceiver blocks, except for the transmitter, energy detect, and PLL circuits.

By default, power-saving mode is disabled after power-up.

3.10.2 ENERGY-DETECT POWER-DOWN MODE

Energy-detect power-down (EDPD) mode is used to further reduce transceiver power consumption when the cable is unplugged. It is enabled by writing a ‘0’ to Register 18h, Bit [11], and is in effect when Auto-Negotiation mode is enabled and the cable is disconnected (no link).

EDPD mode works with the PLL off (set by writing a ‘1’ to Register 10h, Bit [4] to automatically turn the PLL off in EDPD mode) to turn off all KSZ8091RNA/RND transceiver blocks except the transmitter and energy-detect circuits.

Power can be reduced further by extending the time interval between transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the KSZ8091RNA/RND and its link partner, when operating in the same low-power state and with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them.

By default, EDPD mode is disabled after power-up.

3.10.3 POWER-DOWN MODE

Power-down mode is used to power down the KSZ8091RNA/RND device when it is not in use after power-up. It is enabled by writing a ‘1’ to Register 0h, Bit [11].

In this mode, the KSZ8091RNA/RND disables all internal functions except the MII management interface. The KSZ8091RNA/RND exits (disables) power-down mode after Register 0h, Bit [11] is set back to ‘0’.

3.10.4 SLOW-OSCILLATOR MODE

Slow-oscillator mode is used to disconnect the input reference crystal/clock on XI (Pin 8) and select the on-chip slow oscillator when the KSZ8091RNA/RND device is not in use after power-up. It is enabled by writing a ‘1’ to Register 11h, Bit [5].

Slow-oscillator mode works in conjunction with power-down mode to put the KSZ8091RNA/RND device in the lowest power state, with all internal functions disabled except the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1. Disable slow-oscillator mode by writing a ‘0’ to Register 11h, Bit [5].
2. Disable power-down mode by writing a ‘0’ to Register 0h, Bit [11].
3. Initiate software reset by writing a ‘1’ to Register 0h, Bit [15].

3.11 Energy Efficient Ethernet (EEE)

The KSZ8091RNA/RND implements Energy Efficient Ethernet (EEE) as described in the IEEE Standard 802.3az for 100BASE-TX copper signaling by the two differential pairs (analog side) and according to the multi-source agreement (MSA) of collaborating Fast Ethernet chip vendors for the RMII (digital side). The MSA agreement is based on the IEEE Standard’s EEE implementation for the 100 Mbps Media Independent Interface (MII). The IEEE Standard is defined around an EEE-compliant MAC on the host side and an EEE-compliant link partner on the line side that support special signaling associated with EEE. EEE saves power by keeping the AC signal on the copper Ethernet cable at approximately 0V peak-to-peak as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as low-power idle (LPI) mode or state.

During LPI mode, the copper link responds automatically when it receives traffic and resumes normal PHY operation immediately, without blockage of traffic or loss of packet. This involves exiting LPI mode and returning to normal 100 Mbps operating mode. Wake-up time is <30 µs for 100BASE-TX.

The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

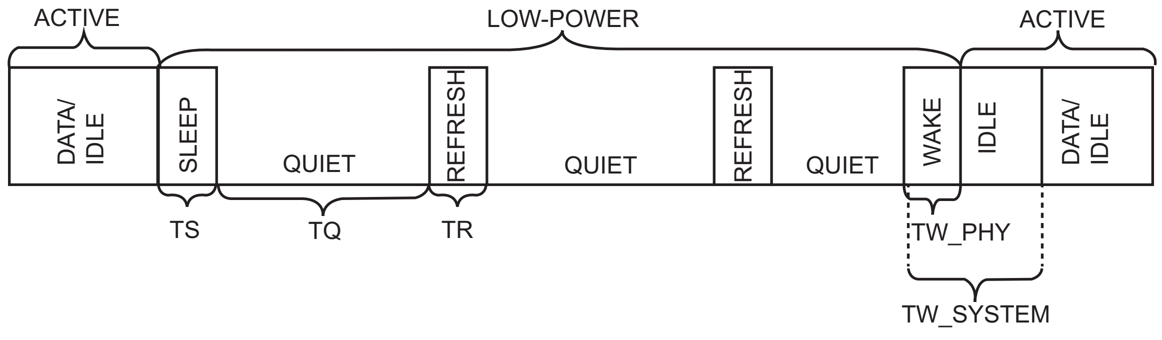
The KSZ8091RNA/RND has the EEE function disabled as the power-up default setting. To enable the EEE function for 100 Mbps mode, use the following programming sequence:

1. Enable 100 Mbps EEE mode advertisement by writing a ‘1’ to MMD address 7h, Register 3Ch, bit [1].
2. Restart auto-negotiation by writing a ‘1’ to standard Register 0h, bit [9].

For standard (non-EEE) 10BASE-T mode, normal link pulses (NLPs) with long periods of no AC signal transmission are used to maintain the link during the idle period when there is no traffic activity. To save more power, the KSZ8091RNA/RND provides the option to enable 10BASE-Te mode, which saves additional power by reducing the transmitted signal amplitude from 2.5V to 1.75V. To enable 10BASE-Te mode, write a ‘1’ to standard Register 13h, bit [4].

During LPI mode, refresh transmissions are used to maintain the link; power savings occur in quiet periods. Approximately every 20 to 22 milliseconds, a refresh transmission of 200 to 220 microseconds is sent to the link partner. The refresh transmissions and quiet periods are shown in Figure 3-9.

FIGURE 3-9: LPI MODE (REFRESH TRANSMISSIONS AND QUIET PERIODS)

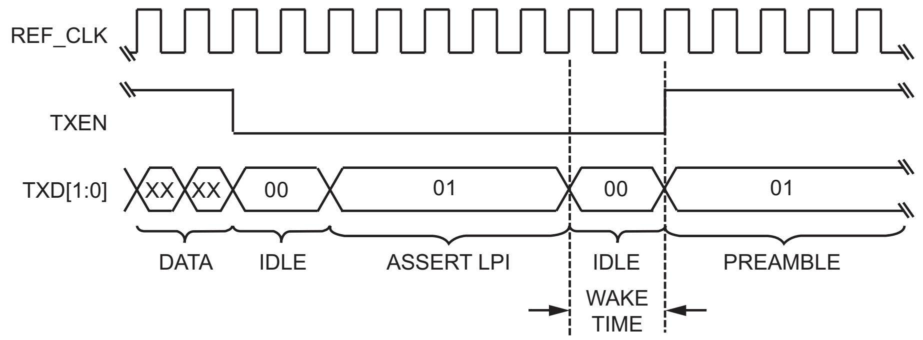


3.11.1 TRANSMIT DIRECTION CONTROL (MAC-TO-PHY)

The KSZ8091RNA/RND enters LPI mode for the transmit direction when its attached EEE-compliant RMII MAC de-asserts TXEN and sets TXD[1:0] to 01. The KSZ8091RNA/RND remains in the LPI transmit state while the RMII MAC maintains the states of these signals. When the RMII MAC changes any of the TXEN or TX data signals from their LPI state values, the KSZ8091RNA/RND exits the LPI transmit state.

Figure 3-10 shows the LPI transition for MII (100 Mbps) transmit.

FIGURE 3-10: LPI TRANSITION - RMII (100 MBPS) TRANSMIT

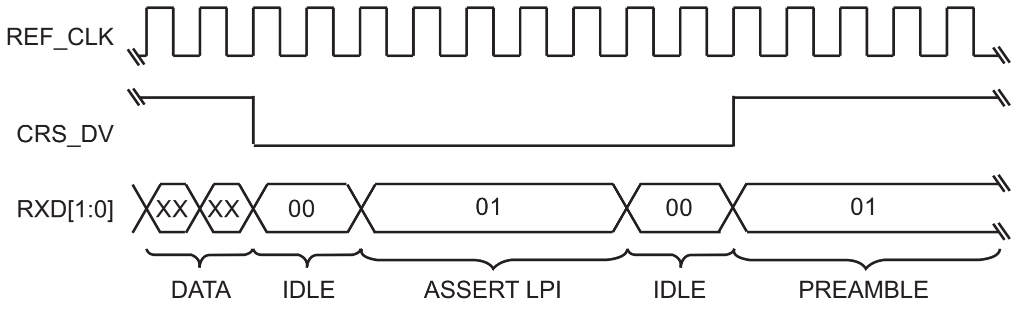


3.11.2 RECEIVE DIRECTION CONTROL (PHY-TO-MAC)

The KSZ8091RNA/RND enters LPI mode for the receive direction when it receives the /P/ code bit pattern (Sleep/Refresh) from its EEE-compliant link partner. It then de-asserts CRS_DV and drives RXD[1:0] to 01. The KSZ8091RNA/RND remains in the LPI receive state while it continues to receive the refresh from its link partner, so it will continue to maintain and drive the LPI output states for the RMII receive signals to inform the attached EEE-compliant RMII MAC that it is in the LPI receive state. When the KSZ8091RNA/RND receives a non /P/ code bit pattern (non-refresh), it exits the LPI receive state and sets the CRS_DV and RX data signals to set a normal frame or normal idle.

Figure 3-11 shows the LPI transition for RMII (100 Mbps) receive.

FIGURE 3-11: LPI TRANSITION - RMII (100 MBPS) RECEIVE



3.11.3 REGISTERS ASSOCIATED WITH EEE

The following registers are provided for EEE configuration and management:

- Standard Register 13h - AFE Control 4 (to enable 10BASE-Te mode)
- MMD address 1h, Register 0h - PMA/PMD Control 1 (to enable LPI)
- MMD address 1h, Register 1h - PMA/PMD Status 1 (for LPI status)
- MMD address 3h, Register 0h - EEE PCS Control 1 (to stop RXC clock for KSZ8091MNX only)
- MMD address 7h, Register 3Ch - EEE Advertisement
- MMD address 7h, Register 3Dh - EEE Link Partner Advertisement

3.12 Wake-On-LAN

Wake-On-LAN (WOL) is normally a MAC-based function to wake up a host system (for example, an Ethernet end device, such as a PC) that is in standby power mode. Wake-up is triggered by receiving and detecting a special packet (commonly referred to as the "magic packet") that is sent by the remote link partner. The KSZ8091RNA/RND can perform the same WOL function if the MAC address of its associated MAC device is entered into the KSZ8091RNA/RND PHY Registers for magic-packet detection. When the KSZ8091RNA/RND detects the magic packet, it wakes up the host by driving its power management event (PME) output pin low.

By default, the WOL function is disabled. It is enabled by setting the enabling bit and configuring the associated registers for the selected PME wake-up detection method.

The KSZ8091RNA/RND provides three methods to trigger a PME wake-up:

- Magic-packet detection
- Customized-packet detection
- Link status change detection

3.12.1 MAGIC-PACKET DETECTION

The magic packet's frame format starts with 6 bytes of 0xFFh and is followed by 16 repetitions of the MAC address of its associated MAC device (local MAC device).

When the magic packet is detected from its link partner, the KSZ8091RNA/RND asserts its PME output pin low.

The following MMD address 1Fh registers are provided for magic-packet detection:

- Magic-packet detection is enabled by writing a '1' to MMD address 1Fh, Register 0h, bit [6]
- The MAC address (for the local MAC device) is written to and stored in MMD address 1Fh, Registers 19h – 1Bh

The KSZ8091RNA/RND does not generate the magic packet. The magic packet must be provided by the external system.

3.12.2 CUSTOMIZED-PACKET DETECTION

The customized packet has associated register/bit masks to select which byte, or bytes, of the first 64 bytes of the packet to use in the CRC calculation. After the KSZ8091RNA/RND receives the packet from its link partner, the selected bytes for the received packet are used to calculate the CRC. The calculated CRC is compared to the expected CRC value that was previously written to and stored in the KSZ8091RNA/RND PHY Registers. If there is a match, the KSZ8091RNA/RND asserts its PME output pin low.

Four customized packets are provided to support four types of wake-up scenarios. A dedicated set of registers is used to configure and enable each customized packet.

The following MMD Registers are provided for customized-packet detection:

- Each of the four customized packets is enabled via MMD address 1Fh, Register 0h,
  - Bit [2] // For customized packets, type 0
  - Bit [3] // For customized packets, type 1
  - Bit [4] // For customized packets, type 2
  - Bit [5] // For customized packets, type 3
- Masks to indicate which of the first 64-bytes to use in the CRC calculation are set in:
  - MMD address 1Fh, Registers 1h – 4h // For customized packets, type 0
  - MMD address 1Fh, Registers 7h – Ah // For customized packets, type 1
  - MMD address 1Fh, Registers Dh – 10h // For customized packets, type 2
  - MMD address 1Fh, Registers 13h – 16h // For customized packets, type 3
- 32-bit expected CRCs are written to and stored in:
  - MMD address 1Fh, Registers 5h – 6h // For customized packets, type 0
  - MMD address 1Fh, Registers Bh – Ch // For customized packets, type 1
  - MMD address 1Fh, Registers 11h – 12h // For customized packets, type 2
  - MMD address 1Fh, Registers 17h – 18h // For customized packets, type 3