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KSZ8462HL/KSZ8462FHL

IEEE 1588 Precision Time Protocol-Enabled
Two-Port 10/100Mb/s Ethernet Switch
with 8 or 16 Bit Host Interface

Revision 1.0

General Description

The KSZ8462 ETHERSYNCH™ product line consists of IEEE 1588v2-enabled Ethernet switches, providing integrated communications and synchronization for a range of industrial Ethernet applications.

The KSZ8462 ETHERSYNCH product enables distributed, daisy-chained topologies preferred for Industrial Ethernet networks. Conventional centralized (i.e., star-wired) topologies are also supported for dual-homed, fault tolerant arrangements.

A flexible 8- or 16-bit general bus interface is provided for interfacing to an external host processor.

The KSZ8462 devices incorporate the IEEE 1588v2 protocol. Sub-microsecond synchronization is available via the use of hardware based time stamping and transparent clocks making it the ideal solution for time synchronized Layer 2 communication in critical industrial applications.

Extensive general purpose I/O (GPIO) capabilities are available to use with the IEEE 1588v2 PTP to efficiently and accurately interface to locally-connected devices.

Complementing the industry's most-integrated IEEE 1588v2 device is a precision timing protocol (PTP) v2 software stack that has been pre-qualified with the KSZ84xx product family. The PTP stack has been optimized around the KSZ84xx chip architecture, and is available in source code format along with Micrel's chip driver.

The wire-speed, store-and-forward switching fabric provides a full complement of quality-of-service (QoS) and congestion control features optimized for real-time Ethernet.



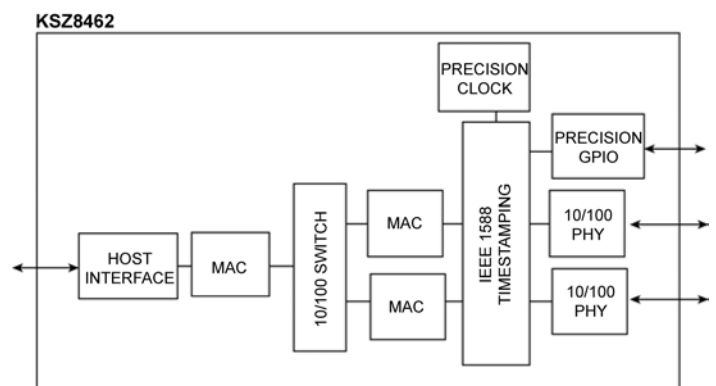
ETHERSYNCH™

The KSZ8462 product is built upon Micrel's industry-leading Ethernet technology, with features designed to offload host processing and streamline your overall design:

- Wire-speed Ethernet switching fabric with extensive filtering
- Two integrated 10/100BASE-TX PHY transceivers, featuring the industry's lowest power consumption
- Full-featured QoS support
- Flexible management options that support common standard interfaces

A robust assortment of power-management features including energy-efficient Ethernet (EEE) have been designed in to satisfy energy-efficient environments.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.



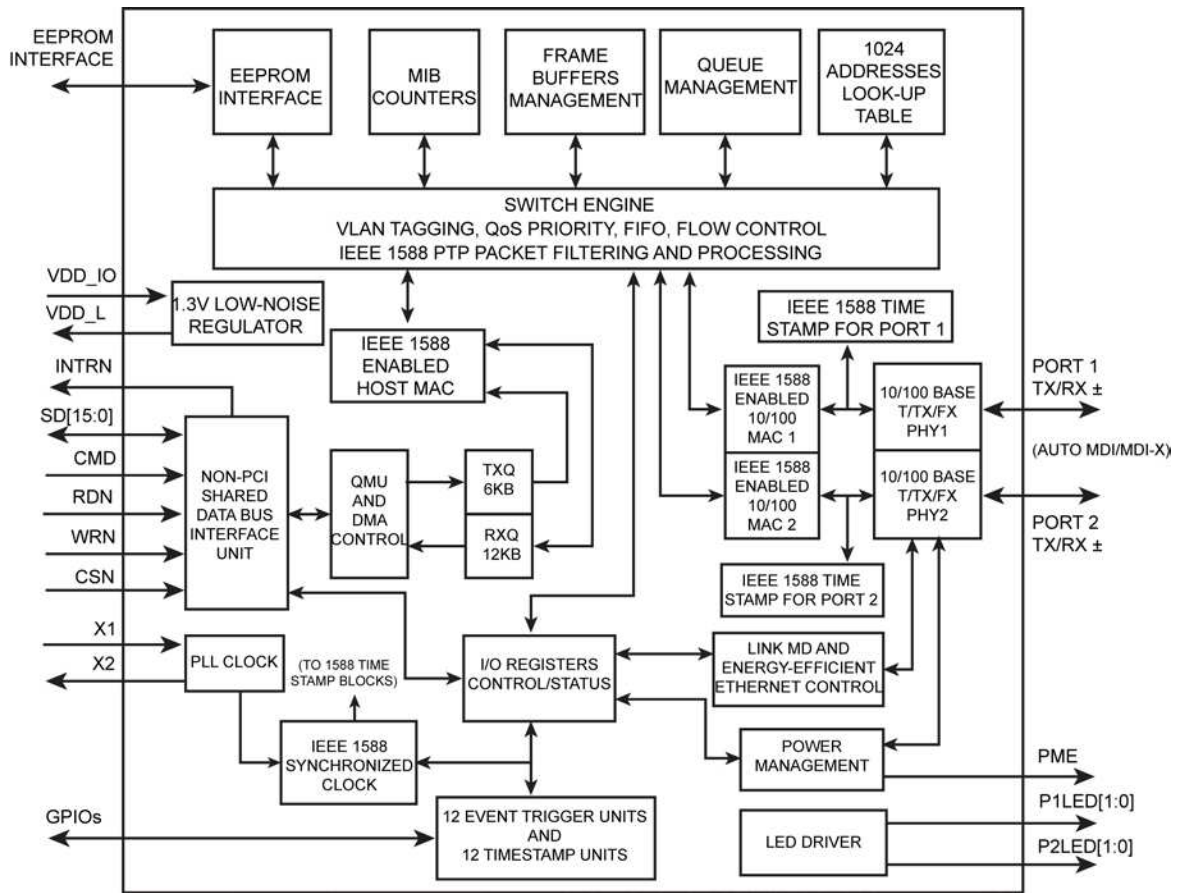
KSZ8462 Top Level Architecture

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Functional Diagram



KSZ8462HL/KSZ8462FHL Functional Diagram

Features

Management Capabilities

- The KSZ8462 includes all the functions of a 10/100BASE-T/TX/FX switch system which combines a switch engine, frame buffer management, address look-up table, queue management, MIB counters, media access controllers (MAC) and PHY transceivers
- Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 1024 entry forwarding table
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- MIB counters for fully-compliant statistics gathering – 34 counters per port
- Loopback modes for remote failure diagnostics
- Rapid spanning tree protocol support (RSTP) for topology management and ring/linear recovery

Robust PHY Ports

- Two integrated IEEE 802.3/802.3u compliant Ethernet transceivers supporting 10BASE-T and 100BASE-TX
- Copper and 100BASE-FX fiber mode support in the KSZ8462FHL
- Copper mode support in the KSZ8462HL
- On-chip termination resistors and internal biasing for differential pairs to reduce power
- HP Auto MDI/MDI-X crossover support eliminating the need to differentiate between straight or crossover cables in applications

MAC Ports

- Three internal media access control (MAC) units
- 2Kbyte jumbo packet support
- Tail tagging mode (one byte added before FCS) support at port 3 to inform the processor which ingress port receives the packet and its priority
- Programmable MAC addresses for port 1 and port 2 and self-address filtering support
- MAC filtering function to filter or forward unknown unicast packets
- Port 1 and port 2 MACs programmable as either end-to-end (E2E) or peer-to-peer (P2P) transparent clock (TC) ports for 1588 support

Advanced Switch Capabilities

- Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 1024 entry forwarding table
- IEEE 802.1Q VLAN for up to 16 groups with full range of VLAN IDs
- IEEE 802.1p/Q tag insertion or removal on a per port basis (egress) and support double-tagging
- VLAN ID tag/untag options on per port basis
- Fully compliant with IEEE 802.3/802.3u standards
- IEEE 802.3x full-duplex with force mode option and half-duplex backpressure collision flow control
- IEEE 802.1w rapid spanning tree protocol support
- IGMP v1/v2/v3 snooping for multicast packet filtering
- QoS/CoS packets prioritization support: 802.1p, DiffServ-based and re-mapping of 802.1p priority field per port basis on four priority levels

IPv4/IPv6 QoS support

- IPv6 multicast listener discovery (MLD) snooping support
- Programmable rate limiting at the ingress and egress ports
- Broadcast storm protection
- 1K entry forwarding table with 32K frame buffer
- 4 priority queues with dynamic packet mapping for IEEE 802.1P, IPv4 TOS (DIFFSERV), IPv6 Traffic Class, etc.
- Source address filtering for implementing ring topologies

Comprehensive Configuration Registers Access

- Complete register access via the parallel host interface
- Facility to load MAC Address from EEPROM at power-up and reset time
- I/O pin strapping facility to set certain register bits from I/O pins at reset time
- Control registers configurable on-the-fly

IEEE 1588v2 PTP and Clock Synchronization

- Fully compliant with the IEEE 1588v2 precision time protocol
- One-step or two-step transparent clock (TC) timing corrections
- End-to-end (E2E) or peer-to-peer (P2P) transparent clock (TC)
- Grandmaster, master, slave, and ordinary clock (OC) support
- IEEE1588v2 PTP multicast and unicast frame support
- Transports of PTP over IPv4/IPv6 UDP and IEEE 802.3 Ethernet
- Delay request-response and peer delay mechanism
- Ingress/egress packet timestamp capture/recording and checksum update
- Correction field update with residence time and link delay
- IEEE1588v2 PTP packet filtering unit to reduce host processor overhead
- A 64-bit adjustable system precision clock
- 12 trigger output units and 12 timestamp input units available for flexible IEEE1588v2 control of 7 programmable GPIO[6:0] pins synchronized to the precision time clock
- GPIO pin usage for 1 PPS generation, frequency generator, control bit streams, event monitoring, precision pulse generation, complex waveform generation

Host Interface

- Selectable 8- or 16-bit wide interface
- Supports big- and little-endian processors
- Indirect data bus for data, address and byte enable to access any I/O registers and RX/TX FIFO buffers
- Large internal memory with 12Kbyte for RX FIFO and 6Kbytes for TX FIFO
- Programmable low, high and overrun water mark for flow control in RX FIFO
- Efficient architecture design with configurable host interrupt schemes to minimize host CPU overhead and utilization
- Queue management unit (QMU) supervises data transfers across this interface

Power and Power Management

- Single 3.3V power supply with optional VDD I/O for 1.8V, 2.5V or 3.3V
- Integrated low voltage (~1.3V) low-noise regulator (LDO) output for digital and analog core power.
- Supports IEEE P802.3az energy-efficient Ethernet (EEE) to reduce power consumption in transceivers in LPI state
- Full-chip hardware or software power down (all registers value are not saved and strap-in value will re-strap after release the power down)
- Energy detect power down (EDPD), which disables the PHY transceiver when cables are removed
- Wake-on-LAN supported with configurable packet control
- Dynamic clock tree control to reduce clocking in areas not in use
- Power consumption less than 0.5W

Additional Features

- Single 25MHz ± 50 ppm reference clock requirement
- Comprehensive programmable two LED indicators support for link, activity, full/half duplex and 10/100 speed
- LED pins directly controllable
- Industrial temperature range: -40°C to $+85^{\circ}\text{C}$
- 64-pin, 10mm \times 10mm, lead free, RoHS, LQFP package
- 0.11 μm technology for lower power consumption

Applications

- Industrial Ethernet applications that employ IEEE 802.3-compliant MACs. (Ethernet/IP, Profinet, MODBUS TCP, etc)
- Real-time Ethernet networks requiring sub-microsecond synchronization over standard Ethernet
- IEC 61850 networks supporting power substation automation
- Networked measurement and control systems
- Industrial automation and motion control systems
- Test and measurement equipment

Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Description
KSZ8462HLI	-40°C to +85°C	64-Pin LQFP	Pb-Free	Industrial Temperature Device with Generic Host Interface
KSZ8462FHLL	-40°C to +85°C	64-Pin LQFP	Pb-Free	Industrial Temperature Device with Generic Host Interface and Fiber (100BASE-FX) support
KSZ8462HLI-EVAL	Evaluation Board with KSZ8462HLI. Also supports the KSZ8462FHLL.			

Revision History

Revision	Date	Summary of Changes
1.0	6/11/14	Initial release of KSZ8462HL/FHL product datasheet.

Contents

General Description	1
Functional Diagram	2
Features	3
Management Capabilities	3
Robust PHY Ports	3
MAC Ports	3
Advanced Switch Capabilities	3
IPv4/IPv6 QoS support	3
Comprehensive Configuration Registers Access	3
IEEE 1588v2 PTP and Clock Synchronization	4
Host Interface	4
Power and Power Management	4
Additional Features	4
Applications	4
Ordering Information	5
Revision History	5
Contents	6
Acronyms	20
Pin Configuration	23
Pin Description	24
Strapping Options	29
Functional Description	30
Direction Terminology	30
Physical (PHY) Block	31
100BASE-TX Transmit	31
100BASE-TX Receive	31
Scrambler/De-Scrambler (100BASE-TX Only)	31
PLL Clock Synthesizer (Recovery)	31
100BASE-FX Operation	31
100BASE-FX Signal Detection	32
100BASE-FX Far-End Fault	32
10BASE-T Transmit	32
10BASE-T Receive	32
MDI/MDI-X Auto Crossover	32
Straight Cable	33
Crossover Cable	33
Auto-Negotiation	34
LinkMD [®] Cable Diagnostics	35
Access	35
Usage	35
On-Chip Termination Resistors	35
Loopback Support	35
Far-End Loopback	36
Near-End (Remote) Loopback	36

Media Access Controller (MAC) Block	37
MAC Operation	37
Address Lookup	37
Learning	37
Migration	37
Aging	37
Forwarding	37
Inter Packet Gap (IPG)	40
Back-Off Algorithm	40
Late Collision	40
Legal Packet Size	40
Flow Control	40
Half-Duplex Backpressure	40
Broadcast Storm Protection	41
Port Individual MAC Address and Source Port Filtering	41
Address Filtering Function	41
Switch Block	43
Switching Engine	43
Spanning Tree Support	43
Rapid Spanning Tree Support	44
Discarding State	44
Learning State	44
Forwarding State	44
Tail Tagging Mode	44
IGMP Support	45
"IGMP" Snooping	45
"Multicast Address Insertion" in the Static MAC Table	45
IPv6 MLD Snooping	45
Port Mirroring Support	46
"Receive Only" Mirror-on-a-Port	46
"Transmit Only" Mirror-on-a-Port	46
"Receive and Transmit" Mirror-on-Two-Ports	46
IEEE 802.1Q VLAN Support	46
QoS Priority Support	47
Port-Based Priority	47
802.1p-Based Priority	47
802.1p Priority Field Re-Mapping	48
DiffServ-Based Priority	48
Rate-Limiting Support	49
MAC Address Filtering Function	49
Queue Management Unit (QMU)	50
Transmit Queue (TXQ) Frame Format	50
Frame Transmitting Path Operation in TXQ	51
Driver Routine for Transmitting Packets from Host Processor to KSZ8462	52
Receive Queue (RXQ) Frame Format	53
Frame Receiving Path Operation in RXQ	53
Driver Routine for Receiving Packets from the KSZ8462 to the Host Processor	54
IEEE 1588 Precision Time Protocol (PTP) Block	56
IEEE 1588 PTP Clock Types	57
IEEE 1588 PTP One-Step or Two-Step Clock Operation	57
IEEE 1588 PTP Best Master Clock Selection	57
IEEE 1588 PTP System Time Clock	57
Updating the System time Clock	59

IEEE 1588 PTP Message Processing	60
IEEE 1588 PTP Ingress Packet Processing	60
IEEE 1588 PTP Egress Packet Processing	60
IEEE 1588 PTP Event Triggering and Timestamping	61
IEEE 1588 PTP Trigger Outputs	61
IEEE 1588 PTP Event Timestamp Input	61
IEEE 1588 PTP Event Interrupts	62
IEEE 1588 GPIO	62
General Purpose and IEEE 1588 Input/Output (GPIO)	63
Overview	63
GPIO Pin Functionality Control	63
GPIO Pin Control Register Layout	64
GPIO Trigger Output Units and Timestamp Input Unit Interrupts	67
Using the GPIO Pins with the Trigger Output Units	68
Creating a Low-Going Pulse at a Specific Time	68
Creating a High-Going Pulse at a Specific Time	68
Creating a Free Running Clock Source	69
Creating Finite Length Periodic Bit Streams at a Specific Time	70
Creating Finite Length Non-Uniform Bit Streams at a Specific Time	70
Creating Complex Waveforms at a Specific Time	71
Using the GPIO Pins with the Timestamp Input Units	72
Timestamp Value	72
Timestamping an Incoming Low-Going Edge	72
Timestamping an Incoming High-Going Edge	73
Device Clocks	74
GPIO and IEEE 1588 Related Clocking	74
Power	75
Power Management	77
Normal Operation Mode	77
Energy Detect Mode	77
Global Soft Power-Down Mode	78
Energy-Efficient Ethernet (EEE)	78
Transmit Direction Control for MII Mode	79
Receive Direction Control for MII Mode	79
Wake-On-LAN	80
Detection of Energy	80
Detection of Linkup	80
Wake-Up Packet	80
Magic Packet™	80
Interrupt Generation on Power Management Related Events	81
To Generate an Interrupt on the PME Signal Pin	81
To Generate an Interrupt on the INTRN Signal Pin	81
Interfaces	82
Bus Interface Unit (BIU) / Host Interface	82
Supported Transfers	82
Physical Data Bus Size	82
Little and Big Endian Support	83
Asynchronous Interface	83
BIU Summary	84
Serial EEPROM Interface	85
Device Registers	86

Register Map of CPU Accessible I/O Registers.....	88
I/O Registers.....	88
Internal I/O Register Space Mapping for Switch Control and Configuration (0x000 – 0x0FF).....	88
Internal I/O Register Space Mapping for Host Interface Unit (0x100 – 0x16F).....	94
Internal I/O Register Space Mapping for the QMU (0x170 – 0x1FF).....	96
Internal I/O Register Space Mapping for PTP Trigger Output (12 Units, 0x200 – 0x3FF).....	98
Internal I/O Register Space Mapping for PTP Event Timestamp Input (12 Units, 0x400 – 0x5FF).....	107
Internal I/O Register Space Mapping for PTP 1588 Clock and Global Control (0x600 – 0x7FF).....	119
Register Bit Definitions.....	122
Internal I/O Register Mapping for Switch Control and Configuration (0x000 – 0x0FF).....	122
Chip ID and Enable Register (0x00 – 0x001): CIDER.....	122
Switch Global Control Register 1 (0x002 – 0x003): SGCR1.....	122
Switch Global Control Register 2 (0x004 – 0x005): SGCR2.....	124
Switch Global Control Register 3 (0x006 – 0x007): SGCR3.....	125
0x008 – 0x00B: Reserved.....	125
Switch Global Control Register 6 (0x00C – 0x00D): SGCR6.....	126
Switch Global Control Register 7 (0x00E – 0x00F): SGCR7.....	127
MAC Address Register 1 (0x010 – 0x011): MACAR1.....	128
MAC Address Register 2 (0x012 – 0x013): MACAR2.....	128
MAC Address Register 3 (0x014 – 0x015): MACAR3.....	128
Type-of-Service (TOS) Priority Control Registers.....	129
TOS Priority Control Register 1 (0x016 – 0x017): TOSR1.....	129
TOS Priority Control Register 2 (0x018 – 0x019): TOSR2.....	130
TOS Priority Control Register 3 (0x01A – 0x01B): TOSR3.....	131
TOS Priority Control Register 4 (0x01C – 0x01D): TOSR4.....	131
TOS Priority Control Register 5 (0x01E – 0x01F): TOSR5.....	132
TOS Priority Control Register 6 (0x020 – 0x021): TOSR6.....	133
TOS Priority Control Register 7 (0x022 – 0x023): TOSR7.....	133
TOS Priority Control Register 8 (0x024 – 0x025): TOSR8.....	134
Indirect Access Data Registers.....	135
Indirect Access Data Register 1 (0x026 – 0x027): IADR1.....	135
Indirect Access Data Register 2 (0x028 – 0x029): IADR2.....	135
Indirect Access Data Register 3 (0x02A – 0x02B): IADR3.....	135
Indirect Access Data Register 4 (0x02C – 0x02D): IADR4.....	135
Indirect Access Data Register 5 (0x02E – 0x02F): IADR5.....	136
Indirect Access Control Register (0x030 – 0x031): IACR.....	136
Power Management Control and Wake-Up Event Status.....	137
Power Management Control and Wake-Up Event Status (0x032 – 0x033): PMCTRL.....	137
Power Management Event Enable Register (0x034 – 0x035): PMEE.....	138
Go Sleep Time and Clock Tree Power-Down Control Registers.....	139
Go Sleep Time Register (0x036 – 0x037): GST.....	139
Clock Tree Power-Down Control Register (0x038 – 0x039): CTPDC.....	139
0x03A – 0x04B: Reserved.....	139
PHY and MII Basic Control Registers.....	140
PHY 1 and MII Basic Control Register (0x04C – 0x04D): P1MBCR.....	140
PHY 1 and MII Basic Status Register (0x04E – 0x04F): P1MBSR.....	141
PHY 1 PHYID Low Register (0x050 – 0x051): PHY1ILR.....	142
PHY 1 PHYID High Register (0x052 – 0x053): PHY1IHR.....	142
PHY 1 Auto-Negotiation Advertisement Register (0x054 – 0x055): P1ANAR.....	143
PHY 1 Auto-Negotiation Link Partner Ability Register (0x056 – 0x057): P1ANLPR.....	144
PHY 2 and MII Basic Control Register (0x058 – 0x059): P2MBCR.....	144
PHY 2 and MII Basic Status Register (0x05A – 0x05B): P2MBSR.....	146
PHY 2 PHYID Low Register (0x05C – 0x05D): PHY2ILR.....	147
PHY 2 PHYID High Register (0x05E – 0x05F): PHY2IHR.....	147
PHY 2 Auto-Negotiation Advertisement Register (0x060 – 0x061): P2ANAR.....	147

PHY 2 Auto-Negotiation Link Partner Ability Register (0x062 – 0x063): P2ANLPR	148
0x064 – 0x065: Reserved.....	148
PHY1 Special Control and Status Register (0x066 – 0x067): P1PHYCTRL	149
0x068 – 0x069: Reserved.....	149
PHY 2 Special Control and Status Register (0x06A – 0x06B): P2PHYCTRL.....	149
Port 1 Control Registers.....	150
Port 1 Control Register 1 (0x06C – 0x06D): P1CR1	150
Port 1 Control Register 2 (0x06E – 0x06F): P1CR2.....	152
Port 1 VID Control Register (0x070 – 0x071): P1VIDCR	153
Port 1 Control Register 3 (0x072 – 0x073): P1CR3	153
Port 1 Ingress Rate Control Register 0 (0x074 – 0x075): P1IRCR0	154
Port 1 Ingress Rate Control Register 1 (0x076 – 0x077): P1IRCR1	155
Port 1 Egress Rate Control Register 0 (0x078 – 0x079): P1ERCR0	155
Port 1 Egress Rate Control Register 1 (0x07A – 0x07B): P1ERCR1	155
Port 1 PHY Special Control/Status, LinkMD (0x07C – 0x07D): P1SCSLMD.....	156
Port 1 Control Register 4 (0x07E – 0x07F): P1CR4.....	157
Port 1 Status Register (0x080 – 0x081): P1SR.....	158
0x082 – 0x083: Reserved.....	159
Port 2 Control Registers.....	160
Port 2 Control Register 1 (0x084 – 0x085): P2CR1	160
Port 2 Control Register 2 (0x086 – 0x087): P2CR2	162
Port 2 VID Control Register (0x088 – 0x089): P2VIDCR	163
Port 2 Control Register 3 (0x08A – 0x08B): P2CR3	163
Port 2 Ingress Rate Control Register 0 (0x08C – 0x08D): P2IRCR0.....	164
Port 2 Ingress Rate Control Register 1 (0x08E – 0x08F): P2IRCR1	164
Port 2 Egress Rate Control Register 0 (0x090 – 0x091): P2ERCR0	165
Port 2 Egress Rate Control Register 1 (0x092 – 0x093): P2ERCR1	165
Port 2 PHY Special Control/Status, LinkMD (0x094 – 0x095): P2SCSLMD	166
Port 2 Control Register 4 (0x096 – 0x097): P2CR4	167
Port 2 Status Register (0x098 – 0x099): P2SR.....	169
0x09A – 0x09B: Reserved.....	170
Port 3 Control Registers.....	171
Port 3 Control Register 1 (0x09C – 0x09D): P3CR1	171
Port 3 Control Register 2 (0x09E – 0x09F): P3CR2.....	172
Port 3 VID Control Register (0x0A0 – 0x0A1): P3VIDCR	173
Port 3 Control Register 3 (0x0A2 – 0x0A3): P3CR3	174
Port 3 Ingress Rate Control Register 0 (0x0A4 – 0x0A5): P3IRCR0	174
Port 3 Ingress Rate Control Register 1 (0x0A6 – 0x0A7): P3IRCR1	175
Port 3 Egress Rate Control Register 0 (0x0A8 – 0x0A9): P3ERCR0	175
Port 3 Egress Rate Control Register 1 (0x0AA – 0x0AB): P3ERCR1.....	175
Switch Global Control Registers	176
Switch Global Control Register 8 (0x0AC – 0x0AD): SGCR8.....	176
Switch Global Control Register 9 (0x0AE – 0x0AF): SGCR9	177
Source Address Filtering Registers	178
Source Address Filtering MAC Address 1 Register Low (0x0B0 – 0x0B1): SAFMACA1L	178
Source Address Filtering MAC Address 1 Register Middle (0x0B2 – 0x0B3): SAFMACA1M.....	178
Source Address Filtering MAC Address 1 Register High (0x0B4 – 0x0B5): SAFMACA1H.....	178
Source Address Filtering MAC Address 2 Register Low (0x0B6 – 0x0B7): SAFMACA2L	178
Source Address Filtering MAC Address 2 Register Middle (0x0B8 – 0x0B9): SAFMACA2M.....	178
Source Address Filtering MAC Address 2 Register High (0x0BA – 0x0BB): SAFMACA2H.....	179
0x0BC – 0x0C7: Reserved.....	179

TXQ Rate Control Registers	180
Port 1 TXQ Rate Control Register 1 (0x0C8 – 0x0C9): P1TXQRCR1	180
Port 1 TXQ Rate Control Register 2 (0x0CA – 0x0CB): P1TXQRCR2	180
Port 2 TXQ Rate Control Register 1 (0x0CC – 0x0CD): P2TXQRCR1	181
Port 2 TXQ Rate Control Register 2 (0x0CE – 0x0CF): P2TXQRCR2	181
Port 3 TXQ Rate Control Register 1 (0x0D0 – 0x0D1): P3TXQRCR1	182
Port 3 TXQ Rate Control Register 2 (0x0D2 – 0x0D3): P3TXQRCR2	182
0x0D4 – 0x0D5: Reserved	182
Input and Output Multiplex Selection Registers	183
Input and Output Multiplex Selection Register (0x0D6 – 0x0D7): IOMUXSEL	183
Configuration Status and Serial Bus Mode Registers	184
Configuration Status and Serial Bus Mode Register (0x0D8 – 0x0D9): CFGR	184
0x0DA – 0x0DB: Reserved	184
Auto-Negotiation Next Page Registers	185
Port 1 Auto-Negotiation Next Page Transmit Register (0x0DC – 0x0DD): P1ANPT	185
Port 1 Auto-Negotiation Link Partner Received Next Page Register (0x0DE – 0x0DF): P1ALPRNP	186
EEE and Link Partner Advertisement Registers	187
Port 1 EEE and Link Partner Advertisement Register (0x0E0 – 0x0E1): P1EEEA	187
Port 1 EEE Wake Error Count Register (0x0E2 – 0x0E3): P1EEEWEC	188
Port 1 EEE Control/Status and Auto-Negotiation Expansion Register (0x0E4 – 0x0E5): P1EEECS	188
Port 1 LPI Recovery Time Counter Register (0x0E6): P1LPIRTC	190
Buffer Load to LPI Control 1 Register (0x0E7): BL2LPIC1	190
Port 2 Auto-Negotiation Next Page Transmit Register (0x0E8 – 0x0E9): P2ANPT	190
Port 2 Auto-Negotiation Link Partner Received Next Page Register (0x0EA – 0x0EB): P2ALPRNP	191
Port 2 EEE and Link Partner Advertisement Register (0x0EC – 0x0ED): P2EEEA	192
Port 2 EEE Wake Error Count Register (0x0EE – 0x0EF): P2EEEWEC	193
Port 2 EEE Control/Status and Auto-Negotiation Expansion Register (0x0F0 – 0x0F1): P2EEECS	193
Port 2 LPI Recovery Time Counter Register (0x0F2): P2LPIRTC	195
PCS EEE Control Register (0x0F3): PCSEEEC	195
Empty TXQ to LPI Wait Time Control Register (0x0F4 – 0x0F5): ETLWTC	195
Buffer Load to LPI Control 2 Register (0x0F6 – 0x0F7): BL2LPIC2	196
0x0F8 – 0x0FF: Reserved	196
Internal I/O Register Space Mapping for Interrupts, BIU, and Global Reset (0x100 – 0x1FF)	197
0x100 – 0x107: Reserved	197
Chip Configuration Register (0x108 – 0x109): CCR	197
0x10A – 0x10F: Reserved	197
Host MAC Address Registers: MARL, MARM and MARH	198
Host MAC Address Register Low (0x110 – 0x111): MARL	198
Host MAC Address Register Middle (0x112 – 0x113): MARM	198
Host MAC Address Register High (0x114 – 0x115): MARH	198
0x116 – 0x121: Reserved	198
EEPROM Control Register (0x122 – 0x123): EEPCR	199
Memory BIST Info Register (0x124 – 0x125): MBIR	199
Global Reset Register (0x126 – 0x127): GRR	200
0x128 – 0x129: Reserved	200
Wake-Up Frame Control Register (0x12A – 0x12B): WFCR	201
0x12C – 0x12F: Reserved	201
Wake-Up Frame 0 CRC0 Register (0x130 – 0x131): WF0CRC0	201
Wake-Up Frame 0 CRC1 Register (0x132 – 0x133): WF0CRC1	202
Wake-Up Frame 0 Byte Mask 0 Register (0x134 – 0x135): WF0BM0	202
Wake-Up Frame 0 Byte Mask 1 Register (0x136 – 0x137): WF0BM1	202
Wake-Up Frame 0 Byte Mask 2 Register (0x138 – 0x139): WF0BM2	202
Wake-Up Frame 0 Byte Mask 3 Register (0x13A – 0x13B): WF0BM3	202
0x13C – 0x13F: Reserved	203
Wake-Up Frame 1 CRC0 Register (0x140 – 0x141): WF1CRC0	203
Wake-Up Frame 1 CRC1 Register (0x142 – 0x143): WF1CRC1	203

Wake-Up Frame 1 Byte Mask 0 Register (0x144 – 0x145): WF1BM0.....	203
Wake-Up Frame 1 Byte Mask 1 Register (0x146 – 0x147): WF1BM1.....	203
Wake-Up Frame 1 Byte Mask 2 Register (0x148 – 0x149): WF1BM2.....	204
Wake-Up Frame 1 Byte Mask 3 Register (0x14A – 0x14B): WF1BM3.....	204
0x14C – 0x14F: Reserved.....	204
Wake-Up Frame 2 CRC0 Register (0x150 – 0x151): WF2CRC0.....	204
Wake-Up Frame 2 CRC1 Register (0x152 – 0x153): WF2CRC1.....	204
Wake-Up Frame 2 Byte Mask 0 Register (0x154 – 0x155): WF2BM0.....	205
Wake-Up Frame 2 Byte Mask 1 Register (0x156 – 0x157): WF2BM1.....	205
Wake-Up Frame 2 Byte Mask 2 Register (0x158 – 0x159): WF2BM2.....	205
Wake-Up Frame 2 Byte Mask 3 Register (0x15A – 0x15B): WF2BM3.....	205
0x15C – 0x15F: Reserved.....	205
Wake-Up Frame 3 CRC0 Register (0x160 – 0x161): WF3CRC0.....	206
Wake-Up Frame 3 CRC1 Register (0x162 – 0x163): WF3CRC1.....	206
Wake-Up Frame 3 Byte Mask 0 Register (0x164 – 0x165): WF3BM0.....	206
Wake-Up Frame 3 Byte Mask 1 Register (0x166 – 0x167): WF3BM1.....	206
Wake-Up Frame 3 Byte Mask 2 Register (0x168 – 0x169): WF3BM2.....	206
Wake-Up Frame 3 Byte Mask 3 Register (0x16A – 0x16B): WF3BM3.....	207
0x16C – 0x16F: Reserved.....	207
Internal I/O Register Space Mapping for the Queue Management Unit (QMU) (0x170 – 0x1FF).....	208
Transmit Control Register (0x170 – 0x171): TXCR.....	208
Transmit Status Register (0x172 – 0x173): TXSR.....	209
Receive Control Register 1 (0x174 – 0x175): RXCR1.....	209
Receive Control Register 2 (0x176 – 0x177): RXCR2.....	210
TXQ Memory Information Register (0x178 – 0x179): TXMIR.....	211
0x17A – 0x17B: Reserved.....	211
Receive Frame Header Status Register (0x17C – 0x17D): RXFHSR.....	211
Receive Frame Header Byte Count Register (0x17E – 0x17F): RXFHBCR.....	212
TXQ Command Register (0x180 – 0x181): TXQCR.....	213
RXQ Command Register (0x182 – 0x183): RXQCR.....	213
TX Frame Data Pointer Register (0x184 – 0x185): TXFDPR.....	214
RX Frame Data Pointer Register (0x186 – 0x187): RXFDPR.....	215
0x188 – 0x18B: Reserved.....	215
RX Duration Timer Threshold Register (0x18C – 0x18D): RXDTTR.....	215
RX Data Byte Count Threshold Register (0x18E – 0x18F): RXDBCTR.....	216
Internal I/O Register Space Mapping for Interrupt Registers (0x190 – 0x193).....	217
Interrupt Enable Register (0x190 – 0x191): IER.....	217
Interrupt Status Register (0x192 – 0x193): ISR.....	218
0x194 – 0x19B: Reserved.....	219
Internal I/O Register Space Mapping for the Queue Management Unit (QMU) (0x19C – 0x1B9).....	220
RX Frame Count and Threshold Register (0x19C – 0x19D): RXFCTR.....	220
TX Next Total Frames Size Register (0x19E – 0x19F): TXNTFSR.....	220
MAC Address Hash Table Register 0 (0x1A0 – 0x1A1): MAHTR0.....	220
Multicast Table Register 0.....	220
MAC Address Hash Table Register 1 (0x1A2 – 0x1A3): MAHTR1.....	221
Multicast Table Register 1.....	221
MAC Address Hash Table Register 2 (0x1A4 – 0x1A5): MAHTR2.....	221
Multicast Table Register 2.....	221
MAC Address Hash Table Register 3 (0x1A6 – 0x1A7): MAHTR3.....	221
Multicast Table Register 3.....	221
0x1A8 – 0x1AF: Reserved.....	221
Flow Control Low Water Mark Register (0x1B0 – 0x1B1): FCLWR.....	221
Flow Control High Water Mark Register (0x1B2 – 0x1B3): FCHWR.....	222
Flow Control Overrun Water Mark Register (0x1B4 – 0x1B5): FCOWR.....	222
RX Frame Count Register (0x1B8 – 0x1B9): RXFC.....	222
0x1BA – 0x1FF: Reserved.....	222

Internal I/O Register Space Mapping for Trigger Output Units (12 Units, 0x200 – 0x3FF)	223
Trigger Error Register (0x200 – 0x201): TRIG_ERR	223
Trigger Active Register (0x202 – 0x203): TRIG_ACTIVE	223
Trigger Done Register (0x204 – 0x205): TRIG_DONE	223
Trigger Enable Register (0x206 – 0x207): TRIG_EN	224
Trigger Software Reset Register (0x208 – 0x209): TRIG_SW_RST	224
Trigger Output Unit 12 Output PPS Pulse Width Register (0x20A – 0x20B): TRIG12_PPS_WIDTH	224
0x20C – 0x21F: Reserved	224
Trigger Output Unit 1 Target Time in Nanoseconds Low-Word Register (0x220 – 0x221): TRIG1_TGT_NSL	225
Trigger Output Unit 1 Target Time in Nanoseconds High-Word Register (0x222 – 0x223): TRIG1_TGT_NSH	225
Trigger Output Unit 1 Target Time in Seconds Low-Word Register (0x224 – 0x225): TRIG1_TGT_SL	225
Trigger Output Unit 1 Target Time in Seconds High-Word Register (0x226 – 0x227): TRIG1_TGT_SH	225
Trigger Output Unit 1 Configuration and Control Register 1 (0x228 – 0x229): TRIG1_CFG_1	226
Trigger Output Unit 1 Configuration and Control Register 2 (0x22A – 0x22B): TRIG1_CFG_2	228
Trigger Output Unit 1 Configuration and Control Register 3 (0x22C – 0x22D): TRIG1_CFG_3	228
Trigger Output Unit 1 Configuration and Control Register 4 (0x22E – 0x22F): TRIG1_CFG_4	228
Trigger Output Unit 1 Configuration and Control Register 5 (0x230 – 0x231): TRIG1_CFG_5	228
Trigger Output Unit 1 Configuration and Control Register 6 (0x232 – 0x233): TRIG1_CFG_6	229
Trigger Output Unit 1 Configuration and Control Register 7 (0x234 – 0x235): TRIG1_CFG_7	229
Trigger Output Unit 1 Configuration and Control Register 8 (0x236 – 0x237): TRIG1_CFG_8	229
0x238 – 0x23F: Reserved	229
Trigger Output Unit 2 Target Time and Output Configuration/Control Registers (0x240 – 0x257)	230
Trigger Output Unit 2 Configuration and Control Register 1 (0x248 – 0x249): TRIG2_CFG_1	230
0x258 – 0x25F: Reserved	230
Trigger Output Unit 3 Target Time and Output Configuration/Control Registers (0x260 – 0x277)	230
0x278 – 0x27F: Reserved	230
Trigger Output Unit 4 Target Time and Output Configuration/Control Registers (0x280 – 0x297)	230
0x298 – 0x29F: Reserved	230
Trigger Output Unit 5 Target Time and Output Configuration/Control Registers (0x2A0 – 0x2B7)	230
0x2B8 – 0x2BF: Reserved	230
Trigger Output Unit 6 Target Time and Output Configuration/Control Registers (0x2C0 – 0x2D7)	230
0x2D8 – 0x2DF: Reserved	230
Trigger Output Unit 7 Target Time and Output Configuration/Control Registers (0x2E0 – 0x2F7)	231
0x2F8 – 0x2FF: Reserved	231
Trigger Output Unit 8 Target Time and Output Configuration/Control Registers (0x300 – 0x317)	231
0x318 – 0x31F: Reserved	231
Trigger Output Unit 9 Target Time and Output Configuration/Control Registers (0x320 – 0x337)	231
0x338 – 0x33F: Reserved	231
Trigger Output Unit 10 Target Time and Output Configuration/Control Registers (0x340 – 0x357)	231
0x358 – 0x35F: Reserved	231
Trigger Output Unit 11 Target Time and Output Configuration/Control Registers (0x360 – 0x377)	231
0x378 – 0x37F: Reserved	231
Trigger Output Unit 12 Target Time and Output Configuration/Control Registers (0x380 – 0x397)	231
0x398 – 0x3FF: Reserved	231

Internal I/O Register Space Mapping for PTP Timestamp Inputs (12 Units, 0x400 – 0x5FF)	232
Timestamp Ready Register (0x400 – 0x401): TS_RDY	232
Timestamp Enable Register (0x402 – 0x403): TS_EN	232
Timestamp Software Reset Register (0x404 – 0x405): TS_SW_RST	232
0x406 – 0x41F: Reserved	232
Timestamp Unit 1 Status Register (0x420 – 0x421): TS1_STATUS	233
Timestamp Unit 1 Configuration and Control Register (0x422 – 0x423): TS1_CFG	233
Timestamp Unit 1 Input 1st Sample Time in Nanoseconds Low-Word Register (0x424 – 0x425):	
TS1_SMPL1_NSL	234
Timestamp Unit 1 Input 1st Sample Time in Nanoseconds High-Word Register (0x426 – 0x427):	
TS1_SMPL1_NSH	234
Timestamp Unit 1 Input 1st Sample Time in Seconds Low-Word Register (0x428 – 0x429):	
TS1_SMPL1_SL	234
Timestamp Unit 1 Input 1st Sample Time in Seconds High-Word Register (0x42A – 0x42B):	
TS1_SMPL1_SH	234
Timestamp Unit 1 Input 1st Sample Time in Sub-Nanoseconds Register (0x42C – 0x42D):	
TS1_SMPL1_SUB_NS	235
0x42E – 0x433: Reserved	235
Timestamp Unit 1 Input 2nd Sample Time in Nanoseconds Low-Word Register (0x434 – 0x435):	
TS1_SMPL2_NSL	235
Timestamp Unit 1 Input 2nd Sample Time in Nanoseconds High-Word Register (0x436 – 0x437):	
TS1_SMPL2_NSH	235
Timestamp Unit 1 Input 2nd Sample Time in Seconds Low-Word Register (0x438 – 0x439):	
TS1_SMPL2_SL	235
Timestamp Unit 1 Input 2nd Sample Time in Seconds High-Word Register (0x43A – 0x43B):	
TS1_SMPL2_SH	236
Timestamp Unit 1 Input 2nd Sample Time in Sub-Nanoseconds Register (0x43C – 0x43D):	
TS1_SMPL2_SUB_NS	236
0x43E – 0x43F: Reserved	236
Timestamp Unit 2 Status/Configuration/Control and Input 1st Sample Time Registers (0x440 – 0x44D)	236
0x44E – 0x453: Reserved	236
Timestamp Unit 2 Input 2nd Sample Time Registers (0x454 – 0x45D)	236
0x45E – 0x45F: Reserved	236
Timestamp Unit 3 Status/Configuration/Control and Input 1st Sample Time Registers (0x460 – 0x46D)	236
0x46E – 0x473: Reserved	236
Timestamp Unit 3 Input 2nd Sample Time Registers (0x474 – 0x47D)	237
0x47E – 0x47F: Reserved	237
Timestamp Unit 4 Status/Configuration/Control and Input 1st Sample Time Registers (0x480 – 0x48D)	237
0x48E – 0x493: Reserved	237
Timestamp Unit 4 Input 2nd Sample Time Registers (0x494 – 0x49D)	237
0x49E – 0x49F: Reserved	237
Timestamp Unit 5 Status/Configuration/Control and Input 1st Sample Time Registers (0x4A0 – 0x4AD)	237
0x4AE – 0x4B3: Reserved	237
Timestamp Unit 5 Input 2nd Sample Time Registers (0x4B4 – 0x4BD)	237
0x4BE – 0x4BF: Reserved	237
Timestamp Unit 6 Status/Configuration/Control and Input 1st Sample Time Registers (0x4C0 – 0x4CD)	237
0x4CE – 0x4D3: Reserved	237
Timestamp Unit 6 Input 2nd Sample Time Registers (0x4D4 – 0x4DD)	238
0x4DE – 0x4DF: Reserved	238
Timestamp Unit 7 Status/Configuration/Control and Input 1st Sample Time Registers (0x4E0 – 0x4ED)	238
0x4EE – 0x4F3: Reserved	238
Timestamp Unit 7 Input 2nd Sample Time Registers (0x4F4 – 0x4FD)	238
0x4FE – 0x4FF: Reserved	238
Timestamp Unit 8 Status/Configuration/Control and Input 1st Sample Time Registers (0x500 – 0x50D)	238
0x50E – 0x513: Reserved	238
Timestamp Unit 8 Input 2nd Sample Time Registers (0x514 – 0x51D)	238

0x51E – 0x51F: Reserved	238
Timestamp Unit 9 Status/Configuration/Control and Input 1st Sample Time Registers (0x520 – 0x52D).....	238
0x52E – 0x533: Reserved	238
Timestamp Unit 9 Input 2nd Sample Time Registers (0x534 – 0x53D)	239
0x53E – 0x53F: Reserved	239
Timestamp Unit 10 Status/Configuration/Control and Input 1st Sample Time Registers (0x540 – 0x54D).....	239
0x54E – 0x553: Reserved	239
Timestamp Unit 10 Input 2nd Sample Time Registers (0x554 – 0x55D)	239
0x55E – 0x55F: Reserved	239
Timestamp Unit 11 Status/Configuration/Control and Input 1st Sample Time Registers (0x560 – 0x56D).....	239
0x56E – 0x573: Reserved	239
Timestamp Unit 11 Input 2nd Sample Time Registers (0x574 – 0x57D)	239
0x57E – 0x57F: Reserved	239
Timestamp Unit 12 Status/Configuration/Control and Input 1st Sample Time Registers (0x580 – 0x58D).....	239
0x58E – 0x593: Reserved	239
Timestamp Unit 12 Input 2nd Sample Time Registers (0x594 – 0x59D)	240
0x59E – 0x5A3: Reserved	240
Timestamp Unit 12 Input 3rd Sample Time Registers (0x5A4 – 0x5AD)	240
0x5AE – 0x5B3: Reserved	240
Timestamp Unit 12 Input 4th Sample Time Registers (0x5B4 – 0x5BD)	240
0x5BE – 0x5C3: Reserved	240
Timestamp Unit 12 Input 5th Sample Time Registers (0x5C4 – 0x5CD)	240
0x5CE – 0x5D3: Reserved	240
Timestamp Unit 12 Input 6th Sample Time Registers (0x5D4 – 0x5DD)	240
0x5DE – 0x5E3: Reserved	240
Timestamp Unit 12 Input 7th Sample Time Registers (0x5E4 – 0x5ED)	240
0x5EE – 0x5F3: Reserved	240
Timestamp Unit 12 Input 8th Sample Time Registers (0x5F4 – 0x5FD).....	241
0x5FE – 0x5FF: Reserved	241
Internal I/O Register Space Mapping for PTP 1588 Clock and Global Control (0x600 – 0x7FF).....	242
PTP Clock Control Register (0x600 – 0x601): PTP_CLK_CTL	242
0x602 – 0x603: Reserved.....	242
PTP Real Time Clock in Nanoseconds Low-Word Register (0x604 – 0x605): PTP_RTC_NSL.....	243
PTP Real Time Clock in Nanoseconds High-Word Register (0x606 – 0x607): PTP_RTC_NSH	243
PTP Real Time Clock in Seconds Low-Word Register (0x608 – 0x609): PTP_RTC_SL	243
PTP Real Time Clock in Seconds High-Word Register (0x60A – 0x60B): PTP_RTC_SH	243
PTP Real Time Clock in Phase Register (0x60C – 0x60D): PTP_RTC_PHASE	244
0x60E – 0x60F: Reserved	244
PTP Rate in Sub-Nanoseconds Low-Word Register (0x610 – 0x611): PTP_SNS_RATE_L	244
PTP Rate in Sub-Nanoseconds High-Word and Control Register (0x612 – 0x613): PTP_SNS_RATE_H	245
PTP Temporary Adjustment Mode Duration in Low-Word Register (0x614 – 0x615): PTP_TEMP_ADJ_DURA_L.....	245
PTP Temporary Adjustment Mode Duration in High-Word Register (0x616 – 0x617): PTP_TEMP_ADJ_DURA_H	245
0x618 – 0x61F: Reserved	245
PTP Message Configuration 1 Register (0x620 – 0x621): PTP_MSG_CFG_1	246
PTP Message Configuration 2 Register (0x622 – 0x623): PTP_MSG_CFG_2.....	247
PTP Domain and Version Register (0x624 – 0x625): PTP_DOMAIN_VER	248
0x626 – 0x63F: Reserved	248
PTP Port 1 Receive Latency Register (0x640 – 0x641): PTP_P1_RX_LATENCY	248
PTP Port 1 Transmit Latency Register (0x642 – 0x643): PTP_P1_TX_LATENCY.....	249
PTP Port 1 Asymmetry Correction Register (0x644 – 0x645): PTP_P1_ASYM_COR.....	249
PTP Port 1 Link Delay Register (0x646 – 0x647): PTP_P1_LINK_DLY	249
PTP Port 1 Egress Timestamp Low-Word Register for Pdelay_Req and Delay_Req (0x648 – 0x649): P1_XDLY_REQ_TSL	249

PTP Port 1 Egress Timestamp High-Word Register for Pdelay_Req and Delay_Req (0x64A – 0x64B):	
P1_XDLY_REQ_TSH	250
PTP Port 1 Egress Timestamp Low-Word Register for Sync (0x64C – 0x64D): P1_SYNC_TSL	250
PTP Port 1 Egress Timestamp High-Word Register for Sync (0x64E – 0x64F): P1_SYNC_TSH	250
PTP Port 1 Egress Timestamp Low-Word Register for Pdelay_Resp (0x650 – 0x651): P1_PDLY_RESP_TSL	250
PTP Port 1 Egress Timestamp High-Word Register for Pdelay_Resp (0x652 – 0x653): P1_PDLY_RESP_TSH	250
0x654 – 0x65F: Reserved	251
PTP Port 2 Receive Latency Register (0x660 – 0x661): PTP_P2_RX_LATENCY	251
PTP Port 2 Transmit Latency Register (0x662 – 0x663): PTP_P2_TX_LATENCY	251
PTP Port 2 Asymmetry Correction Register (0x664 – 0x665): PTP_P2_ASYM_COR	251
PTP Port 2 Link Delay Register (0x666 – 0x667): PTP_P2_LINK_DLY	251
PTP Port 2 Egress Timestamp Low-Word Register for Pdelay_Req and Delay_Req (0x668 – 0x669):	
P2_XDLY_REQ_TSL	251
PTP Port 2 Egress Timestamp High-Word Register for Pdelay_Req and Delay_Req (0x66A – 0x66B):	
P2_XDLY_REQ_TSH	252
PTP Port 2 Egress Timestamp Low-Word Register for Sync (0x66C – 0x66D): P2_SYNC_TSL	252
PTP Port 2 Egress Timestamp High-Word Register for Sync (0x66E – 0x66F): P2_SYNC_TSH	252
PTP Port 2 Egress Timestamp Low-Word Register for Pdelay_Resp (0x670 – 0x671): P2_PDLY_RESP_TSL	252
PTP Port 2 Egress Timestamp High-Word Register for Pdelay_Resp (0x672 – 0x673): P2_PDLY_RESP_TSH	252
0x674 – 0x67F: Reserved	253
GPIO Monitor Register (0x680 – 0x681): GPIO_MONITOR	253
GPIO Output Enable Register (0x682 – 0x683): GPIO_OEN	253
0x684 – 0x687: Reserved	253
PTP Trigger Unit Interrupt Status Register (0x688 – 0x689): PTP_TRIG_IS	253
PTP Trigger Unit Interrupt Enable Register (0x68A – 0x68B): PTP_TRIG_IE	253
PTP Timestamp Unit Interrupt Status Register (0x68C – 0x68D): PTP_TS_IS	254
PTP Timestamp Unit Interrupt Enable Register (0x68E – 0x68F): PTP_TS_IE	254
0x690 – 0x733: Reserved	255
DSP Control 1 Register (0x734 – 0x735): DSP_CNTRL_6	255
0x736 – 0x747: Reserved	255
Analog Control 1 Register (0x748 – 0x749): ANA_CNTRL_1	255
Analog Control 3 Register (0x74C – 0x74D): ANA_CNTRL_3	256
0x74E – 0x7FF: Reserved	256
Management Information Base (MIB) Counters	257
MIB Counter Examples:	259
Additional MIB Information	259
Static MAC Address Table	260
Static MAC Table Lookup Examples:	261
Dynamic MAC Address Table	262
Dynamic MAC Address Lookup Example:	262
VLAN Table	263
VLAN Table Lookup Examples:	263
Absolute Maximum Ratings	264
Operating Ratings	264
Electrical Characteristics	264
Timing Specifications	268
Host Interface Read / Write Timing	268
Auto-Negotiation Timing	269
Trigger Output Unit and Timestamp Input Unit Timing	270
Serial EEPROM Interface Timing	272
Reset Timing and Power Sequencing	273
Reset Circuit Guidelines	274

Reference Circuits – LED Strap-In Pins.....	275
Reference Clock – Connection and Selection	276
Selection of Reference Crystal.....	276
Selection of Isolation Transformers.....	277
Package Information and Recommended Landing Pattern	278

List of Figures

Figure 1. Typical Straight Cable Connection	33
Figure 2. Typical Crossover Cable Connection	33
Figure 3. Auto Negotiation and Parallel Operation	34
Figure 4. Near-End and Far-End Loopback.....	36
Figure 5. Destination Address Lookup Flow Chart in Stage One	38
Figure 6. Destination Address Resolution Flow Chart in Stage Two	39
Figure 7. Tail Tag Frame Format	44
Figure 8. 802.1p Priority Field Format	48
Figure 9. Host TX Single Frame in Manual Enqueue Flow Diagram	52
Figure 10. Host RX Single or Multiple Frames in Auto-Dequeue Flow Diagram	55
Figure 11. PTP System Clock Overview	58
Figure 12. Trigger Output Unit Organization and Associated Registers.....	65
Figure 13. Timestamp Input Unit Organization and Associated Registers	66
Figure 14. Trigger Unit Interrupts	67
Figure 15. Timestamp Input Unit Interrupts	67
Figure 16. Complex Waveform Generation using Cascade Mode	71
Figure 17. Recommended Low-Voltage Power Connection using an External Low-Voltage-Regulator.....	75
Figure 18. Recommended Low-Voltage Power Connections using the Internal Low-Voltage Regulator	76
Figure 19. Traffic Activity and EEE	78
Figure 20. KSZ8462 8-Bit and 16-Bit Data Bus Connections	84
Figure 21. Interface and Register Mapping.....	86
Figure 22. Host Interface Read/Write Timing.....	268
Figure 23. Auto-Negotiation Timing	269
Figure 24. Trigger Output Unit and Timestamp Input Unit Timing	270
Figure 25. Serial EEPROM Timing	272
Figure 26. KSZ8462 Reset and Power Sequence Timing	273
Figure 27. Sample Reset Circuit	274
Figure 28. Recommended Reset Circuit for Interfacing with a CPU/FPGA Reset Output	274
Figure 29. Typical LED Strap-In Circuit	275
Figure 30. 25MHz Crystal and Oscillator Clock Connection Options	276

List of Tables

Table 1. MDI/MDI-X Pin Definitions	32
Table 2. MAC Address Filtering Scheme	42
Table 3. Spanning Tree States	43
Table 4. Tail Tag Rules	45
Table 5. FID + DA Lookup in VLAN Mode	46
Table 6. FID + SA Lookup in VLAN Mode	47
Table 7. Frame Format for Transmit Queue	50
Table 8. Transmit Control Word Bit Fields	50
Table 9. Transmit Byte Count Format	51
Table 10. Register Setting for Transmit Function Block	51
Table 11. Frame Format for Receive Queue	53
Table 12. Register Settings for Receive Function Block	54
Table 13. KSZ8462 GPIO Pin Resources	63
Table 14. Trigger Output Units and Timestamp Input Units Summary	64
Table 15. GPIO Pin Control Register Layout	64
Table 16. KSZ8462 Device Clocks	74
Table 17. Voltage Options and Requirements	75
Table 18. Power Management and Internal Blocks	77
Table 19. Available Interfaces	82
Table 20. Bus Interface Unit Signal Grouping	83
Table 21. KSZ8462 Serial EEPROM Format	85
Table 22. Mapping of Functional Areas within the Address Space	87
Table 23. Ingress or Egress Data Rate Limits	154
Table 24. Format of Per-Port MIB Counters	257
Table 25. Port 1 MIB Counters – Indirect Memory Offset	258
Table 26. "All Ports Dropped Packet" MIB Counter Format	259
Table 27. "All Ports Dropped Packet" MIB Counters– Indirect Memory Offsets	259
Table 28. Static MAC Table Format (8 Entries)	260
Table 29. Dynamic MAC Address Table Format (1024 Entries)	262
Table 30. VLAN Table Format (16 Entries)	263
Table 31. Host Interface Read/Write Timing Parameters	268
Table 32. Auto-Negotiation Timing Parameters	269
Table 33. Trigger Output Unit and Timestamp Input Unit Timing Parameters	271
Table 34. Serial EEPROM Timing Parameters	272
Table 35. Reset Timing Parameters	273
Table 36. Typical Reference Crystal Characteristics	276
Table 37. Transformer Selection Criteria	277
Table 38. Qualified Single Port Magnetic	277

Acronyms

BIU	Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU	Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS	Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC	Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
CUT-THROUGH SWITCH		A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet.
DA	Destination Address	The address to send packets.
DMA	Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EMI	Electromagnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS	Frame Check Sequence	See CRC.
FID	Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
GPIO	General Purpose Input/Output	General purpose input/output pins are signal pins that can be controlled or monitored by hardware and software to perform specific tasks.
IGMP	Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG	Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI	Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
ISA	Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
JUMBO PACKET		A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.

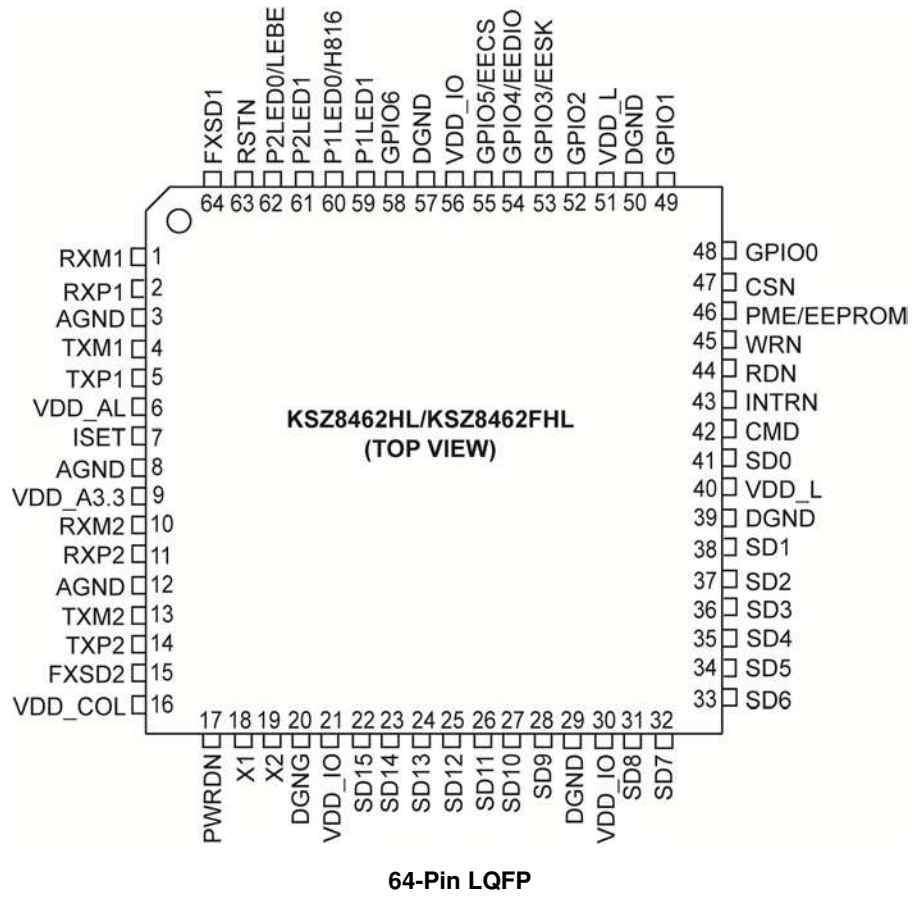
Acronyms (Continued)

MAC	Media Access Controller	A functional block responsible for implementing the Media Access Control layer which is a sub layer of the Data Link Layer.
MDI	Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore "media dependent".
MDI-X	Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB	Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII	Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC	Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID	Non-Port VLAN ID	The port VLAN ID value is used as a VLAN reference.
NRZ	Non-Return to Zero	A type of signal data encoding whereby the signal does not return to a zero state in between bits.
PHY		A device or functional block which performs the physical layer interface function in a network.
PLL	Phase-Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
PTP	Precision Time Protocol	A protocol, IEEE 1588 as applied to this device, for synchronizing the clocks of devices attached to a specific network.
QMU	Queue Management Unit	Manages packet traffic between the port 3 internal MAC and the system host (processor) interface. The QMU has built-in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue). For the QMU, "transmit" means into port 3 of the switch from the external host, and "receive" is from the switch to the external host. This terminology is the opposite of the terminology used for other KSZ8462 switch blocks.
SA	Source Address	The address from which information has been sent.
TSU	Timestamp Input Unit	The functional block which captures signals on the GPIO pins and assigns a time to the specific event.

Acronyms (Continued)

TDR	Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the whole or part of the signal to return.
TSU	Timestamp Input Unit	The functional block which captures signals on the GPIO pins and assigns a time to the specific event.
UTP	Unshielded Twisted Pair	Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.
VLAN	Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

Pin Configuration



Pin Description

Pin Number	Pin Name	Type	Pin Function
1	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential).
2	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential).
3	AGND	GND	Analog Ground.
4	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential).
5	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential).
6	VDD_AL	P	This pin is used as an input for the low-voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
7	ISET	O	Current Set: Sets the physical transmit output current. Pull–down this pin with a 6.49K Ω (1%) resistor to ground.
8	AGND	GND	Analog Ground.
9	VDD_A3.3	P	3.3V analog VDD input power supply (must be well decoupled).
10	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (– differential).
11	RXP2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential).
12	AGND	GND	Analog Ground.
13	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (– differential).
14	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential).
15	FXSD2	I	Fiber signal detect input for port 2 in 100BASE–FX fiber mode. When in copper mode, this input is unused and should be pulled to GND. Note: This functionality is available only on the KSZ8462FHL.
16	VDD_COL	P	This pin is used as a second input for the low-voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
17	PWRDN	IPU	Full–Chip Power–Down: Active Low (Low = power down; High or floating = normal operation). While this pin is asserted low, all I/O pins will be tri–stated. All registers will be set to their default state. While this pin is asserted, power consumption will be minimal. When the pin is de–asserted, power consumption will climb to nominal and the device will be in the same state as having been reset by the reset pin (RSTN, pin 63).
18	X1	I	25MHz Crystal or Oscillator Clock Connection: Pins (X1, X2) connect to a crystal or frequency oscillator source. If an oscillator is used, X1 connects to a VDD_IO voltage tolerant oscillator and X2 is a no connect. This clock requirement is ± 50 ppm.
19	X2	O	

Legend:

P = Power supply GND = Ground

I/O = Bi–directional I = Input O = Output.

IPD = Input with internal pull–down (58K $\pm 30\%$).

IPU = Input with internal pull–up (58K $\pm 30\%$).

OPD = Output with internal pull–down (58K $\pm 30\%$).

Opu = Output with internal pull–up (58K $\pm 30\%$).

IPU/O = Input with internal pull–up (58K $\pm 30\%$) during power–up/reset; output pin otherwise.

IPD/O = Input with internal pull–down (58K $\pm 30\%$) during power–up/reset; output pin otherwise.

I/O (PD) = Bi–directional Input/Output with internal pull–down (58K $\pm 30\%$).

I/O (pu) = Bi–directional Input/Output with internal pull–up (58K $\pm 30\%$).

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
20	DGND	GND	Digital Ground
21	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power pin for IO logic and the internal low-voltage regulator.
22	SD15/BE3	I/O (PD)	Shared Data Bus Bit[15] or BE3: This is data bit (D15) access when CMD = "0". This is Byte Enable 3 (BE3, 4th byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = "1". This pin must be tied to GND in 8-bit bus mode.
23	SD14/BE2	I/O (PD)	Shared Data Bus Bit[14] or BE2: This is data bit (D14) access when CMD = "0". This is Byte Enable 2 (BE2, 3rd byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = "1". This pin must be tied to GND in 8-bit bus mode.
24	SD13/BE1	I/O (PD)	Shared Data Bus Bit[13] or BE1: This is data bit (D13) access when CMD = "0". This is Byte Enable 1 (BE1, 2nd byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = "1". This pin must be tied to GND in 8-bit bus mode.
25	SD12/BE0	I/O (PD)	Shared Data Bus Bit[12] or BE0: This is data bit (D12) access when CMD = "0". This is Byte Enable 0 (BE0, 1st byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = "1". This pin must be tied to GND in 8-bit bus mode.
26	SD11	I/O (PD)	Shared Data Bus Bit[11]: This is data bit (D11) access when CMD = "0". Don't care when CMD = "1". This pin must be tied to GND in 8-bit bus mode.
27	SD10/A10	I/O (PD)	Shared Data Bus bit[10]: This is data bit (D10) access when CMD = "0". In 8-bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A10 access when CMD = "1".
28	SD9/A9	I/O (PD)	Shared Data Bus Bit[9] or A9: This is data bit (D9) access when CMD = "0". In 8-bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A9 access when CMD = "1".
29	DGND	GND	Digital Ground.
30	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power pin for IO logic and the internal low-voltage regulator.
31	SD8/A8	IPU/O	Shared Data Bus Bit[8] or A8: This is data bit (D8) access when CMD = "0". In 8-bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A8 access when CMD = "1".
32	SD7/A7	IPD/O	Shared Data Bus Bit[7] or A7: This is data bit (D7) access when CMD = "0". In 8-bit bus mode, this is address A7 (1 st write) or Don't care (2 nd write) access when CMD = "1". In 16-bit bus mode, this is address A7 access when CMD = "1".
33	SD6/A6	IPU/O	Shared Data Bus Bit[6] or A6: This is data bit (D6) access when CMD = "0". In 8-bit bus mode, this is address A6 (1 st write) or Don't care (2 nd write) access when CMD = "1". In 16-bit bus mode, this is address A6 access when CMD = "1".
34	SD5/A5	IPU/O	Shared Data Bus Bit[5] or A5: This is data bit (D5) access when CMD = "0". In 8-bit bus mode, this is address A5 (1 st write) or Don't care (2 nd write) access when CMD = "1". In 16-bit bus mode, this is address A5 access when CMD = "1".
35	SD4/A4	IPD/O	Shared Data Bus Bit[4] or A4: This is data bit (D4) access when CMD = "0". In 8-bit bus mode, this is address A4 (1 st write) or Don't care (2 nd write) access when CMD = "1". In 16-bit bus mode, this is address A4 access when CMD = "1".