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KSZ8462HL/KSZ8462FHL

IEEE 1588 Precision Time Protocol-Enabled Two-Port 10/100Mb/s Ethernet Switch with 8 or 16 Bit Host Interface

Revision 1.0

General Description

The KSZ8462 ETHERSYNCH™ product line consists of IEEE 1588v2-enabled Ethernet switches, providing integrated communications and synchronization for a range of industrial Ethernet applications.

The KSZ8462 ETHERSYNCH product enables distributed, daisy−chained topologies preferred for Industrial Ethernet networks. Conventional centralized (i.e., star−wired) topologies are also supported for dual−homed, fault tolerant arrangements.

A flexible 8- or 16−bit general bus interface is provided for interfacing to an external host processor.

The KSZ8462 devices incorporate the IEEE 1588v2 protocol. Sub-microsecond synchronization is available via the use of hardware based time stamping and transparent clocks making it the ideal solution for time synchronized Layer 2 communication in critical industrial applications.

Extensive general purpose I/O (GPIO) capabilities are available to use with the IEEE 1588v2 PTP to efficiently and accurately interface to locally-connected devices.

Complementing the industry's most-integrated IEEE 1588v2 device is a precision timing protocol (PTP) v2 software stack that has been pre−qualified with the KSZ84xx product family. The PTP stack has been optimized around the KSZ84xx chip architecture, and is available in source code format along with Micrel's chip driver.

The wire−speed, store−and−forward switching fabric provides a full complement of quality-of-service (QoS) and congestion control features optimized for real−time Ethernet.

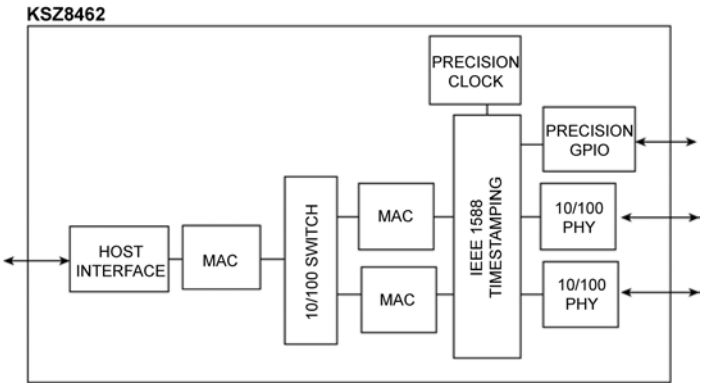
ETHERSYNCH™

The KSZ8462 product is built upon Micrel's industry−leading Ethernet technology, with features designed to offload host processing and streamline your overall design:

- Wire−speed Ethernet switching fabric with extensive filtering
- Two integrated 10/100BASE-TX PHY transceivers, featuring the industry's lowest power consumption
- Full−featured QoS support
- Flexible management options that support common standard interfaces

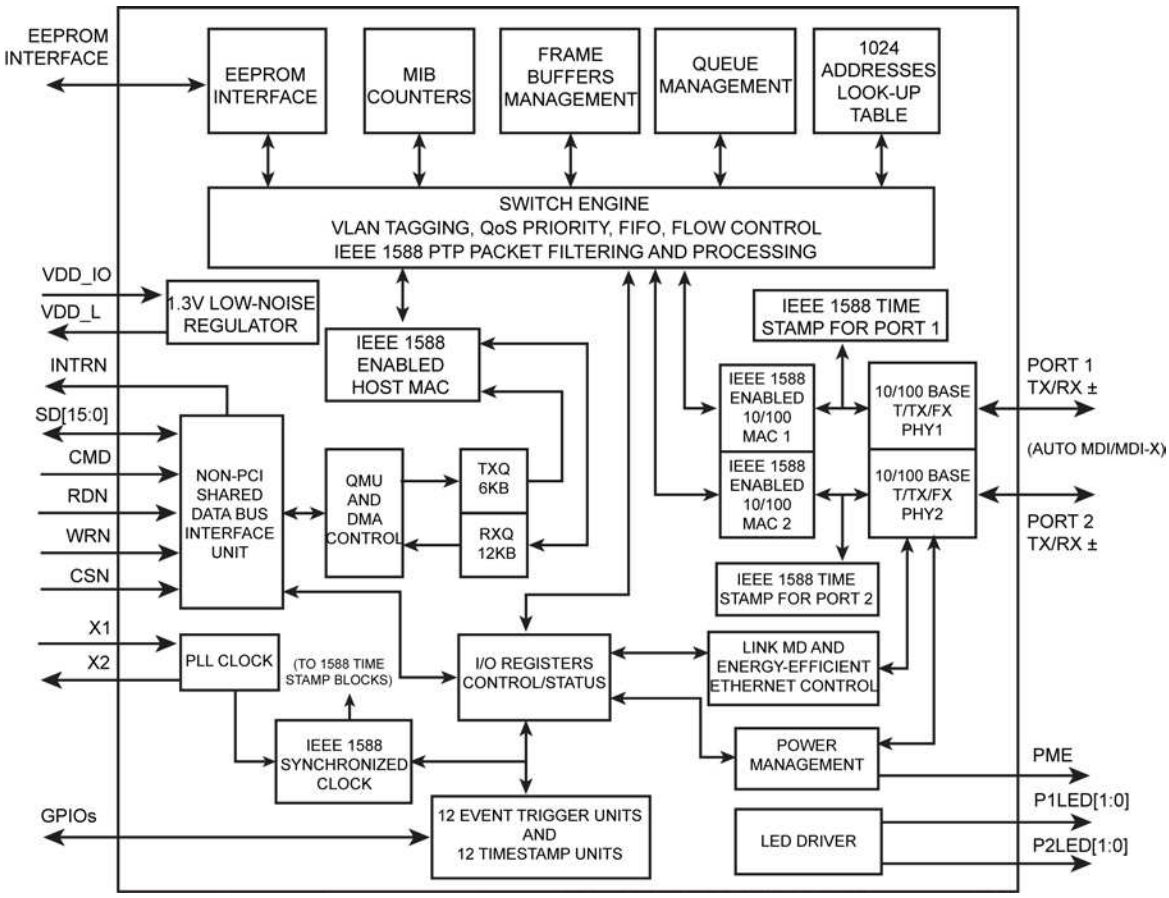
A robust assortment of power-management features including energy-efficient Ethernet (EEE) have been designed in to satisfy energy-efficient environments.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.



KSZ8462 Top Level Architecture

Functional Diagram



KSZ8462HL/KSZ8462FHL Functional Diagram

Features

Management Capabilities

- The KSZ8462 includes all the functions of a 10/100BASE−T/TX/FX switch system which combines a switch engine, frame buffer management, address look-up table, queue management, MIB counters, media access controllers (MAC) and PHY transceivers
- Non−blocking store−and−forward switch fabric assures fast packet delivery by utilizing 1024 entry forwarding table
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- MIB counters for fully-compliant statistics gathering − 34 counters per port
- Loopback modes for remote failure diagnostics
- Rapid spanning tree protocol support (RSTP) for topology management and ring/linear recovery

Robust PHY Ports

- Two integrated IEEE 802.3/802.3u compliant Ethernet transceivers supporting 10BASE-T and 100BASE-TX
- Copper and 100BASE-FX fiber mode support in the KSZ8462FHL
- Copper mode support in the KSZ8462HL
- On−chip termination resistors and internal biasing for differential pairs to reduce power
- HP Auto MDI/MDI−X crossover support eliminating the need to differentiate between straight or crossover cables in applications

MAC Ports

- Three internal media access control (MAC) units
- 2Kbyte jumbo packet support
- Tail tagging mode (one byte added before FCS) support at port 3 to inform the processor which ingress port receives the packet and its priority
- Programmable MAC addresses for port 1 and port 2 and self−address filtering support
- MAC filtering function to filter or forward unknown unicast packets
- Port 1 and port 2 MACs programmable as either end-to-end (E2E) or peer-to-peer (P2P) transparent clock (TC) ports for 1588 support

Advanced Switch Capabilities

- Non−blocking store−and−forward switch fabric assures fast packet delivery by utilizing 1024 entry forwarding table
- IEEE 802.1Q VLAN for up to 16 groups with full range of VLAN IDs
- IEEE 802.1p/Q tag insertion or removal on a per port basis (egress) and support double−tagging
- VLAN ID tag/untag options on per port basis
- Fully compliant with IEEE 802.3/802.3u standards
- IEEE 802.3x full−duplex with force mode option and half−duplex backpressure collision flow control
- IEEE 802.1w rapid spanning tree protocol support
- IGMP v1/v2/v3 snooping for multicast packet filtering
- QoS/CoS packets prioritization support: 802.1p, DiffServ−based and re−mapping of 802.1p priority field per port basis on four priority levels

IPv4/IPv6 QoS support

- IPv6 multicast listener discovery (MLD) snooping support
- Programmable rate limiting at the ingress and egress ports
- Broadcast storm protection
- 1K entry forwarding table with 32K frame buffer
- 4 priority queues with dynamic packet mapping for IEEE 802.1P, IPv4 TOS (DIFFSERV), IPv6 Traffic Class, etc.
- Source address filtering for implementing ring topologies

Comprehensive Configuration Registers Access

- Complete register access via the parallel host interface
- Facility to load MAC Address from EEPROM at power-up and reset time
- I/O pin strapping facility to set certain register bits from I/O pins at reset time
- Control registers configurable on−the−fly

IEEE 1588v2 PTP and Clock Synchronization

- Fully compliant with the IEEE 1588v2 precision time protocol
- One−step or two−step transparent clock (TC) timing corrections
- End-to-end (E2E) or peer-to-peer (P2P) transparent clock (TC)
- Grandmaster, master, slave, and ordinary clock (OC) support
- IEEE1588v2 PTP multicast and unicast frame support
- Transports of PTP over IPv4/IPv6 UDP and IEEE 802.3 Ethernet
- Delay request−response and peer delay mechanism
- Ingress/egress packet timestamp capture/recording and checksum update
- Correction field update with residence time and link delay
- IEEE1588v2 PTP packet filtering unit to reduce host processor overhead
- A 64-bit adjustable system precision clock
- 12 trigger output units and 12 timestamp input units available for flexible IEEE1588v2 control of 7 programmable GPIO[6:0] pins synchronized to the precision time clock
- GPIO pin usage for 1 PPS generation, frequency generator, control bit streams, event monitoring, precision pulse generation, complex waveform generation

Host Interface

- Selectable 8- or 16-bit wide interface
- Supports big- and little-endian processors
- Indirect data bus for data, address and byte enable to access any I/O registers and RX/TX FIFO buffers
- Large internal memory with 12Kbyte for RX FIFO and 6Kbytes for TX FIFO
- Programmable low, high and overrun water mark for flow control in RX FIFO
- Efficient architecture design with configurable host interrupt schemes to minimize host CPU overhead and utilization
- Queue management unit (QMU) supervises data transfers across this interface

Power and Power Management

- Single 3.3V power supply with optional VDD I/O for 1.8V, 2.5V or 3.3V
- Integrated low voltage (~1.3V) low-noise regulator (LDO) output for digital and analog core power.
- Supports IEEE P802.3az energy-efficient Ethernet (EEE) to reduce power consumption in transceivers in LPI state
- Full−chip hardware or software power down (all registers value are not saved and strap−in value will re−strap after release the power down)
- Energy detect power down (EDPD), which disables the PHY transceiver when cables are removed
- Wake-on-LAN supported with configurable packet control
- Dynamic clock tree control to reduce clocking in areas not in use
- Power consumption less than 0.5W

Additional Features

- Single 25MHz ±50ppm reference clock requirement
- Comprehensive programmable two LED indicators support for link, activity, full/half duplex and 10/100 speed
- LED pins directly controllable
- Industrial temperature range: –40°C to +85°C
- 64-pin, 10mm × 10mm, lead free, RoHS, LQFP package
- 0.11µm technology for lower power consumption

Applications

- Industrial Ethernet applications that employ IEEE 802.3-compliant MACs. (Ethernet/IP, Profinet, MODBUS TCP, etc)
- Real−time Ethernet networks requiring sub−microsecond synchronization over standard Ethernet
- IEC 61850 networks supporting power substation automation
- Networked measurement and control systems
- Industrial automation and motion control systems
- Test and measurement equipment

Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Description
KSZ8462HLI	–40°C to +85°C	64-Pin LQFP	Pb-Free	Industrial Temperature Device with Generic Host Interface
KSZ8462FHLI	–40°C to +85°C	64-Pin LQFP	Pb-Free	Industrial Temperature Device with Generic Host Interface and Fiber (100BASE-FX) support
KSZ8462HLI-EVAL	Evaluation Board with KSZ8462HLI. Also supports the KSZ8462FHLI.			

Revision History

Revision	Date	Summary of Changes
1.0	6/11/14	Initial release of KSZ8462HL/FHL product datasheet.

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Acronyms

BIU	Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU	Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS	Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC	Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
CUT-THROUGH SWITCH		A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut−through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut−through switches do not store the packet.
DA	Destination Address	The address to send packets.
DMA	Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EMI	Electromagnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS	Frame Check Sequence	See CRC.
FID	Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
GPIO	General Purpose Input/Output	General purpose input/output pins are signal pins that can be controlled or monitored by hardware and software to perform specific tasks.
IGMP	Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG	Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI	Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
ISA	Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
JUMBO PACKET		A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.

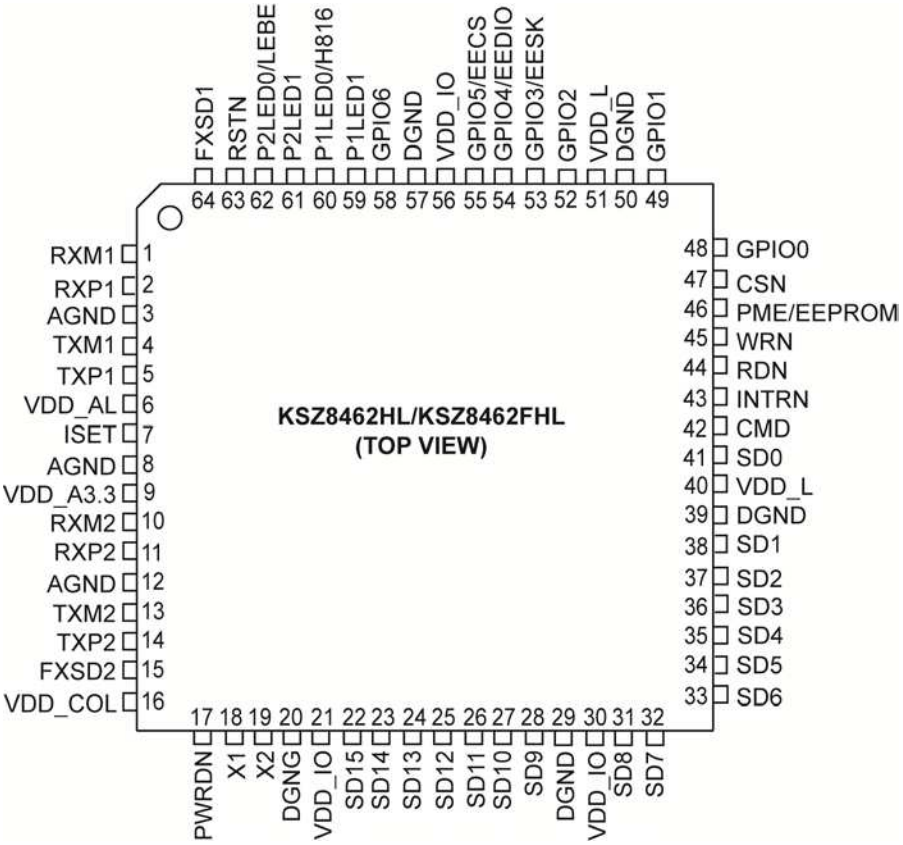
Acronyms (Continued)

MAC	Media Access Controller	A functional block responsible for implementing the Media Access Control layer which is a sub layer of the Data Link Layer.
MDI	Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null−modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore “media dependent”.
MDI-X	Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null−modem, or crossover, cable. For 10/100 full−duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI−X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB	Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII	Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC	Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID	Non-Port VLAN ID	The port VLAN ID value is used as a VLAN reference.
NRZ	Non-Return to Zero	A type of signal data encoding whereby the signal does not return to a zero state in between bits.
PHY		A device or functional block which performs the physical layer interface function in a network.
PLL	Phase-Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
PTP	Precision Time Protocol	A protocol, IEEE 1588 as applied to this device, for synchronizing the clocks of devices attached to a specific network.
QMU	Queue Management Unit	Manages packet traffic between the port 3 internal MAC and the system host (processor) interface. The QMU has built−in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue). For the QMU, “transmit” means into port 3 of the switch from the external host, and “receive” is from the switch to the external host. This terminology is the opposite of the terminology used for other KSZ8462 switch blocks.
SA	Source Address	The address from which information has been sent.
TSU	Timestamp Input Unit	The functional block which captures signals on the GPIO pins and assigns a time to the specific event.

Acronyms (Continued)

TDR	Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the whole or part of the signal to return.
TSU	Timestamp Input Unit	The functional block which captures signals on the GPIO pins and assigns a time to the specific event.
UTP	Unshielded Twisted Pair	Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.
VLAN	Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

Pin Configuration



64-Pin LQFP

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (− differential).
2	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential).
3	AGND	GND	Analog Ground.
4	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (− differential).
5	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential).
6	VDD_AL	P	This pin is used as an input for the low-voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
7	ISET	O	Current Set: Sets the physical transmit output current. Pull−down this pin with a 6.49KΩ (1%) resistor to ground.
8	AGND	GND	Analog Ground.
9	VDD_A3.3	P	3.3V analog VDD input power supply (must be well decoupled).
10	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (− differential).
11	RXP2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential).
12	AGND	GND	Analog Ground.
13	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (− differential).
14	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential).
15	FXSD2	I	Fiber signal detect input for port 2 in 100BASE−FX fiber mode. When in copper mode, this input is unused and should be pulled to GND. Note: This functionality is available only on the KSZ8462FHL.
16	VDD_COL	P	This pin is used as a second input for the low-voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
17	PWRDN	IPU	Full−Chip Power−Down**:** Active Low (Low = power down; High or floating = normal operation). While this pin is asserted low, all I/O pins will be tri−stated. All registers will be set to their default state. While this pin is asserted, power consumption will be minimal. When the pin is de−asserted, power consumption will climb to nominal and the device will be in the same state as having been reset by the reset pin (RSTN, pin 63).
18	X1	I	25MHz Crystal or Oscillator Clock Connection: Pins (X1, X2) connect to a crystal or frequency oscillator source. If an oscillator is used, X1 connects to a VDD_IO voltage tolerant oscillator and X2 is a no connect. This clock requirement is ±50ppm.
19	X2	O	

Legend:

P = Power supply GND = Ground

I/O = Bi−directional I = Input O = Output.

IPD = Input with internal pull−down (58K ±30%).

IPU = Input with internal pull−up (58K ±30%).

OPD = Output with internal pull−down (58K ±30%).

Opu = Output with internal pull−up (58K ±30%).

IPU/O = Input with internal pull−up (58K ±30%) during power−up/reset; output pin otherwise.

IPD/O = Input with internal pull−down (58K ±30%) during power−up/reset; output pin otherwise.

I/O (PD) = Bi−directional Input/Output with internal pull−down (58K ±30%).

I/O (pu) = Bi−directional Input/Output with internal pull−up (58K ±30%).

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
20	DGND	GND	Digital Ground
21	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power pin for IO logic and the internal low-voltage regulator.
22	SD15/BE3	I/O (PD)	Shared Data Bus Bit[15] or BE3: This is data bit (D15) access when CMD = “0”. This is Byte Enable 3 (BE3, 4th byte enable and active high) at double−word boundary access in 16−bit bus mode when CMD = “1”. This pin must be tied to GND in 8−bit bus mode.
23	SD14/BE2	I/O (PD)	Shared Data Bus Bit[14] or BE2: This is data bit (D14) access when CMD = “0”. This is Byte Enable 2 (BE2, 3rd byte enable and active high) at double−word boundary access in 16−bit bus mode when CMD = “1”. This pin must be tied to GND in 8−bit bus mode.
24	SD13/BE1	I/O (PD)	Shared Data Bus Bit[13] or BE1: This is data bit (D13) access when CMD = “0”. This is Byte Enable 1 (BE1, 2nd byte enable and active high) at double−word boundary access in 16−bit bus mode when CMD = “1”. This pin must be tied to GND in 8−bit bus mode.
25	SD12/BE0	I/O (PD)	Shared Data Bus Bit[12] or BE0: This is data bit (D12) access when CMD = “0”. This is Byte Enable 0 (BE0, 1st byte enable and active high) at double−word boundary access in 16−bit bus mode when CMD = “1”. This pin must be tied to GND in 8−bit bus mode.
26	SD11	I/O (PD)	Shared Data Bus Bit[11]: This is data bit (D11) access when CMD = “0”. Don’t care when CMD = “1”. This pin must be tied to GND in 8−bit bus mode.
27	SD10/A10	I/O (PD)	Shared Data Bus bit[10]: This is data bit (D10) access when CMD = “0”. In 8−bit bus mode, this pin must be tied to GND. In 16−bit bus mode, this is address A10 access when CMD = “1”.
28	SD9/A9	I/O (PD)	Shared Data Bus Bit[9] or A9: This is data bit (D9) access when CMD = “0”. In 8−bit bus mode, this pin must be tied to GND. In 16−bit bus mode, this is address A9 access when CMD = “1”.
29	DGND	GND	Digital Ground.
30	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power pin for IO logic and the internal low-voltage regulator.
31	SD8/A8	IPU/O	Shared Data Bus Bit[8] or A8: This is data bit (D8) access when CMD = “0”. In 8−bit bus mode, this pin must be tied to GND. In 16−bit bus mode, this is address A8 access when CMD = “1”.
32	SD7/A7	IPD/O	Shared Data Bus Bit[7] or A7: This is data bit (D7) access when CMD = “0”. In 8−bit bus mode, this is address A7 (1^{st} write) or Don’t care (2^{nd} write) access when CMD = “1”. In 16−bit bus mode, this is address A7 access when CMD = “1”.
33	SD6/A6	IPU/O	Shared Data Bus Bit[6] or A6: This is data bit (D6) access when CMD = “0”. In 8−bit bus mode, this is address A6 (1^{st} write) or Don’t care (2^{nd} write) access when CMD = “1”. In 16−bit bus mode, this is address A6 access when CMD = “1”.
34	SD5/A5	IPU/O	Shared Data Bus Bit[5] or A5: This is data bit (D5) access when CMD = “0”. In 8−bit bus mode, this is address A5 (1^{st} write) or Don’t care (2^{nd} write) access when CMD = “1”. In 16−bit bus mode, this is address A5 access when CMD = “1”.
35	SD4/A4	IPD/O	Shared Data Bus Bit[4] or A4: This is data bit (D4) access when CMD = “0”. In 8−bit bus mode, this is address A4 (1^{st} write) or Don’t care (2^{nd} write) access when CMD = “1”. In 16−bit bus mode, this is address A4 access when CMD = “1”.