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# KSZ8463ML/RL/FML/FRL

## IEEE 1588 Precision Time Protocol-Enabled, Three-Port, 10/100-Managed Switch with MII or RMII

**Revision 1.0**

## General Description

The KSZ8463 ETHERSYNCH™ product line consists of IEEE 1588v2 enabled Ethernet switches, providing integrated communications and synchronization for a range of Industrial Ethernet applications.

The KSZ8463 ETHERSYNCH product line enables distributed, daisy-chained topologies preferred for Industrial Ethernet networks. Conventional centralized (i.e., star-wired) topologies are also supported for dual-homed, fault-tolerant arrangements.

A flexible set of standard MAC interfaces is provided to interface to external host processors with embedded Ethernet MACs:

- KSZ8463ML: Media Independent Interface (MII)
- KSZ8463RL: Reduced Media Independent Interface (RMII)
- KSZ8463FML: MII, supports 100BASE-FX fiber in addition to 10/100BASE-TX copper
- KSZ8463FRL: RMII, supports 100BASE-FX fiber in addition to 10/100BASE-TX copper

The KSZ8463 devices incorporate the IEEE 1588v2 protocol. Sub-microsecond synchronization is available via the use of hardware-based time-stamping and transparent clocks making it the ideal solution for time synchronized Layer 2 communication in critical industrial applications.

Extensive general purpose I/O (GPIO) capabilities are available to use with the IEEE 1588v2 PTP to efficiently and accurately interface to locally connected devices.

Complementing the industry's most-integrated IEEE 1588v2 device is a precision timing protocol (PTP) v2 software stack that has been pre-qualified with the KSZ84xx product family. The PTP stack has been optimized around the KSZ84xx chip architecture, and is available in source code format along with Micrel's chip driver.

**ETHERSYNCH™**

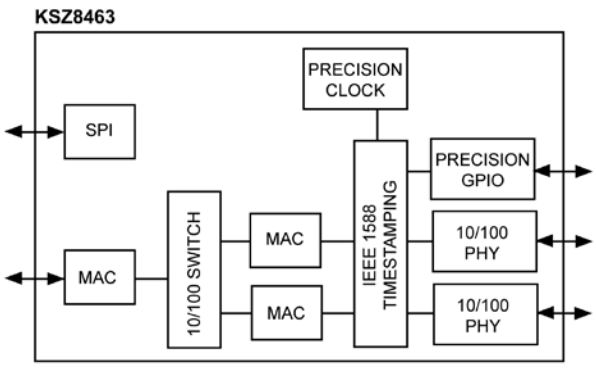
The KSZ8463 product line is built upon Micrel's industry-leading Ethernet technology, with features designed to offload host processing and streamline your overall design.

- Wire-speed Ethernet switching fabric with extensive filtering
- Two integrated 10/100BASE-TX PHY transceivers, featuring the industry's lowest power consumption
- Full-featured quality-of-service (QoS) support
- Flexible management options that support common standard interfaces

The wire-speed, store-and-forward switching fabric provides a full complement of QoS and congestion control features optimized for real-time Ethernet.

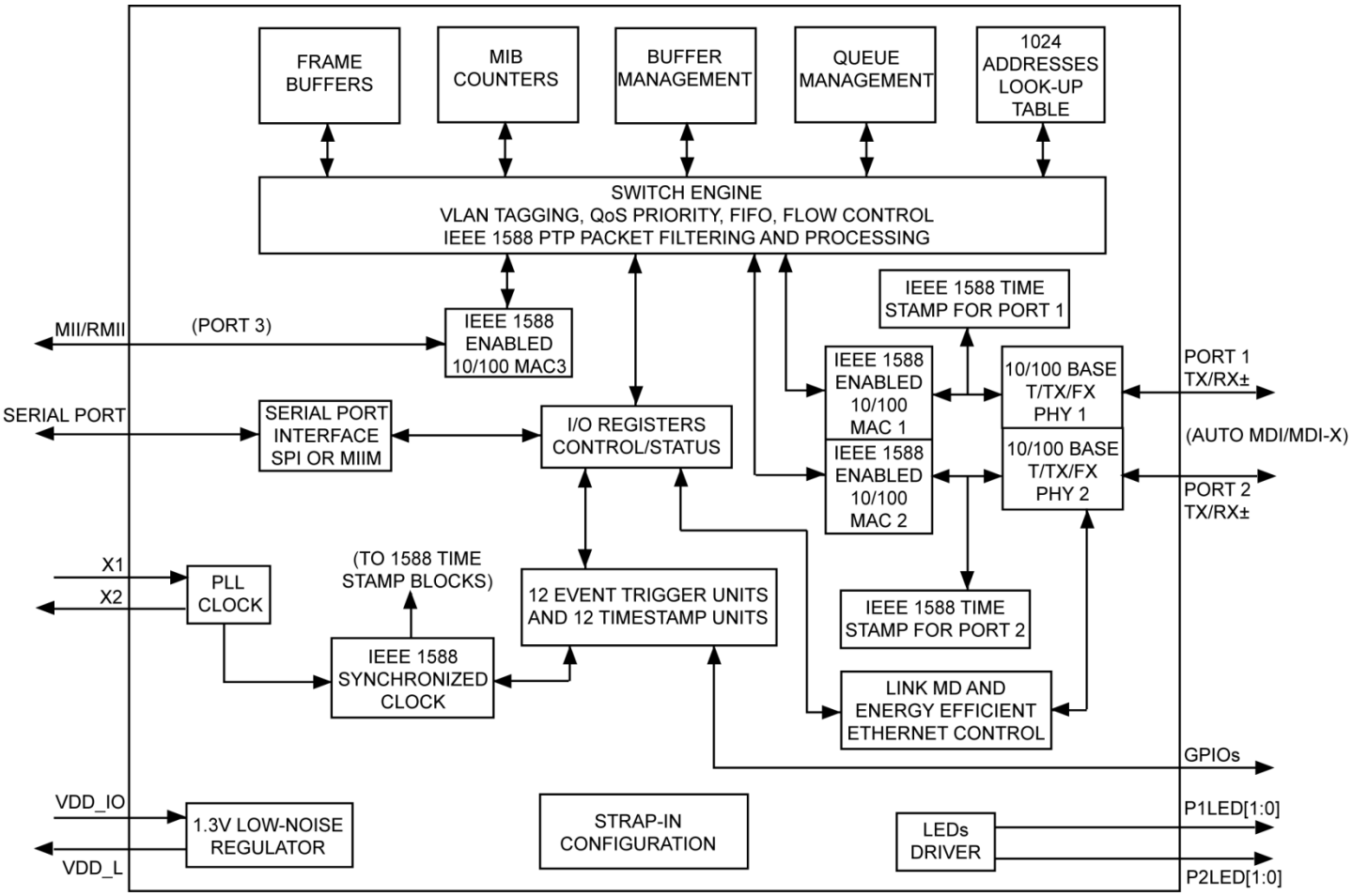
A robust assortment of power-management features including energy-efficient Ethernet (EEE) have been designed in to satisfy energy efficient environments.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.




**Functional Diagram**

## Functional Diagram




**KSZ8463ML/RL/FML/FRL Functional Diagram**

# Features

### Management Capabilities

- The KSZ8463ML/RL/FML/FRL includes all the functions of a 10/100BASE-T/TX/FX switch system which combines a switch engine, frame buffer management, address look-up table, queue management, MIB counters, media access controllers (MAC) and PHY transceivers
- Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 1024 entry forwarding table
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- MIB counters for fully-compliant statistics gathering – 34 counters per port
- Loopback modes for remote failure diagnostics
- Rapid spanning tree protocol support (RSTP) for topology management and ring/linear recovery
- Bypass mode, which ensure continuity even when a Host is disabled or fails

### Robust PHY Ports

- Two integrated IEEE 802.3/802.3u-compliant Ethernet transceivers supporting 10BASE-T and 100BASE-TX
- Copper and 100BASE-FX fiber mode support in the KSZ8463FML and KSZ8463FRL
- Copper mode support in the KSZ8463ML and KSZ8463RL
- On-chip termination resistors and internal biasing for differential pairs to reduce power
- HP Auto MDI/MDI-X crossover support eliminating the need to differentiate between straight or crossover cables in applications

### MAC Ports

- Three internal media access control (MAC) units
- MII or RMII interface support on MAC port 3
- 2Kbyte jumbo packet support
- Tail tagging mode (one byte added before FCS) support at port 3 to inform the processor which ingress port receives the packet and its priority
- Supports reduced media independent interface (RMII) with 50MHz reference clock input or output
- Support Media Independent Interface (MII) in either PHY mode or MAC mode on port 3
- Programmable MAC addresses for port 1 and port 2 and self-address filtering support
- MAC filtering function to filter or forward unknown unicast packets
- Port 1 and port 2 MACs programmable as either E2E or P2P transparent clock (TC) ports for 1588 support
- Port 3 MAC programmable as slave or master of ordinary clock (OC) port for 1588 support
- Micrel LinkMD® cable diagnostic capabilities for determining cable opens, shorts, and length

### Advanced Switch Capabilities

- Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 1024 entry forwarding table
- IEEE 802.1Q VLAN for up to 16 groups with full range of VLAN IDs
- IEEE 802.1p/Q tag insertion or removal on a per port basis (egress) and support double-tagging
- VLAN ID tag/untag options on per port basis
- Fully compliant with IEEE 802.3/802.3u standards
- IEEE 802.3x full-duplex with force-mode option and half-duplex backpressure collision flow control
- IEEE 802.1w rapid spanning tree protocol support
- IGMP v1/v2/v3 snooping for multicast packet filtering
- QoS/CoS packets prioritization support: 802.1p, DiffServ-based and re-mapping of 802.1p priority field per-port basis on four priority levels
- IPv4/IPv6 QoS support
- IPv6 multicast listener discovery (MLD) snooping support
- Programmable rate limiting at the ingress and egress ports
- Broadcast storm protection
- Bypass mode to sustain the switch function between port 1 and port 2 when CPU (port 3) goes into sleep mode
- 1K entry forwarding table with 32K frame buffer
- Four priority queues with dynamic packet mapping for IEEE 802.1p, IPv4 TOS (DIFFSERV), IPv6 Traffic Class, etc.
- Source address filtering for implementing ring topologies

**Comprehensive Configuration Registers Access**

- High-speed SPI (4-wire, up to 50 MHz) Interface to access all internal registers
- MII Management (MIIM, MDC/MDIO 2-wire) Interface to access all PHY registers per clause 22.2.4.5 of the IEEE 802.3 specification
- I/O pin strapping facility to set certain register bits from I/O pins at reset time
- Control registers configurable on-the-fly

**IEEE 1588v2 PTP and Clock Synchronization**

- Fully compliant with the IEEE 1588v2 precision time protocol
- One-step or two-step transparent clock (TC) timing corrections
- E2E (end-to-end) or P2P (peer-to-peer) transparent clock (TC)
- Grandmaster, master, slave, ordinary clock (OC) support
- IEEE1588v2 PTP Multicast and Unicast frame support
- Transports of PTP over IPv4/IPv6 UDP and IEEE 802.3 Ethernet
- Delay request-response and peer delay mechanism
- Ingress/egress packet timestamp capture/recording and checksum update
- Correction field update with residence time and link delay
- IEEE1588v2 PTP packet filtering unit to reduce host processor overhead
- A 64-bit adjustable system precision clock
- Twelve trigger output units and twelve timestamp input units available for flexible IEEE1588v2 control of twelve programmable GPIO[11:0] pins synchronized to the precision time clock
- GPIO pin usage for 1 PPS generation, frequency generator, control bit streams, event monitoring, precision pulse generation, complex waveform generation

**Power and Power Management**

- Single 3.3V power supply with optional VDD I/O for 1.8V, 2.5V or 3.3V
- Integrated low voltage (~1.3V) low-noise regulator (LDO) output for digital and analog core power
- Supports IEEE P802.3az™ energy-efficient Ethernet (EEE) to reduce power consumption in transceivers in LPI state
- Full-chip hardware or software power-down (all registers value are not saved and strap-in value will re-strap after release the power-down)
- Energy detect power-down (EDPD), which disables the PHY transceiver when cables are removed
- Dynamic clock tree control to reduce clocking in areas not in use
- Power consumption less than 0.5W

**Additional Features**

- Single 25MHz ±50ppm reference clock requirement for MII mode
- Selectable 25MHz or 50MHz inputs for RMII mode
- Comprehensive programmable two LED indicators support for link, activity, full/half duplex and 10/100 speed.
- LED pins directly controllable.
- Industrial temperature range: –40°C to +85°C
- 64-pin (10mm x 10mm) lead free (ROHS) LQFP package
- 0.11µm technology for lower power consumption

## Applications

- Industrial Ethernet applications that employ IEEE 802.3-compliant MACs. (Ethernet/IP, Profinet, MODBUS TCP, etc)
- Real-time Ethernet networks requiring sub-microsecond synchronization over standard Ethernet
- IEC 61850 networks supporting power substation automation
- Networked measurement and control systems
- Industrial automation and motion control systems
- Test and measurement equipment

## Ordering Information

| Part Number | Temperature Range | Package | Lead Finish | Description |
|---|---|---|---|---|
| KSZ8463MLI | –40°C to +85°C | 64-Pin LQFP | Pb-Free | Industrial Temperature Device with MII Interface |
| KSZ8463FMLI | –40°C to +85°C | 64-Pin LQFP | Pb-Free | Industrial Temperature Device with MII Interface and Fiber (100BASE-FX) support |
| KSZ8463RLI | –40°C to +85°C | 64-Pin LQFP | Pb-Free | Industrial Temperature Device with RMII Interface |
| KSZ8463FRLI | –40°C to +85°C | 64-Pin LQFP | Pb-Free | Industrial Temperature Device with RMII Interface and Fiber (100BASE-FX) support |
| KSZ8463MLI-EVAL | Evaluation Board with KSZ8463MLI. Also supports KSZ8463FMLI, KSZ8463RLI and KSZ8463FRLI. | | | |

## Revision History

| Revision | Date | Summary of Changes |
|---|---|---|
| 1.0 | 6/11/14 | Initial release of product – S. Thompson |
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## Acronyms

| | | |
|---|---|---|
| **BIU** | Bus Interface Unit | The host interface function that performs code conversion, buffering, and the like required for communications to and from a network. |
| **BPDU** | Bridge Protocol Data Unit | A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination. |
| **CMOS** | Complementary Metal Oxide Semiconductor | A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip. |
| **CRC** | Cyclic Redundancy Check | A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long. |
| **CUT-THROUGH SWITCH** | | A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet. |
| **DA** | Destination Address | The address to send packets. |
| **EMI** | Electro-Magnetic Interference | A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI. |
| **FCS** | Frame Check Sequence | See CRC. |
| **FID** | Frame or Filter ID | Specifies the frame identifier. Alternately is the filter identifier. |
| **GPIO** | General Purpose Input/Output | General Purpose Input/Output pins are signal pins that can be controlled or monitored by hardware and software to perform specific tasks. |
| **IGMP** | Internet Group Management Protocol | The protocol defined by RFC 1112 for IP multicast transmissions. |
| **IPG** | Inter-Packet Gap | A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity. |
| **ISI** | Inter-Symbol Interference | The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other. |
| **ISA** | Industry Standard Architecture | A bus architecture used in the IBM PC/XT and PC/AT. |
| **Jumbo Packet** | | A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc. |
| **MAC** | Media Access Controller | a functional block responsible for implementing the media access control layer which is a sub layer of the data link layer. |

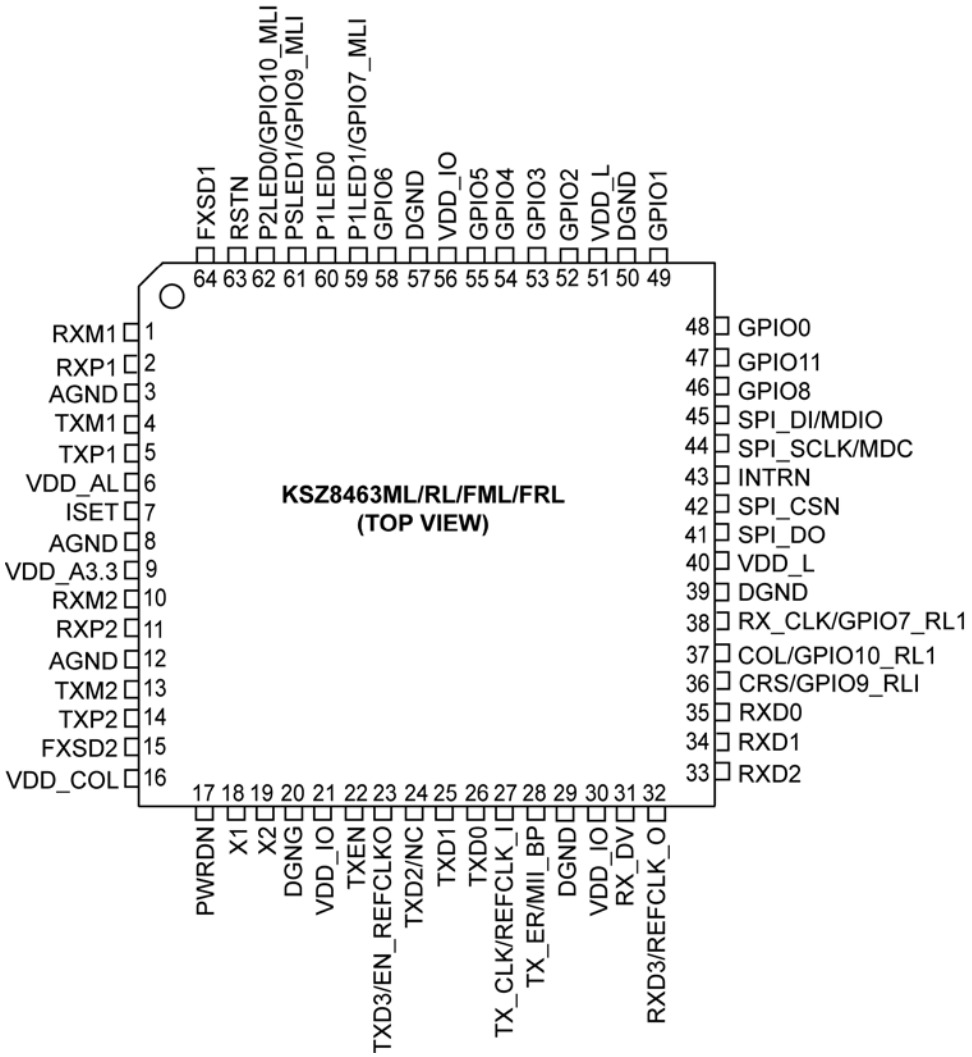
## Acronyms (Continued)

| | | |
|---|---|---|
| **MDI** | Medium Dependent Interface | An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore “media dependent”. |
| **MDI-X** | Medium Dependent Interface Crossover | An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion. |
| **MIB** | Management Information Base | The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses). |
| **MII** | Media Independent Interface | The MII accesses PHY registers as defined in the IEEE 802.3 specification. |
| **NIC** | Network Interface Card | An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks. |
| **NPVID** | Non-Port VLAN ID | The port VLAN ID value is used as a VLAN reference. |
| **NRZ** | Non-Return to Zero | A type of signal data encoding whereby the signal does not return to a zero state in between bits. |
| **PHY** | | A device or functional block which performs the physical layer interface function in a network. |
| **PLL** | Phase-Locked Loop | An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency. |
| **PTP** | Precision Time Protocol | A protocol, IEEE 1588 as applied to this device, for synchronizing the clocks of devices attached to a specific network. |
| **SA** | Source Address | The address from which information has been sent. |
| **TDR** | Time Domain Reflectometry | TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal -- or part of the signal -- to return. |
| **TSU** | Timestamp Input Unit | The functional block which captures signals on the GPIO pins and assigns a time to the specific event. |
| **TOU** | Trigger Output Unit | The functional block which generates user configured waveforms on a specified GPIO pin at a specific trigger time. |

## Acronyms (Continued)

| | | |
|---|---|---|
| **UTP** | Unshielded Twisted Pair | Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required. |
| **VLAN** | Virtual Local Area Network | A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere. |

## Pin Configuration




**64-Pin LQFP**

## Pin Description

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 1 | RXM1 | I/O | Port 1 physical receive (MDI) or transmit (MDIX) signal (- differential). |
| 2 | RXP1 | I/O | Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential). |
| 3 | AGND | GND | Analog Ground. |
| 4 | TXM1 | I/O | Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential). |
| 5 | TXP1 | I/O | Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential). |
| 6 | VDD_AL | P | This pin is used as an input for the Low Voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors. |
| 7 | ISET | O | Set physical transmits output current.<br>Pull-down this pin with a 6.49KΩ (1%) resistor to ground. |
| 8 | AGND | GND | Analog Ground. |
| 9 | VDD_A3.3 | P | 3.3V analog VDD input power supply (Must be well decoupled). |
| 10 | RXM2 | I/O | Port 2 physical receive (MDI) or transmit (MDIX) signal (- differential). |
| 11 | RXP2 | I/O | Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential). |
| 12 | AGND | GND | Analog Ground. |
| 13 | TXM2 | I/O | Port 2 physical transmit (MDI) or receive (MDIX) signal (– differential). |
| 14 | TXP2 | I/O | Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential). |
| 15 | FXSD2 | I | Fiber signal detect input for port 2 in 100BASE-FX fiber mode. When in copper mode, this input is unused and should be pulled to GND.<br>Note: This functionality is available only on the KSZ8463FML/FRL devices. |
| 16 | VDD_COL | P | This pin is used as a second input for the low-voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors. |
| 17 | PWRDN | IPU | **Full-Chip Power-Down.**<br>Active Low (Low = Power-down; High or floating = Normal operation).<br>While this pin is asserted low, all I/O pins will be tri-stated. All registers will be set to their default state. While this pin is asserted, power consumption will be minimal. When the pin is de-asserted, power consumption will climb to nominal and the device will be in the same state as having been reset by the reset pin (RSTN, pin 63). |

**Legend:**

P = Power supply GND = Ground.

I/O = Bi-directional: I = Input, O = Output.

IPD = Input with internal pull-down (58K ±30%).

IPU = Input with internal pull-up (58K ±30%).

OPD = Output with internal pull-down (58K ±30%).

OPU = Output with internal pull-up (58K ±30%).

IPU/O = Input with internal pull-up (58K ±30%) during power-up/reset; output pin otherwise.

IPD/O = Input with internal pull-down (58K ±30%) during power-up/reset; output pin otherwise.

I/O (PD) = Bi-directional input/output with internal pull-down (58K ±30%).

I/O (PU) = Bi-directional input/output with internal pull-up (58K ±30%).

## Pin Description (Continued)

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 18 | X1 | I | **25MHz Crystal or Oscillator Clock Connection.**<br>Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a VDD_IO voltage tolerant oscillator and X2 is a no connect. This clock requirement is ±50ppm.<br>The KSZ8463RL has the option to use REFCLK_I (50MHz) as its primary clock input instead of X1 and X2. This is determined by the state of pin 41 (SPI_DO) at power-up/reset time. See *Strapping Options* section for details. (Applies to the KSZ8463RL/FRL devices only) |
| 19 | X2 | O | |
| 20 | DGND | GND | Digital Ground. |
| 21 | VDD_IO | P | 3.3V, 2.5V, or 1.8V digital VDD input power pin for IO logic and the internal low-voltage regulator. |
| 22 | TX_EN | IPD | **(8463ML, 8463FML) – MII Mode:**<br>Transmit Enable. Active high input indicates there is valid transmit data on TXD[3:0].<br>**(8463RL, 8463FRL) – RMII Mode:**<br>Transmit Enable. Active high indicates there is valid transmit data on TXD[1:0]. |
| 23 | TXD3/<br>EN_REFCLKO | IPD | **(8463ML, 8463FML) – MII Mode:**<br>Transmit data input bit[3]. This data is synchronous to the TX_CLK (2.5 MHz in 10BT mode or 25MHz in 100BT mode)<br>**(8463RL, 8463FRL) – RMII Mode:**<br>EN_REFCLKO is used to enable REFCLK_O output on pin 32. If pulled up, the REFCLK_O output is enabled. If pulled down to disable, the REFCLK_O output is disabled. |
| 24 | TXD2/NC | IPD | **(8463ML, 8463FML) – MII Mode:**<br>Transmit data input bit[2]. This data is synchronous to TX_CLK (2.5MHz in 10BT mode or 25MHz in 100BT mode).<br>**(8463RL, 8463FRL) – RMII Mode:**<br>No connect. Is not used. |
| 25 | TXD1 | IPD | **(8463ML, 8463FML) – MII Mode:**<br>Transmit data input bit[1]. This data is synchronous to TX_CLK (2.5MHz in 10BT mode or 25MHz in 100BT mode).<br>**(8463RL, 8463FRL) – RMII Mode:**<br>Transmit data input bit[1]. This data is synchronous to REFCLK (50MHz). |
| 26 | TXD0 | IPD | **(8463ML, 8463FML) – MII Mode:**<br>Transmit data input bit[0]. This data is synchronous to TX_CLK (2.5MHz in 10BT mode or 25MHz in 100BT mode).<br>**(8463RL, 8463FRL) – RMII Mode:**<br>Transmit data input bit[0]. This data is synchronous to REFCLK (50MHz). |
| 27 | TX_CLK/<br>REFCLK_I | I/O(PD) | **(8463ML, 8463FML) – MII Mode:**<br>Transmit clock. This is the output clock in PHY MII mode and input clock in MAC MII mode (2.5MHz in 10BT mode or 25MHz in 100BT mode).<br>**(8463RL, 8463FRL) – RMII Mode:**<br>Reference input clock (50MHz). |
| 28 | TX_ER/<br>MII_BP | IPD | **(8463ML, 8463FML) – MII Mode:**<br>Transmit error input in MII MAC mode.<br>In MII PHY mode:<br>1 = Disable the MII PHY mode link and enable the bypass mode.<br>0 = Set MII PHY mode in normal operation.<br>**(8463RL, 8463FRL) – RMII Mode:**<br>No connect. Not used. |

## Pin Description (Continued)

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 29 | DGND | GND | Digital Ground. |
| 30 | VDD_IO | P | 3.3V, 2.5V, or 1.8V digital VDD input power pin for IO logic and the internal low-voltage regulator. |
| 31 | RX_DV | IPU/O | **(8463ML, 8463FML) – MII Mode:**<br>Receive data valid, active high indicates that receive data on RXD[3:0] is valid.<br>**(8463RL, 8463FRL) – RMII Mode:**<br>Receive data valid, active high indicates that receive data on RXD[1:0] is valid.<br>**Config Mode:**<br>This pin is pulled up or down and its value is latched during the power-up / reset to select either PHY MII mode or MAC MII mode. See *Strapping Options* section for details. |
| 32 | RXD3/<br>REFCLK_O | IPD/O | **(8463ML, 8463FML) – MII Mode:**<br>Receive data output bit[3]. This data is synchronous to RX_CLK (2.5MHz in 10BT mode or 25MHz in 100BT mode)<br>**(8463RL, 8463FRL) – RMII Mode:**<br>REFCLK_O (50MHz) output when EN_REFCLKO (pin 23) is pulled-up. (16 ma. drive) |
| 33 | RXD2 | IPU/O | **(8463ML, 8463FML) – MII Mode:**<br>Receive data output bit[2]. This data is synchronous to RX_CLK (2.5MHz in 10BT mode or 25MHz in 100BT mode)<br>**(8463RL, 8463FRL) – RMII Mode:**<br>Not used.<br>**Config Mode:**<br>This pin is pulled up or down via an external resistor and its value is latched during power-up/reset to select either high-speed SPI or low-speed SPI mode. See *Strapping Options* section for details. |
| 34 | RXD1 | IPU/O | **(8463ML, 8463FML) – MII Mode:**<br>Receive data output bit[1]. This data is synchronous to RX_CLK (2.5MHz in 10BT mode or 25MHz in 100BT mode)<br>**(8463RL, 8463FRL) – RMII Mode:**<br>Receive data output bit[1]. This data is synchronous to REFCLK (50MHz).<br>**Config Mode:**<br>This pin is pulled up or down via an external resistor and its value is latched during power-up/reset to select serial bus mode. See *Strapping Options* section for details. |
| 35 | RXD0 | IPD/O | **(8463ML, 8463FML) – MII Mode:**<br>Receive data output bit[0]. This data is synchronous to RX_CLK (2.5MHz in 10BT mode or 25MHz in 100BT mode)<br>**(8463RL, 8463FRL) – RMII Mode:**<br>Receive data output bit[0]. This data is synchronous to REFCLK (50MHz).<br>**Config Mode:**<br>This pin is pulled up or down via an external resistor and its value is latched during power-up/reset to select serial bus mode. See *Strapping Options* section for details. |
| 36 | CRS/<br>GPIO9_RLI | I/O(PD) | **(8463ML, 8463FML) – MII Mode:**<br>Carrier Sense. This is an output signal in PHY MII mode and an input signal in MAC MII mode.<br>**(8463RL, 8463FRL) – RMII Mode:**<br>This is GPIO9 while in RMII mode. (Refer to GPIO0 pin 48 description). |

## Pin Description (Continued)

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 37 | COL/ GPIO10_RLI | I/O(PD) | **(8463ML, 8463FML) – MII Mode:**<br>Collision Detect. This is an output signal in PHY MII mode and an input signal in MAC MII mode.<br>**(8463RL, 8463FRL) – RMII Mode:**<br>This is GPIO10 while in RMII Mode. (Refer to GPIO0 pin 48 description). |
| 38 | RX_CLK/ GPIO7_RLI | I/O(PD) | **(8463ML, 8463FML) – MII Mode:**<br>Receive Clock. This is an output clock in PHY MII mode and an input clock in MAC MII mode (2.5MHz in 10BT mode or 25MHz in 100BT mode).<br>**(8463RL, 8463FRL) – RMII Mode:**<br>This is GPIO7 while in RMII mode. (Refer to GPIO0 pin 48 description). |
| 39 | DGND | GND | Digital Ground |
| 40 | VDD_L | P | This pin can be used in two ways; as the pin to input a low voltage to the device if the internal low-voltage regulator is not used, or as the low-voltage output if the internal low-voltage regulator is used. |
| 41 | SPI_DO | IPU/O | **Serial Data Output in SPI Slave Mode.**<br>**Config Mode:**<br>This pin pull-up/pull-down value is latched to select clock input either 25MHz from X1/X2 or 50MHz from REFCLK_I during power-up/reset. See *Strapping Options* section for detail.<br>The REFCLK_I (50MHz) option is available only on the KSZ8463RL and KSZ8463FRL. For the KSZ8463ML and KSZ8463FML, this pin must NOT be pulled down at power-up/reset. |
| 42 | SPI_CSN | IPD | **Chip Select (active low) in SPI Slave Mode**.<br>When SPI_CSN is high, the device is deselected and SPI_DO is held in a high-impedance state. A high-to-low transition is used to initiate the SPI data transfer.<br>Note: An external 4.7K pull-up is needed on this pin when it is in use. |
| 43 | INTRN | OPU | **Interrupt Output.**<br>This is an active low signal going to the host CPU to indicate an interrupt status bit is set. This pin needs an external 4.7KΩ pull-up resistor. |
| 44 | SPI_SCLK/ MDC | IPU | Serial Clock input in SPI (SPI_SCLK) slave mode.<br>MIIM (MDC) mode is clock input. |
| 45 | SPI_DI/ MDIO | I/O(PU) | **Serial Data Input in SPI (SPI_DI) Slave Mode**.<br>Serial Data input/output in MIIM (MDIO) mode.<br>This pin needs an external 4.7KΩ pull-up resistor. |
| 46 | GPIO8 | I/O(PD) | This pin is GPIO8 (refer to GPIO0 pin 48 description). |
| 47 | GPIO11 | I/O(PU) | This pin is GPIO11 (refer to GPIO0 pin 48 description). |
| 48 | GPIO0 | I/O(PU) | **General Purpose Input/Output [0]**<br>This pin can be used as an input or output pin for use by the IEEE 1588 event trigger or timestamp capture units. It will be synchronized to the internal IEEE 1588 clock. The host processor can also directly drive or read this GPIO pin. |
| 49 | GPIO1 | I/O(PU) | This pin is GPIO1 (refer to GPIO0 pin 48 description). |
| 50 | DGND | GND | Digital Ground. |
| 51 | VDD_L | P | This pin can be used in two ways; as the pin to input a low voltage to the device if the internal low-voltage regulator is not used, or as the low-voltage output if the internal low-voltage regulator is used. |

## Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>52</td><td>GPIO2</td><td>I/O(PU)</td><td>This pin is GPIO2 (refer to GPIO0 pin 48 description).</td></tr>
<tr><td>53</td><td>GPIO3</td><td>I/O(PD)</td><td>This pin is GPIO3 (refer to GPIO0 pin 48 description).</td></tr>
<tr><td>54</td><td>GPIO4</td><td>I/O(PD)</td><td>This pin is GPIO4 (refer to GPIO0 pin 48 description).</td></tr>
<tr><td>55</td><td>GPIO5</td><td>I/O(PD)</td><td>This pin is GPIO5 (refer to GPIO0 pin 48 description).</td></tr>
<tr><td>56</td><td>VDD_IO</td><td>P</td><td>3.3V, 2.5V, or 1.8V digital VDD input power pin for IO logic and the internal low-voltage regulator.</td></tr>
<tr><td>57</td><td>DGND</td><td>GND</td><td>Digital ground.</td></tr>
<tr><td>58</td><td>GPIO6</td><td>I/O(PU)</td><td>This pin is GPIO6 (refer to GPIO0 pin 48 description).</td></tr>
<tr><td>59</td><td>P1LED1/<br>GPIO7_MLI</td><td>I/O(PU)</td><td rowspan="4">Programmable LED Output to Indicate Port 1 and Port 2 Activity/Status.<br>The LED is ON (active) when output is low; the LED is OFF (inactive) when output is high.<br>The port 1 LED pins outputs are determined by the table below if Reg. 0x06C – 0x06D, bits [14:12] are set to ‘000’. Otherwise, the port 1 LED pins are controlled via the processor by setting Reg. 0x06C – 0x06D, bits [14:12] to a non-zero value.<br>The port 2 LED pins outputs are determined by the table below if Reg. 0x084 – 0x085, bits [14:12] are set to ‘000’. Otherwise, the port 2 LED pins are controlled via the processor by setting Reg. 0x084 – 0x085, bits [14:12] to a non-zero value.<br>Automatic port 1 and port 2 indicators are defined as follows:<br><table><tr><td></td><td colspan="4">Two bits [9:8] in SGCR7 Control Register</td></tr><tr><td></td><td>00 (Default)</td><td>01</td><td>10</td><td>11</td></tr><tr><td>P1LED1/P2LED1</td><td>Speed</td><td>ACT</td><td>Duplex</td><td>Duplex</td></tr><tr><td>P1LED0/P2LED0</td><td>LINK/ACT</td><td>LINK</td><td>LINK/ACT</td><td>LINK</td></tr></table>LINK = LED ON ACT = LED Blink LINK/ACT = LED On/Blink<br>Speed = LED ON (100BT) LED OFF (10BT)<br>Duplex = LED ON (Full duplex) LED OFF (Half duplex)<br><br>(8463ML, 8463FML) – MII Mode:<br>Functionality is controlled by IOMXSEL register D6h.<br>Pin 59 is P1LED1 (default) or GPIO7.<br>Pin 60 is P1LED0.<br>Pin 61 is P2LED1 (default) or GPIO9.<br>Pin 62 is P2LED0 (default) or GPIO10.<br>(8463RL, 8463FRL) – RMII Mode:<br>Pin 59 is P1LED1.<br>Pin 60 is P1LED0.<br>Pin 61 is P2LED1.<br>Pin 62 is P2LED0.</td></tr>
<tr><td>60</td><td>P1LED0</td><td>I/O(PU)</td></tr>
<tr><td>61</td><td>P2LED1/<br>GPIO9_MLI</td><td>I/O(PU)</td></tr>
<tr><td>62</td><td>P2LED0/<br>GPIO10_MLI</td><td>I/O(PU)</td></tr>
</table>