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KSZ8692MPB/KSZ8692XPB

Integrated Networking and Communications Controller

Rev.4.0

General Description

The KSZ8692MPB/KSZ8692XPB is a highly-integrated System-on-Chip (SoC) containing an ARM 922T 32-bit processor and a rich set of peripherals to address the cost-sensitive, high-performance needs of a wide variety of high-bandwidth networking and communications applications.

Features

ARM 922T High-Performance Processor Core

- 250 MHz ARM 922T RISC processor core
- 8KB I-cache and 8KB D-cache
- Configurable Memory Management Unit (MMU) for Linux and WinCE

Memory Controller

- 8/16-bit external bus interface for FLASH, ROM, SRAM, and external I/O
- NAND FLASH controller with boot option
- 200MHz 32-bit DDR controller
- Two JEDEC Specification JESD82-1 compliant differential clock drivers for a glueless DDR interface solution

Ethernet Interfaces

- Two Ethernet (10/100 Mbps) MACs
- MII interface
- Fully compliant with IEEE 802.3 Ethernet standards

PCI Interface

- Version PCI 2.3
- 32-bit 33/66MHz
- Integrated PCI Arbiter supports three external masters for KSZ8692MPB and one external master for KSZ8692XPB
- Configurable as Host bridge or Guest device
- Glueless Support for mini-PCI or CardBus devices

Dual High-Speed USB 2.0 Interfaces

- Two USB2.0 ports with integrated PHY
- Can be configured as 2-port host, or host + device

SDIO/SD Host Controller (for KSZ8692MPB only)

- Meets SD Host Controller Standard Specification Version 1.0
- Meets SDIO card specification Version 1.0

DMA Controllers

- Dedicated DMA channels for PCI, USB, SDIO and Ethernet ports.

Peripherals

- Four high-speed UART ports up to 5Mbps
- Two programmable 32-bit timers with watchdog timer capability
- Interrupt Controller
- Twenty GPIO ports
- One shared SPI/I2C interface
- One I2S port

Debugging

- ARM9 JTAG debug interface
- JTAG Boundary Scan Support

Power Management

- CPU and system clock speed step-down options
- Ethernet port Wake-on-LAN
- DDR and PCI power-down

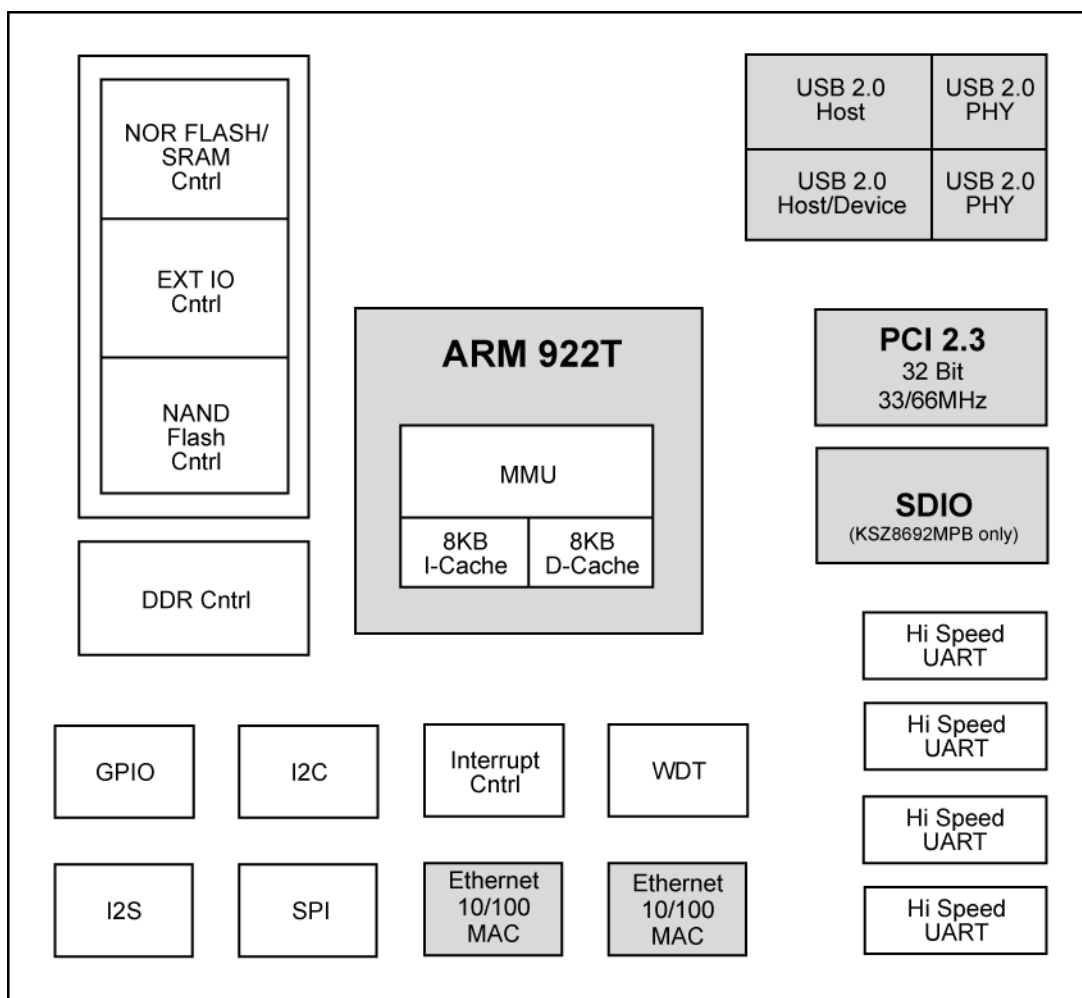
Operating Voltage

- 1.3V power for core
- 3.3V power for I/O
- 2.5V or 2.6V power for DDR memory interface

Reference Hardware and Software Evaluation Kit

- Hardware Evaluation Kit
- Software Evaluation Kit includes WinCE BSP, Open WRT BSP, Linux based SOHO Router packages

Block Diagram



Note: SDIO block for KSZ8692MPB only.

Figure 1. KSZ8692MPB/XPB Block Diagram

Applications

- Enhanced residential gateways
- High-end printer servers
- USB device servers
- IP-based multimedia systems
- Voice-over-Internet Protocol (VoIP) systems
- Set-top box
- Industrial control
- Wireless Access Points or Mesh Nodes

Ordering Information

Part Number	Temp. Range	Package	Lead Finish
KSZ8692MPB	0°C to 70°C	400-Pin PBGA	Pb-Free
KSZ8692MPBI ⁽¹⁾	-40°C to 85°C	400-Pin PBGA	Pb-Free
KSZ8692XPB ⁽²⁾	0°C to 70°C	400-Pin PBGA	Pb-Free

Notes:

1. Industrial version of KSZ8692MPB.
2. Support for one PCI Master. No SDIO.

Revision History

Revision	Date	Summary of Changes
1.0	10/14/08	Initial Release
2.0	3/10/09	Power Sequencing, Added A1 (PMEN) to pin list, 1.3V Supply for Core, Power Consumption table
3.0	8/10/09	DDR Data Width Changed to 16-bit
4.0	01/28/10	DDR Data Width Changed to 32-bit

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System Level Applications

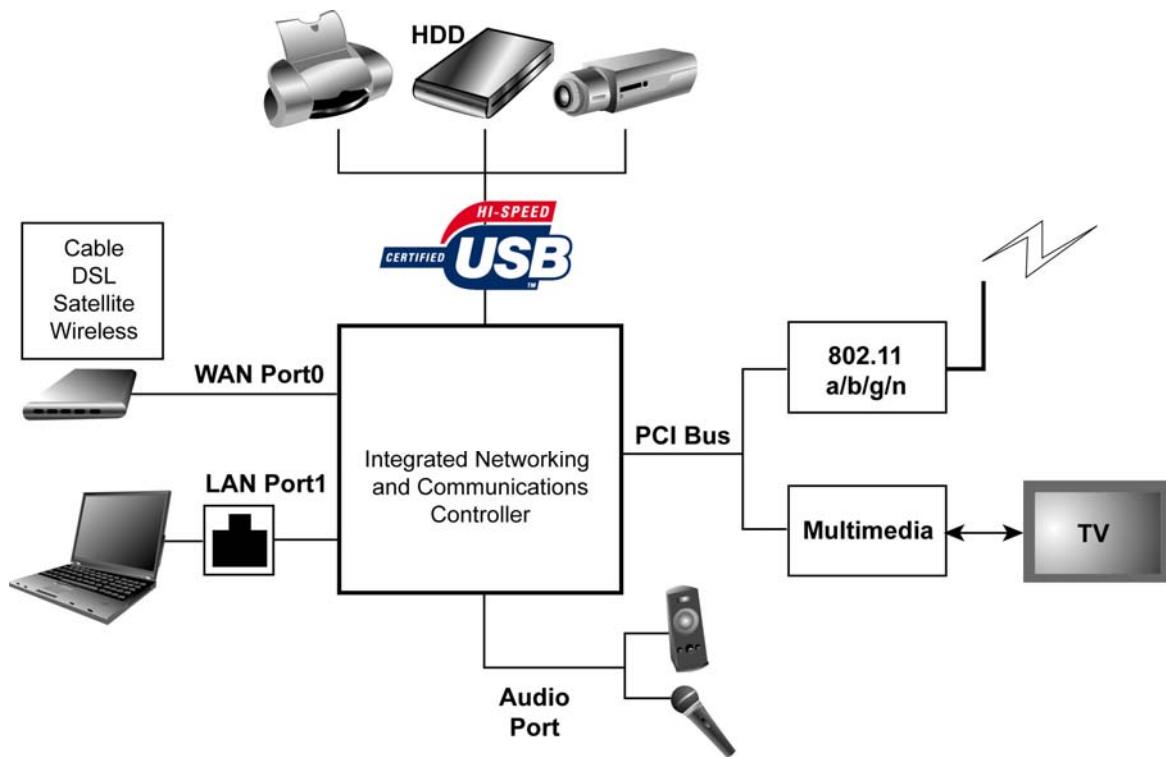


Figure 2. Peripheral Options and Examples

Functional Description

The KSZ8692MPB/KSZ8692XPB is a highly integrated embedded application controller that is designed to provide a single-chip solution for a wide range of applications that require high-speed networking, multiple I/O controllers and interface to standard peripherals. It features a powerful 32-bit ARM RISC processor, DDR memory controller, FLASH/ROM/SRAM/External I/O interface, NAND memory controller, two Ethernet MACs, two USB 2.0 ports, PCI 2.3 bus interface, SDIO interface (for KSZ8692MPB only), and a large number of standard peripherals including UARTs, I2C, I2S, SPI, MIB counters, Station Manager, timers, interrupt controller and GPIOs.

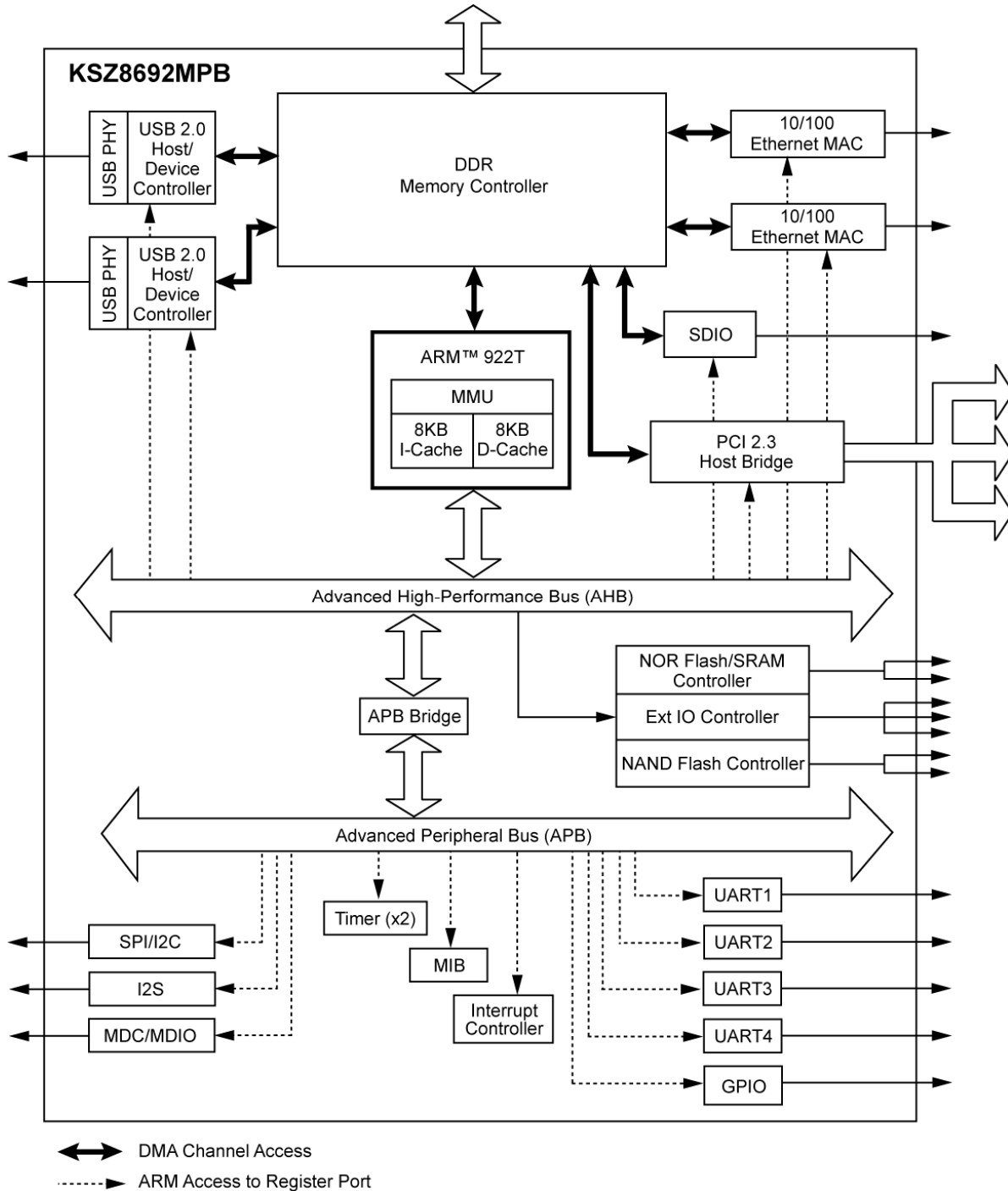


Figure 3. KSZ8692MPB Functional Block Diagram

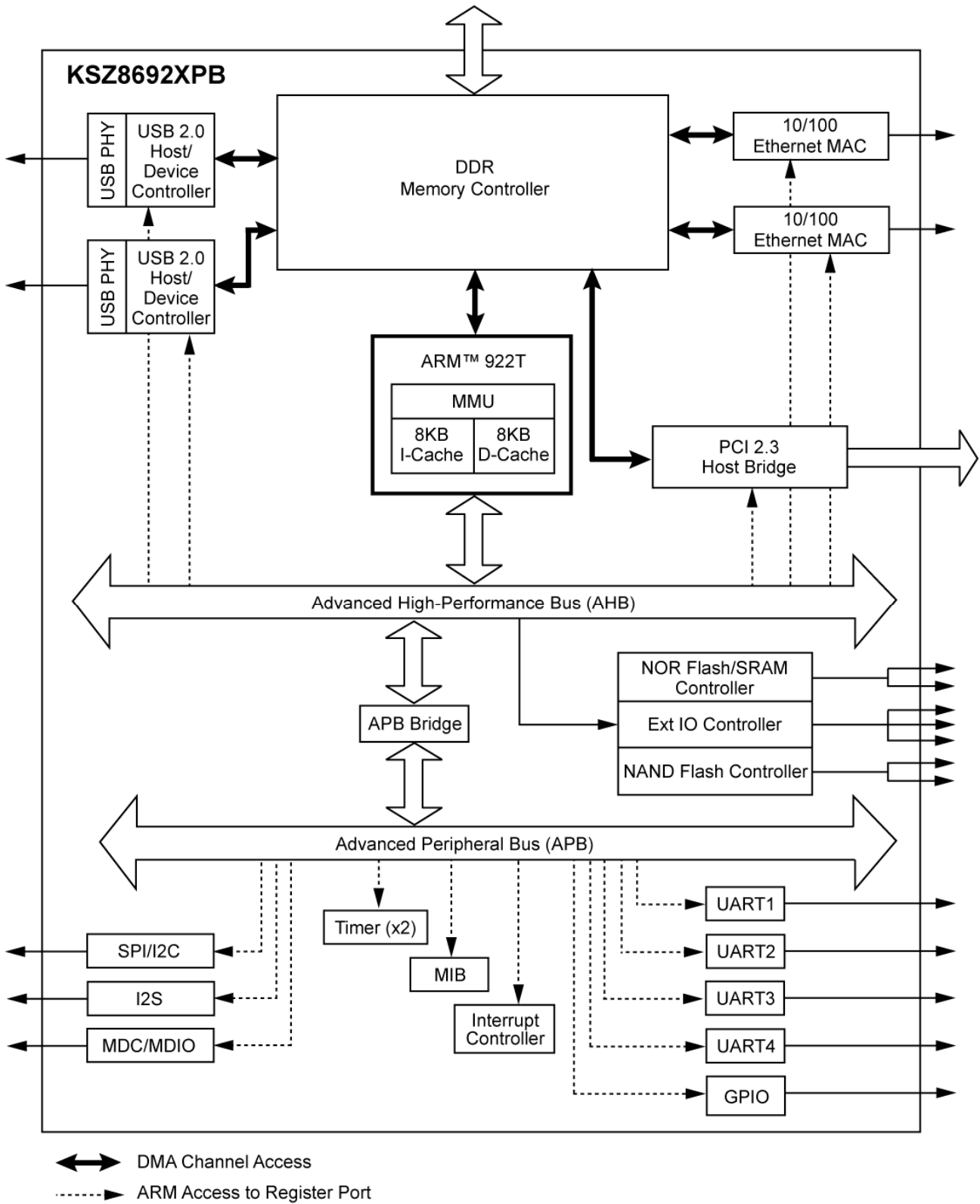


Figure 4. KSZ8692XPB Functional Block Diagram

ARM High-Performance Processor

The KSZ8692MPB/KSZ8692XPB is built around the 16/32-bit ARM922T RISC processor designed by Advanced RISC Machines. The ARM922T is a scalable, high-performance processor that was developed for highly integrated SoC applications. Its simple, elegant, and fully static design is particularly suited to cost-effective and power-sensitive embedded systems. It also offers a separate 8KB D-cache and 8KB I-cache that reduces memory access latency. 16-bit thumb instruction sets are supported to minimize memory footprint. The ARM processor core can be programmed to maximum of 250MHz for highest possible performance.

The Advanced Microprocessor Bus Architecture/Advanced High Performance Bus (AMBA AHB) is a 32-bit wide ARM system bus to which is connected the processor, the register ports of the DDR memory controller, the FLASH/ROM/SRAM/External I/O controller, the NAND memory controller, the Ethernet MACs, the PCI bridge, the USB ports and the SDIO controller (for KSZ8692MPB only). The ARM processor is the master of AHB and responsible for configuring the operational characteristics of each AHB device via their individual register port. The AHB is programmable up to 166MHz for maximum system bus performance. AHB interfaces to devices are shown in the functional block diagram.

Also connected to AHB is the ARM Advanced Peripheral Bus or APB bridge which is attached the standard peripherals. The APB Bridge transparently converts the AHB accesses into slower APB accesses. The ARM processor is the master of APB bridge and responsible for configuring the operational characteristics and transfer of data for each APB attached peripheral. APB interfaces to standard peripherals are shown in functional block diagram.

- 250MHz ARM922T RISC processor core
- 166MHz AMBA Bus 2.0
- 16-bit thumb instruction sets
- 8KB D-cache and 8KB I-cache
- Supports Little-Endian mode
- Configurable MMU
- Power saving options include clock down of both processor core and AMBA AHB

FLASH/ROM/SRAM Memory and External I/O Interface

The KSZ8692MPB/KSZ8692XPB memory controller provides glueless interface for static memory, i.e., ROM, SRAM, and NOR Flash and three banks of external I/O. NOR Flash bank0 can be configured by power-up strap option to operate as boot bank from a 8 or 16 bit device.

- Glueless connection to two banks of FLASH/ROM/SRAM memory with programmable 8 or 16 bit data width and programmable access timing
- Support for AMD/Intel like Flash
- Automatic address line mapping for 8 or 16-bit accesses on Flash, ROM, and SRAM interfaces
- Supports three external I/O banks with programmable 8 or 16 bit data width and programmable access timing
- Total 64MB address space for two banks of FLASH/ROM/SRAM and and three banks of external I/O

The memory interface for the static memory has a special automatic address mapping feature. This allows the designer to connect address bit 0 on the memory to ADDR[0] on the KSZ8692MPB/KSZ8692XPB and address bit 1 on the memory to ADDR[1] on the KSZ8692MPB/KSZ8692XPB, regardless of whether the designer is trying to achieve half word or byte addressing. The KSZ8692MPB/KSZ8692XPB memory controller performs the address mapping internally. This gives the designer the flexibility to use 8 or 16 bit data width devices interchangeably on the same PCB (see Figure 4). For external I/O, however, the designer still needs to resolve the address mapping (see Figure 5).

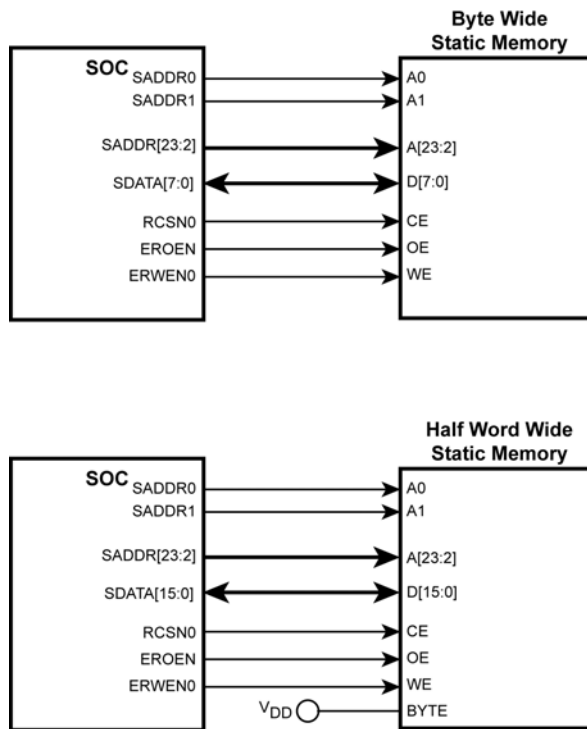


Figure 4. Static Memory Interface Examples

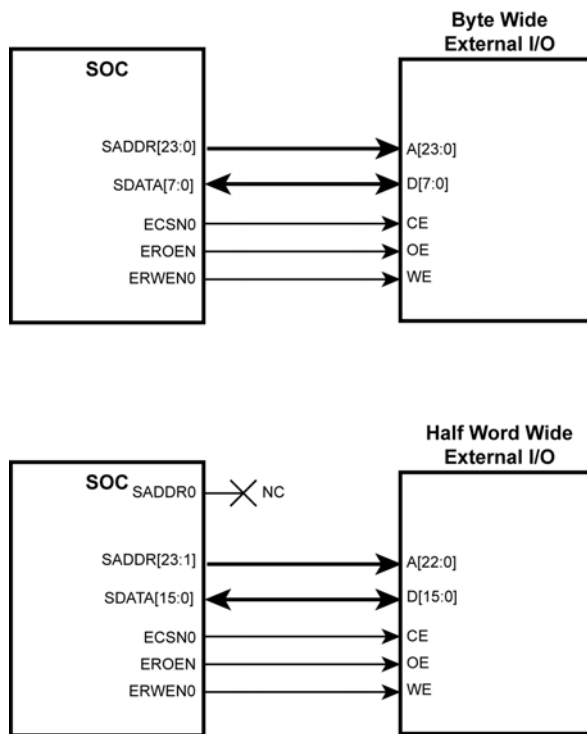


Figure 5. External I/O Interface Examples

NAND Flash Memory Interface

The KSZ8692MPB/KSZ8692XPB NAND controller provides interface to external NAND Flash memory. A total of two banks are supported. NAND Flash bank0 can be configured by power-up strap option to operate as boot bank. Both NAND Flash banks share data bus with FLASH/ROM/SRAM memory banks.

- Glueless connection to two banks with programmable 8 or 16 bit data width and programmable access timing
- Hardware ECC not supported
- Small page size 512 + 16 bytes
- Large page size 2048 + 64 bytes
- Large and small block size
- Boot option with automatic page crossing where pages are automatically opened sequentially by hardware
- Boot option with two 8-bit device in parallel to form a 16-bit bank
- Boot option with bank0 and bank1 as active banks in cascade
- Support for following device densities:
 - 64Mbit
 - 128Mbit
 - 256Mbit
 - 512Mbit
 - 1Gbit
 - 2Gbit
 - 4Gbit
 - 8Gbit

The following figures illustrate examples of NAND Flash bank configuration:

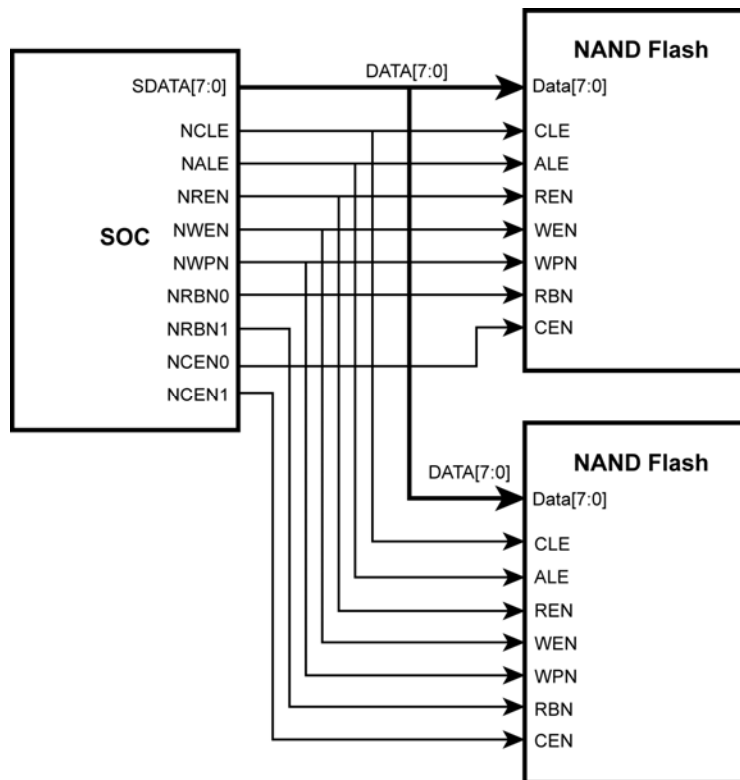


Figure 6. 8-bit NAND Interface Examples

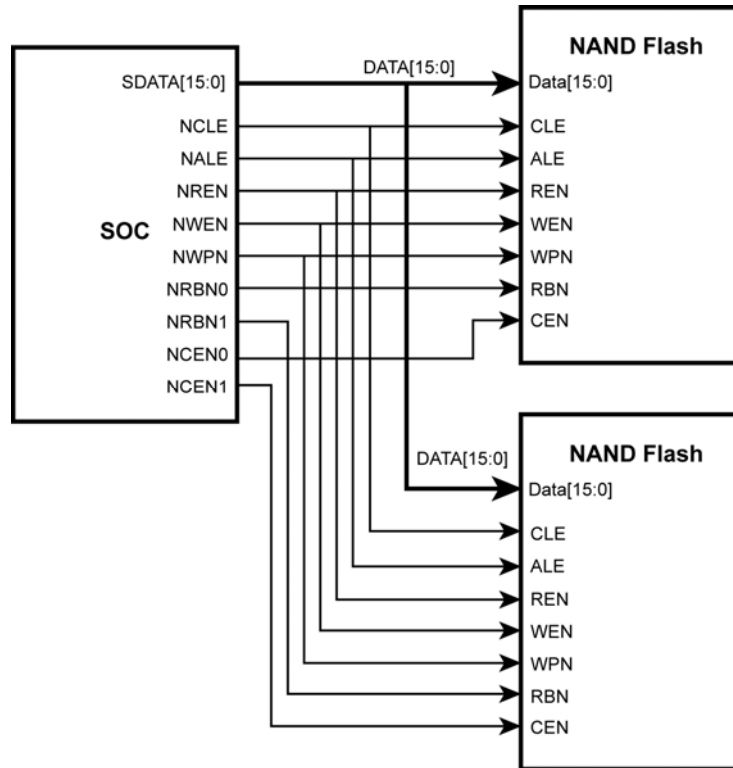


Figure 7. 16-bit NAND Interface Examples

DDR Controller

The KSZ8692MPB/KSZ8692XPB DDR memory controller provides interface for accessing external Double Data Rate Synchronous DRAM. In addition, the KSZ8692MPB/KSZ8692XPB provides two integrated DDR differential clock drivers for a complete glueless DDR interface solution.

- Up to 200MHz clock frequency (400 MHz data rate)
- Supports one 32-bit data width bank (16-bit optional)
- Up to 128 MB of addressable space is available with 12 columns and 14 row address lines
- Supports all DDR device densities up to 1Gb
- Supports all DDR device data width x8 and x16
- Configurable DDR RAS and CAS timing parameters
- Two integrated JEDEC Specification JESD82-1 compliant differential clock drivers for a glueless DDR interface solution
- JEDEC Specification SSTL_2 I/Os

A dedicated internal PLL provides clocking to the DDR memory controller and the two differential clock drivers. This PLL is programmable up to 200MHz and independent of AHB and ARM processor core clocks.

Figures 8 and 9 illustrate examples of bank configurations.

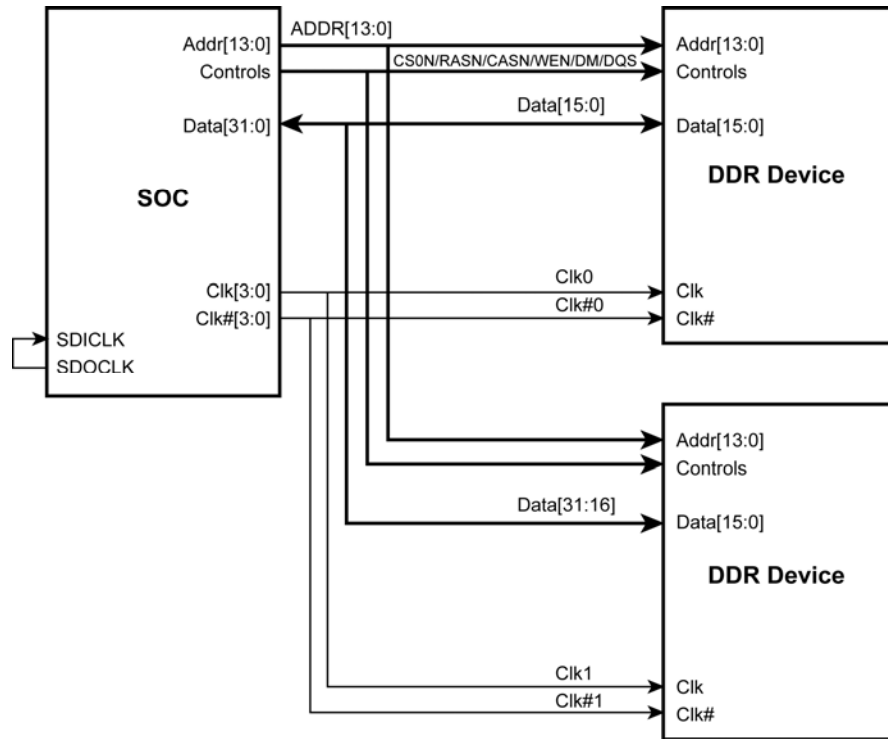


Figure 8. Two 16-bit DDR Memory Device Interface Example

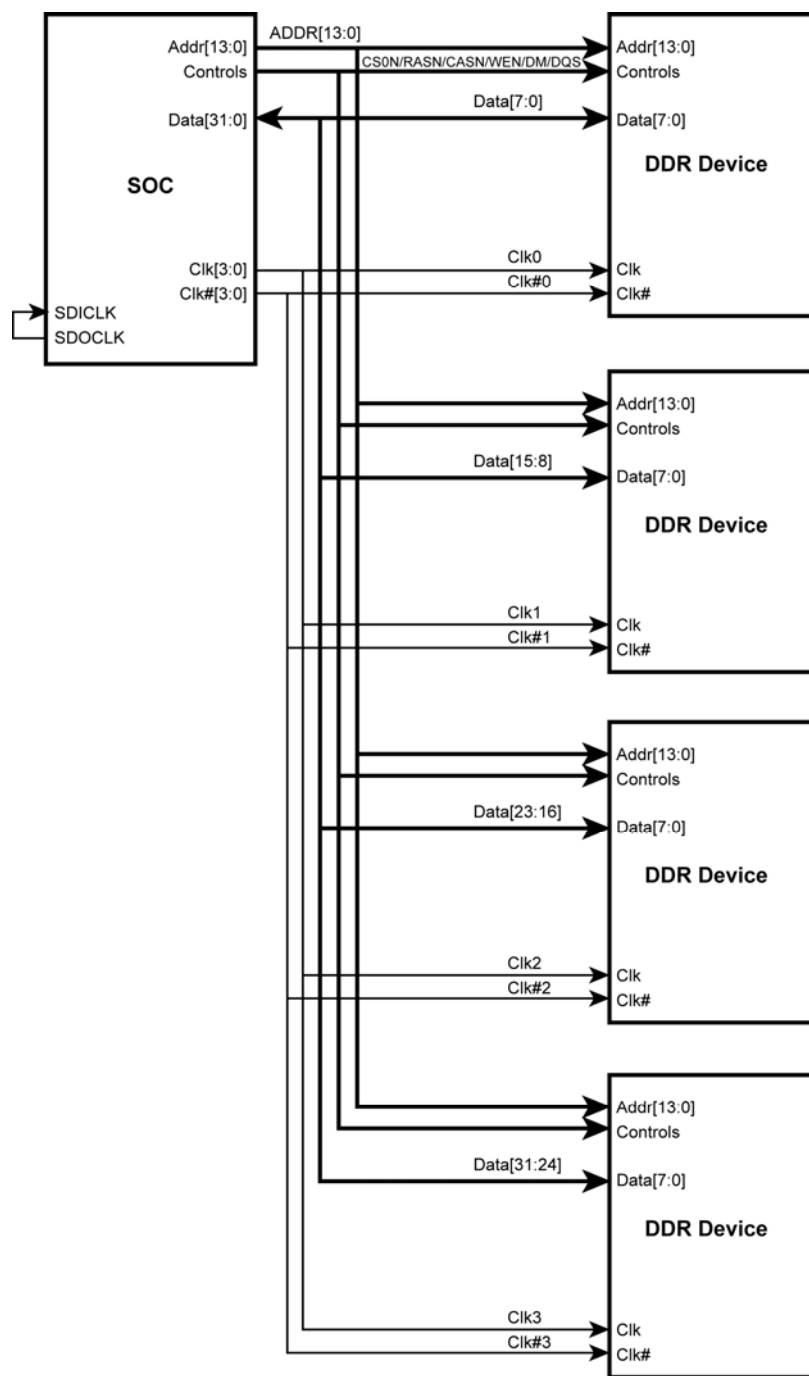


Figure 9. Four 8-bit DDR Memory Devices Interface Example

DDR memory controller access to memory bank is typically of the burst type. Figures 10 and 11 are examples of burst read and write cycles.

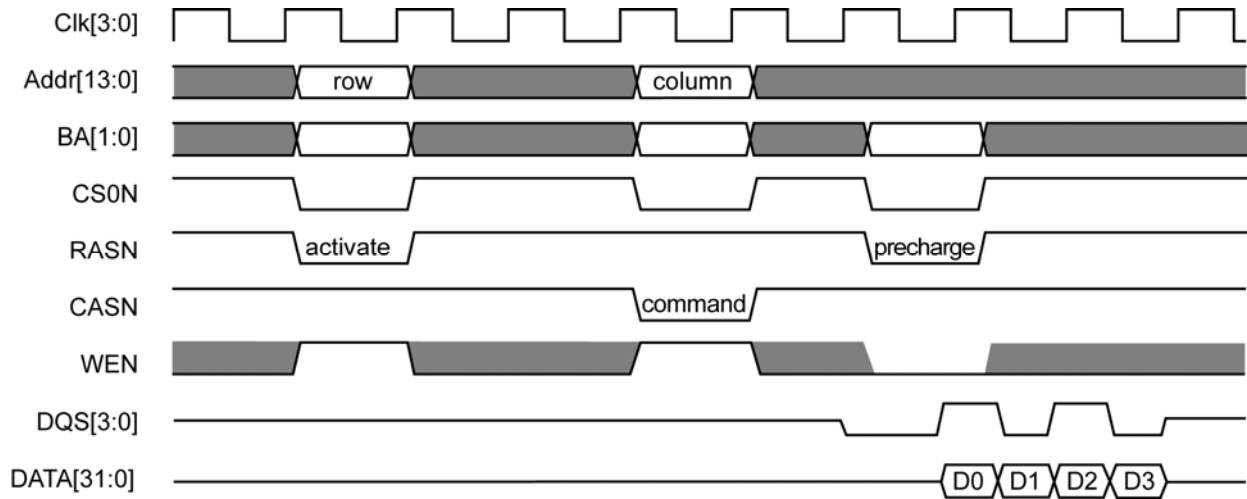


Figure 10. Burst DDR Read Timing

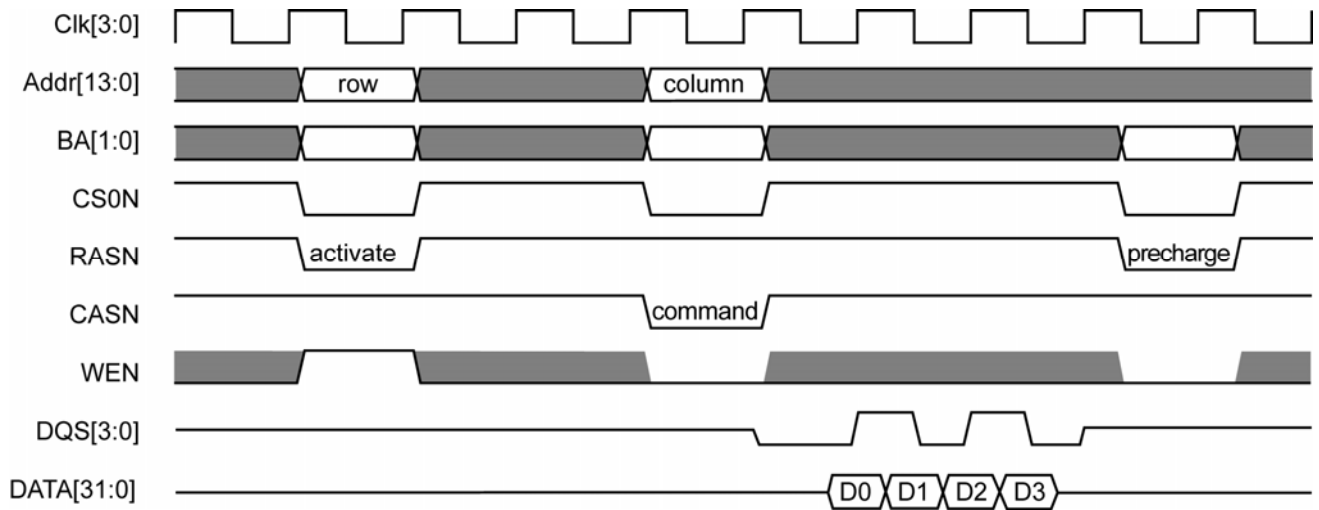


Figure 11. Burst DDR Write Timing

SDIO/SD Host Controller (for KSZ8692MPB only)

Integrated SDIO/SD host controller provides interface for removable mass storage memory card and I/O devices.

- Meets SD Host Controller Standard Specification Version 1.0
- Meets SD memory card spec 1.01 . MMC spec 3.31
- Meets SDIO card specification version 1.0
- 1 or 4 bit mode supported
- Card detection-insertion/removal
- Line Status LED driver
- Password protection of cards
- Supports read wait control, suspend/resume operation
- Support multi block read and write
- Up to 12.5 Mbytes per second read and write rates using 4 parallel line for full speed card.
- Dedicated DMA or programmed I/O data transfer

USB 2.0 Interface

Integrated dual USB 2.0 interface can be configured as 2-port host, or host + device. Figures 12 and 13 illustrate examples of USB 2.0 interface applications.

- Compliant with USB Specification Revision 2.0
- Compliant with Open Host Controller Interface (OHCI) Specification Rev 1.0a
- Compliant with Enhanced Host Controller Interface (EHCI) Specification Rev 1.0
- Root hub with 2 (max) downstream facing ports which are shared by OHCI and EHCI host controller cores
- All downstream facing ports can handle High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps) transaction
- OTG not supported
- Integrated 45-ohm termination, 1.5K pull-up and 15K pull-down resistors
- Support endpoint zero, and up to 6 configurable endpoints (IN/OUT, isochronous/ control/ interrupt/ bulk)
- One isochronous endpoint (IN or OUT)
- Dedicated DMA Channel for each port

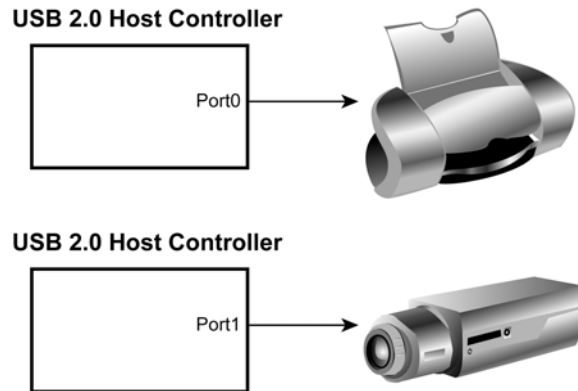


Figure 12. USB 2.0 Configuration as Two-Port Host

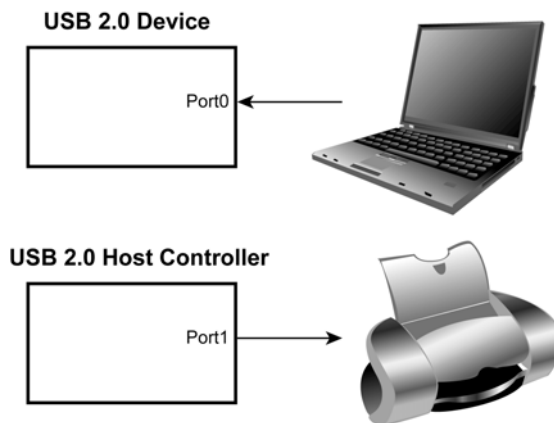


Figure 13. USB 2.0 Configuration as Host + Device

PCI Interface

The KSZ8692MPB/KSZ8692XPB integrates a PCI-to-AHB bridge solution for interfacing with 32-bit PCI, including miniPCI, and cardbus devices where it is common for 802.11x-based Wireless products. The PCI-AHB bridge supports two modes of operation in the PCI bus environment; host bridge mode and guest bridge mode. In the host bridge mode, the ARM processor acts as the host of the entire system. It configures other PCI devices and coordinates their transactions, including initiating transactions between the PCI devices and AHB bus subsystem. An on-chip PCI arbiter is included to determine the PCI bus ownership among up to three PCI master devices.

In guest bridge mode, all of the I/O registers are programmed by either the external host CPU on the PCI bus or the local ARM host processor through the AHB bus and the KSZ8692MPB/KSZ8692XPB can be configured by either the ARM or the PCI host CPU. In guest bridge mode, the on-chip PCI arbiter is disabled. In both cases, the KSZ8692MPB/KSZ8692XPB memory subsystem is accessible from either the PCI host or the ARM processor. Communications between the external host CPU and the ARM processor is accomplished through message passing or through shared memory.

- Compliant to PCI revision 2.3
- Support 33 and 66MHz, 32-bit data PCI bus
- Support 32-bit miniPCI or cardbus devices
- Supports both regular and memory-mapped I/O on the PCI interface
- AHB bus and PCI bus operate at independent clock domains
- Supports big endian and little endian on AHB
- PCI bus Round Robin arbiter for three external masters (for KSZ8692MPB only)
- PCI bus arbiter for one external master (for KSZ8692XPB only)
- Supports high speed bus request and bus parking
- Dedicated DMA channel for bulk data transfer to/from DDR memory

Ethernet MAC Ports (Port 0 = WAN, Port 1 = LAN)

The KSZ8692MPB/KSZ8692XPB integrates two Ethernet controllers that operate at 10 and 100 Mbps. Each controller has an interface that operates as MII to an external 10/100 PHY to complete Ethernet network connectivity. An integrated 25 MHz clock eliminates external crystal or oscillator requirement for PHY to reduce cost. Integrated 2-pin (MDC & MDIO) Station Manager allows ARM processor to access PHY registers and pass control and status parameters. Wake-on-LAN is supported as part of the power management mechanism. Each port has a dedicated MIB counter to accumulate statistics for received and transmitted traffic.

- IEEE 802.3 compliant MAC layer function
- MII interface compliant to Clause 22.2.4.5 of the IEEE 802.3u Specification
- 10/100 Mbps half and full-duplex operation
- Automatic CRC generation and checking
- Automatic error packet discard
- Supports IPv4 Header and IPv4/IPv6 TCP/UDP checksum generation to offload host CPU
- Supports IPv4 Header and IPv4/IPv6 TCP/UDP checksum error detection
- Supports 32 rules ACL filtering
- Maximum frame length support is 2000 Byte at WAN port and 9K-byte at LAN port
- Contains large independent receive and transmit FIFOs (8KB receive / 8KB transmit at WAN and 24KB receive / 22KB transmit at LAN) for back-to-back packet receive, and guaranteed no-under run packet transmit
- Data alignment logic and scatter gather capability
- Configurable as MAC or PHY mode
- Separate transmit and receive DMA channels for each port

Wake-on-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. In all of these instances, the network device is

pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic.

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state.

A wake-up signal is caused by:

1. Detection of a change in the network link state
2. Receipt of a network wake-up frame
3. Receipt of a Magic Packet

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own way.

Link Change

Link status wake events are useful to indicate a change in the network's availability, especially when this change may impact the level at which the system should re-enter the sleeping state. For example, a change from link off to link on may trigger the system to re-enter sleep at a higher level (D2 versus D3¹) so that wake frames can be detected. Conversely, a transition from link on to link off may trigger the system to re-enter sleep at a deeper level (D3 versus D2) since the network is not currently available.

Wake-up Packet

Wake-up packets are certain types of packets with specific CRC values that a system recognizes to as a 'wake up' frame. The KSZ8692MPB/KSZ8692XPB supports up to four user defined wake-up frames on each network controller port:

Magic Packet

Magic Packet technology is used to remotely wake up a sleeping or powered off PC or device on network. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC or device capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the networkcontroller, and when the networkcontroller receives a Magic Packet frame, it will alerts the system to wake up.

Magic Packet is a standard feature integrated into the KSZ8692MPB/KSZ8692XPB. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ8692MPB/KSZ8692XPB has been put into Magic Packet Enable mode, it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the networktechnology chosen, such as Source Address (SA), or Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of XoffFFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

Example:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the networkcontroller would be scanning for the data sequence (assuming an Ethernet frame):

```
DESTINATION SOURCE – MISC - : FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -
11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -
11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -
11 22 33 44 55 66 - MISC - CIRC.
```

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the

¹ References to D0, D1, D2, and D3 are power management states defined in a similar fashion to the way they are defined for PCI. For more information, refer to the PCI specification at www.pcisig.com/specifications/conventional/pcipm1.2.pdf.

frame's destination.

If the network controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8692MPB/KSZ8692XPB controller detects the data sequence, however, it then alerts the device's power management circuitry to wake up the system.

IPv6 Support

The KSZ8692MPB/KSZ8692XPB provides the following IPv6 support in the hardware:

- Generates the checksum for IPv6 TCP/UDP packets based on register configuration (LAN MAC DMA Transmit Control Register and WAN MAC DMA Transmit Control Register) or Transmit Descriptor 1 (TDES1). The register setting is static configuration and the TDES1 setting is packet-based configuration.
- Filters IPv6 packets with TCP/UDP errors (LAN MAC DMA Receive Control Register and WAN MAC DMA Receive Control Register).
- Supports up to 8 Source IP or Destination IP-based filtering (LAN/WAN Access Control List)

Refer to the Register Description Document for more details.

DMA Controller

Integrated DMA controller connects data port of two Ethernet MACs, two USB 2.0 ports, PCI 2.3 bus interface, and SDIO interface (for KSZ8692MPB only) via dedicated channels to DDR memory controller for moving large amounts of data without significant ARM processor intervention. A typical DMA channel usage is to move data from these interfaces into DDR memory. The data in the memory is processed by the ARM processor and driven back by the DMA channel to the external interface. Additionally, the ARM processor itself has a dedicated DMA channel to access the DDR memory controller. Flash/ROM/SRAM, NAND controller, and peripherals do not have dedicated DMA channel and therefore, depend on the ARM processor for transfer of data to DDR memory. DMA channel interfaces are shown in the functional block diagram on page 8 and 9.

The arbitration of all requests from DMA channels are handled by the DDR memory controller and pipelined for best performance. The memory controller supports programmable bandwidth allocation for each DMA channel, thus enabling the designer to optimize I/O resource utilization of memory.

UART Interface

The KSZ8692MPB/KSZ8692XPB support four independent, high-speed UARTs; UART1, UART2, UART3 and UART4. The UART ports enhance the system availability for legacy serial communication application and console port display.

UART1, UART2, UART3 and UART4 support maximum baud rate of 5 Mbps including standard rates. The higher rates allow for Bluetooth and GSM applications.

UART1 supports CTSN, DSRN, DCDN modem control pins in addition to RXD and TXD data pins. For UART2, UART3, UART4 only CTSN and RTSN control pins in addition to RXD and TXD data pins are supported.

Timers and Watchdog

Two programmable 32-bit timers with one capable of watchdog timer function. These timers can operate in a very flexible way. The host can control the timeout period as well as the pulse duration. Both timers can be enabled with interrupt capability. When the watchdog timer is programmed and the timer setting expires, the KSZ8692MPB/KSZ8692XPB resets itself and also asserts WRSTO to reset other devices in the system.

GPIO

Twenty general purpose I/O (GPIO) are individually programmable as input or output. Some GPIO ports are programmable for alternate function as listed below:

- Four GPIO programmable as inputs for external interrupts
- Two GPIO programmable as 32-bit timers output
- Six GPIO programmable as CTSN and RTSN control pins for UART2, UART3, UART4
- One GPIO programmable as SDIO Line Status LED driver (for KSZ8692MPB only)
- One GPIO programmable as ARM CPU interrupt line activity.

See Signal Description list for detailed GPIO map.

I2C

The I2C interface is a 2-pin (SCL & SDA) generic serial bus interface for both control and data. The KSZ8692MPB/KSZ8692XPB supports master mode I2C interface. To increase the firmware efficiency, KSZ8692MPB/KSZ8692XPB is equipped with hardware assisted logic to take care I2C bus sequence and protocol.

- Supports one master (KSZ8692MPB/KSZ8692XPB) in the system
- 8-bit or 10-bit addressing
- Up to 8 byte burst for read and write
- Programmable SCL clock rate for up to 400kHz

The I2C interface shares the same pins with the SPI interface.

SPI

The Serial Peripheral Interface (SPI) is a synchronous serial data link that provides communication with external devices.

- 8- to 16-bit Programmable Data Length
- Programmable Serial Clock Phase and Polarity
- Programmable Active Level of Chip Select (CS)
- Programmable Delays between Two Active CS
- Programmable Delays between Consecutive Transfers without Removing CS
- Programmable Delays between Assertion CS and 1st SPCK
- Programmable SPI clock (SPCK) rate in the range of AMBA System Clock (SYSCLK) divided by a value between 16 and 65536

The SPI interface shares the same pins with the I2C interface.

I2S

I2S provides programmable 16-, 18-, 20-, 24-bit resolution audio for two (stereo) channels playback and recording.

Interrupt Controller

Interrupt controller handles external and internal interrupt sources.

- Normal or fast interrupt mode (IRQ, FIQ) supported
- Prioritized interrupt handling

System Level Interfaces

The following figures illustrate the high-level system connections to the KSZ8692MPB/KSZ8692XPB. Note that these figures are for illustration purpose only. The system designer must refer to Evaluation Design Kit for actual circuit implementation.

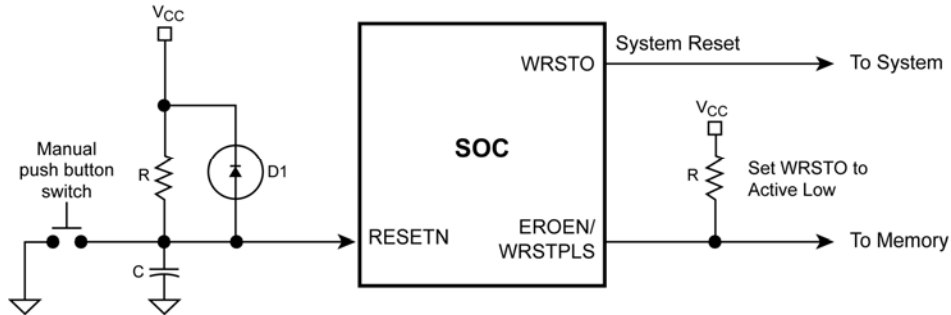


Figure 14. Reset Circuit

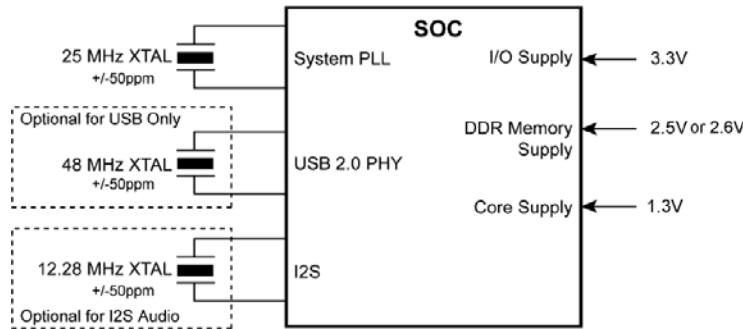


Figure 15. Power and Clocks

According to some DDR device manufacturer’s electrical specification, DDR400 devices operating at 200 MHz require a 2.6V power supply. DDR333 and DDR266 devices require 2.5V power supply. Power to the SoC DDR Memory Controller must be based on DDR device power requirement specification.

Signal Descriptions by Group

Pin Number	Pin Name	Pin Type	Pin Description
System Interface			
R5	RESETN	I	Reset, asserted Low. RESETN will force the KSZ8692MPB/KSZ8692XPB to reset ARM9 CPU and all functional blocks. Once asserted, RESETN must remain asserted for a minimum duration of 256 system clock cycles. When in the reset state, all the output pins are put into Tri-state and all open drain signals are floated.
N5	WRSTO	O	Watchdog Timer Reset Output When the Watchdog Timer expires, this signal will be asserted for at least 200 msec.
W1	XCLK2	I	System Clock Input 2. External crystal or clock input 2. The clock frequency should be 25MHz \pm 100ppm.
Y1	XCLK1	I	System Clock Input 1. Used with XCLK1 pin when other polarity of crystal is needed. This is unused for a normal clock input.
H19	CLK25MHz	O	25MHz output to external PHY
Y15, Y14	DDCLKO[1:0]	O	DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
W15, W14	DDCLKON[1:0]	O	The negative of differential pair of DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
U13	SDCLKEO	O	Clock Enable output for SDRAM (for Power Down Mode)
T7, U7	VREF	I	Reference Voltage for SSTL interface. Must be half of the voltage for the DDR VDD supply. See EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5V, SSTL_2)
W3	SDOCLK	O	DDR Clock Out for loopback from De-skew PLL
Y3	SDICLK	I	DDR Clock In from loopback to De-skew PLL. This pin must connect to SDOCLK with appropriate de-skew length. See Engineering Evaluation Design Kit for detailed implementation.
Y17, Y16	DDCLKO[3:2]	O	Factory Reserved
W17, W16	DDCLKON[3:2]	O	Factory Reserved
NAND/SRAM/ROM/EXIO Interface			
L2, K1, K2, J3, H5, H4, J2, H3, J1, H2, G5, H1, G3, G4, G2, F1, G1, F2, F3, F5, F4, E1, E2, E3	SADDR[23..0]	O	SRAM Address Bus. The 24-bit address bus covers 16M word memory space of ROM/SRAM/FLASH, and 16M byte external I/O banks. This address bus is shared between ROM/SRAM/FLASH/EXTIO devices.

Pin Number	Pin Name	Pin Type	Pin Description
T2, U1, L5, N4, P3, R2, T1, M4, K5, N3, P2, R1, L4, M3, P1, K4	SDATA[15..0]	Ipu/O	SRAM DATA Bus. Bidirectional Bus for 16-bit DATA In and DATA Out. The KSZ8692MPB/KSZ8692XPB also supports 8-bit data bus for ROM/SRAM/FLASH/EXTIO cycles. This data bus is shared between NAND, ROM/SRAM/FLASH/EXTIO devices.
L3	ECS2	O	External I/O Chip Select 2, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
N1	ECS1	O	External I/O Chip Select 1, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
M2	ECS0	O	External I/O Chip Select 0, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
K3	RCSN1	O	ROM/SRAM/FLASH(NOR) Chip select 1, asserted Low. The KSZ8692MPB/KSZ8692XPB can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks.
L1	RCSN0	O	ROM/SRAM/FLASH(NOR) Chip select 0, asserted Low. The KSZ8692MPB/KSZ8692XPB can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks. This bank is configurable as boot option
N2	EWAITN	I	External Wait asserted Low. This signal is asserted when an external I/O device or ROM/SRAM/FLASH(NOR) bank needs more access cycles than those defined in the corresponding control register.
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device.
J5	ERWEN1	O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[15..8] for ROM/SRAM/FLASH and EXTIO access.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[7..0 or 15..0] for ROM/SRAM/FLASH and EXTIO access.
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash.
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash.
T3	NCEN1	O	NAND Bank Chip Enable 1, asserted low NAND device bank 1 selection control.

Pin Number	Pin Name	Pin Type	Pin Description
V3	NCEN0	O	NAND Bank Chip Enable 0, asserted low NAND device bank 0 selection control. This bank is configurable as boot option
R4	NREN	Ipu/O	NAND Read Enable, asserted low
T4	NWEN	Ipu/O	NAND Write Enable, asserted low
U3	NWPN	Ipu/O	NAND Write Protection, asserted low
P4, U4	NRBN[1:0]	I	NAND Ready/Busy, asserted low for busy.
DDR Interface			
T17, V18, U17, T16, W20, W19, Y20, Y19, W18, V17, U16, T15, Y18, V16	DADDR[13..0]	O	DDR Address Bus.
V13, U11, V12, W13, Y13, W12, V11, U10, V10, Y11, W10, U9, Y10, V9, W9, Y9, W8, Y8, Y7, W7, V7, Y6, W6, V6, Y5, V5, W5, U5, T5, Y4, V4, W4	DDATA[31..0]	I/O	DDR Data Bus.
T13, V14	BA[1:0]	O	DDR Bank Address.
U14	CSN	O	DDR Chip Select, asserted Low. Chip select pins for DDR, the KSZ8692MPB/KSZ8692XPB supports only one DDR bank.
T14	RASN	O	DDR Row Address Strobe, asserted Low. The Row Address Strobe pin for DDR.
U15	CASN	O	DDR Column Address Strobe, asserted Low. The Column Address Strobe pin for DDR.
V15	WEN	O	DDR Write Enable, asserted Low. The write enable signal for DDR.
T12, Y12, U8, T6	DM[3:0]	O	DDR Data Input/Output Mask Data Input/Output mask signals for DDR. DM is sampled High and is an output mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a Write cycle. DM0 corresponds to DDATA[7:0], DM1 corresponds to DDATA[15:8], DM2 corresponds to DDATA[23:16] and DM3 corresponds to DDATA[31:24].
U12, W11, V8, U6	DQS[3:0]	I/O	DDR only Data Strobe Input with read data, output with write data. DQS0 corresponds to DDATA[7:0], DQS1 corresponds to DDATA[15:8], DQS2 corresponds to DDATA[23:16] and DQS3 corresponds to DDATA[31:24].