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KSZ8775CLX

Integrated 5–Port 10/100 Managed Ethernet Switch with Port 4 RMII and Port 5 RGMII/MII/ RMII Interfaces

Features

- Management Capabilities
  - The KSZ8775CLX includes all the functions of a 10/100BASE-T/TX switch system, which combines a switch engine, frame buffer management, address look-up table, queue management, MIB counters, media access controllers (MAC), and PHY transceivers
  - Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing a 1024-entry forwarding table
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
  - MIB counters for fully compliant statistics gathering - 36 counters per port
  - Hardware support for port-based flush and freeze command in MIB counter.
  - Multiple loopback of remote, PHY, and MAC modes support for the diagnostics
  - Rapid spanning tree support (RSTP) for topology management and ring/linear recovery
- Robust PHY Ports
  - Four integrated IEEE 802.3/802.3u-compliant Ethernet transceivers supporting 10Base-T and 100BASE-TX
  - 802.1az EEE supported
  - On-chip termination resistors and internal biasing for differential pairs to reduce power
  - HP Auto MDI/MDI-X™ crossover support eliminates the need to differentiate between straight or crossover cables in applications
- MAC and GMAC Ports
  - Four internal media access control (MAC1 to MAC4) units and one internal Gigabit media access control (GMAC5) unit
  - RGMII, MII, or RMII interfaces support for the Port 5 GMAC5 with uplink and RMII interface for Port 4 MAC4
  - 2 kb jumbo packet support
  - Tail tagging mode (one byte added before FCS) support on Port 5 to inform the processor which ingress port receives the packet and its priority
  - Supports reduced media independent interface (RMII) with 50 MHz reference clock output
  - Supports media independent interface (MII) in either PHY mode or MAC mode on Port 5
  - LinkMD® cable diagnostic capabilities for determining cable opens, shorts, and length
- Advanced Switch Capabilities
  - Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing a 1024-entry forwarding table
  - 64kb frame buffer RAM
  - IEEE 802.1q VLAN support for up to 128 active VLAN groups (full-range 4096 of VLAN IDs)
  - IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
  - VLAN ID tag/untag options on per port basis
  - Fully compliant with IEEE 802.3/802.3u standards
  - IEEE 802.3x full-duplex with force mode option and half-duplex back-pressure collision flow control
  - IEEE 802.1w rapid spanning tree protocol support
  - IGMP v1/v2/v3 snooping for multicast packet filtering
  - QoS/CoS packets prioritization support: 802.1p, DiffServ-based and re-mapping of 802.1p priority field per port basis on four priority levels
  - IPv4/IPv6 QoS support
  - IPv6 multicast listener discovery (MLD) snooping
  - Programmable rate limiting at the ingress and egress ports on a per port basis
  - Jitter-free per-packet-based rate limiting support
  - Tail tagging mode (one byte added before FCS) support on Port 5 to inform the processor which ingress port receives the packet and its priority
  - Broadcast storm protection with percentage control (global and per port basis)

  - 1 kb entry forwarding table with 64 kb frame buffer
  - Four priority queues with dynamic packet mapping for IEEE 802.1p, IPv4 ToS (DIFF-SERV), IPv6 traffic class, etc.
  - Supports Wake-on-LAN (WoL) using AMD's Magic Packet™
  - VLAN and address filtering
  - Supports 802.1x port-based security, authentication, and MAC-based authentication via access control lists (ACL)
  - Provides port-based and rule-based ACLs to support Layer 2 MAC SA/DA address, Layer 3 IP address and IP mask, Layer 4 TCP/UDP port number, IP protocol, TCP flag, and compensation for the port security filtering
  - Ingress and egress rate limit based on bit per second (bps) and packet-based rate limiting (pps)
- Configuration Registers Access
  - High speed (4-wire, up to 50 MHz) interface (SPI) to access all internal registers
  - MII management interface (MIIM, MDC/MDIO 2-wire) to access all PHY registers per clause 22.2.4.5 of the IEEE 802.3 specification
  - I/O pin strapping facility to set certain register bits from I/O pins during reset time
  - Control registers configurable on-the-fly
- Power and Power Management
  - Full-chip software power down (all registers value are not saved and strap-in value will re-strap after release of the power down)
  - Per-port software power down
  - Energy detect power down (EDPD), which disables the PHY transceiver when cables are removed
  - Supports IEEE P802.3az Energy Efficient Ethernet to reduce power consumption in transceivers in LPI state even though cables are not removed
  - Dynamic clock tree control to reduce clocking in areas not in use
  - Low power consumption without extra power consumption on transformers
  - Voltages: Using external LDO power supplies.
  - Analog VDDAT 3.3V
  - VDDIO support
  - s 3.3V, 2.5V, and 1.8V
  - Low 1.2V voltage for analog and digital core power
  - Wake-on-LAN support with configurable packet control
- Additional Features
  - Single 25 MHz +50 ppm reference clock requirement
- Comprehensive programmable two LED indicator support for link, activity, full/half-duplex, and 10/100 speed
- Packaging and Environmental
  - Commercial temperature range: 0°C to +70°C
- Industrial temperature range: –40°C to +85°C
  - Package available in an 80-pin lead free (RoHS) LQFP form factor
  - Supports HBM ESD rating of 5 kV
  - 0.065 µm CMOS technology for lower power consumption
- Applications
  - Set-Top Boxes
  - Networked Printers and Servers
  - Test Instrumentation
  - LAN on Motherboard
  - Embedded Telecom Applications
  - Video Record/Playback Systems
  - Cable Modems/Routers
  - DSL Modems/Routers
  - Digital Video Recorders
  - IP and Video Phones
  - Wireless Access Points
  - Digital Televisions
  - Digital Media Adapters/Servers
  - Gaming Consoles

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1.0 INTRODUCTION

1.1 General Description

The KSZ8775CLX is a highly integrated, Layer 2-managed, five-port switch with numerous features designed to reduce system cost. It is intended for cost-sensitive applications requiring three 10/100 Mbps copper ports, one RMII on Port 4, and one 10/100/1000Mbps Gigabit uplink port on Port 5. The KSZ8775CLX incorporates a small package outline, the lowest power consumption with internal biasing, and on-chip termination. Its extensive set of features include enhanced power management, programmable rate limiting and priority ratio, tagged and port-based VLAN, port-based security and ACL rule-based packet filtering technology, QoS priority with four queues, management interfaces, enhanced MIB counters, high-performance memory bandwidth, and a shared memory-based switch fabric with non-blocking support. The KSZ8775CLX provides support for multiple CPU data interfaces to effectively address both current and emerging fast Ethernet and Gigabit Ethernet applications where the Port 5 GMAC can be configured to any of the RGMII, MII, and RMII modes.

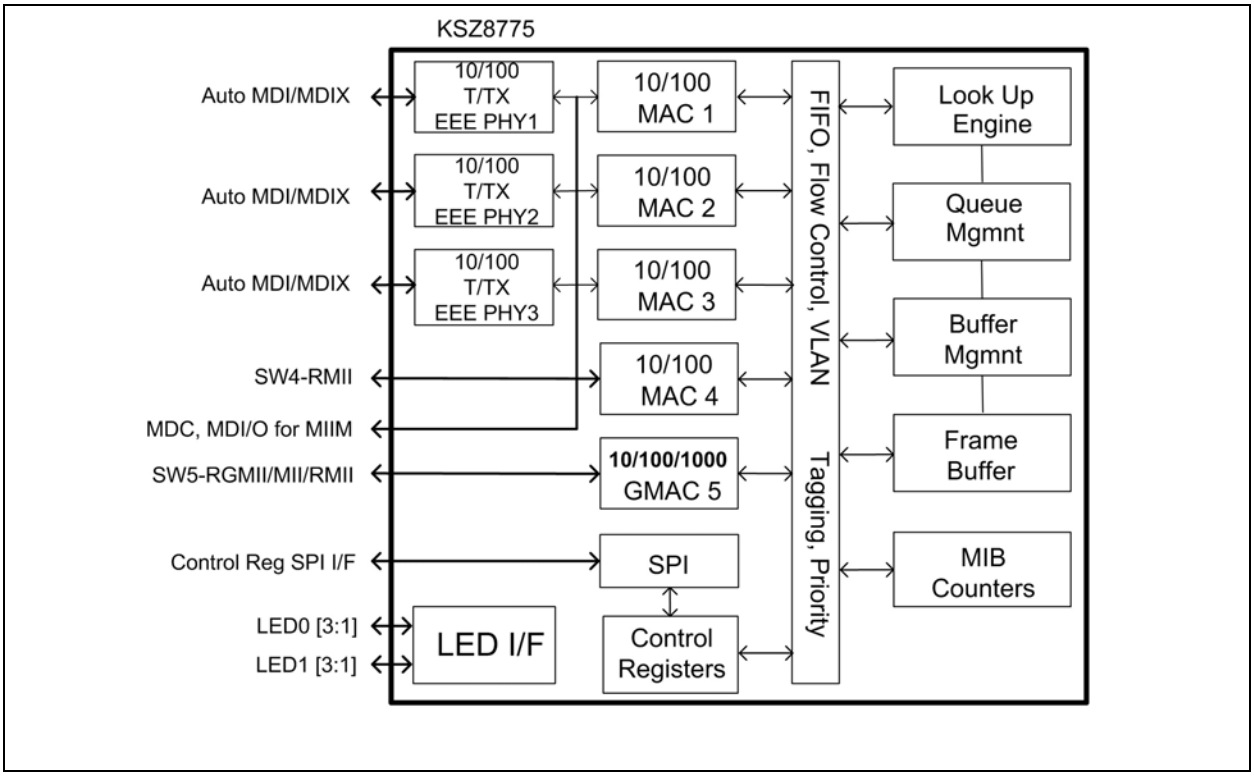
The KSZ8775CLX product is built upon industry-leading analog and digital technology, with features designed to offload host processing and streamline the overall design.

- Three integrated 10/100BASE-T/TX MAC/PHYs
- One integrated 10/100BASE-T/TX MAC with RMII interface
- One integrated 10/100/1000Base-T/TX GMAC with selectable RGMII, MII, and RMII interfaces
- Small 80-pin LQFP package

A robust assortment of power management features including Energy Efficient Ethernet (EEE), power management event (PME), and Wake-on-LAN (WoL) have been designed in to satisfy energy efficient environments.

All registers in the MAC/PHY units can be managed through the SPI interface. MIIM PHY registers can be accessed through the MDC/MDIO interface.

FIGURE 1-1: BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 80-QFN PIN ASSIGNMENT (TOP VIEW)

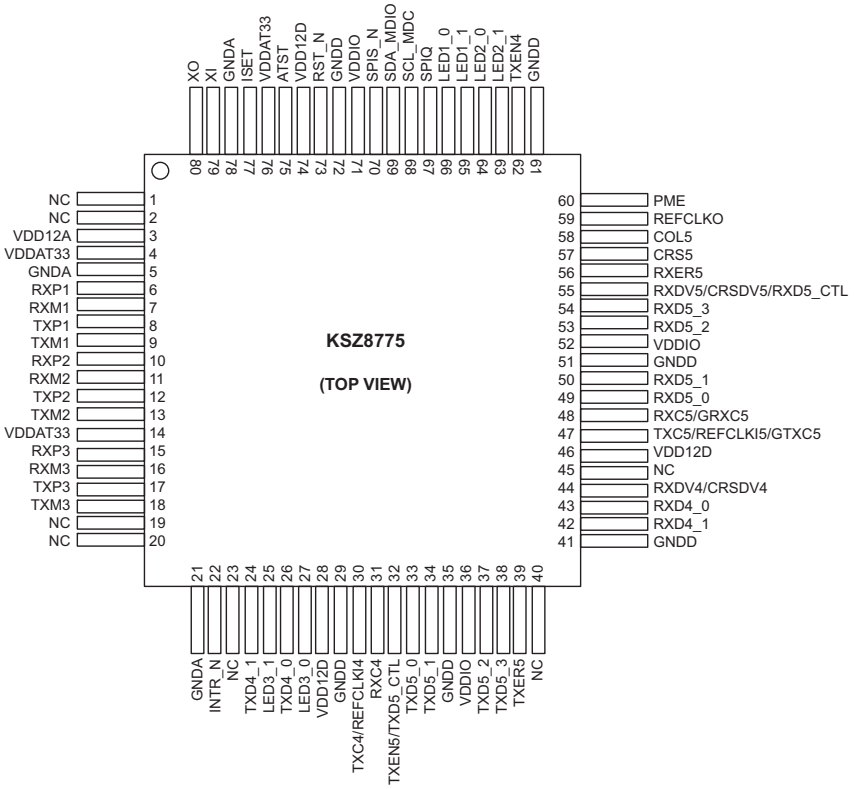


TABLE 2-1: SIGNALS

Num Pins	Pin Name	Type	Port	Pin Description
1	NC	NC		No connect
2	NC	NC		No connect
3	VDD12A	P		1.2V core power
4	VDDAT	P		3.3V or 2.5V analog power
5	GNDA	GND		Analog ground

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Pin Name	Type	Port	Pin Description
6	RXP1	I	1	Port 1 physical receive signal + (differential).
7	RXM1	I	1	Port 1 physical receive signal - (differential).
8	TXP1	O	1	Port 1 physical transmit signal + (differential).
9	TXM1	O	1	Port 1 physical transmit signal - (differential).
10	RXP2	I	2	Port 2 physical receive signal + (differential).
11	RXM2	I	2	Port 2 physical receive signal - (differential).
12	TXP2	O	2	Port 2 physical transmit signal + (differential)
13	TXM2	O	2	Port 2 physical transmit signal - (differential).
14	VDDAT	P		3.3V or 2.5V analog power
15	RXP3	I	3	Port 3 physical receive signal + (differential).
16	RXM3	I	3	Port 3 physical receive signal - (differential).
17	TXP3	O	3	Port 3 physical transmit signal + (differential).
18	TXM3	O	3	Port 3 physical transmit signal – (differential).
19	NC	NC		No connect
20	NC	NC		No connect
21	GNDA	GND		Analog ground
22	INTR_N	OPU		**Interrupt.** Active low. This pin is an open-drain output pin. **Note**: an external pull-up resistor is needed on this pin when it is in use.
23	NC	NC		No connect
24	TXD4_1	IPD	4	**RMII:** Port 4 RMII transmit bit [1].
25	LED3_1	IPU/O	3	**Port 3 LED Indicator 1.** See global Register 11 bits [5:4] for details. Strap option: Switch Port 5 GMAC5 interface mode select by LED3[1:0] 00 = MII for SW5-MII 01 = RMII for SW5-RMII 10 = Reserved 11 = RGMII for SW5-RGMII (default)
26	TXD4_0	IPD	4	**RMII:** Port 4 RMII transmit bit [0]
27	LED3_0	IPU/O	3	**Port 3 LED Indicator 0.** See global Register 11 bits [5:4] for details. Strap option: see LED3_1
28	VDD12D	P		1.2V core power.
29	GNDD	GND		Digital ground.

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Pin Name	Type	Port	Pin Description
30	TXC4/REF-CLKI4	I/O	4	**Port 4 Switch MAC4 SW4-RMII Reference Clock Input** RMII: Input for receiving 50 MHz clock in normal mode.
31	RXC4	I/O	4	Port 4 Switch MAC4 SW4-RMII reference clock out: RMII: Output 50 MHz reference clock for the receiving/transmit in the clock mode.
32	TXEN5/ TXD5_CTL	IPD	5	**MII/RMII:** Port 5 switch transmit enable. **RGMII:** Transmit data control.
33	TXD5_0	IPD	5	**RGMII/MII/RMII:** Port 5 switch transmit bit [0].
34	TXD5_1	IPD	5	**RGMII/MII/RMII:** Port 5 switch transmit bit [1].
35	GNDD	GND		Digital ground.
36	VDDIO	P		3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry.
37	TXD5_2	IPD	5	**RGMII/MII:** Port 5 switch transmit bit [2]. **RMII:** No connection.
38	TXD5_3	IPD	5	**RGMII/MII:** Port 5 switch transmit bit [3]. **RMII:** No connection.
39	TXER5	IPD	5	**MII:** Port 5 switch transmit error. **RGMII/RMII:** No connection.
40	NC	NC		No connect
41	GNDD	GND		Digital ground
42	RXD4_1	IPD/O	4	**RMII:** Port 4 SW4-RMII receive bit [1]

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Pin Name	Type	Port	Pin Description
43	RXD4_0	Ipd/O	4	**RMII:** Port 4 SW4-RMII receive bit [0]. Strap Option: Clock or Normal Mode Select in Port 4 RMII PU = Clock mode in RMII, using 25MHz OSC clock and provide 50 MHz RMII clock from pin RXC4 (Default) PD = Normal mode in RMII, the TXC4/REFCLKI4 pin on the Port 4 RMII will receive an external 50 MHz clock Note: Port 4 also can use either an internal or external clock in RMII mode based on this strap pin or the setting of the Register 70 (0x46) bit [7]. An external pull-up/down resistor is requested for the strap-in.
44	RXDV4/CRS-DV4	IPD/O	4	**RMII:** CRSDV4 is for Port 4 RMII carrier sense/receive data valid output.
45	NC	NC		No connect
46	VDD12D	P	5	1.2V core power
47	TXC5/REF-CLKI5/ GTXC5	I/O	5	Port 5 Switch GMAC5 Clock Pin: **MII:** 2.5/25 MHz clock, PHY mode is output, MAC mode is input. **RMII:** Input for receiving 50 MHz in normal mode. **RGMII:** Input 125 MHz clock with falling and rising edge to latch data for the data transfer.
48	RXC5/ GRXC5	I/O	5	Port 5 Switch GMAC5 Clock Pin: **MII:** 2.5/25 MHz clock, PHY mode is output, MAC mode is input. **RMII:** Output 50 MHz reference clock for the receiving/transmit in the clock mode. **RGMII:** Output 125 MHz clock with falling and rising edge to latch data for the receiving.
49	RXD5_0	IPD/O	5	**RGMII/MII/RMII:** Port 5 switch receive bit [0]
50	RXD5_1	IPD/O	5	**RGMII/MII/RMII:** Port 5 switch receive bit [1]
51	GNDD	GND		Digital ground
52	VDDIO	P		3.3V, 2.5V, or 1.8V digital VDD for digital I/O circuitry.
53	RXD5_2	IPD/O	5	**RGMII/MII:** Port 5 switch receive bit [2] **RMII:** No connection.

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Pin Name	Type	Port	Pin Description
54	RXD5_3	IPD/O	5	**RGMII/MII:** Port 5 switch receive bit [3] **RMII:** No connection.
55	RXDV5/CRS-DV5 /RXD5_CTL	IPD/O	5	**MII:** RXDV5 is for Port 5 switch MII receiving data valid. **RMII:** CRSDV5 is for Port 5 RMII carrier sense/receive data valid output. **RGMII:** RXD5_CTL is for Port 5 RGMII receiving data control.
56	RXER5	IPD/O	5	**MII:** Port 5 switch receive error. **RGMII/RMII:** No connection.
57	CRS5	IPD/O	5	**MII:** Port 5 switch MII modes carrier sense. **RGMII/RMII:** No connection.
58	COL5	IPD/O	5	**MII:** Port 5 Switch MII collision detect. **RGMII/RMII:** No connection.
59	REFCLKO	IPU/O		25 MHz clock output (Option) Controlled by the strap pin LED2_0. Default is enabled; it is better to disable it if not using it.
60	PME_N	I/O		Power Management Event This output signal indicates that a wake-on-LAN event has been detected as a result of a wake-up frame detection. The KSZ8775CLX is requesting the system to wake up from low power mode. Its assertion polarity is programmable with the default polarity set to active low.
61	GNDD	GND		Digital ground
62	TXEN4	IPD	4	**RMII:** Port 4 switch SW4-RMII transmit enable.

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Pin Name	Type	Port	Pin Description
63	LED2_1	IPU/O	2	Port 2 LED Indicator 1. See global Register 11 bits [5:4] for details. Strap option: Port 5 MII and RMII modes select When Port 5 is MII mode: PU = MAC mode. PD = PHY mode. When Port 5 is RMII mode: PU = Clock mode in RMII, using 25 MHz OSC clock and provide 50 MHz RMII clock from pin RXC5. PD = Normal mode in RMII, the TXC5/REFCLKI5 pin on the Port 5 RMII will receive an external 50 MHz clock **Note:** Port 5 also can use either an internal or external clock in RMII mode based on this strap pin or the setting of the Register 86 (0x56) bit[7].
64	LED2_0	IPU/O	2	Port 2 LED Indicator 0. See global Register 11 bits [5:4] for details. Strap option: REFCLKO enable PU = REFCLK_O (25 MHz) is enabled. (default) PD = REFCLK_O is disabled **Note:** It is better to disable this 25 MHz clock if not providing an extra 25 MHz clock for system.
65	LED1_1	IPU/O	1	Port 1 LED Indicator 1. See global Register 11 bits [5:4] for details. Strap option: PLL clock source select PU = Still use 25 MHz clock from XI/XO pins even though it is in Port 5 RMII normal mode. PD = Use external clock from TXC5 in Port 5 RMII normal mode. **Note:** If received clock in Port 5 RMII normal mode has too much clock jitter, you can still select the 25 MHz crystal/oscillator as the switch's clock source.
66	LED1_0	IPU/O	1	**Port 1 LED Indicator 0.** See global Register 11 bits [5:4] for details. Strap option: Speed select in Port 5 RGMII PU = 1 Gbps in RGMII. (default) PD = 10/100 Mbps in RGMII. **Note:** Programmable through internal registers also.
67	SPIQ	IPD/O	All	SPI Serial Data Output in SPI Slave Mode. Strap option: Serial bus configuration PD = SPI slave mode. PU = MDC/MDIO mode. **Note:** An external pull-up or pull-down resistor is required.
68	SCL_MDC	IPU	All	Clock Input for SPI or MDC/MDIO Interface. Input clock up to 50 MHz in SPI slave mode. Input clock up to 25 MHz in MDC/MDIO for MIIM access.

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Pin Name	Type	Port	Pin Description
69	SDA_MDIO	IPU/O	All	Data for SPI or MDC/MDIO Interface. Serial data input in SPI slave mode. MDC/MDIO interface data input/output.
70	SPIS_N	IPU	All	SPI Interface Chip Select. When SPIS_N is high, the KSZ8775CLX is deselected and SPIQ is held in the high impedance state. A high-to-low transition initiates the SPI data transfer. This pin is active low.
71	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry.
72	GNDD	GND	—	Digital ground.
73	RST_N	IPU	—	**Reset** This active low signal resets the hardware in the device. See the timing requirements in the Section 7.0, Timing Diagrams section.
74	VDD12D	P	—	1.2V core power
75	ATST	NC	—	No connect. Factory test pin.
76	VDDAT	P	—	3.3V or 2.5V analog power.
77	ISET		—	**Transmit Output Current Set** This pin configures the physical transmit output current. It should be connected to GND through a 12.4 kΩ 1% resistor.
78	GNDA	GND	—	Analog ground.
79	XI	I	—	Crystal Clock Input/Oscillator Input When using a 25 MHz crystal, this input is connected to one end of the crystal circuit. When using a 3.3V oscillator, this is the input from the oscillator. The crystal or oscillator should have a tolerance of ±50 ppm.
80	XO	O	—	Crystal Clock Output When using a 25 MHz crystal, this output is connected to one end of the crystal circuit.

The KSZ8775CLX can function as a managed switch and utilizes strap-in pins to configure the device for different modes. The strap-in option pins are configured by using external pull-up/down resistors to create a high or low state on the pins which are sampled during the power down reset or warm reset. The functions are described in the table below.

TABLE 2-2: STRAP-IN OPTIONS

Pin Number	Pin Name	PU/PD	Description
43	RXD4_0	IPD/O	Clock or Normal Mode Select in Port 4 RMII **Strap Option:** PU = Clock mode in RMII, using 25 MHz OSC clock and provide 50 MHz RMII clock from pin RXC4. PD = Normal mode in RMII, the TXC4/REFCLKI4 pin on the Port 5 RMII will receive an external 50 MHz clock **Note:** Port 4 also can use either an internal or external clock in RMII mode based on this strap pin or the setting of the Register 70 (0x46) bit[7]. An external pull-up/down resistor is requested.
64	LED2_0	IPU/O	REFCLKO Enable Strap Option: PU = REFCLK_O (25 MHz) is enabled. PD = REFCLK_O is disabled
63	LED2_1	IPU/O	Port 5 MII and RMII Modes Select Strap Option: When Port 5 is MII mode: PU = MAC mode. PD = PHY mode. When Port 5 is RMII mode: PU = Clock mode in RMII, using 25 MHz OSC clock and provide 50 MHz RMII clock from pin RXC5. PD = Normal mode in RMII, the TXC5/REFCLKI5 pin on the Port 5 RMII will receive an external 50 MHz clock **Note:** Port 5 also can use either an internal or external clock in RMII mode based on this strap pin or the setting of the Register 86 (0x56) bit[7].
25,27	LED3[1,0]	IPU/O	Switch Port 5 GMAC5 Interface Mode Select **Strap Option:** 00 = MII for SW5-MII 01 = RMII for SW5-RMII 10 = Reserved 11 = RGMII for SW5-RGMII (default)
66	LED1_0	IPU/O	Port 5 Gigabit Select Strap Option: PU = 1 Gbps in RGMII (default). PD = 10/100 Mbps in RGMII. **Note:** Also programmable through internal register.
65	LED1_1	IPU/O	PLL Clock Source Select Strap Option: PU = Still uses 25 MHz clock from XI/XO pin even though it is in Port 5 RMII normal mode (default). PD = Uses external clock from TXC5 pin in Port 5 RMII normal mode. **Note:** If received clock in Port 5 RMII normal mode has too much clock jitter, you still can select the 25 MHz crystal/oscillator as the switch's clock source.

TABLE 2-2: STRAP-IN OPTIONS

Pin Number	Pin Name	PU/PD	Description
67	SPIQ	IPD/O	Serial Bus Configuration Strap Option: PD = SPI slave mode. PU = MDC/MDIO mode. **Note:** An external pull-up or pull-down resistor is required.If the uplink port is used for RGMII interface, recommend using SPI mode to have opportunity setting the register 86 (0x56) bits [4:3] for RGMII V 2.0. MDC/MDIO mode can’t set this feature.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8775CLX contains three 10/100 physical layer transceivers, four media access control (MAC) units, and one Gigabit media access control (GMAC) unit with an integrated Layer 2-managed switch. The device runs in two modes. The first mode is as a three-port standalone switch. The second is as a five-port switch where the fifth port is provided through a Gigabit media independent interface that supports RGMII, MII, and RMII. This is useful for implementing an integrated broadband router.

The KSZ8775CLX has the flexibility to reside in a managed mode. In a managed mode, a host processor has complete control of the KSZ8775CLX via the SPI bus or the MDC/MDIO interface.

On the media side, the KSZ8775CLX supports IEEE 802.3 10BASE-T/100BASE-TX on all copper ports with Auto-MDI/MDI-X. The KSZ8775CLX can be used as a fully managed five-port switch or hooked up to a microprocessor via its SW-RGMII/MII/RMII interfaces to allow for integrating into a variety of environments.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry and DSP technology that makes the design more efficient, allows for reduced power consumption, and smaller die size.

Major enhancements from the KSZ8995 and KS8895 to the KSZ8775CLX include high speed host interface options such as the RGMII interface, power saving features such as IEEE 802.1az Energy Efficient Ethernet (EEE), MLD snooping, Wake-on-LAN (WoL), port-based ACL filtering for port security, enhanced QoS priority, rapid spanning tree, IGMP snooping, port mirroring support, and flexible rate limiting.

3.1 Functional Overview: Physical Layer (PHY)

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 12.4 kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

3.1.2.1 PLL Clock Synthesizer

The KSZ8775CLX generates 125 MHz, 83 MHz, 41 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator.

3.1.2.2 Scrambler/Descrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

3.1.3 10BASE-T TRANSMIT

The 10BASE-T output driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

3.1.4 10BASE-T RECEIVE

On the receive side, input buffers and level-detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into a clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse-widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8775CLX decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.5 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8775CLX supports HP Auto-MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto-MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8775CLX device. This feature is extremely useful when end users are unaware of cable types, and also, saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers or MIIM PHY registers. The IEEE 802.3u standard MDI and MDI-X definitions are in the table below.

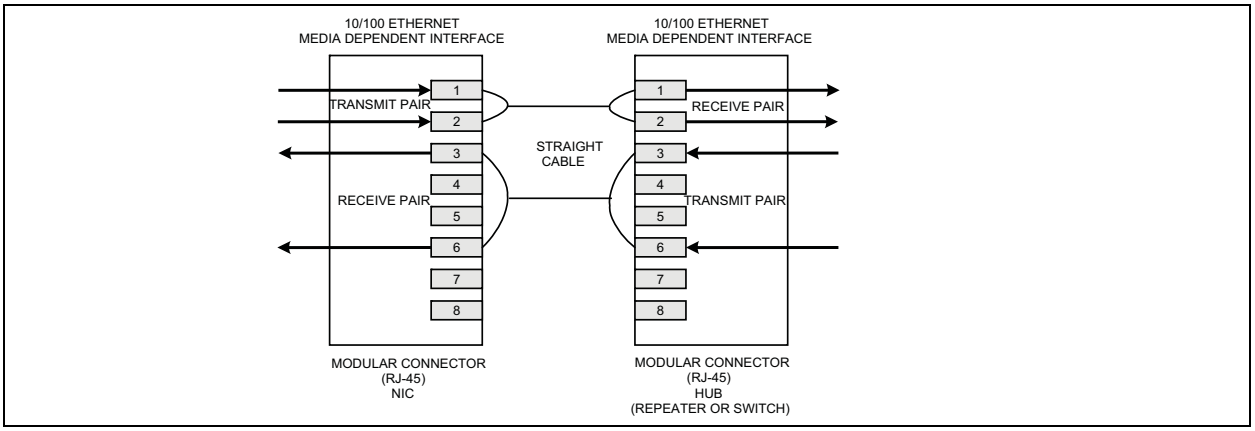
TABLE 3-1: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.1.5.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device or an MDI-X device to an MDI device. The following diagram depicts a typical straight cable connection between a NIC (MDI) and a switch or hub (MDI-X).

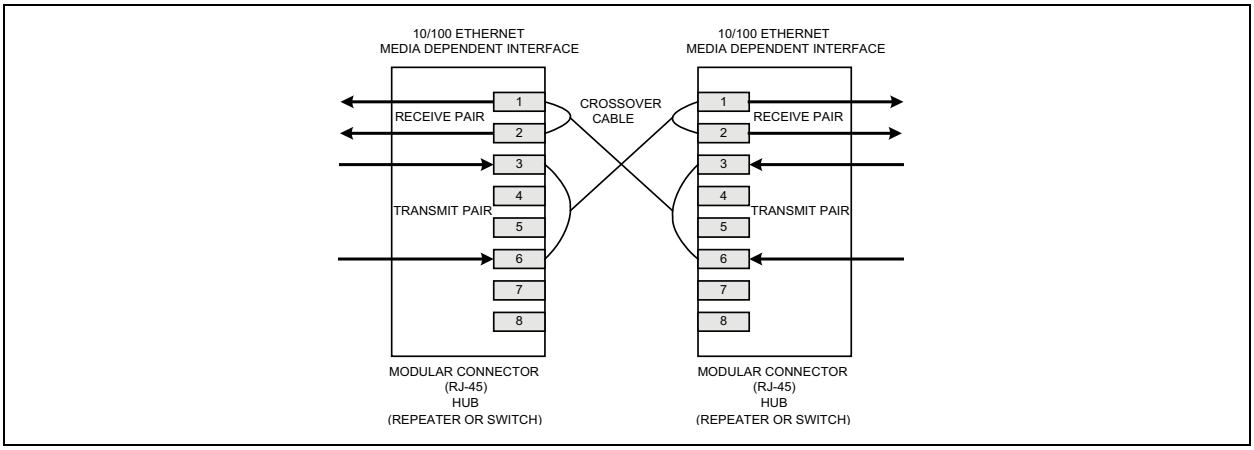
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.1.5.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



3.1.6 AUTO-NEGOTIATION

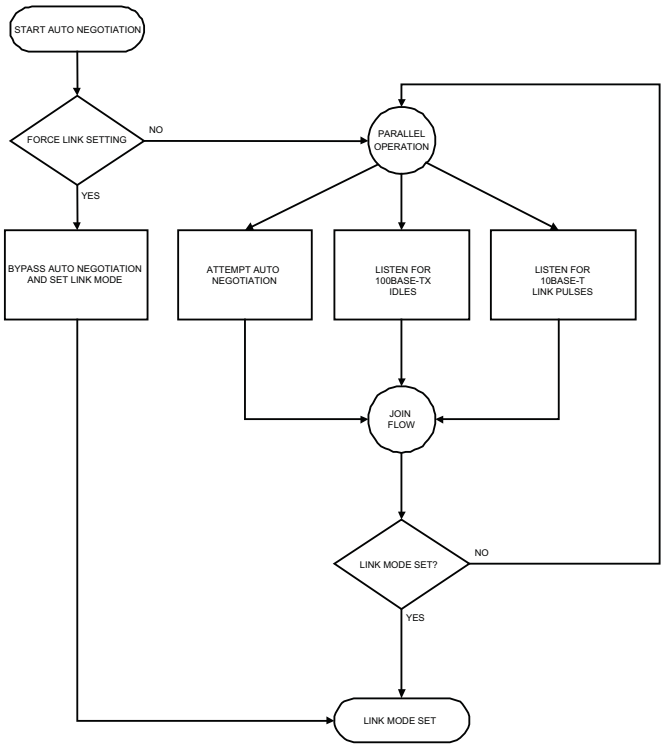
The KSZ8775CLX conforms to the auto-negotiation protocol as described by the IEEE 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation. Auto-negotiation is supported only for the copper ports.

The following list shows the speed and duplex operation mode from highest to lowest.

- Highest: 100BASE-TX, full-duplex
- High: 100BASE-TX, half-duplex
- Low: 10Base-T, full-duplex
- Lowest: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8775CLX link partner is forced to bypass auto-negotiation, the KSZ8775-CLX sets its operating mode by observing the signal at its receiver. This is known as parallel detection and allows the KSZ8775CLX to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. The auto-negotiation link up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.1.7 CABLE DIAGNOSTICS

The LinkMD® feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with maximum distance of 200m and accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format.

Please note that cable diagnostics are only valid for copper connections.

3.1.8 ACCESS

LinkMD is initiated by accessing the PHY's special control/status Registers {26, 42, 58} and the LinkMD result Registers {27, 43, 59} for Ports 1, 2, and 3 respectively and in conjunction with the Port control 10 Register for Ports 1, 2, and 3 respectively to disable Auto-MDI/MDI-X.

Alternatively, the MIIM PHY Registers 0 and 1d can also be used for LinkMD access.

3.1.9 USAGE

The following is a sample procedure for using LinkMD with Registers {26, 27, 29} on Port 1.

1. Disable Auto-MDI/MDI-X by writing a '1' to Register 29, bit [2] to enable manual control over the differential pair used to transmit the LinkMD pulse.
2. Start cable diagnostic test by writing a '1' to Register 26, bit [4]. This enable bit is self-clearing.
3. Wait (poll) for Register 26, bit [4] to return a '0', and indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in Register 26, bits [6:5]. The results are as follows:
   - •00 = normal condition (valid test)
   - •01 = open condition detected in cable (valid test)

- 10 = short condition detected in cable (valid test)
- 11 = cable diagnostic test failed (invalid test)

The '11' case, invalid test, occurs when the KSZ8775CLX is unable to shut down the link partner. In this instance, the test is not run because it would be impossible for the KSZ8775CLX to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating Register 26, bit [0] and Register 27, bits [7:0] and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

D (distance to cable fault meter) = 0.4 x (Register 26, bit [0], Register 27, bits [7:0])

D (distance to cable fault) is expressed in meters.

Concatenated value of Registers 26 bit [0] and 27 bits [7:0] should be converted to decimal before multiplying by 0.4.

The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

For Port 2, Port 3, and using the MIIM PHY registers, LinkMD® usage is similar.

3.1.10 A LINKMD® EXAMPLE

The following is a sample procedure for using LinkMD® on Port 1, Port 2, and Port 3.

```
//Disable Auto-MDI/MDI-X and force to MDI-X mode
//'w' is WRITE the register. 'r' is READ register below
w 1d 04
w 2d 04
w 3d 04
//Set internal registers temporary by indirect registers, adjust for LinkMD
w 6e a0
w 6f 4d
w a0 80
//Enable LinkMD testing with fault cable for Port 1, Port 2, and Port 3
w 1a 10
w 2a 10
w 3a 10
//Wait until Port Register Control 8 bit [4] returns a '0' (self-clear)
//Diagnosis results
r 1a
r 1b
r 2a
r 2b
r 3a
r 3b
//For example on Port 1, the result analysis based on the values of the register 0x1a and 0x1b
//The register 0x1a bits [6-5] are for the open or the short detection.
//The register 0x1a bit [0] + the register 0x1b bits [7-0] = CDT_Fault_Count [8-0]
//The distance to fault is about 0.4 x (CDT_Fault_Count [8-0])
```

3.2 On-Chip Termination and Internal Biasing

The KSZ8775CLX reduces the board cost and simplifies the board layout by using on-chip termination resistors for all ports and RX/TX differential pairs without external termination resistors. The combination of the on-chip termination and the internal biasing will save more PCB space and power consumption in system, compared with using external biasing and termination resistors for multiple ports' switches because the transformers do not consume power anymore. The center taps of the transformer should not need to be tied to the analog power.

3.3 Functional Overview: Media Access Controller (MAC)

3.3.1 MEDIA ACCESS CONTROLLER OPERATION

The KSZ8775CLX strictly abides by IEEE 802.3 standards to maximize compatibility.

3.3.2 INTER-PACKET GAP (IPG)

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

3.3.3 BACK-OFF ALGORITHM

The KSZ8775CLX implements the IEEE 802.3 standard binary exponential backoff algorithm and optional "aggressive mode" back-off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration in Register 3.

3.3.4 LATE COLLISION

If a transmit packet experiences collisions after 512-bit times of the transmission, the packet will be dropped.

3.3.5 ILLEGAL FRAMES

The KSZ8775CLX discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Register 4. For special applications, the KSZ8775CLX can also be programmed to accept frames up to 2k bytes in Register 3 bit [6]. Because the KSZ8775CLX supports VLAN tags, the maximum sizing is adjusted when these tags are present.

3.3.6 FLOW CONTROL

The KSZ8775CLX supports standard IEEE 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8775CLX receives a pause control frame, the KSZ8775CLX will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow-controlled), only flow control packets from the KSZ8775CLX will be transmitted.

On the transmit side, the KSZ8775CLX has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues, and available receive queues.

The KSZ8775CLX flow controls a port that has just received a packet if the destination port resource is busy. The KSZ8775CLX issues a flow control frame (XOFF) containing the maximum pause time defined in the IEEE 802.3x standard. Once the resource is freed up, the KSZ8775CLX sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is also provided to prevent over-activation and deactivation of the flow control mechanism. The KSZ8775CLX flow controls all ports if the receive queue becomes full.

3.3.7 HALF-DUPLEX BACK PRESSURE

The KSZ8775CLX also provides a half-duplex back pressure option (this is not in IEEE 802.3 standards). The activation and deactivation conditions are the same as the ones given for full-duplex mode. If back pressure is required, then the KSZ8775CLX sends preambles to defer the other station's transmission (carrier sense deference). To avoid jabber and excessive deference as defined in IEEE 802.3 standards, after a certain period of time, the KSZ8775CLX discontinues carrier sense but raises it quickly after it drops packets to inhibit other transmissions. This short silent time (no carrier sense) prevents other stations from sending out packets and keeps other stations in a carrier-sense-deferred state. If the port has packets to send during a back pressure situation, then the carrier-sense-type back pressure is interrupted and those packets are transmitted instead. If there are no more packets to send, carrier-sense-type back pressure

becomes active again until switch resources are free. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets. To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive back-off (Register 3, bit [0])
- No excessive collision drop (Register 4, bit [3])
- Back pressure (Register 4, bit [5])

These bits are not set as the default because this is not the IEEE standard.

3.3.8 BROADCAST STORM PROTECTION

The KSZ8775CLX has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets are normally forwarded to all ports except the source port and thus use too many switch resources (bandwidth and available space in transmit queues). The KSZ8775CLX has the option to include multicast packets for storm control. The broadcast storm rate parameters are programmed globally and can be enabled or disabled on a per port basis. The rate is based on a 50 ms (0.05s) interval for 100BT and a 500 ms (0.5s) interval for 10BT. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Registers 6 and 7. The default setting for Registers 6 and 7 is 0x4A (74 decimal). This is equal to a rate of 1%, as calculated in Equation 3-1.

EQUATION 3-1:

$$(148800\ frames)/(se) \times (50ms) \times (0.05s)/interval \times 1\% = (74\ \text{frames})/\text{interval (approx)} = 0x4A$$

3.4 Functional Overview: Switch Core

The internal look-up table stores MAC addresses and their associated information. It contains a 1k unicast address table plus switching information. The KSZ8775CLX is guaranteed to learn 1k addresses and distinguishes itself from a hash-based look-up table, which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.4.1 LEARNING

The internal look-up engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted first to make room for the new entry.

3.4.2 MIGRATION

The internal look-up engine also monitors whether a station is moved. If this occurs, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table, but the associated source port information is different.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

3.4.3 AGING

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 ±75 seconds. This feature can be enabled or disabled through Register 3 bit [2].

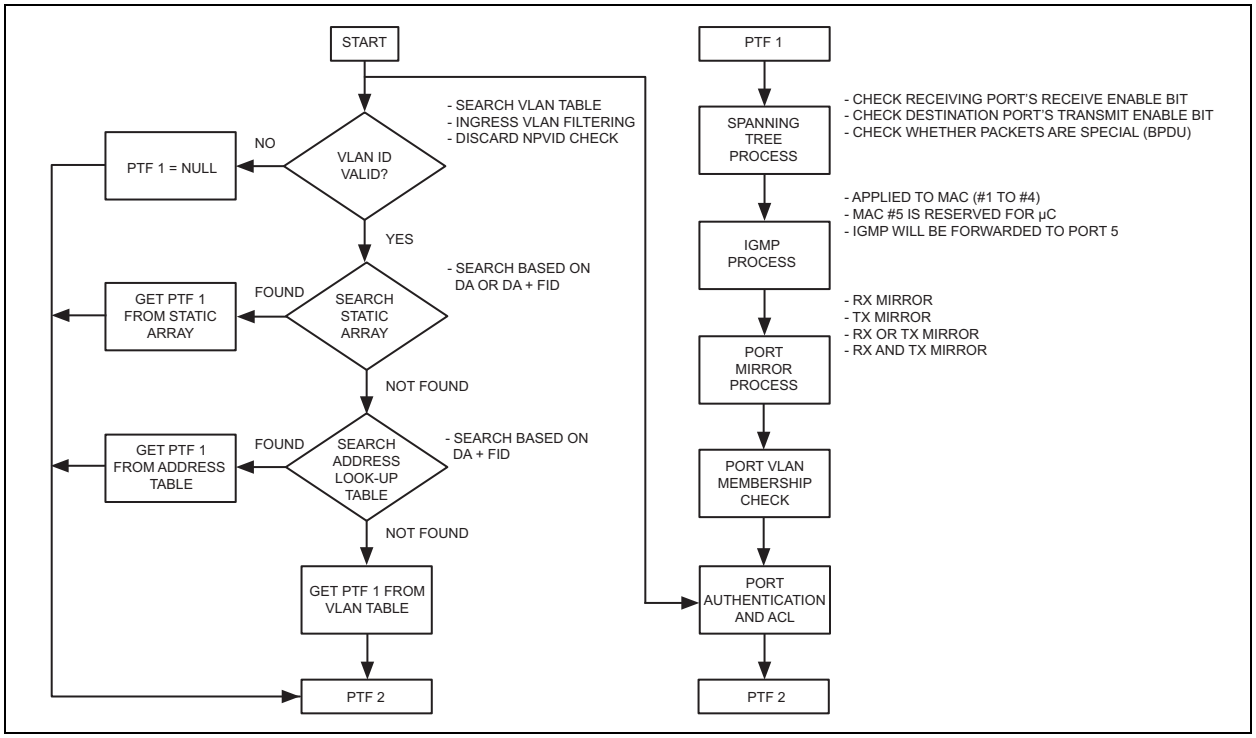
3.4.4 FORWARDING

The KSZ8775CLX will forward packets using an algorithm that is depicted in the following flowcharts. The next figure shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and then comes up with port to forward 1 (PTF1). PTF1 is then further modified by the spanning tree, IGMP snooping, port mirroring, and port VLAN processes and authentication to come up with port to forward 2 (PTF2), as shown in the Equation 3-4. The authentication and ACL have highest priority in the forwarding process, ACL result will overwrite the result of the forwarding process. This is where the packets will be sent.

The KSZ8775CLX will not forward the following packets:

- Error packets: These include framing errors, frame check sequence (FCS) errors, alignment errors, and illegal size packet errors.
- IEEE 802.3x PAUSE frames: KSZ8775CLX intercepts these packets and performs full-duplex flow control accordingly.
- Local packets: Based on destination address (DA) lookup, if the destination port from the look-up table matches the port from which the packet originated, the packet is defined as local.

FIGURE 3-4: DESTINATION ADDRESS LOOK-UP AND RESOLUTION FLOW CHART



3.4.5 SWITCHING ENGINE

The KSZ8775CLX features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward modes, while the efficient switching mechanism reduces overall latency. The KSZ8775-CLX has a 64kb internal frame buffer. This resource is shared between all five ports. There are a total of 512 buffers available. Each buffer is sized at 128 bytes.

3.5 Functional Overview

3.5.1 POWER

The KSZ8775CLX device requires 3.3V analog power. An external 1.2V LDO provides the necessary 1.2V to power the analog and digital logic cores. The various I/Os can be operated at 1.8V, 2.5V, and 3.3V. The table below illustrates the various voltage options and requirements of the device.

TABLE 3-2: VOLTAGE OPTIONS AND REQUIREMENTS

Power Signal Name	Device Pin	Requirement
VDDAT	4, 14, 76	3.3V input power to the analog blocks of transceiver in the device.
VDDIO	36, 52, 71	Choice of 1.8V or 2.5V or 3.3V for the I/O circuits. These input power pins power the I/O circuitry of the device.

TABLE 3-2: VOLTAGE OPTIONS AND REQUIREMENTS

Power Signal Name	Device Pin	Requirement
VDD12A	3	1.2V core power. Filtered 1.2V input voltage. These pins feed 1.2V to power the internal analog and digital cores.
VDD12D	28, 46, 74	
GNDA	5, 21, 78	Analog ground.
GNDD	29, 35, 41, 51, 61, 72	Digital ground.

3.5.2 POWER MANAGEMENT

The KSZ8775CLX supports enhanced power management in a low power state, with energy detection to ensure low power dissipation during device idle periods. There are three operation modes under the power management function which are controlled by the Register 14 bits [4:3] and the Port Control 10 Register bit [3] as shown below:

- Register 14 bits [4:3] = 00 normal operation mode
- Register 14 bits [4:3] = 01 energy detect mode
- Register 14 bits [4:3] = 10 soft power-down mode
- Register 14 bits [4:3] = 11 reserved

The Port Control 10 Register 29, 45, 61 bit [3] = 1 are for the port-based power-down mode.

Table 3-3 indicates all internal function block statuses under four different power management operation modes.

TABLE 3-3: INTERNAL FUNCTION BLOCK STATUS

KSZ8775CLX Function Blocks	Power Management		
	Normal Mode	Energy Detect Mode	Soft Power-Down Mode
Internal PLL Clock	Enabled	Disabled	Disabled
TX/RX PHY	Enabled	Energy detect at RX	Disabled
MAC	Enabled	Disabled	Disabled
Host Interface	Enabled	Disabled	Disabled

3.5.2.1 Normal Operation Mode

This is the default setting bits [4:3] = 00 in Register 14 after chip power-up or hardware reset. When KSZ8775CLX is in normal operation mode, all PLL clocks are running, PHY and MAC are on, and the host interface is ready for CPU read or write.

During normal operation mode, the host CPU can set the bits [4:3] in Register 14 to change the current normal operation mode to any one of the other three power management operation modes.

3.5.2.2 Energy Detect Mode

Energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8775-CLX port is not connected to an active link partner. In this mode, the device will save more power when the cables are unplugged. If the cable is not plugged in, the device can automatically enter a low power state—the energy detect mode. In this mode, the device will keep transmitting 120 ns-wide pulses at a rate of 1 pulse per second. Once activity resumes due to plugging in a cable or an attempt by the far end to establish a link, the device can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of the normal power state and low power state. While in low power state, the device reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bits [4:3] = 01 in Register 14. When the KSZ8775CLX is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than the pre-configured value at bits [7:0] go-sleep time in Register 15, then the KSZ8775CLX will go into low power state. When the KSZ8775CLX is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable, the device will enter normal power state. When the device is at normal power state, it is able to transmit or receive packet from the cable.

3.5.2.3 Soft Power-Down Mode

The soft power-down mode is entered by setting bits [4:3] = 10 in Register 14. When the KSZ8775CLX is in this mode, all PLL clocks are disabled, also all of the PHYs and MACs are off. Any dummy host access will wake-up this device from current soft power-down mode to normal operation mode and internal reset will be issued to make all internal registers go to the default values.

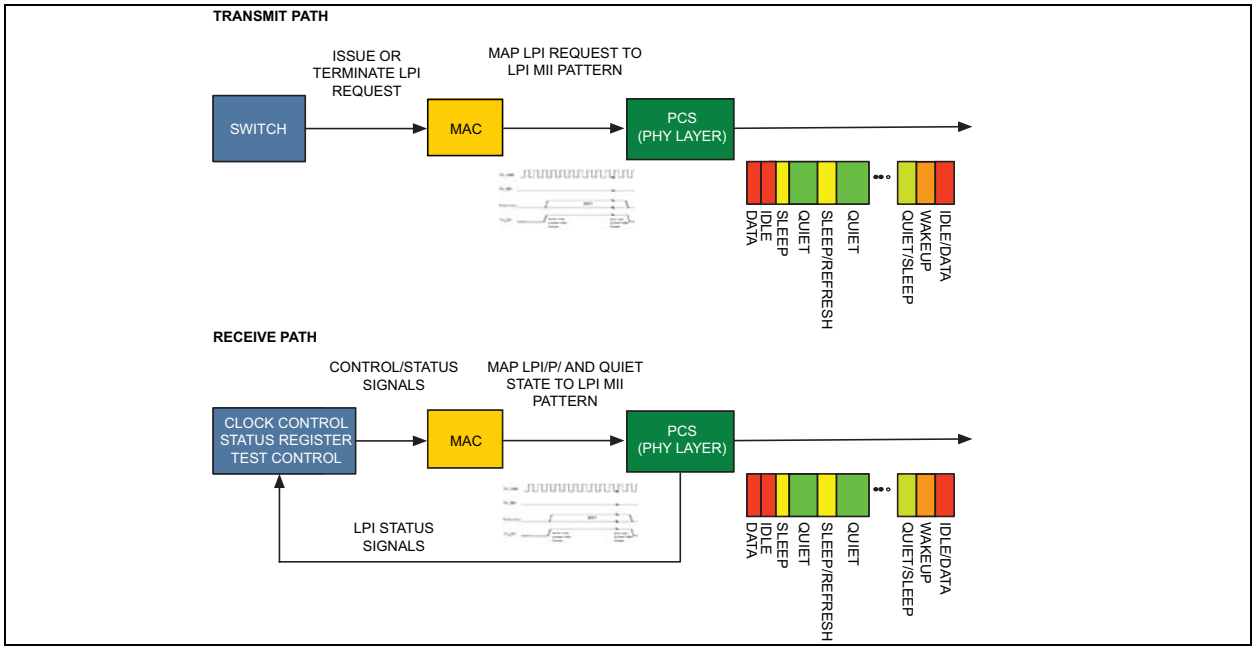
3.5.2.4 Port-Based Power-Down Mode

In addition, the KSZ8775CLX features a per-port power-down mode. To save power, a PHY port that is not in use can be powered down via the Port Control 10 Register bit [3] or MIIM PHY Register 0 bit [11].

3.5.2.5 Energy Efficient Ethernet (EEE)

Along with supporting different power saving modes, the KSZ8775CLX extends its green functionality by supporting EEE features defined in IEEE P802.3az/D2.3, March 2010. Both 10Base-T and 100BASE-TX EEE functions are supported in KSZ8775CLX. In 100BASE-TX, the EEE operation is asymmetric on the same link, which means one direction could be in low power idle (LPI) state while another direction could handle packet transfer activity. Different from other types of power saving modes, EEE is able to maintain the link while conserving power. Based on IEEE specification, the energy saving from EEE is done at the PHY level. KSZ8775CLX reduces the power consumption not only at PHY level but also at MAC and switch level by shutting down the unused clocks as much as possible when the device is in low power idle phase.

FIGURE 3-5: EEE TRANSMIT AND RECEIVE SIGNALING PATHS



The KSZ8775CLX supports the IEEE 802.3az Energy Efficient Ethernet standard for both 10 Mbps and 100 Mbps interfaces. The EEE capability combines switch, MAC, and PHY to support operation in low power idle (LPI) mode. When the LPI mode is enabled, systems on both sides of the link can save power during periods of low link utilization.

EEE implementation provides a protocol to coordinate transitions to or from lower power consumption without changing the link status and without dropping or corrupting frames. The transition time into and out of the lower power consumption is kept small enough to be transparent to upper layer protocols and applications. EEE specifies the means to exchange capabilities between link partners to determine whether EEE is supported and to select the best set of parameters common to both sides.

Besides supporting the 100BASE-TX PHY EEE, the KSZ8775CLX also supports 10BASE-T with reduced transmit amplitude requirements for 10 Mbps mode to allow a reduction in power consumption.

3.5.2.5.1 LPI Signaling

Low power idle signaling allows the switch to indicate to the PHY, and to the link partner, that a break in the data stream is expected. The switch can use this information to enter power-saving modes that require additional time to resume normal operation. LPI signaling also informs the switch when the link partner has sent such an indication. The definition of LPI signaling uses the MAC for simplified full-duplex operation with carrier sense deferral. This provides full-duplex operation but uses the carrier sense signal to defer transmission when the PHY is in the LPI mode.

The decision on when to signal LPI (LPI request) to the link partner is made by the switch and communicated to the PHY through the MAC MII interface. The switch is also informed when the link partner is signaling LPI and indicating LPI activation (LPI indication) on the MAC interface. The conditions under which the switch decides to send LPI and what actions are taken by the switch when it receives LPI from the link partner, are specified in the implementation section.

3.5.2.5.2 LPI Assertion

Without LPI assertion, the normal traffic transition continues on the MII interface. As soon as an LPI request is asserted, the LPI assert function starts to transmit the “Assert LPI” encoding on the MII and stops the MAC from transmitting normal traffic. Once the LPI request is de-asserted, the LPI assert function starts to transmit the normal inter-frame encoding on the MII again. After a delay, the MAC is allowed to start transmitting again. This delay is provided to allow the link partner to prepare for normal operation. Figure 8 illustrates the EEE LPI between two active data idles.

3.5.2.5.3 LPI Detection

In the absence of “Assert LPI” encoding on the receive MII, the LPI detect function maps the receive MII signals as normal conditions. At the start of LPI, indicated by the transition from normal inter-frame encoding to the “Assert LPI” encoding on the receive MII, the LPI detect function continues to indicate idle on interface and asserts LP_IDLE indication. At the end of LPI, indicated by the transition from the “Assert LPI” encoding to any other encoding on the receive MII, LP_IDLE indication is de-asserted and the normal decoding operation resumes.

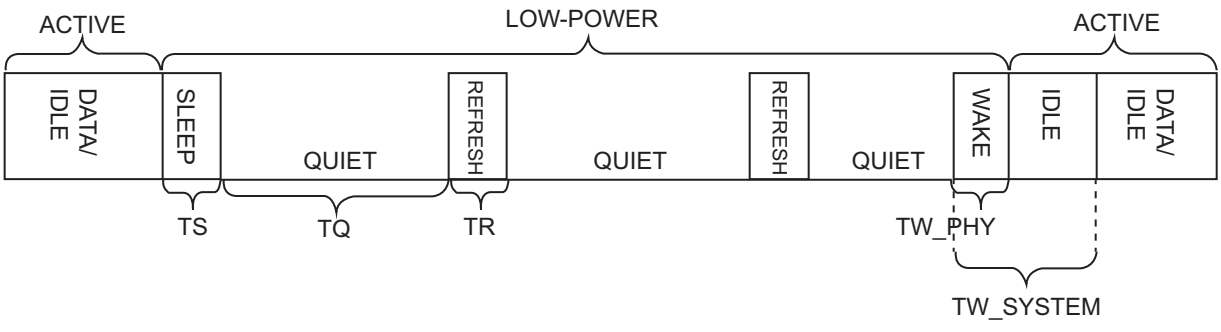
3.5.2.5.4 PHY LPI Transmit Operation

When the PHY detects the start of “Assert LPI” encoding on the MII, the PHY signals sleep to its link partner to indicate that the local transmitter is entering LPI mode. The EEE capability requires the PHY transmitter to go quiet after sleep is signaled. LPI requests are passed from one end of the link to the other and system energy savings can be achieved even if the PHY link does not go into a low power mode.

The transmit function of the local PHY is enabled periodically to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. This quiet-refresh cycle continues until the reception of the normal inter-frame encoding on the MII. The transmit function in the PHY communicates this to the link partner by sending a wake signal for a predefined period of time. The PHY then enters the normal operating state. No data frames are lost or corrupted during the transition to or from the LPI mode.

In 100BT/full-duplex EEE operation, refresh transmissions are used to maintain the link and the quiet periods are used for power saving. Approximately every 20-22 ms a refresh of 200-220 µs is sent to the link partner. The refresh transmission and quiet periods are shown in Figure 3-6.

FIGURE 3-6: TRAFFIC ACTIVITY AND EEE LPI OPERATIONS



Ts = THE PERIOD OF TIME THAT THE PHY TRANSMITS THE SLEEP SIGNAL BEFORE TURNING ALL TRANSMITTERS OFF, 200 ≤ Ts ≤ 220 USED IN 100BASE-TX.
Tq = THE PERIOD OF TIME THAT THE PHY REMAINS QUIET BEFORE SENDING THE REFRESH SIGNAL, 20_000 ≤ Tq ≤ 22_000 USED IN 100BASE-TX.
Tr = DURATION OF THE REFRESH SIGNAL, 200 ≤ Tr ≤ 220 USED IN 100BASE-TX.