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Integrated 4-Port 10/100 Managed Ethernet Switch with Gigabit RGMII/MII/RMII Interface

Target Applications

- Industrial Ethernet Applications that Employ IEEE 802.3-Compliant MACs. (Ethernet/IP, Profinet, MODBUS TCP, etc.)
- VoIP Phone
- Set-Top/Game Box
- Automotive
- Industrial Control
- IPTV POF
- SOHO Residential Gateway with Full-Wire Speed of Four LAN Ports
- Broadband Gateway/Firewall/VPN
- Integrated DSL/Cable Modem
- Wireless LAN Access Point + Gateway
- Standalone 10/100 Switch
- Networked Measurement and Control Systems

Features

- Management Capabilities
 - The KSZ8794CNX Includes All the Functions of a 10/100BASE-T/TX Switch System Which Combines a Switch Engine, Frame Buffer Management, Address Look-Up Table, Queue Management, MIB Counters, Media Access Controllers (MAC), and PHY Transceivers
 - Non-Blocking Store-and-Forward Switch Fabric Assures Fast Packet Delivery by Utilizing a 1024-Entries Forwarding Table
 - Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port
 - MIB Counters for Fully Compliant Statistics Gathering (36 Counters per Port)
 - Support Hardware for Port-Based Flush and Freeze Command in MIB Counter.
 - Multiple Loopback of Remote PHY, and MAC Modes Support for the Diagnostics
 - Rapid Spanning Tree Support (RSTP) for Topology Management and Ring/Linear Recovery
- Robust PHY Ports
 - Four Integrated IEEE 802.3/802.3u-Compliant Ethernet Transceivers Supporting 10BASE-T and 100BASE-TX
 - IEEE 802.1az EEE Supported

- On-Chip Termination Resistors and Internal Biasing for Differential Pairs to Reduce Power
- HP Auto MDI/MDI-X Crossover Support Eliminates the Need to Differentiate Between Straight or Crossover Cables in Applications
- MAC and GMAC Ports
 - Three Internal Media Access Control (MAC1 to MAC3) Units and One Internal Gigabit Media Access Control (GMAC4) Unit
 - RGMII, MII, or RMII Interfaces Support for the Port 4 GMAC4 with Uplink
 - 2 KByte Jumbo Packet Support
 - Tail Tagging Mode (One Byte Added Before FCS) Support on Port 4 to Inform the Processor in which Ingress Port Receives the Packet and its Priority
 - Supports Reduced Media Independent Interface (RMII) with 50 MHz Reference Clock Output
 - Supports Media Independent Interface (MII) in Either PHY Mode or MAC Mode on Port 4
 - LinkMD[®] Cable Diagnostic Capabilities for Determining Cable Opens, Shorts, and Length
- Advanced Switch Capabilities
 - Non-Blocking Store-and-Forward Switch Fabric Assures Fast Packet Delivery by Utilizing a 1024-Entries Forwarding Table
 - 64 KB Frame Buffer RAM
 - IEEE 802.1q VLAN Support for up to 128 Active VLAN Groups (Full-Range 4096 of VLAN IDs)
 - IEEE 802.1p/Q Tag Insertion or Removal on a Per Port Basis (Egress)
 - VLAN ID Tag/Untag Options on Per Port Basis
 - Fully Compliant with IEEE 802.3/802.3u Standards
 - IEEE 802.3x Full-Duplex with Force-Mode Option and Half-Duplex Back-Pressure Collision Flow Control
 - IEEE 802.1w Rapid Spanning Tree Protocol Support
 - IGMP v1/v2/v3 Snooping for Multicast Packet Filtering

- QoS/CoS Packets Prioritization Support: 802.1p, DiffServ-Based and Re-Mapping of 802.1p Priority Field Per Port Basis on Four Priority Levels
- IPv4/IPv6 QoS Support
- IPv6 Multicast Listener Discovery (MLD) Snooping
- Programmable Rate Limiting at the Ingress and Egress Ports on a Per Port Basis
- Jitter-Free Per Packet Based Rate Limiting Support
- Tail Tag Mode (1 byte Added before FCS) Support on Port 4 to Inform the Processor which Ingress Port Receives the Packet
- Broadcast Storm Protection with Percentage Control (Global and Per Port Basis)
- 1K Entry Forwarding Table with 64 KB Frame Buffer
- 4 Priority Queues with Dynamic Packet Mapping for IEEE 802.1P, IPv4 TOS (DIFF-SERV), IPv6 Traffic Class, etc.
- Supports WoL Using AMD's Magic Packet
- VLAN and Address Filtering
- Supports 802.1x Port-Based Security, Authentication and MAC-Based Authentication via Access Control Lists (ACL)
- Provides Port-Based and Rule-Based ACLs to Support Layer 2 MAC SA/DA Address, Layer 3 IP Address and IP Mask, Layer 4 TCP/UDP Port Number, IP Protocol, TCP Flag and Compensation for the Port Security Filtering
- Ingress and Egress Rate Limit Based on Bit per Second (bps) and Packet-Based Rate Limiting (pps)
- Configuration Registers Access
 - High-Speed SPI (4-Wire, up to 50 MHz) Interface to Access All Internal Registers
 - MII Management (MIIM, MDC/MDIO 2-Wire) Interface to Access All PHY Registers per Clause 22.2.4.5 of the IEEE 802.3 Specification
 - I/O Pin Strapping Facility to Set Certain Register Bits from I/O Pins During Reset Time
 - Control Registers Configurable On-the-Fly
- Power and Power Management
 - Full-Chip Software Power-Down (All Register Values are Not Saved and Strap-In Value Will Re-Strap After it Releases the Power-Down)
 - Per-Port Software Power-Down
 - Energy Detect Power-Down (EDPD), which Disables the PHY Transceiver When Cables are Removed
 - Supports IEEE P802.3az Energy Efficient Ethernet (EEE) to Reduce Power Consumption in Transceivers in LPI State Even Though Cables are Not Removed
- Dynamic Clock Tree Control to Reduce Clocking in Areas that are Not in Use
- Low Power Consumption without Extra Power Consumption on Transformers
- Voltages: Using External LDO Power Supplies
 - Analog V_{DDAT} 3.3V or 2.5V
 - V_{DDIO} Support 3.3V, 2.5V, and 1.8V
 - Low 1.2V Voltage for Analog and Digital Core Power
- WoL Support with Configurable Packet Control
- Additional Features
 - Single 25 MHz ± 50 ppm Reference Clock Requirement
 - Comprehensive Programmable Two-LED Indicator Support for Link, Activity, Full-/Half-Duplex, and 10/100 Speed
- Packaging and Environmental
 - Commercial Temperature Range: 0°C to +70°C
 - Industrial Temperature Range: -40°C to +85°C
 - Small Package Available in a Lead-Free, RoHS-Compliant 64-Pin QFN
 - 0.065 μ m CMOS Technology for Lower Power Consumption

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KSZ8794CNX

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1.0 INTRODUCTION

1.1 General Description

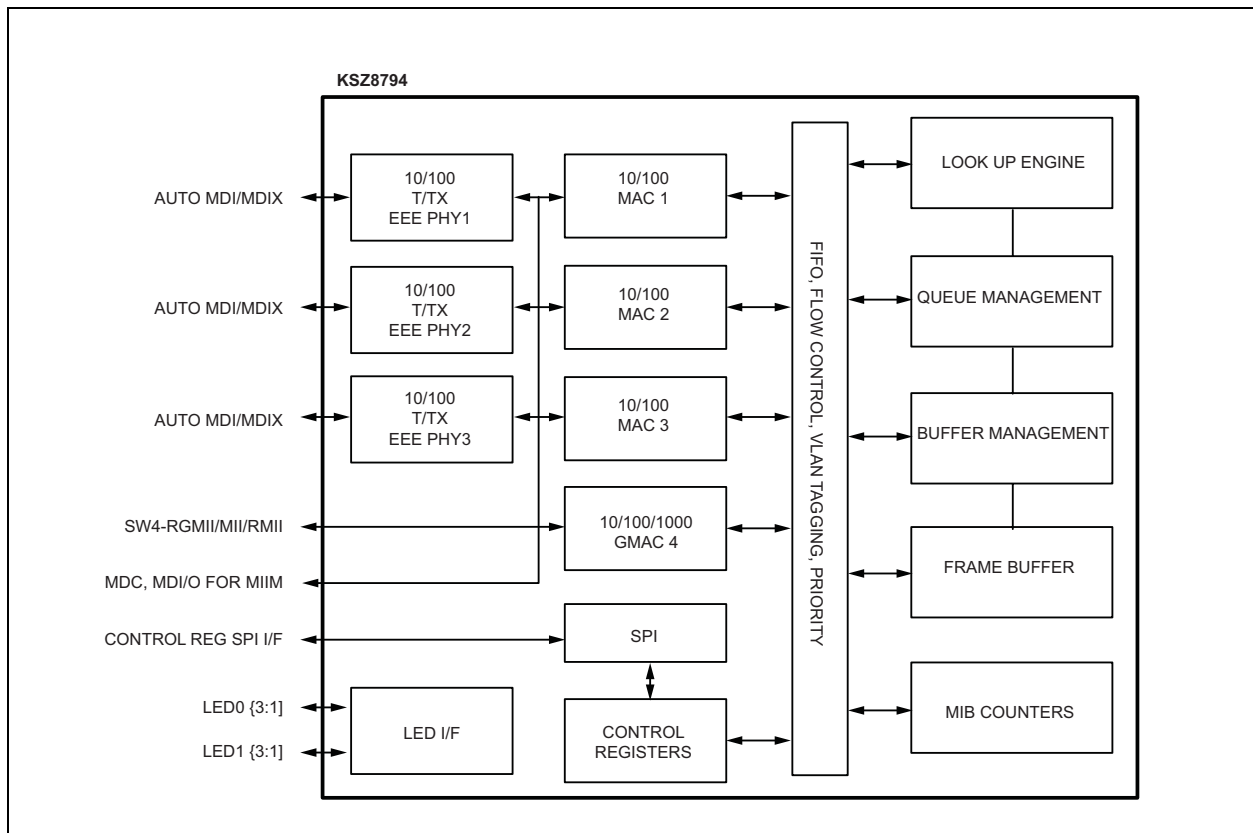
The KSZ8794CNX is a highly integrated, Layer 2-managed, four-port switch with numerous features designed to reduce system cost. It is intended for cost-sensitive applications requiring three 10/100 Mbps copper ports and one 10/100/1000 Mbps Gigabit uplink port. The KSZ8794CNX incorporates a small package outline, lowest power consumption with internal biasing, and on-chip termination. Its extensive features set includes enhanced power management, programmable rate limiting and priority ratio, tagged and port-based VLAN, port-based security and ACL rule-based packet filtering technology, QoS priority with four queues, management interfaces, enhanced MIB counters, high-performance memory bandwidth, and a shared memory-based switch fabric with non-blocking support. The KSZ8794CNX provides support for multiple CPU data interfaces to effectively address both current and emerging fast Ethernet and Gigabit Ethernet applications where the GMAC interface can be configured to any of RGMII, MII, and RMII modes. The KSZ8794CNX is built on the latest industry-leading Ethernet analog and digital technology, with features designed to offload host processing and streamline the overall design:

- Three integrated 10/100BASE-T/TX MAC/PHYs.
- One integrated 10/100/1000BASE-T/TX GMAC with selectable RGMII, MII, or RMII interfaces.
- Small 64-pin QFN package.

A robust assortment of power management features including Energy Efficient Ethernet (EEE), PME, and WoL have been designed in to satisfy energy efficient environments.

All registers in the MAC and PHY units can be managed through the SPI interface. MIIM PHY registers can be accessed through the MDC/MDIO interface.

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



KSZ8794CNX

2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 64-QFN PIN ASSIGNMENT (TOP VIEW)

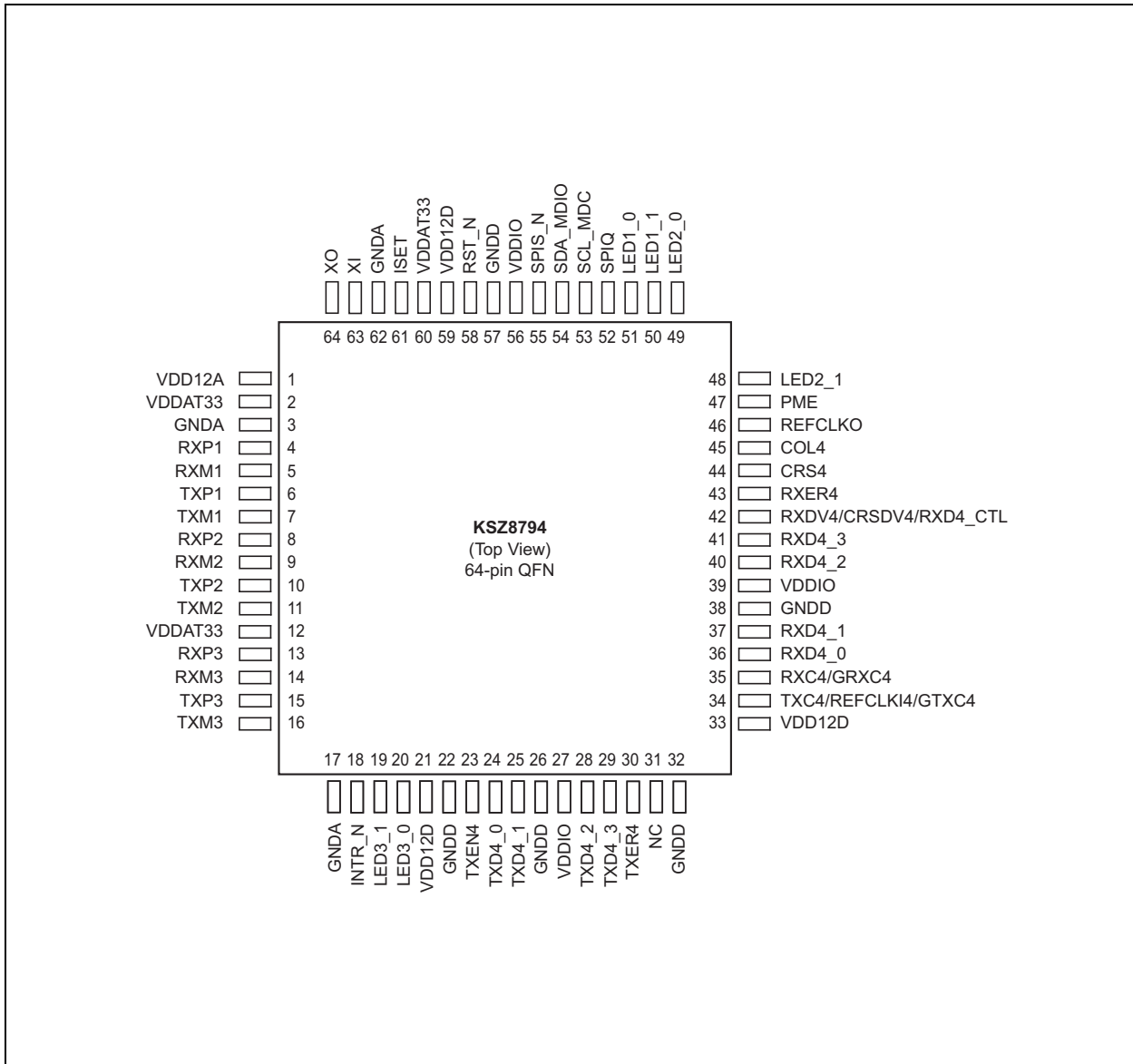


TABLE 2-1: SIGNALS - KSZ8794CNX

Pin Number	Pin Name	Type Note 2-1	Port	Description
1	VDD12A	P	—	1.2V Core Power
2	VDDAT	P	—	3.3V or 2.5V Analog Power.
3	GNDA	GND	—	Analog Ground.
4	RXP1	I	1	Port 1 Physical Receive Signal + (Differential).
5	RXM1	I	1	Port 1 Physical Receive Signal - (Differential).
6	TXP1	O	1	Port 1 Physical Transmit Signal + (Differential).
7	TXM1	O	1	Port 1 Physical Transmit Signal - (Differential).
8	RXP2	I	2	Port 2 Physical Receive Signal + (Differential).
9	RXM2	I	2	Port 2 Physical Receive Signal - (Differential).
10	TXP2	O	2	Port 2 Physical Transmit Signal + (Differential).
11	TXM2	O	2	Port 2 Physical Transmit Signal - (Differential).
12	VDDAT	P	—	3.3V or 2.5V Analog Power.
13	RXP3	I	3	Port 3 Physical Receive Signal + (Differential).
14	RXM3	I	3	Port 3 Physical Receive Signal - (Differential).
15	TXP3	O	3	Port 3 Physical Transmit Signal + (Differential).
16	TXM3	O	3	Port 3 Physical Transmit Signal – (Differential).
17	GNDA	GND	—	Analog Ground.
18	INTR_N	Opu	—	Interrupt: Active-Low This pin is an open-drain output pin. Note: an external pull-up resistor is needed on this pin when it is in use.
19	LED3_1	Ipu/O	3	Port 3 LED Indicator 1: See Global Register 11 bits [5:4] for details. Strap Option: Switch Port 4 GMAC4 interface mode select by LED3[1:0] 00 = MII for SW4-MII 01 = RMII for SW4-RMII 10 = Reserved 11 = RGMII for SW4-RGMII (Default)
20	LED3_0	Ipu/O	3	Port 3 LED Indicator 0: See Global Register 11 bits [5:4] for details. Strap Option: See LED3_1.
21	VDD12D	P	—	1.2V Core Power.
22	GNDD	GND	—	Digital Ground.
23	TXEN4/ TXD4_CTL	Ipd	4	MII/RMII: Port 4 Switch transmit enable. RGMII: Transmit data control.
24	TXD4_0	Ipd	4	RGMII/MII/RMII: Port 4 Switch transmit bit [0].

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TABLE 2-1: SIGNALS - KSZ8794CNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Port	Description
25	TXD4_1	lpd	4	RGMI/II/MII/RMII: Port 4 Switch transmit bit [1].
26	GNDD	GND	—	Digital Ground.
27	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V _{DD} for digital I/O circuitry.
28	TXD4_2	lpd	4	RGMI/II/MII: Port 4 Switch transmit bit [2]. RMII: No connection.
29	TXD4_3	lpd	4	RGMI/II/MII: Port 4 Switch transmit bit [3]. RMII: No connection.
30	TXER4	lpd	4	MII: Port 4 Switch transmit error. RGMI/II/RMII: No connection.
31	NC	NC	—	No Connect.
32	GNDD	GND	—	Digital Ground.
33	VDD12D	P	—	1.2V Core Power.
34	TXC4/ REFCLKI4 /GTXC4	I/O	4	Port 4 Switch GMAC4 Clock Pin MII: 2.5/25 MHz clock, PHY mode is output, MAC mode is input. RMII: Input for receiving 50 MHz clock in normal mode RGMII: Input 125 MHz clock with falling and rising edge to latch data for the transmit.
35	RXC4/ GRXC4	I/O	4	Port 4 Switch GMAC4 Clock Pin MII: 2.5/25 MHz clock, PHY mode is output, MAC mode is input. RMII: Output 50 MHz reference clock for the receiving/transmit in the clock mode. RGMII: Output 125 MHz clock with falling and rising edge to latch data for the receiving.
36	RXD4_0	lpd/O	4	RGMI/II/MII/RMII: Port 4 Switch receive bit [0].
37	RXD4_1	lpd/O	4	RGMI/II/MII/RMII: Port 4 Switch receive bit [1].
38	GNDD	GND	—	Digital Ground.
39	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V _{DD} for digital I/O circuitry.
40	RXD4_2	lpd/O	4	RGMI/II/MII: Port 4 Switch receive bit [2]. RMII: No connection.
41	RXD4_3	lpd/O	4	RGMI/II/MII: Port 4 Switch receive bit [3]. RMII: No connection.
42	RXDV4/ CRSDV4 /RXD4_CTL	lpd/O	4	MII: RXDV4 is for Port 4 Switch GMII/MII receive data valid. RMII: CRSDV4 is for Port 4 RMII carrier sense/receive data valid output. RGMII: RXD4_CTL is for Port 4 RGMII receive data control
43	RXER	lpd/O	4	MII: Port 4 Switch receives error. RGMI/II/RMII: No connection.
44	CRS4	lpd/O	4	MII: Port 4 Switch MII modes carrier sense. RGMII/RMII: No connection.

TABLE 2-1: SIGNALS - KSZ8794CNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Port	Description
45	COL4	lpd/O	4	MII: Port 4 Switch MII collision detects. RGMII/RMII: No connection.
46	REFCLKO	lpu/O	—	25 MHz Clock Output (Option) Controlled by the strap pin LED2_0. Default is enabled, it is better to disable it if it's not being used.
47	PME_N	I/O	—	Power Management Event This output signal indicates that a Wake On LAN event has been detected as a result of a Wake-Up frame being detected. The KSZ8794CNX is requesting the system to wake up from low power mode. Its assertion polarity is programmable with the default polarity to be active low.
48	LED2_1	lpu/O	2	Port 2 LED Indicator 1 See Global Register 11 bits [5:4] for details. Strap Option: Port 4 MII and RMII Modes Select When Port 4 is MII mode: PU = MAC mode. PD = PHY mode. When Port 4 is RMII mode: PU = Clock mode in RMII, using 25 MHz OSC clock and provide 50 MHz RMII clock from pin RXC4. PD = Normal mode in RMII, the TXC4/REFCLKI4 pin on the Port 4 RMII will receive an external 50 MHz clock. Note: Port 4 also can use either an internal or external clock in RMII mode based on this strap pin or the setting of the Register 86 (0x56) bit [7].
49	LED2_0	lpu/O	2	Port 2 LED Indicator 0 See Global Register 11 bits [5:4] for details. Strap Option: REFCLKO Enable PU = REFCLK_O (25 MHz) is enabled. (Default) PD = REFCLK_O is disabled Note: It is better to disable this 25 MHz clock if not providing an extra 25 MHz clock for system.
50	LED1_1	lpu/O	1	Port 1 LED Indicator 1. See Global Register 11 bits [5:4] for details. Strap Option: PLL Clock Source Select PU = Still use 25 MHz clock from XI/XO pin even though it is in Port 4 RMII normal mode. PD = Use external clock from TXC4 in Port 4 RMII normal mode. Note: If received clock in Port 4 RMII normal mode has bigger clock jitter, one can still select the 25 MHz Crystal/Oscillator as switch's clock source.
51	LED1_0	lpu/O	1	Port 1 LED Indicator 0 See Global Register 11 bits [5:4] for details. Strap Option: Speed Select in RGMII PU = 1 Gbps in RGMII. (Default) PD = 10/100 Mbps in RGMII. Note: Programmable through internal registers also.

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TABLE 2-1: SIGNALS - KSZ8794CNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Port	Description
52	SPIQ	lpd/O	All	SPI Serial Data Output in SPI Slave Mode Strap Option: Serial Bus Configuration PD = SPI slave mode. PU = MDC/MDIO mode. Note: An external pull-up or pull-down resistor is required.
53	SCL_MDC	lpu	All	Clock for SPI or MDC/MDIO Interfaces Input clock up to 50 MHz in SPI slave mode. Input clock up to 25 MHz in MDC/MDIO for MIIM access.
54	SDA_MDIO	lpu/O	All	Data Line for SPI or MDC/MDIO Interfaces Serial data input in SPI slave mode. MDC/MDIO interface input/output data line.
55	SPIS_N	lpu	All	SPI Interface Chip Select When SPIS_N is high, the KSZ8794CNX is deselected and SPIQ is held in the high impedance state. A high-to-low transition initiates the SPI data transfer. This pin is active-low.
56	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V _{DD} for digital I/O circuitry.
57	GNDD	GND	—	Digital Ground.
58	RST_N	lpu	—	Reset This active-low signal resets the hardware in the device. See the timing requirements in the Timing Diagram Section.
59	VDD12D	P	—	1.2V Core Power.
60	VDDAT	P	—	3.3V or 2.5V Analog Power.
61	ISET	—	—	Transmit Output Current Set This pin configures the physical transmit output current. It should be connected to GND through a 12.4 kΩ 1% resistor.
62	GNDA	GND	—	Analog Ground.
63	XI	I	—	Crystal Clock Input/Oscillator Input When using a 25 MHz crystal, this input is connected to one end of the crystal circuit. When using a 3.3V oscillator, this is the input from the oscillator. The crystal or oscillator should have a tolerance of ±50 ppm.
64	XO	O	—	Crystal Clock Output. When using a 25 MHz crystal, this output is connected to one end of the crystal circuit.

Note 2-1 P = power supply; GND = ground; I = input; O = output
I/O = bi-directional
lpu = Input w/internal pull-up.
lpd = Input w/internal pull-down.
lpd/O = Input w/internal pull-down during reset, output pin otherwise.
lpu/O = Input w/internal pull-up during reset, output pin otherwise.
OTRI = Output tri-stated.
PU = Strap pin pull-up.
PD = Strap pin pull-down.
NC = No connect or tie-to-ground for this product.

The KSZ8794CNX can function as a managed switch and utilizes strap-in pins to configure the device for different modes. The strap-in pins are configured by using external pull-up/down resistors to create a high or low state on the pins which are sampled during the power-down reset or warm reset. The functions are described in following table.

TABLE 2-2: STRAP-IN OPTIONS - KSZ8794CNX

Pin Number	Pin Name	Type (Note 2-2)	Description
19, 20	LED3[1,0]	Ipu/O	Switch Port 4 GMAC4 Interface Mode Select Strap Option: 00 = MII for SW4-MII 01 = RMII for SW4-RMII 10 = Reserved 11 = RGMII for SW4-RGMII (Default)
48	LED2_1	Ipu/O	Port 4 MII and RMII Modes Select Strap Option: When Port 4 is MII mode: PU = MAC mode. PD = PHY mode. When Port 4 is RMII mode: PU = Clock mode in RMII, using 25 MHz OSC clock and provide 50 MHz RMII clock from pin RXC4. PD = Normal mode in RMII, the TXC4/REFCLKI4 pin on the Port 4 RMII will receive an external 50 MHz clock Note: Port 4 also can use either an internal or external clock in RMII mode based on this strap pin or the setting of the Register 86 (0x56) bit [7].
49	LED2_0	Ipu/O	REFCLKO Enable Strap Option: PU = REFCLK_O (25 MHz) is enabled. (Default) PD = REFCLK_O is disabled
50	LED1_1	Ipu/O	PLL Clock Source Select Strap Option: PU = Still use 25 MHz clock from XI/XO pin even though it is in Port 4 RMII normal mode. PD = Use external clock from TXC4 in Port 4 RMII normal mode. Note: If received clock in Port 4 RMII normal mode has bigger clock jitter, one can still select the 25 MHz Crystal/Oscillator as switch's clock source.
51	LED1_0	Ipu/O	Port 4 Gigabit Select Strap Option: PU = 1 Gbps in RGMII. (Default) PD = 10/100 Mbps in RGMII. Note: Also programmable through internal register.
52	SPIQ	Ipd/O	Serial Bus Configuration Strap Option: PD = SPI slave mode. (Default) PU = MDC/MDIO mode. Note: An external pull-up or pull-down resistor is required. If the uplink port is used for RGMII interface, recommend using SPI mode to have opportunity setting the register 86 (0x56) bits [4:3] for RGMII v2.0. MDC/MDIO mode can't set this feature.

Note 2-2 Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
Ipu/O = Input w/internal pull-up during reset, output pin otherwise.

KSZ8794CNX

3.0 FUNCTIONAL DESCRIPTION

The KSZ8794CNX contains three 10/100 physical layer transceivers, three media access control (MAC) units, and one Gigabit media access control (GMAC) units with an integrated Layer 2-managed switch. The device runs in two modes. The first mode is as a three-port stand-alone switch. The second is as four-port switch with a fourth port that is provided through a Gigabit media independent interface that supports RGMII, MII, and RMII. This is useful for implementing an integrated broadband router.

The KSZ8794CNX has the flexibility to reside in a managed mode. In a managed mode, a host processor has complete control of the KSZ8794CNX via the SPI bus or the MDC/MDIO interface.

On the media side, the KSZ8794CNX supports IEEE 802.3 10BASE-T, 100BASE-TX on all copper ports with Auto-MDI/MDIX. The KSZ8794CNX can be used as a fully managed four-port switch or hooked up to a microprocessor via its RGMII/MII/RMII interfaces to allow for integration into a variety of environments.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry and DSP technology that makes the design more efficient and allows for reduced power consumption and smaller die size.

Major enhancements from the KSZ8864RMN to the KSZ8794CNX include high speed host interface options such as the RGMII interfaces, power saving features such as IEEE 802.1az Energy Efficient Ethernet (EEE), MLD snooping, Wake On LAN (WoL), port-based ACL filtering and port security, programmable QoS priority, and flexible rate limiting.

3.1 Physical Layer (PHY)

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 12.4 k Ω resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, descrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the descrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.1.3 PLL CLOCK SYNTHESIZER

The KSZ8794CNX generates 125 MHz, 83 MHz, 41 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator.

3.1.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then descramble the incoming data stream with the same sequence at the transmitter.

3.1.5 10BASE-T TRANSMIT

The 10BASE-T output driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

3.1.6 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into a clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8794CNX decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.7 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8794CNX supports HP Auto-MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. Note that HP Auto-MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8794CNX device. This feature is extremely useful when end users are unaware of cable types, and also saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers, or MIIM PHY registers. The IEEE 802.3u standard MDI and MDI-X definitions are illustrated in [Table 3-1](#).

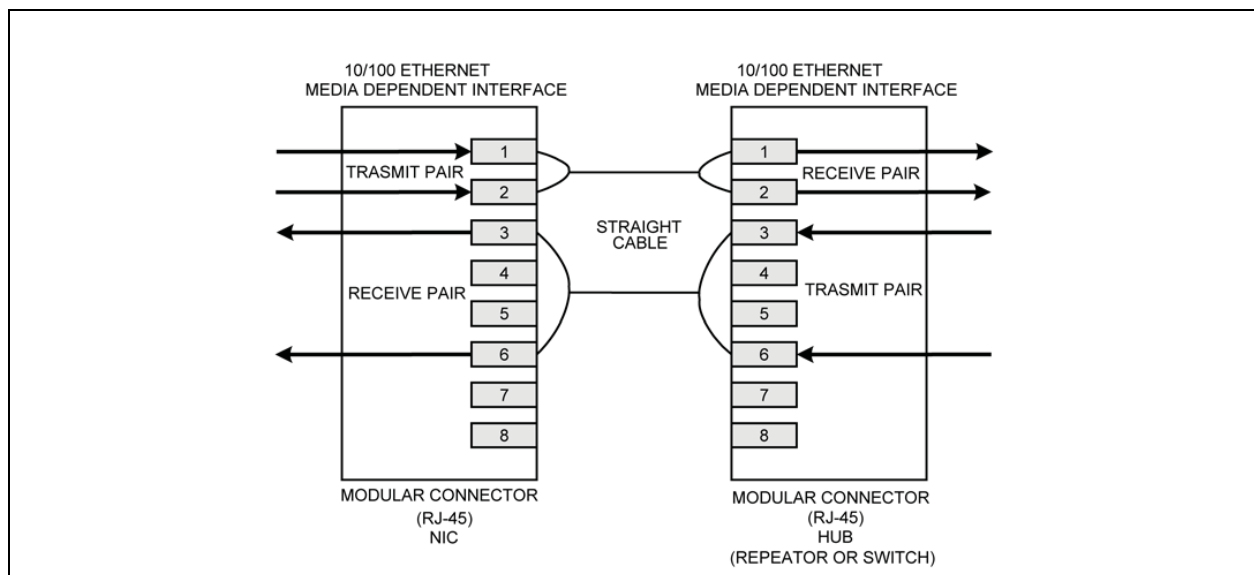
TABLE 3-1: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	Signals	RJ-45 Pins	Signals
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

3.1.7.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. [Figure 3-1](#) depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION

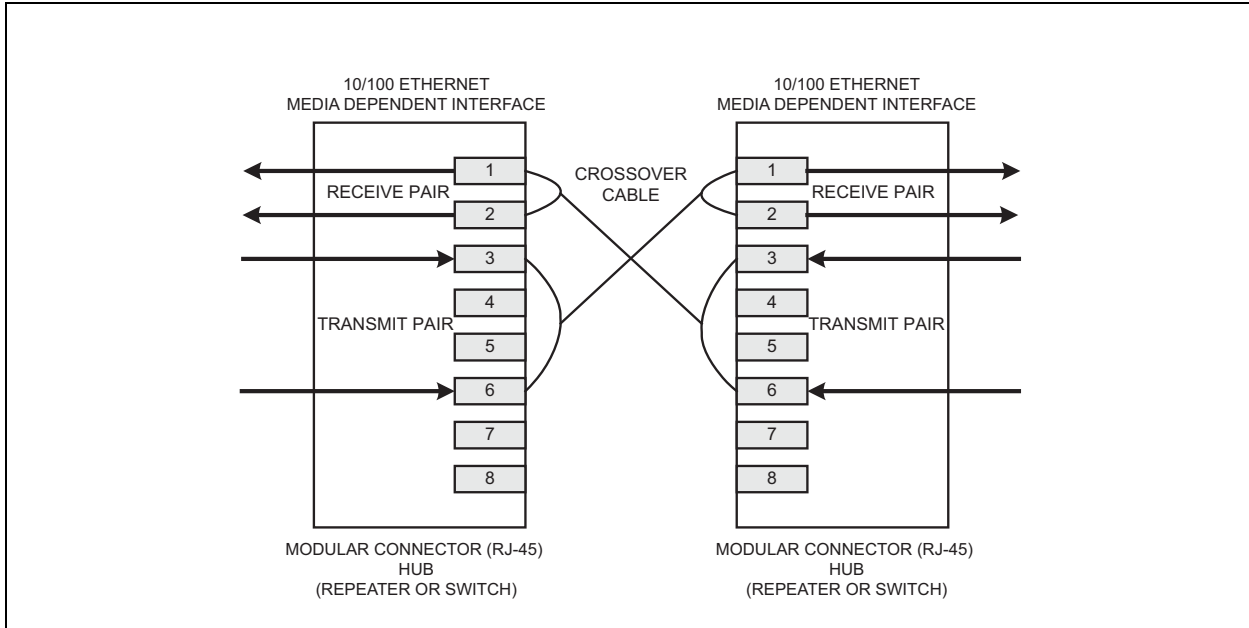


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3.1.7.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



3.1.8 AUTO-NEGOTIATION

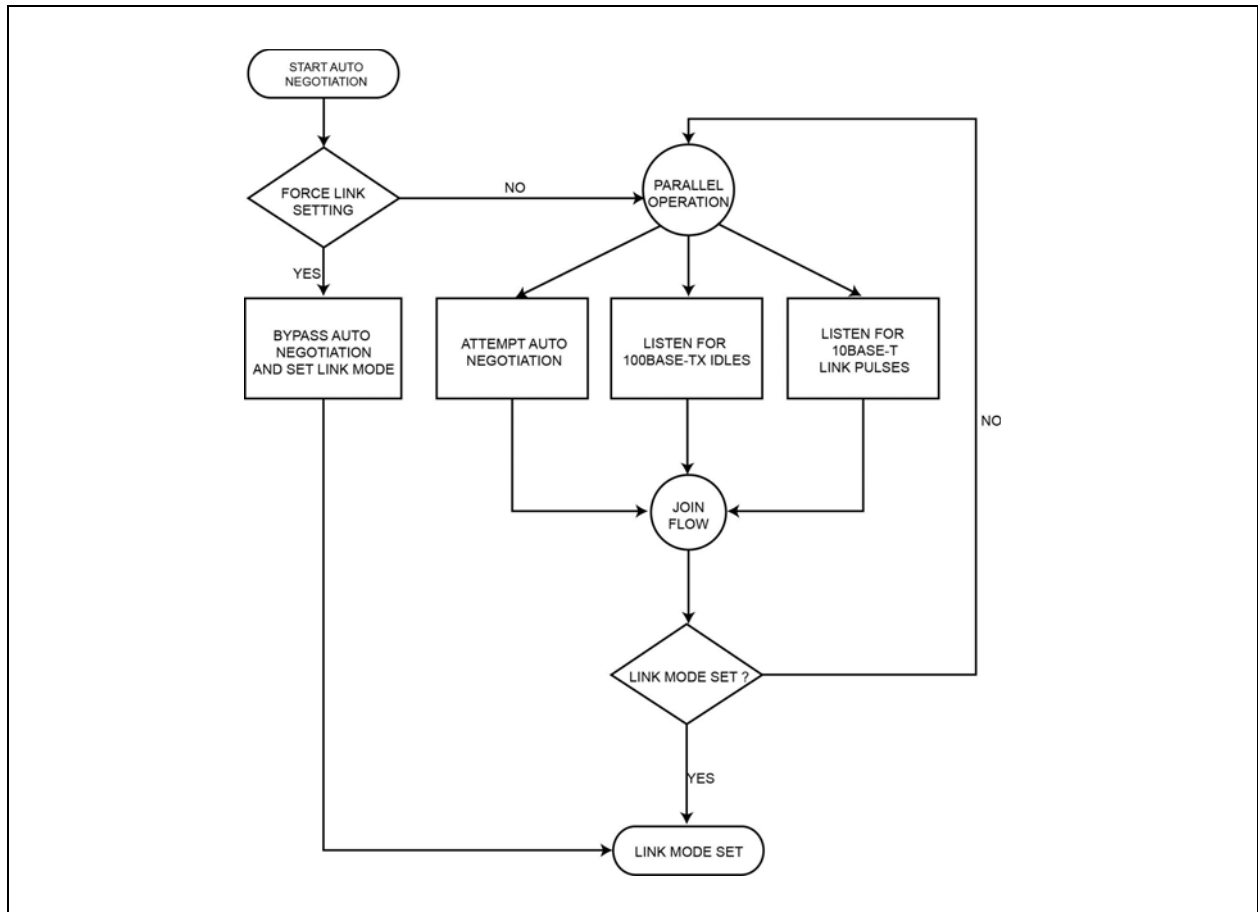
The KSZ8794CnX conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode-of-operation. Link partners advertise their capabilities to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode-of-operation. Auto-negotiation is supported for the copper ports only.

The following list shows the speed and duplex operation mode (highest to lowest):

- 100BASE-TX, full-duplex
- 100BASE-TX, half-duplex
- 10BASE-T, full-duplex
- 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ8794CNX link partner is forced to bypass auto-negotiation, the KSZ8794CNX sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8794CNX to establish link by listening for a fixed-signal protocol in the absence of auto-negotiation advertisement protocol. The auto-negotiation link up process is shown in [Figure 3-3](#).

FIGURE 3-3: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.1.9 LINKMD® CABLE DIAGNOSTICS

The LinkMD feature utilizes time-domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with maximum distance of 200m and accuracy of $\pm 2\text{m}$. Internal circuitry displays the TDR information in a user-readable digital format.

Note: Cable diagnostics are only valid for copper connections only.

3.1.9.1 Access

LinkMD is initiated by accessing the PHY special control/status Registers {26, 42, 58} and the LinkMD result Registers {27, 43, 59} for Ports 1, 2, and 3 respectively; and in conjunction with the Port Control 10 Register for Ports 1, 2, and 3 respectively to disable Auto-MDI/MDI-X.

Alternatively, the MIIM PHY Registers 0 and 1d can also be used for LinkMD access.

3.1.9.2 Usage

The following is a sample procedure for using LinkMD with Registers {26, 27, and 29} on Port 1:

1. Disable auto MDI/MDI-X by writing a '1' to Register 29, Bit[2] to enable manual control over the differential pair used to transmit the LinkMD pulse.
2. Start cable diagnostic test by writing a '1' to Register 26, Bit[4]. This enable bit is self-clearing.
3. Wait (poll) for Register 26, Bit[4] to return a '0', and indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in Register 26, bits [6:5]. The results are as follows:

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- 00 = normal condition (valid test)
- 01 = open condition detected in cable (valid test)
- 10 = short condition detected in cable (valid test)
- 11 = cable diagnostic test failed (invalid test)

The '11' case, invalid test, occurs when the KSZ8794CNX is unable to shut down the link partner. In this instance, the test is not run because it would be impossible for the KSZ8794CNX to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating Register 26, bit[0] and Register 27, bits [7:0]; and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

$$D \text{ (distance to cable fault, expressed in meters)} = 0.4 \times (\text{Register 26, Bit[0], Register 27, bits [7:0]})$$

Concatenated value of Registers 26 Bit[0] and 27 bits [7:0] should be converted to decimal before multiplying by 0.4.

The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

For Ports 2, 3, and for using the MIIM PHY registers, LinkMD usage is similar.

3.1.9.3 A LinkMD Example

The following is a sample procedure for using LinkMD on Ports 1, 2, and 3 with force MDI-X mode:

```
//Disable MDI/MDI-X and force to MDI-X mode
//'w' is WRITE the register. 'r' is READ register below
w 1d 04
w 2d 04
w 3d 04
//Set Internal registers temporary by indirect registers, adjust for LinkMD
w 6e a0
w 6f 4d
w a0 08
//Enable LinkMD Testing with fault cable port 1, port 2 and port 3 by Port Register Control 8 bit [4]
w 1a 10
w 2a 10
w 3a 10
//Wait until Port Register Control 8 Bit[4] returns a '0' (Self Clear)
//Diagnosis results
r 1a
r 1b
r 2a
r 2b
r 3a
r 3b
//For example on Port 1, the result analysis based on the values of the register 0x1a and 0x1b
//The register 0x1a Bits[6-5] are for the open or the short detection.
//The register 0x1a Bit[0] + the register 0x1b bits [7-0] = CDT_Fault_Count [8-0]
//The distance to fault is about 0.4 x (CDT_Fault_Count [8-0])
```

3.1.10 ON-CHIP TERMINATION AND INTERNAL BIASING

The KSZ8794CNX reduces the board cost and simplifies the board layout by using on-chip termination resistors for all ports and RX/TX differential pairs without the external termination resistors. The combination of the on-chip termination and the internal biasing will save more PCB spacing and power consumption, compared using external biasing and termination resistors for multiple ports' switches, because the transformers don't consume the power anymore. The center taps of the transformer shouldn't need to be tied to the analog power.

3.2 Media Access Controller (MAC) Operation

The KSZ8794CNX strictly abides by IEEE 802.3 standards to maximize compatibility.

3.2.1 INTER-PACKET GAP (IPG)

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

3.2.2 BACKOFF ALGORITHM

The KSZ8794CNX implements the IEEE Standard 802.3 binary exponential backoff algorithm, and optional "aggressive mode" backoff. After 16 collisions, the packet will be optionally dropped, depending on the chip configuration in Register 3.

3.2.3 LATE COLLISION

If a transmit packet experiences collisions after 512-bit times of the transmission, the packet will be dropped.

3.2.4 ILLEGAL FRAMES

The KSZ8794CNX discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Register 4. For special applications, the KSZ8794CNX can also be programmed to accept frames up to 2K bytes in Register 3 Bit[6]. Because the KSZ8794CNX supports VLAN tags, the maximum sizing is adjusted when these tags are present.

3.2.5 FLOW CONTROL

The KSZ8794CNX supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8794CNX receives a pause control frame, the KSZ8794CNX will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow-control packets from the KSZ8794CNX will be transmitted.

On the transmit side, the KSZ8794CNX has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8794CNX flow controls a port that has just received a packet if the destination port resource is busy. The KSZ8794CNX issues a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8794CNX sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is also provided to prevent over-activation and deactivation of the flow control mechanism.

The KSZ8794CNX flow controls all ports if the receive queue becomes full.

3.2.6 HALF-DUPLEX BACK PRESSURE

The KSZ8794CNX also provides a half-duplex back pressure option (note that this is not in IEEE 802.3 standards). The activation and deactivation conditions are the same as the ones given for full-duplex mode. If back pressure is required, the KSZ8794CNX sends preambles to defer the other station's transmission (carrier sense deference). To avoid jabber and excessive deference as defined in IEEE 802.3 standards, after a certain period of time, the KSZ8794CNX discontinues carrier sense but raises it quickly after it drops packets to inhibit other transmissions. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in a carrier sense-deferred state. If the port has packets to send during a back pressure situation, the carrier sense-type back pressure is interrupted and those packets are transmitted instead. If there are no more packets to send, carrier sense-type back pressure becomes active again until switch resources are free. If a collision occurs, the binary exponential backoff algorithm is

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skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets. To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive backoff (Register 3, Bit[0])
- No excessive collision drop (Register 4, Bit[3])
- Back pressure (Register 4, Bit[5])

These bits are not set as the default because this is not the IEEE standard.

3.2.7 BROADCAST STORM PROTECTION

The KSZ8794CNX has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets are normally forwarded to all ports except the source port and thus use too many switch resources (bandwidth and available space in transmit queues). The KSZ8794CNX has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally and can be enabled or disabled on a per port basis. The rate is based on a 50 ms (0.05s) interval for 100BT and a 500 ms (0.5s) interval for 10BT. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Registers 6 and 7. The default setting for Registers 6 and 7 is 0x4A (74 decimal). This is equal to a rate of 1%, calculated as follows:

$148.80 \text{ frames/sec} \times 50 \text{ ms (0.05s)/interval} \times 1\% = 74 \text{ frames/interval (approx.)} = 0x4A$

3.3 Switch Core

3.3.1 ADDRESS LOOK-UP

The internal look-up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KSZ8794CNX is guaranteed to learn 1K addresses and distinguishes itself from a hash-based look-up table, which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.3.2 LEARNING

The internal look-up engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted first to make room for the new entry.

3.3.3 MIGRATION

The internal look-up engine also monitors whether a station is moved. If this occurs, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

3.3.4 AGING

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300s ($\pm 75s$). This feature can be enabled or disabled through Register 3 Bit[2].

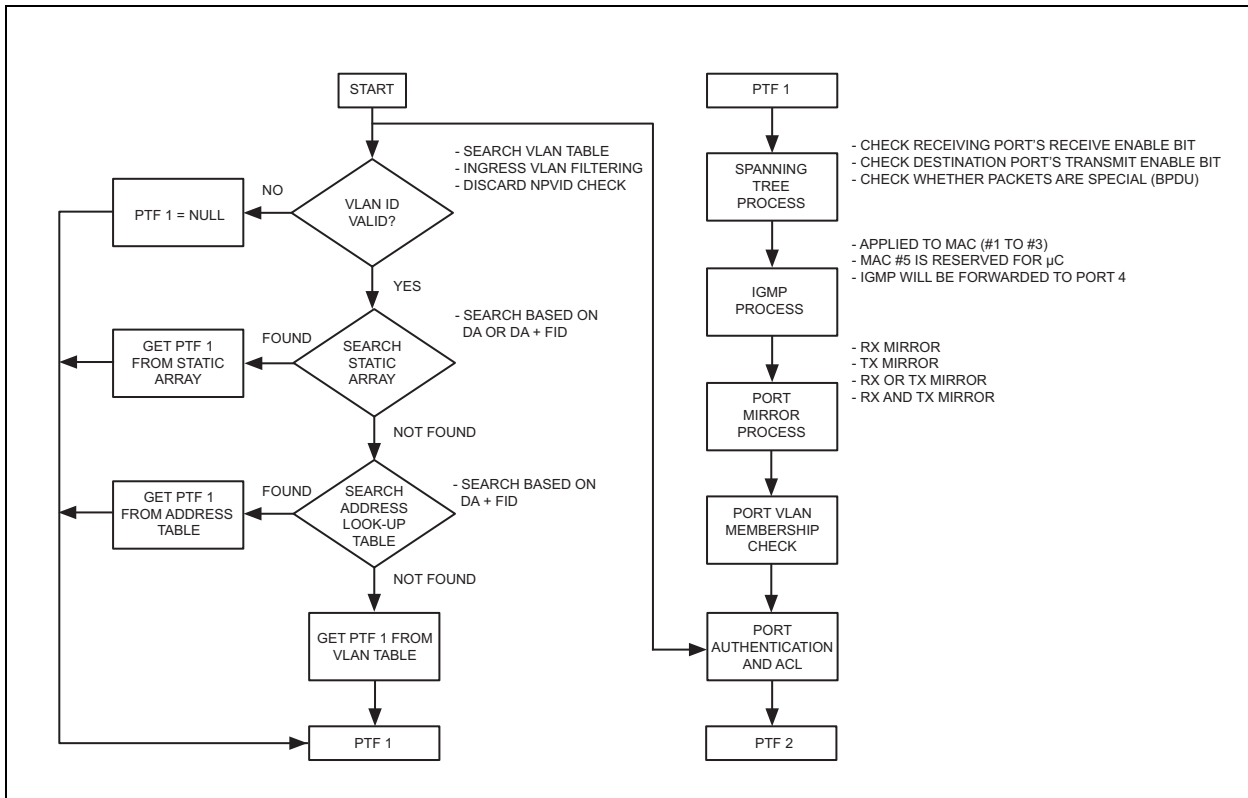
3.3.5 FORWARDING

The KSZ8794CNX will forward packets using an algorithm that is depicted in the following flowcharts. [Figure 3-4](#) shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by the spanning tree, IGMP snooping, port mirroring, and port VLAN processes and authentication to come up with “port to forward 2” (PTF2), as shown in [Figure 3-4](#). The authentication and ACL have highest priority in the forwarding process; ACL result will overwrite the result of the forwarding process. This is where the packet will be sent.

The KSZ8794CNX will not forward the following packets:

- Error packets. These include framing errors, frame check sequence (FCS) errors, alignment errors, and illegal size packet errors.
- IEEE802.3x PAUSE frames. KSZ8794CNX intercepts these packets and performs full-duplex flow control accordingly.
- "Local" packets. Based on destination address (DA) lookup, if the destination port from the lookup table matches the port from which the packet originated, the packet is defined as "local."

FIGURE 3-4: DESTINATION ADDRESS LOOKUP AND RESOLUTION FLOW CHART



3.3.6 SWITCHING ENGINE

The KSZ8794CNX features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency. The KSZ8794CNX has a 64 kB internal frame buffer. This resource is shared between all five ports. There are a total of 512 buffers available. Each buffer is sized at 128 bytes.

3.4 Power and Power Management

The KSZ8794CNX device requires 3.3V analog power. An external 1.2V LDO provides the necessary 1.2V to power the analog and digital logic cores. The various I/Os can be operated at 1.8V, 2.5V, and 3.3V. Table 3-2 illustrates the various voltage options and requirements of the device.

TABLE 3-2: KSZ8794CNX VOLTAGE OPTIONS AND REQUIREMENTS

Power Signal Name	Device Pin	Requirement
VDDAT	2, 12, 60	3.3V or 2.5V input power to the analog blocks of transceiver in the device.
VDDIO	27, 39, 56	Choice of 1.8V or 2.5V or 3.3V for the I/O circuits. These input power pins power the I/O circuitry of the device.

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TABLE 3-2: KSZ8794CNX VOLTAGE OPTIONS AND REQUIREMENTS (CONTINUED)

Power Signal Name	Device Pin	Requirement
VDD12A	1	1.2V core power. Filtered 1.2V input voltage. These pins feed 1.2V to power the internal analog and digital cores.
VDD12D	21, 33, 59	
GNDA	3, 17, 62	Analog ground.
GNDD	22, 26, 32, 38, 57	Digital ground.

The KSZ8794CNX supports enhanced power management in a low power state, with energy detection to ensure low power dissipation during device idle periods. There are multiple operation modes under the power management function which are controlled by the Register 14 Bits[4:3] and the Port Control 10 Register Bit[3] as:

- Register 14 Bits[4:3] = 00 Normal Operation Mode
- Register 14 Bits[4:3] = 01 Energy Detect Mode
- Register 14 Bits[4:3] = 10 Soft Power-Down Mode
- Register 14 Bits[4:3] = 11 Reserved

The Port Control 10 Register 29, 45, 61 Bit[3] = 1 are for the port-based power-down mode. [Table 3-3](#) indicates all internal function blocks' status under four different power management operation modes.

TABLE 3-3: INTERNAL FUNCTION BLOCK STATUS

KSZ8794CNX Function Blocks	Power Management Operation Modes		
	Normal Mode	Energy Detect Mode	Soft Power-Down Mode
Internal PLL Clock	Enabled	Disabled	Disabled
TX/RX PHY	Enabled	Energy Detect at RX	Disabled
MAC	Enabled	Disabled	Disabled
Host Interface	Enabled	Disabled	Disabled

3.4.1 NORMAL OPERATION MODE

This is the default setting Bits[4:3] = 00 in Register 14 after chip power-up or hardware reset. When KSZ8794CNX is in normal operation mode, all PLL clocks are running, PHY and MAC are on, and the host interface is ready for CPU read or writes.

During normal operation mode, the host CPU can set the Bits [4:3] in Register 14 to change the current normal operation mode to any one of the other three power management operation modes.

3.4.2 ENERGY DETECT MODE

Energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8794CNX port is not connected to an active link partner. In this mode, the device will save more power when the cables are unplugged. If the cable is not plugged in, the device can automatically enter a low power state: the energy detect mode. In this mode, the device will keep transmitting 120 ns width pulses at a rate of 1 pulse per second. Once activity resumes due to plugging a cable in or attempting by the far end to establish link, the device can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low-power state. While in low power state, the device reduces power consumption by disabling all circuitry except the energy-detect circuitry of the receiver. The energy detect mode is entered by setting bits [4:3] = 01 in Register 14. When the KSZ8794CNX is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than the pre-configured value at bits [7:0] Go-Sleep time in Register 15, KSZ8794CNX will go into low power state. When KSZ8794CNX is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable, the device will enter normal power state. When the device is at normal power state, it is able to transmit or receive packet from the cable.

3.4.3 SOFT POWER-DOWN MODE

The soft power-down mode is entered by setting bits [4:3] = 10 in Register 14. When KSZ8794CNX is in this mode, all PLL clocks are disabled, also all of PHYs and the MACs are off. Any dummy host access will wake-up this device from current soft power-down mode to normal operation mode and internal reset will be issued to make all internal registers go to the default values.

3.4.4 PORT-BASED POWER-DOWN MODE

In addition, the KSZ8794CNX features a per-port power down mode. To save power, a PHY port that is not in use can be powered down via the Port Control 10 Register Bit[3], or MIIM PHY Register 0 Bit[11].

3.4.5 ENERGY EFFICIENT ETHERNET (EEE)

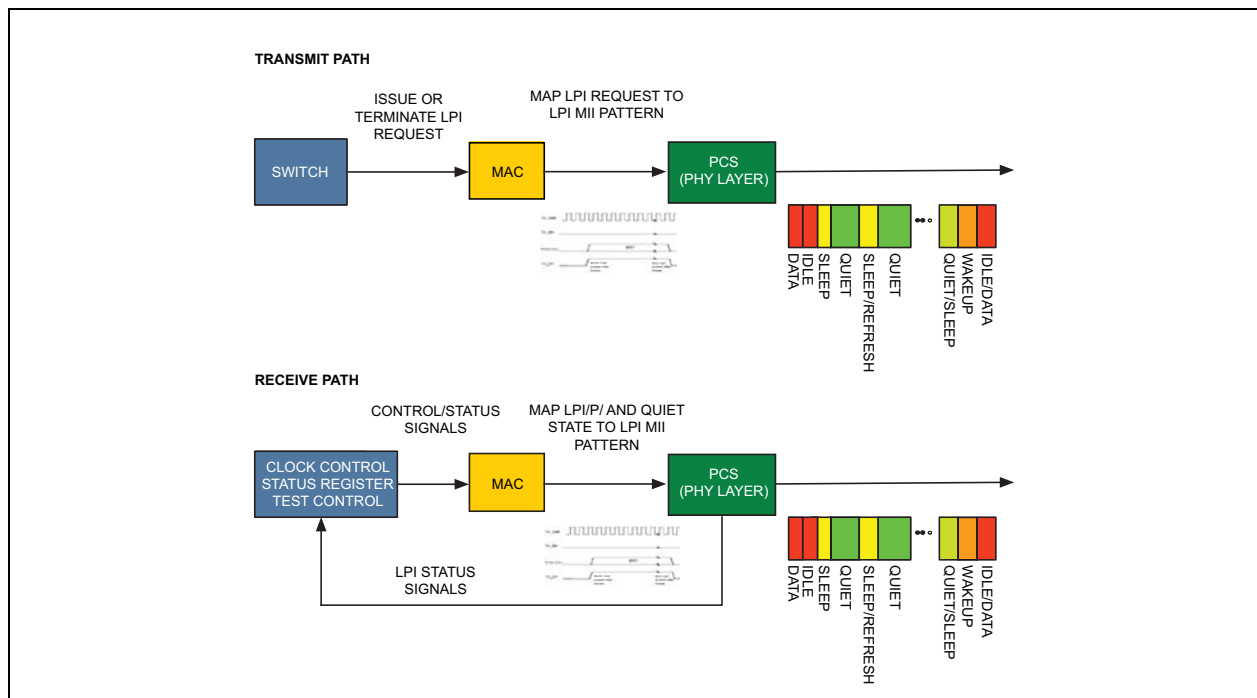
Along with supporting different types of power saving modes (H/W power down, S/W power down, and energy detect mode), the KSZ8794CNX extends the green function capability by supporting Energy Efficient Ethernet (EEE) features defined in IEEE P802.3az, March 2010. Both 10BASE-T and 100BASE-TX EEE functions are supported in KSZ8794CNX. In 100BASE-TX the EEE operation is asymmetric on the same link, which means one direction could be at low-power idle (LPI) state, in the meanwhile, another direction could exist packet transfer activity. Different from other type of power saving mode, EEE is able to maintain the link while power saving is achieved. Based on EEE specification, the energy saving from EEE is done at PHY level. KSZ8794CNX reduces the power consumption not only at PHY level but also at MAC and switch level by shutting down the unused clocks as much as possible when the device is at low-power idle phase.

The KSZ8794CNX supports the 802.3az IEEE standard for both 10 Mbps and 100 Mbps interfaces. The EEE capability combines Switch, MAC, and PHY to support operation in the LPI mode. When the LPI mode is enabled, systems on both sides of the link can save power during periods of low link utilization.

EEE implementation provides a protocol to coordinate transitions to or from lower power consumption without changing the link status and without dropping or corrupting frames. The transition time into and out of the lower power consumption is kept small enough to be transparent to upper layer protocols and applications. EEE specifies means to exchange capabilities between link partners to determine whether EEE is supported and to select the best set of parameters common to both sides.

Besides supporting the 100BASE-TX PHY EEE, KSZ8794CNX also supports 10BASE-T with reduced transmit amplitude requirements for 10 Mbps mode to allow a reduction in power consumption.

FIGURE 3-5: EEE TRANSMIT AND RECEIVE SIGNALING PATHS



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3.4.5.1 LPI Signaling

LPI signaling allows switch to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and switch can use this information to enter power-saving modes that require additional time to resume normal operation. LPI signaling also informs the switch when the link partner has sent such an indication. The definition of LPI signaling uses of the MAC for simplified full duplex operation (with carrier sense deferral). This provides full-duplex operation but uses the carrier sense signal to defer transmission when the PHY is in the LPI mode.

The decision on when to signal LPI (LPI request) to the link partner is made by the switch and communicated to the PHY through MAC MII interface. The switch is also informed when the link partner is signaling LPI, indication of LPI activation (LPI indication) on the MAC interface. The conditions under which switch decides to send LPI, and what actions are taken by switch when it receives LPI from the link partner, are specified in implementation section.

3.4.5.2 LPI Assertion

Without LPI assertion, the normal traffic transition continues on the MII interface. As soon as an LPI request is asserted, the LPI assert function starts to transmit the “Assert LPI” encoding on the MII and stop the MAC from transmitting normal traffic. Once the LPI request is de-asserted, the LPI assert function starts to transmit the normal inter-frame encoding on the MII again. After a delay, the MAC is allowed to start transmitting again. This delay is provided to allow the link partner to prepare for normal operation. [Figure 3-6](#) illustrates the EEE LPI between two active data idles.

3.4.5.3 LPI Detection

In the absence of “Assert LPI” encoding on the receive MII, the LPI detect function maps the receive MII signals as normal conditions. At the start of LPI, indicated by the transition from normal inter-frame encoding to the “Assert LPI” encoding on the receive MII, the LPI detect function continues to indicate idle on interface, and asserts LP_IDLE indication. At the end of LPI, indicated by the transition from the “Assert LPI” encoding to any other encoding on the receive MII, LP_IDLE indication is de-asserted and the normal decoding operation resumes.

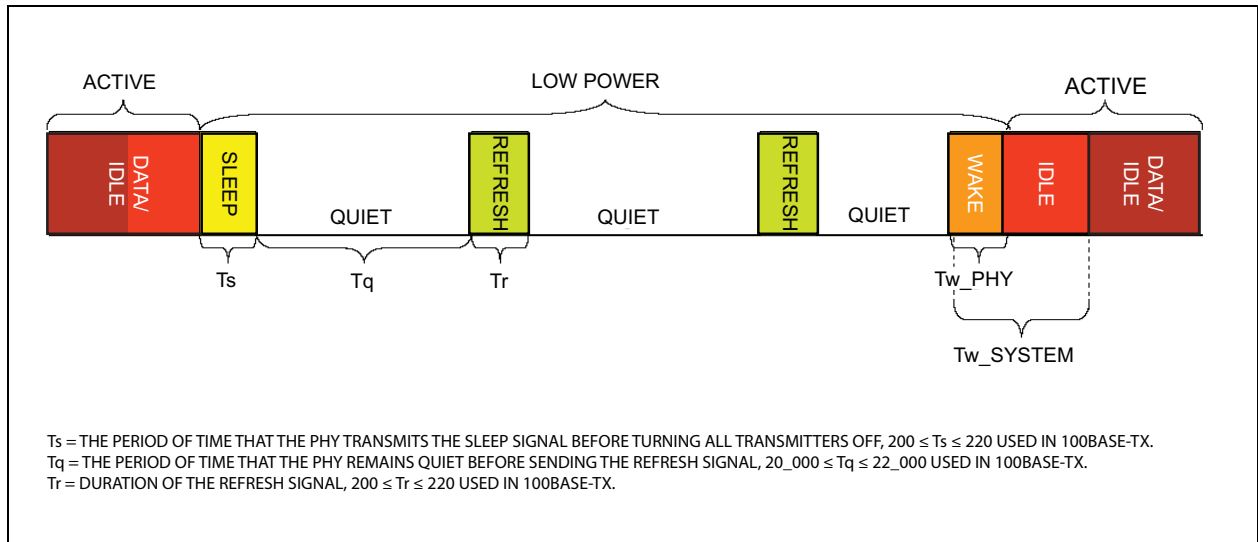
3.4.5.4 PHY LPI Transmit Operation

When the PHY detects the start of “Assert LPI” encoding on the MII, the PHY signals sleep to its link partner to indicate that the local transmitter is entering LPI mode. The EEE capability requires the PHY transmitter to go quiet after sleep is signaled. LPI requests are passed from one end of the link to the other and system energy savings can be achieved even if the PHY link does not go into a low power mode.

The transmit function of the local PHY is periodically enabled in order to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits. This maintains link integrity. This quiet-refresh cycle continues until the reception of the normal inter-frame encoding on the MII. The transmit function in the PHY communicates this to the link partner by sending a wake signal for a predefined period of time. The PHY then enters the normal operating state. No data frames are lost or corrupted during the transition to or from the LPI mode.

In 100BT/full-duplex EEE operation, refresh transmissions are used to maintain link and quiet periods are used for the power saving. Approximately, every 20 ms to 22 ms, a refresh of 200 μ s to 220 μ s is sent to the link partner. The refresh transmission and quiet periods are shown in [Figure 3-6](#).

FIGURE 3-6: TRAFFIC ACTIVITY AND EEE LPI OPERATIONS



3.4.5.5 PHY LPI Receive Operation

On receive, entering the LPI mode is triggered by the reception of a sleep signal from the link partner, which indicates that the link partner is about to enter the LPI mode. After sending the sleep signal, the link partner ceases transmission. When the receiver detects the sleep signal, the local PHY indicates “Assert LPI” on the MII and the local receiver can disable some functionality to reduce power consumption. The link partner periodically transmits refresh signals that are used by the local PHY. This quiet-refresh cycle continues until the link partner initiates transition back to normal mode by transmitting the wake signal for a predetermined period of time controlled by the LPI assert function. This allows the local receiver to prepare for normal operation and transition from the “Assert LPI” encoding to the normal inter-frame encoding on the MII. After a system specified recovery time, the link supports the nominal operational data rate.

3.4.5.6 Negotiation with EEE Capability

The EEE capability shall be advertised during the Auto-Negotiation stage. Auto-Negotiation provides a linked device with the capability to detect the abilities supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed at power up or reset, on command from management, due to link failure, or due to user intervention.

During Auto-Negotiation, both link partners indicate their EEE capabilities. EEE is supported only if during Auto-Negotiation both the local device and link partner advertise the EEE capability for the resolved PHY type. If EEE is not supported, all EEE functionality is disabled and the LPI client does not assert LPI. If EEE is supported by both link partners for the negotiated PHY type, then the EEE function can be used independently in either direction.

3.4.6 WAKE-ON-LAN (WOL)

Wake-on-LAN (WoL) allows a computer to be turned on or woken up by a network message. The message is usually sent by a program executed on another computer on the same local area network. Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet™, a management request from a remote administrator, or simply network traffic directly targeted to the local system. The KSZ8794CNX can be programmed to notify the host of the wake-up frame detection with the assertion of the interrupt signal (INTR_N) or assertion of the power management event signal (PME). The PME control is by PME indirect registers.

KSZ8794CNX MAC supports the detection of the following wake-up events:

- Detection of energy signal over a pre-configured value: Port PME Control Status Register Bit[0] in PME indirect registers.
- Detection of a link-up in the network link state: Port PME Control Status Register Bit[1] in the PME indirect registers.
- Receipt of a Magic Packet: Port PME Control Status Register Bit[2] in the PME indirect registers.

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There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own ways.

3.4.6.1 Direction of Energy

The energy is detected from the cable and is continuously presented for a time longer than pre-configured value, especially when this energy change may impact the level at which the system should re-enter to the normal power state.

3.4.6.2 Direction of Link-Up

Link status wake events are useful to indicate a linkup in the network's connectivity status.

3.4.6.3 Magic Packet

The Magic Packet is a broadcast frame containing anywhere within its payload 6 bytes of all 1s (FF FF FF FF FF FF) followed by sixteen repetitions of the target computer's 48-bit DA MAC address. Since the magic packet is only scanned for the above string, and not actually parsed by a full protocol stack, it may be sent as any network- and transport-layer protocol.

Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a LAN. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the LAN controller, and when the LAN controller receives a Magic Packet frame, it will alert the system to wake up. Once the KSZ8794CNX has been enabled for Magic Packet Detection in Port PME Control Mask Register Bit[2] in the PME indirect register, it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as source address (SA), destination address (DA), which may be the receiving station's IEEE MAC address, or a multicast or broadcast address and CRC. The specific sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of 0xFF. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

Example of Magic Packet:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller would be scanning for the data sequence (assuming an Ethernet frame):

```
DA - SA - TYPE - FF FF FF FF FF FF - 11 22 33 44 55 66 -11 22 33 44 55 66-11 22 33 44 55 66 - 11 22 33 44 55 66 -  
11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -11 22 33 44 55 66  
- 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66  
-MISC-CRC.
```

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination. If the scans do not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8794CNX detects the data sequence, however, it then alerts the PC's power management circuitry (assert the PME pin) to wake-up the system.

3.4.7 INTERRUPT (INT_N/PME_N)

INT_N is an interrupt signal that is used to inform the external controller that there has been a status update in the KSZ8794CNX interrupt status register. Bits [3:0] of Register 125 are the interrupt mask control bits to enable and disable the conditions for asserting the INT_N signal. Bits [3:0] of Register 124 are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading those bits in the Register 124.

PME_N is an optional PME interrupt signal that is used to inform the external controller that there has been a status update in the KSZ8794CNX interrupt status register. Bits [4] of Register 125 are the PME mask control bits to enable and disable the conditions for asserting the PME_N signal. Bits [4] of Register 124 are the PME interrupt status bits to indicate which PME interrupt conditions have occurred. The PME interrupt status Bit[4] is cleared after reading this bit of the Register 124.

Additionally, the interrupt pins of INT_N and PME_N eliminate the need for the processor to poll the switch for status change.

3.5 Interfaces

The KSZ8794CNX device incorporates a number of interfaces to enable it to be designed into a standard network environment as well as a vendor unique environment. The available interfaces are summarized in [Table 3-4](#). The detail of each usage in this table is provided in the sections that follow.

TABLE 3-4: AVAILABLE INTERFACES

Interface	Type	Usage	Registers Accessed
SPI	Configuration and Register Access	[As Slave Serial Bus] - External CPU or controller can R/W all internal registers thru this interface.	All
MIIM	Configuration and Register Access	MDC/MDIO capable CPU or controllers can R/W 4 PHYs registers.	PHYs Only
MII	Data Flow	Interface to the Port 4 GMAC using the standard MII timing.	N/A
RGMII	Data Flow	Interface to the Port 4 GMAC using the faster reduced RGMII timing.	N/A
RMII	Data Flow	Interface to the Port 4 GMAC using the faster reduced MII timing.	N/A

3.5.1 CONFIGURATION INTERFACE

3.5.1.1 SPI Slave Serial Bus Configuration

The KSZ8794CNX can also act as an SPI slave device. Through the SPI, the entire feature set can be enabled, including “VLAN,” “IGMP snooping,” “MIB counters,” etc. The external SPI master device can access any registers randomly in the data sheet shown. The SPI mode can configure all the desired settings including indirect registers and tables. KSZ8794 default is in the ‘start switch’ mode with the register 1 bit [0] = ‘1’, to disable the switch, write a “0” to Register 1 bit [0].

Two standard SPI commands are supported (00000011 for “READ DATA,” and 00000010 for “WRITE DATA”). To speed configuration time, the KSZ8794CNX also supports multiple reads or writes. After a byte is written to or read from the KSZ8794CNX, the internal address counter automatically increments if the SPI slave select signal (SPIS_N) continues to be driven low. If SPIS_N is kept low after the first byte is read, the next byte at the next address will be shifted out on SPIQ. If SPIS_N is kept low after the first byte is written, bits on the master out slave input (SPID) line will be written to the next address. Asserting SPIS_N high terminates a read or write operation. This means that the SPIS_N signal must be asserted high and then low again before issuing another command and address. The address counter wraps back to zero once it reaches the highest address. Therefore the entire register set can be written to or read from by issuing a single command and address.

The KSZ8794CNX is able to support SPI bus up to a maximum of 50 MHz. A high-performance SPI master is recommended to prevent internal counter overflow.

To use the KSZ8794CNX SPI:

1. At the board level, connect the KSZ8794CNX pins as detailed in [Table 3-5](#).
2. Configure the serial communication to SPI slave mode by pulling down pin SPIQ with a pull-down resistor.
3. Write configuration data to registers using a typical SPI write data cycle as shown in [Figure 3-7](#) or SPI multiple write as shown in [Figure 3-8](#). Note that data input on SDA is registered on the rising edge of SCL clock.
4. Registers can be read and the configuration can be verified with a typical SPI read data cycle as shown in [Figure 3-7](#) or a multiple read as shown in [Figure 3-8](#). Note that read data is registered out of SPIQ on the falling edge of SCL clock.

TABLE 3-5: SPI CONNECTIONS

KSZ8794CNX Signal Name	Microprocessor Signal Description
SPIS_N (S_CS)	SPI Slave Select
SCL (S_CLK)	SPI Clock
SDA (S_DI)	Master Output. Slave Input.
SPIQ (S_DO)	Master Input. Slave Output.