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KSZ8841-16/32MQL/MVL/MVLI/MBL

Single-Port Ethernet MAC Controller

with Non-PCI Interface

Rev. 1.6

General Description

The KSZ8841-series single-port chip includes PCI and non-PCI CPU interfaces, and are available in 8/16-bit and 32-bit bus designs. This datasheet describes the KSZ8841M-series of non-PCI CPU interface chips. For information on the KSZ8841 PCI CPU interface chips, refer to the KSZ8841P datasheet.

The KSZ8841M is a single chip, mixed analog/digital device offering Wake-on-LAN technology for effectively addressing Fast Ethernet applications. It consists of a Fast Ethernet MAC controller, an 8-bit, 16-bit, and 32-bit generic host processor interface and incorporates a unique dynamic memory pointer with 4-byte buffer boundary and a fully utilizable 8KB for both TX and RX directions in host buffer interface.

The KSZ8841M is designed to be fully compliant with the appropriate IEEE 802.3 standards. An industrial temperature-grade version of the KSZ8841M, the KSZ8841MVLI, also can be ordered (see "Ordering Information section).

LinkMD®

Physical signal transmission and reception are enhanced through the use of analog circuitry, making the design more efficient and allowing for lower-power consumption. The KSZ8841M is designed using a low-power CMOS process that features a single 3.3V power supply with 5V tolerant I/O. It has an extensive feature set that offers management information base (MIB) counters and CPU control/data interfaces.

The KSZ8841M includes a unique cable diagnostics feature called LinkMD®. This feature determines the length of the cabling plant and also ascertains if there is an open or short condition in the cable. Accompanying software enables the cable length and cable conditions to be conveniently displayed. In addition, the KSZ8841M supports Hewlett Packard (HP) Auto-MDIX thereby eliminating the need to differentiate between straight or crossover cables in applications.

Functional Diagram

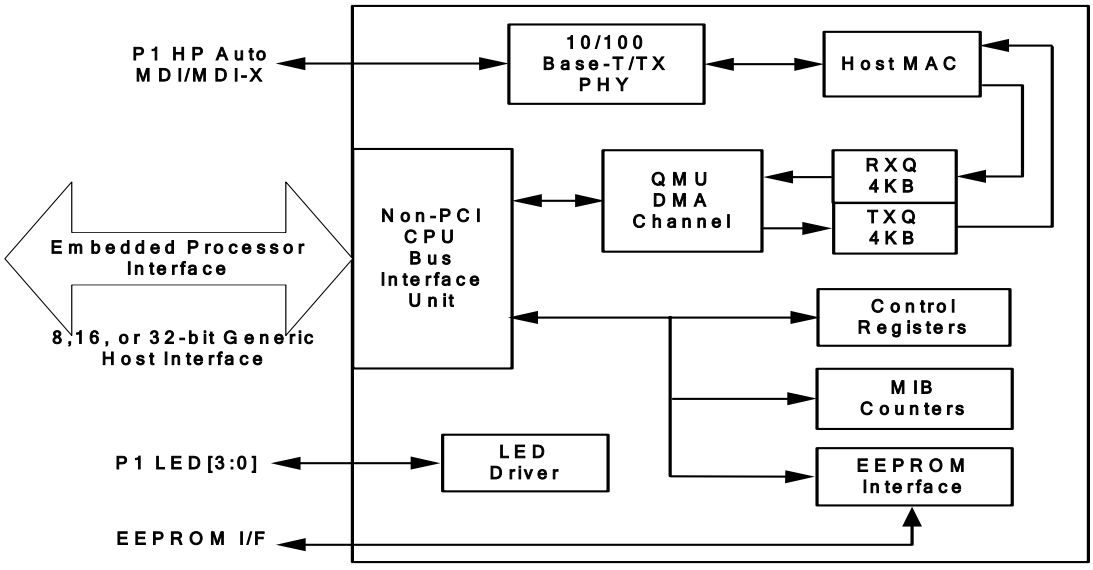

Figure 1. KSZ8841M Functional Diagram

Features

- Single chip Ethernet controller with IEEE802.3u support
- Supports 10BASE-T/100BASE-TX
- Supports IEEE 802.3x full-duplex flow control and half-duplex backpressure collision flow control
- Supports burst data transfers
- 8KB internal memory for RX/TX FIFO buffers
- Early TX/RX functions to minimize latency through the device
- Optional to use external serial EEPROM configuration for both KSZ8841-16MQL and KSZ8841-32MQL
- Single 25MHz reference clock for both PHY and MAC

Network Features

- Fully integrated to comply with IEEE802.3u standards
- 10BASE-T and 100BASE-TX physical layer support
- Auto-negotiation: 10/100Mbps full and half duplex
- Adaptive equalizer
- Baseline wander correction

Power Modes, Power Supplies, and Packaging

- Single power supply (3.3V) with 5V tolerant I/O buffers
- Enhanced power management feature with power-down feature to ensure low-power dissipation during device idle periods
- Comprehensive LED indicator support for link, activity, full/half duplex, and 10/100 speed (4 LEDs)
  – User programmable
- Low-power CMOS design
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 128-pin PQFP and 100-ball LFBGA (128-pin LQFP optional)

Additional Features

In addition to offering all of the features of a Layer 2 controller, the KSZ8841M offers:

- Dynamic buffer memory scheme
  – Essential for applications such as Video over IP where image jitter is unacceptable
- Flexible 8-bit, 16-bit, and 32-bit generic host processor interfaces
- Micrel LinkMD™ cable diagnostic capabilities to determine cable length, diagnose faulty cables, and determine distance to fault
- Wake-on-LAN functionality
  – Incorporates Magic Packet™, network link state, and wake-up frame technology
- HP Auto MDI-X™ crossover with disable/enable option
- Ability to transmit and receive frames up to 1916 bytes

Applications

- Video Distribution Systems
- High-end Cable, Satellite, and IP set-top boxes
- Video over IP
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Motion Control
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

Ordering Information

Part Number	Temperature Range	Package
KSZ8841-16MQL	0°C to 70°C	128-Pin PQFP
KSZ8841-32MQL	0°C to 70°C	128-Pin PQFP
KSZ8841-16MVL	0°C to 70°C	128-Pin LQFP
KSZ8841-32MVL	0°C to 70°C	128-Pin LQFP
KSZ8841-16MVLI	–40°C to +85°C	128-Pin LQFP
KSZ8841-32MVLI	–40°C to +85°C	128-Pin LQFP
KSZ8841-16MBL	0°C to 70°C	100-Ball LFBGA
KSZ8841-16MBLI	–40°C to +85°C	100-Ball LFBGA
KSZ8841-16MQL-Eval	Evaluation Board for the KSZ8841-16MQL	
KSZ8841-16MBL-Eval	Evaluation Board for the KSZ8841-16MBL	

Revision History

Revision	Date	Summary of Changes
1.0	06/30/05	First released Preliminary Information.
1.1	08/08/05	Updated General Description, Functional Diagram, Pin Description and Features. Added this Revision History Table and Loopback support sections.
1.2	10/04/05	Update Power Saving bit description in P1PHYCTRL and P1SCSLMD registers.
1.3	11/01/05	Updated Figure 12/13/14 Asynchronous Timing and Table 16/17/18 parameters, PQFP package information.
1.4	03/31/06	Added QMU RX Flow Control High Watermark QRFCR register and updated body text
1.5	4/10/07	Improve the ARDY low time in read cycle to 40 ns and in write cycle to 50 ns during QMU data register access
1.6	10/22/07	Add KSZ8841-16MBL 100-Ball BGA package information

Contents

List of Figures

List of Tables

Pin Configuration for KSZ8841-16 Chip (8/16-Bit)

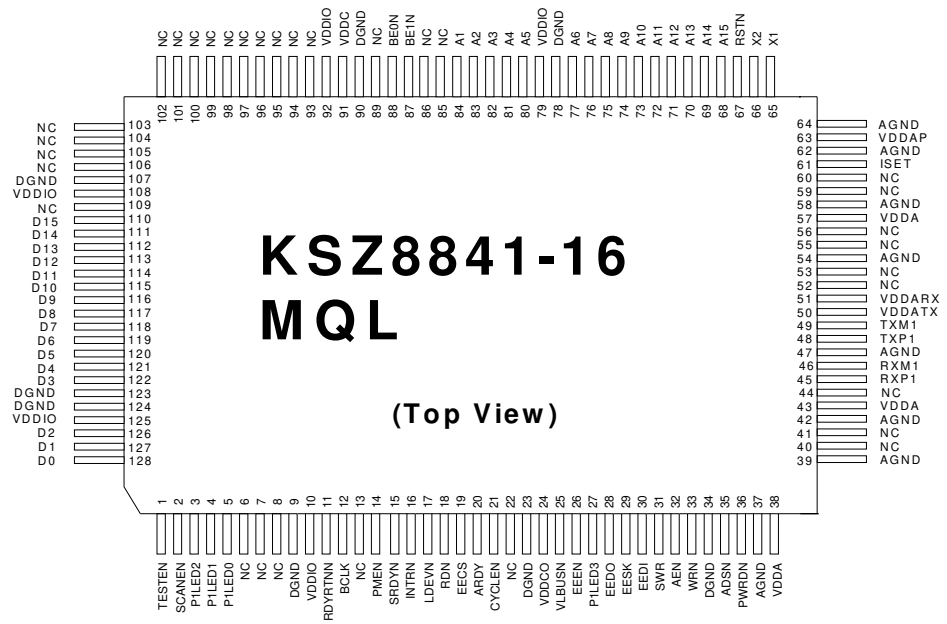

Figure 2. Standard – KSZ8841-16MQL 128-Pin PQFP

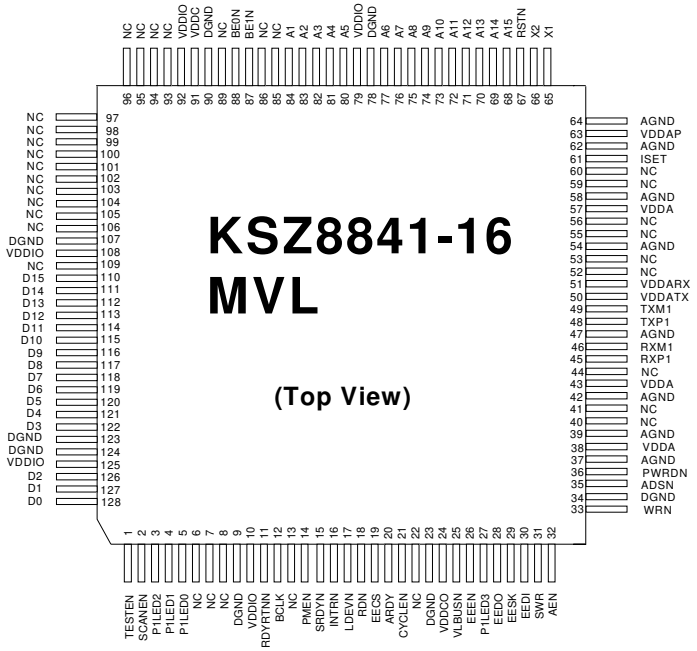

Figure 3. Option – KSZ8841-16MVL 128-Pin LQFP

Ball Configuration for KSZ8841-16 Chip (8/16-Bit)

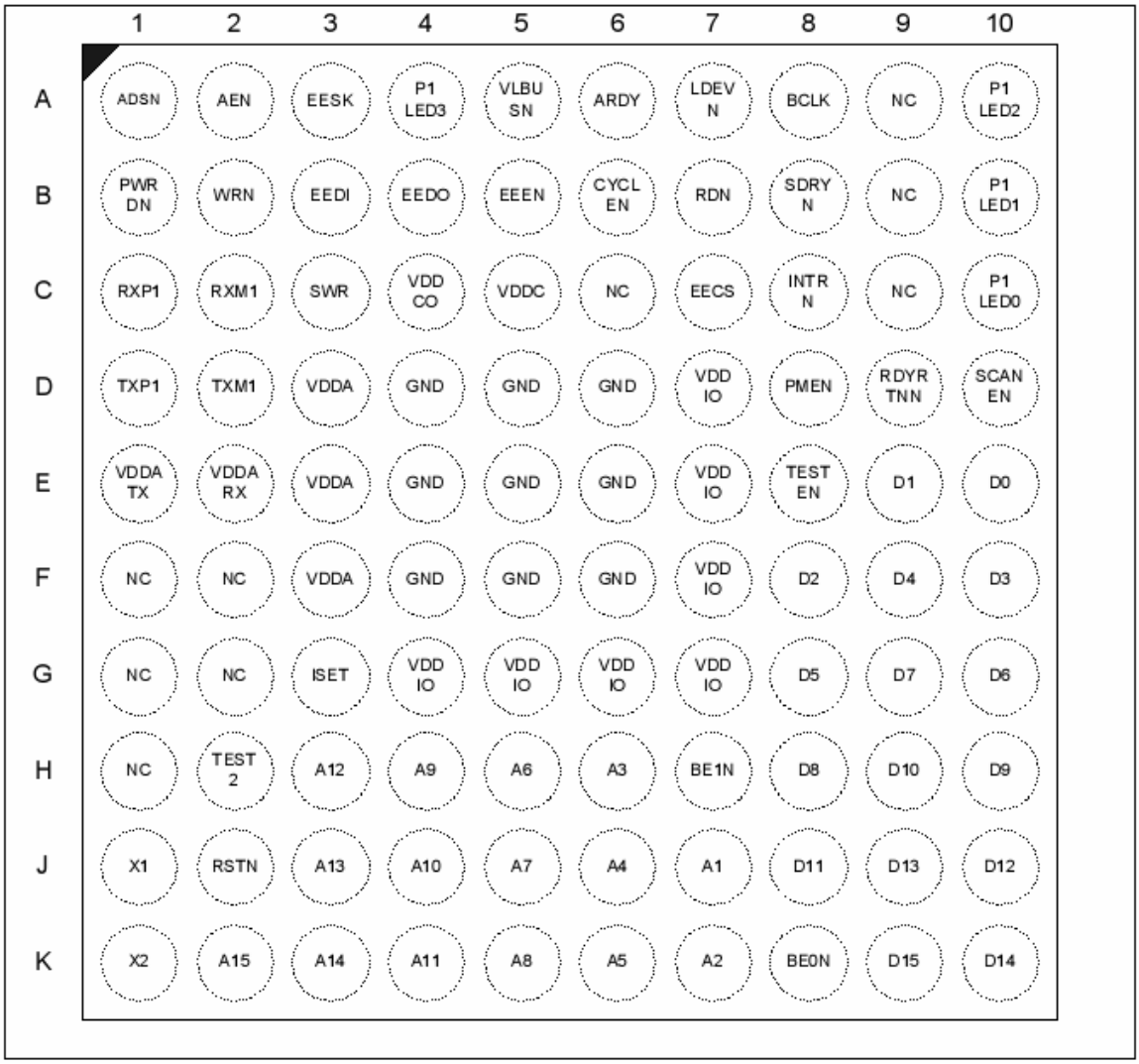

Figure 4. KSZ8841-16MBL 100-Ball LFBGA (Top View)

Pin Description for KSZ8841-16 Chip (8/16-Bit)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>3</td><td>P1LED2</td><td>Opu</td><td rowspan="3">Port 1 LED indicators[1] defined as follows:
<table>
<tr><td></td><td colspan="2">Chip Global Control Register: CGCR bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2]</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. CGCR bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2]</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27.</td></tr>
<tr><td>4</td><td>P1LED1</td><td>Opu</td></tr>
<tr><td>5</td><td>P1LED0</td><td>Opu</td></tr>
<tr><td>6</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>7</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>8</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.
For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
<tr><td>12</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.
This pin should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>13</td><td>NC</td><td>Ipu</td><td>No Connect.</td></tr>
<tr><td>14</td><td>PMEN</td><td>Opu</td><td>Power Management Event Not
When asserted (Low), this signal indicates that a power management event has occurred in the system when a wake-up signal is detected by KSZ8841M.</td></tr>
</table>

Pin Number	Pin Name	Type	Pin Function
15	SRDYN	Opu	Synchronous Ready Not Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses. For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK. For burst mode (32-bit interface only), the KSZ8841M drives this pin low to signal wait states.
16	INTRN	Opd	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor.
17	LDEVN	Opd	Local Device Not Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8841M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
19	EECS	Opu	EEPROM Chip Select This signal is used to select an external EEPROM device.
20	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. this pin need an external 4.7K pull-up resistor.
21	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles.
22	NC	Opd	No Connect
23	DGND	Gnd	Digital IO ground
24	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins. It is recommended this pin should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite bead and capacitors).
25	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 8-bit or 16-bit asynchronous mode or EISA-like burst mode.
26	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	Opd	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	EEPROM Serial Clock A 4µs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.

Pin Number	Pin Name	Type	Pin Function
30	EEDI	Ipd	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin can be pull-down for 8-bit bus mode, pull-up for 16-bus mode or don't care for 32-bus mode when EEEN is pull-down (without EEPROM).
31	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
32	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
33	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
34	DGND	Gnd	Digital IO ground
35	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
36	PWRDN	Ipu	Full-chip power-down. Active Low (Low = Power down; High or floating = Normal operation).
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
39	AGND	Gnd	Analog ground
40	NC	—	No Connect
41	NC	—	No Connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
44	NC	—	No Connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	NC	—	No Connect
53	NC	—	No Connect
54	AGND	Gnd	Analog ground
55	NC	—	No Connect
56	NC	—	No Connect
57	VDDA	P	1.2 analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
58	AGND	Gnd	Analog ground
59	NC	Ipu	No connect
60	NC	Ipu	No connect
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground

Pin Number	Pin Name	Type	Pin Function
63	VDDAP	P	1.2V analog V_{DD} for PLL input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
64	AGND	Gnd	Analog ground
65	X1	I	25MHz crystal or oscillator clock connection.
66	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is 50ppm for either crystal or oscillator.
67	RSTN	Ipu	Reset Not Hardware reset pin (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
68	A15	I	Address 15
69	A14	I	Address 14
70	A13	I	Address 13
71	A12	I	Address 12
72	A11	I	Address 11
73	A10	I	Address 10
74	A9	I	Address 9
75	A8	I	Address 8
76	A7	I	Address 7
77	A6	I	Address 6
78	DGND	Gnd	Digital IO ground
79	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
80	A5	I	Address 5
81	A4	I	Address 4
82	A3	I	Address 3
83	A2	I	Address 2
84	A1	I	Address 1
85	NC	I	No Connect
86	NC	I	No Connect
87	BE1N	I	Byte Enable 1 Not, Active low for Data byte 1 enable (don't care in 8-bit bus mode).
88	BE0N	I	Byte Enable 0 Not, Active low for Data byte 0 enable (there is an internal inverter enabled and connected to the BE1N for 8-bit bus mode).
89	NC	I	No Connect
90	DGND	Gnd	Digital core ground
91	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
92	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
93	NC	I	No Connect
94	NC	I	No Connect
95	NC	I	No Connect
96	NC	I	No Connect
97	NC	I	No Connect
98	NC	I	No Connect
99	NC	I	No Connect
100	NC	I	No Connect
101	NC	I	No Connect
102	NC	I	No Connect

Pin Number	Pin Name	Type	Pin Function
103	NC	I	No Connect
104	NC	I	No Connect
105	NC	I	No Connect
106	NC	I	No Connect
107	DGND	Gnd	Digital IO ground
108	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
109	NC	I	No Connect
110	D15	I/O	Data 15
111	D14	I/O	Data 14
112	D13	I/O	Data 13
113	D12	I/O	Data 12
114	D11	I/O	Data 11
115	D10	I/O	Data 10
116	D9	I/O	Data 9
117	D8	I/O	Data 8
118	D7	I/O	Data 7
119	D6	I/O	Data 6
120	D5	I/O	Data 5
121	D4	I/O	Data 4
122	D3	I/O	Data 3
123	DGND	Gnd	Digital IO ground
124	DGND	Gnd	Digital core ground
125	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
126	D2	I/O	Data 2
127	D1	I/O	Data 1
128	D0	I/O	Data 0

Legend:

P = Power supply Gnd = Ground

I/O = Bi-directional I = Input O = Output.

Ipd = Input with internal pull-down.

Ipu = Input with internal pull-up.

Opd = Output with internal pull-down.

Opu = Output with internal pull-up.

Ball Description for KSZ8841-16 Chip (8/16-Bit)

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type</th><th>Ball Function</th></tr>
<tr><td>E8</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this ball to ground.</td></tr>
<tr><td>D10</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this ball to ground.</td></tr>
<tr><td>A10
B10
C10</td><td>P1LED2
P1LED1
P1LED0</td><td>Opu
Opu
Opu</td><td>Port 1 LED indicators[1] defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2]</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2]</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is ball A4.</td></tr>
<tr><td>D9</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this ball, assert this ball.</td></tr>
<tr><td>A8</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.
This ball should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>D8</td><td>PMEN</td><td>Opu</td><td>Power Management Event Not
When asserted (Low), this signal indicates that a power management event has occurred in the system when a wake-up signal is detected by KSZ8841M.</td></tr>
<tr><td>B8</td><td>SRDYN</td><td>Opu</td><td>Synchronous Ready Not
Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses.
For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK.</td></tr>
<tr><td>C8</td><td>INTRN</td><td>Opd</td><td>Interrupt
Active Low signal to host CPU to indicate an interrupt status bit is set, this ball need an external 4.7K pull-up resistor.</td></tr>
<tr><td>A7</td><td>LDEVN</td><td>Opd</td><td>Local Device Not</td></tr>
</table>

Ball Number	Ball Name	Type	Ball Function
			Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8841M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
B7	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
C7	EECS	Opu	EEPROM Chip Select
A6	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. This ball needs an external 4.7K pull-up resistor.
B6	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this ball follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this ball stays High for read cycles and Low for write cycles.
A5	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 8-bit or 16-bit asynchronous mode or EISA-like burst mode.
B5	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this ball is pull-up. EEPROM is disabled when this ball is pull-down or no connect.
A4	P1LED3	Opd	Port 1 LED indicator See the description in balls A10, B10, and C10.
B4	EEDO	Opd	EEPROM Data Out This ball is connected to DI input of the serial EEPROM.
A3	EESK	Opd	EEPROM Serial Clock A 4μs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.
B3	EEDI	Ipd	EEPROM Data In This ball is connected to DO output of the serial EEPROM when EEEN is pull-up. This ball can be pull-down for 8-bit bus mode, pull-up for 16-bit bus mode or don't care for 32-bit bus mode when EEEN is pull-down (without EEPROM).
C3	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
A2	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
B2	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
A1	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
B1	PWRDN	Ipu	Full-chip power-down. Low = Power down; High or floating = Normal operation.

Ball Number	Ball Name	Type	Ball Function
C1	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
C2	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
D1	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
D2	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
H2	TEST2	Ipu	Test input 2 For normal operation, left this ball open.
G3	ISET	O	Set physical transmits output current. Pull-down this ball with a 3.01K 1% resistor to ground.
J1	X1	I	25MHz crystal or oscillator clock connection.
K1	X2	O	Balls (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ± 50ppm for either crystal or oscillator.
J2	RSTN	Ipu	Hardware reset ball (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
K2	A15	I	Address 15
K3	A14	I	Address 14
J3	A13	I	Address 13
H3	A12	I	Address 12
K4	A11	I	Address 11
J4	A10	I	Address 10
H4	A9	I	Address 9
K5	A8	I	Address 8
J5	A7	I	Address 7
H5	A6	I	Address 6
K6	A5	I	Address 5
J6	A4	I	Address 4
H6	A3	I	Address 3
K7	A2	I	Address 2
J7	A1	I	Address 1
H7	BE1N	I	Byte Enable 1 Not, Active low for Data byte 1 enable (don't care in 8-bit bus mode).
K8	BE0N	I	Byte Enable 0 Not, Active low for Data byte 0 enable (there is an internal inverter enabled and connected to the BE1N for 8-bit bus mode).
K9	D15	I/O	Data 15
K10	D14	I/O	Data 14
J9	D13	I/O	Data 13
J10	D12	I/O	Data 12
J8	D11	I/O	Data 11
H9	D10	I/O	Data 10
H10	D9	I/O	Data 9
H8	D8	I/O	Data 8
G9	D7	I/O	Data 7
G10	D6	I/O	Data 6
G8	D5	I/O	Data 5
F9	D4	I/O	Data 4
F10	D3	I/O	Data 3

Ball Number	Ball Name	Type	Ball Function
F8	D2	I/O	Data 2
E9	D1	I/O	Data 1
E10	D0	I/O	Data 0
C4	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output ball provides power to all VDDC/VDDA balls. It is recommended this ball should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application. Note: Internally generated power voltage. Do not connect an external power supply to this ball. This ball is used for connecting external filter (Ferrite bead and capacitors).
C5	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (ball C4) through external Ferrite bead and capacitor.
D3, E3, F3	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (ball C4) through external Ferrite bead and capacitor.
E1	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
E2	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
D7, E7, F7, G4, G5, G6, G7	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
D4, D5, D6, E4, E5, E6, F4, F5, F6	GND	Gnd	All digital and analog grounds
H1, A9, B9, C9, C6, F2, F1, G2, G1	NC	I/O	No Connect

Pin Configuration for KSZ8841-32 Chip (32-Bit)

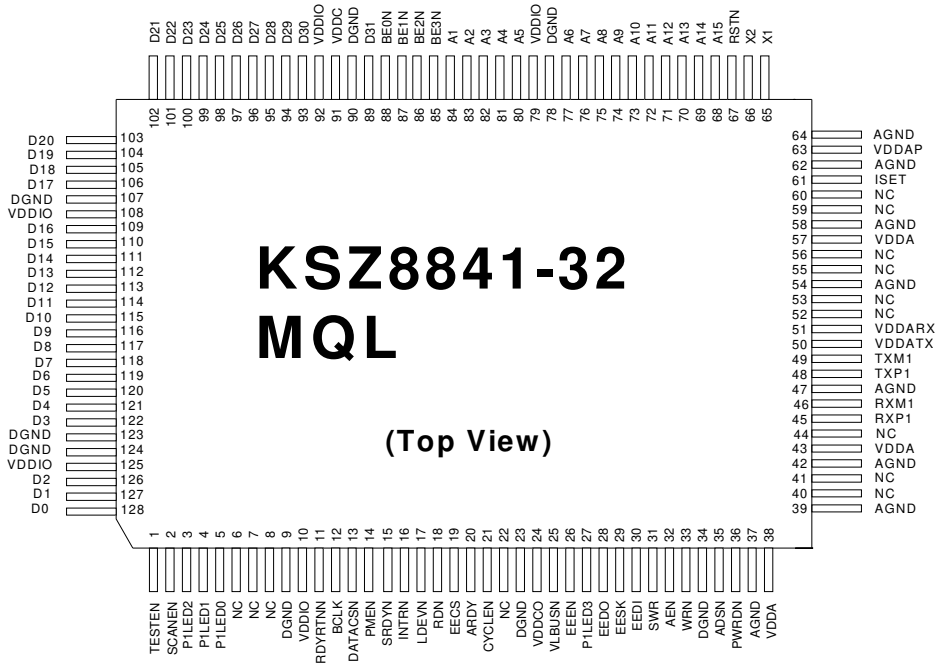

Figure 5. Standard – KSZ8841-32MQL 128-Pin PQFP

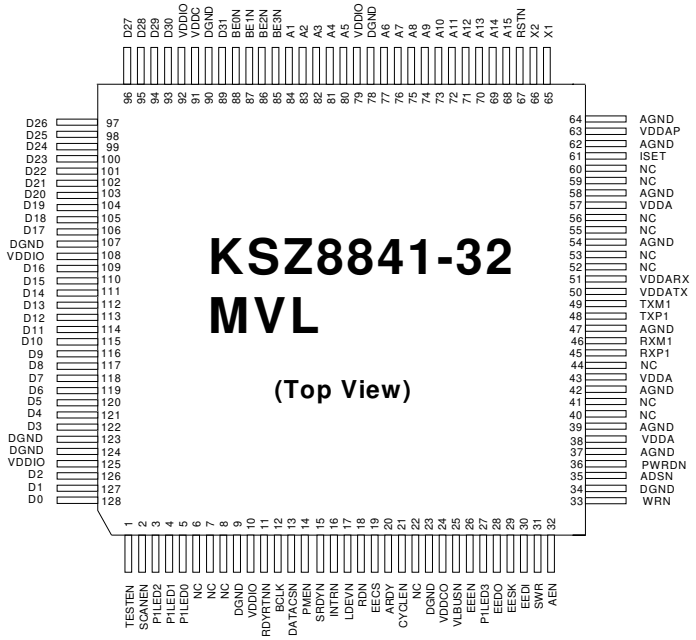

Figure 6. Option – KSZ8841-32MVL 128-Pin LQFP

Pin Description for KSZ8841-32 Chip (32-Bit)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>3</td><td>P1LED2</td><td>Opu</td><td rowspan="3">Port 1 LED indicators[1] defined as follows:
<table>
<tr><td></td><td colspan="2">Chip Global Control Register: CGCR bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2]</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. CGCR bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2]</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27.</td></tr>
<tr><td>4</td><td>P1LED1</td><td>Opu</td></tr>
<tr><td>5</td><td>P1LED0</td><td>Opu</td></tr>
<tr><td>6</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>7</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>8</td><td>NC</td><td>Opu</td><td>No Connect.</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.
For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
<tr><td>12</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.
This pin should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>13</td><td>DATACSN</td><td>Ipu</td><td>DATA Chip Select Not (For KSZ8841-32 Mode only)
Chip select signal for QMU data register (QDRH, QDRL), active Low.
When DATACSN is Low, the data path can be accessed regardless of the value of AEN, A15-A1, and the content of the BANK select register.</td></tr>
<tr><td>14</td><td>PMEN</td><td>Opu</td><td>Power Management Event Not
When asserted (Low), this signal indicates that a power management event has occurred in the system when a wake-up signal is detected by KSZ8841M.</td></tr>
</table>

Pin Number	Pin Name	Type	Pin Function
15	SRDYN	Opu	Synchronous Ready Not Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses. For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK. For burst mode (32-bit interface only), the KSZ8841M drives this pin low to signal wait states.
16	INTRN	Opd	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor
17	LDEVN	Opd	Local Device Not Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8841M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
19	EECS	Opu	EEPROM Chip Select This signal is used to select an external EEPROM device.
20	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. this pin need an external 4.7K pull-up resistor.
21	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles.
22	NC	Opd	No Connect
23	DGND	Gnd	Digital IO ground
24	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins. It is recommended this ball should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application. Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite bead and capacitors).
25	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 32-bit asynchronous mode or EISA-like burst mode.
26	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	Opd	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	EEPROM Serial Clock A 4μs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.

Pin Number	Pin Name	Type	Pin Function
30	EEDI	Ipd	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin can be pull-down for 8-bit bus mode, pull-up for 16-bus mode or don't care for 32-bus mode when EEEN is pull-down (without EEPROM).
31	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
32	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
33	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
34	DGND	Gnd	Digital IO ground
35	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
36	PWRDN	Ipu	Full-chip power-down. Active Low (Low = Power down; High or floating = Normal operation).
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
39	AGND	Gnd	Analog ground
40	NC	—	No Connect
41	NC	—	No Connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
44	NC	—	No Connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	NC	—	No Connect
53	NC	—	No Connect
54	AGND	Gnd	Analog ground
55	NC	—	No Connect
56	NC	—	No Connect
57	VDDA	P	1.2 analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
58	AGND	Gnd	Analog ground
59	NC	Ipu	No connect
60	NC	Ipu	No connect
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground

Pin Number	Pin Name	Type	Pin Function
63	VDDAP	P	1.2V analog V_{DD} for PLL input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
64	AGND	Gnd	Analog ground
65	X1	I	25MHz crystal or oscillator clock connection.
66	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is 50ppm for either crystal or oscillator.
67	RSTN	Ipu	Reset Not Hardware reset pin (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
68	A15	I	Address 15
69	A14	I	Address 14
70	A13	I	Address 13
71	A12	I	Address 12
72	A11	I	Address 11
73	A10	I	Address 10
74	A9	I	Address 9
75	A8	I	Address 8
76	A7	I	Address 7
77	A6	I	Address 6
78	DGND	Gnd	Digital IO ground
79	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
80	A5	I	Address 5
81	A4	I	Address 4
82	A3	I	Address 3
83	A2	I	Address 2
84	A1	I	Address 1
85	BE3N	I	Byte Enable 3 Not, Active low for Data byte 3 enable
86	BE2N	I	Byte Enable 2 Not, Active low for Data byte 2 enable
87	BE1N	I	Byte Enable 1 Not, Active low for Data byte 1 enable
88	BE0N	I	Byte Enable 0 Not, Active low for Data byte 0 enable
89	D31	I/O	Data 31
90	DGND	Gnd	Digital core ground
91	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
92	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
93	D30	I/O	Data 30
94	D29	I/O	Data 29
95	D28	I/O	Data 28
96	D27	I/O	Data 27
97	D26	I/O	Data 26
98	D25	I/O	Data 25
99	D24	I/O	Data 24
100	D23	I/O	Data 23
101	D22	I/O	Data 22
102	D21	I/O	Data 21