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KSZ8841-PMQL

Single-Port Ethernet MAC Controller with PCI Interface

Rev.1.5

General Description

The KSZ8841-series single-port chip includes PCI and non-PCI CPU interfaces. This datasheet describes the KSZ8841-PMQL with PCI CPU interface chips. For information on the KSZ8841 non-PCI CPU interface chips, refer to the KSZ8841-MQL datasheet.

The KSZ8841-PMQL is a single port Fast Ethernet MAC chip with a 32-bit/33MHz PCI processor interface. Designed to be fully compliant with the IEEE 802.3u standard, the KSZ8841-PMQL is also available in an industrial temperature-grade version of the KSZ8841-PMQL, the KSZ8841-PMQLI. (See Ordering Information).

Physical signal transmission and reception are enhanced through the use of analog circuitry, making the design more efficient and allowing for lower power consumption. The KSZ8841-PMQL is designed using a low-power CMOS process that features a single 3.3V power supply with 5V tolerant I/O.

LinkMD®

The KSZ8841-PMQL is a mixed signal analog/digital device offering Wake-on-LAN technology. Its extensive feature set includes management information base (MIB) counters and CPU control/data interfaces.

The KSZ8841-PMQL includes a unique cable diagnostics feature called LinkMD®. This feature calculates the length of the cabling plant and determines if there is an open/short condition in the cable. Accompanying software allows the cable length and cable conditions to be conveniently displayed. In addition, the KSZ8841-PMQL supports Hewlett Packard (HP) Auto-MDIX thereby eliminating the need to differentiate between straight or crossover cables in applications.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Diagram

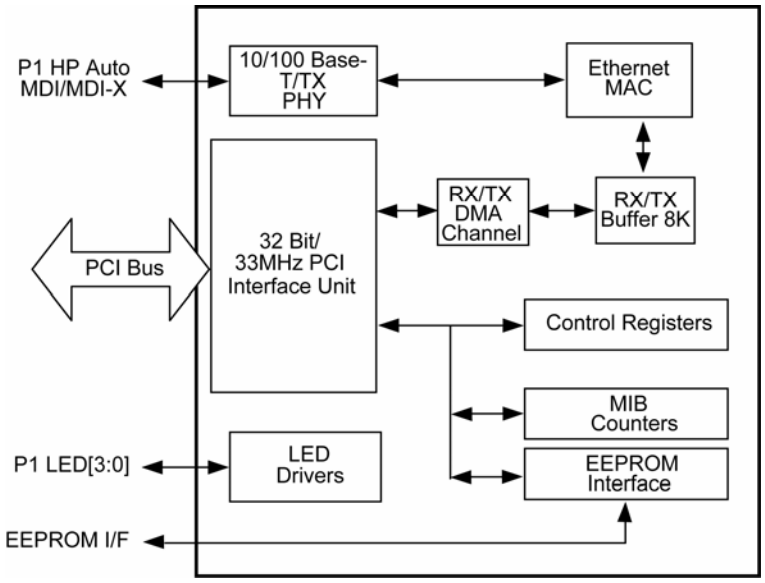

Figure 1. KSZ8841-PMQL Function Diagram

Features

- Fully compliant with the IEEE802.3u standard
- Supports 10/100BASE-T/TX
- Supports IEEE 802.3x full-duplex flow control and half-duplex backpressure collision flow control
- Supports burst data transfers
- 8KB internal memory for RX/TX FIFO buffers
- Early TX/RX functions to minimize latency through the device
- Serial EEPROM configuration
- Single 25MHz reference clock for both PHY and MAC

Network Features

- Fully integrated to comply with IEEE802.3u standards
- 10BASE-T and 100BASE-TX physical layer support
- Auto-negotiation: 10/100Mbps full and half duplex
- Supports IEEE 802.1Q multiple VLAN tagging
- On-chip wave shaping – No external filters required
- Adaptive equalizer
- Baseline wander correction

Power Modes, Packaging, and Power Supplies

- Single power supply (3.3V) with 5V tolerant I/O buffers
- Enhanced power management feature with power down feature to ensure low power dissipation during device idle periods
- Comprehensive LED indicator support for link, activity, full/half duplex, and 10/100 speed (4 LEDs)
- Low power CMOS design
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C (KSZ8841-PMQLI)
- Available in 128-pin PQFP

Additional Features

- Single chip Ethernet controller with IEEE 802.3u support
- 32 bit/33MHz PCI bus for different host processor interfaces
- Dynamic buffer memory scheme
  - Essential for applications such as Video over IP where image jitter is unacceptable
- Micrel LinkMD® cable diagnostic capabilities to determine cable length and distance to fault, and to diagnose faulty cables
- Wake-on-LAN technology
  - Incorporates Magic Packet™, network link state, and wake-up frame technology
- HP Auto MDIX crossover with disable and enable option
- Enhanced power management feature with power-down feature

Applications

- Video Distribution Systems
- High-end Cable, Satellite, and IP set-top boxes
- Video over IP
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

Ordering Information

Part Number	Junction Temp. Range	Package
KSZ8841-PMQL	0°C to 70°C	128-Pin PQFP
KSZ8841-PMQLI	–40°C to +85°C	128-Pin PQFP

Revision History

Revision	Date	Summary of Changes
1.0	09/29/05	Data sheet created.
1.1	01/13/06	Used detail package information.
1.2	06/12/06	Corrected MRFCE field for MDRXC register. The NC Pin 13 was changed from Ipu to –. The PWRDN Pin 36 was changed from I to Ipu.
1.3	02/16/07	Update support transformer and other.
1.4	06/01/07	Add the package thermal information in the operating ratings.
1.5	10/02/07	In VDDCO pin description, add 100ohm resistor for internal LDO application.

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Pin Configuration

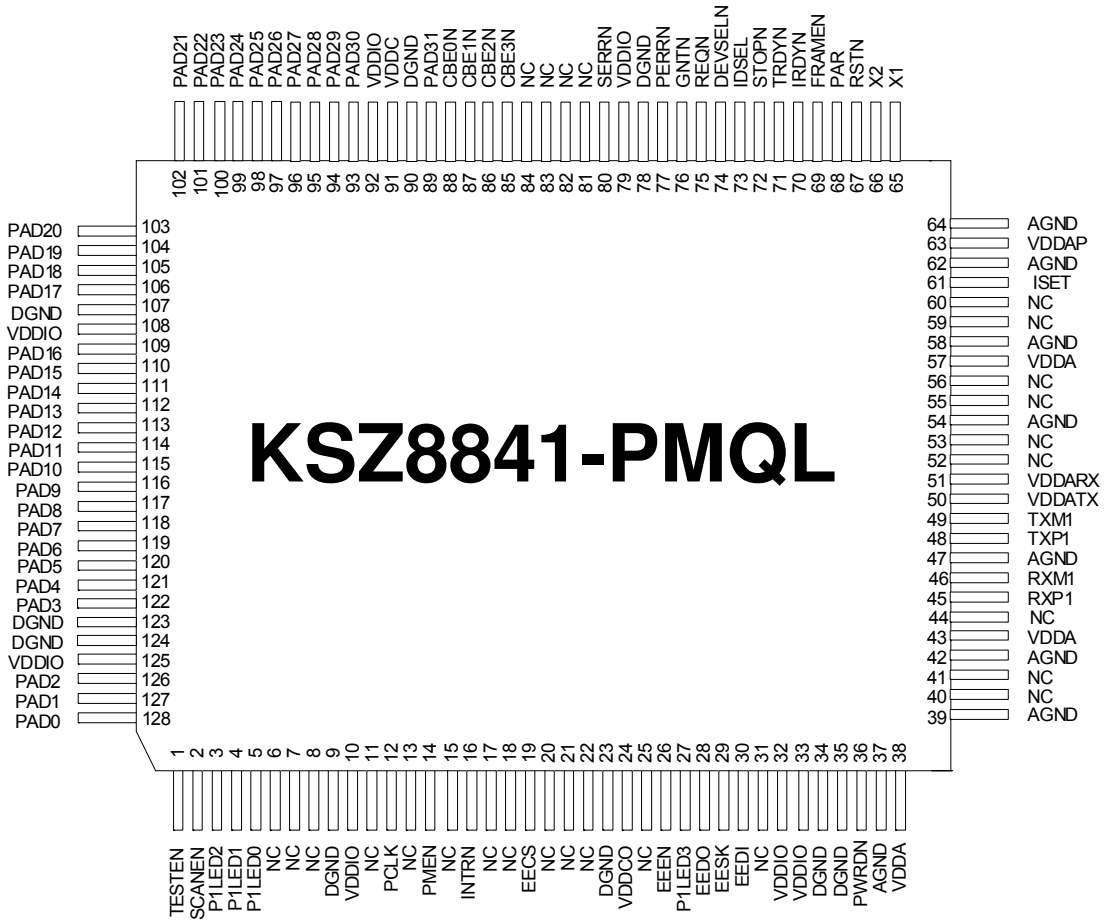

Figure 2. KSZ8841-PMQL 128-Pin PQFP (Top View)

Pin Description

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>3
4
5</td><td>P1LED2
P1LED1
P1LED0</td><td>Opu
Opu
Opu</td><td>Port 1 LED indicators[1] defined as follows:
LEDs turn on when low.
<table>
<tr><td></td><td colspan="2">Chip Global Control Register: CGCR bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2]</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. CGCR bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2]</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27.</td></tr>
<tr><td>6</td><td>NC</td><td>—</td><td>No connect</td></tr>
<tr><td>7</td><td>NC</td><td>—</td><td>No connect</td></tr>
<tr><td>8</td><td>NC</td><td>—</td><td>No connect</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital I/O V_{DD}</td></tr>
<tr><td>11</td><td>NC</td><td>—</td><td>No connect</td></tr>
<tr><td>12</td><td>PCLK</td><td>Ipd</td><td>PCI Bus Clock
This Clock provides the timing for all PCI bus phases. The rising edge defines the start of each phase. The clock maximum frequency is 33MHz.</td></tr>
<tr><td>13</td><td>NC</td><td>—</td><td>No connect</td></tr>
<tr><td>14</td><td>PMEN</td><td>Opu</td><td>Power Management Enable
Asserted low.
When asserted, this signal indicates that a Wake-on-LAN packet has been received in this Ethernet MAC chip.</td></tr>
<tr><td>15</td><td>NC</td><td>—</td><td>No connect</td></tr>
<tr><td>16</td><td>INTRN</td><td>Opd</td><td>Interrupt Request</td></tr>
</table>

Pin Number	Pin Name	Type	Pin Function
			Active Low signal to host CPU to request an interrupt when any one of the interrupt conditions occurs in the registers. This pin should be pull-up externally.
17	NC	—	No connect
18	NC	—	No connect
19	EECS	Opu	***EEPROM Chip Select*** This signal is used to select an external EEPROM device
20	NC	—	No connect
21	NC	—	No connect
22	NC	—	No connect
23	DGND	Gnd	Digital Ground
24	VDDCO	P	***1.2V Core Voltage Output. (Internal 1.2V LDO power supply output)*** This pin provides 1.2V power supply to all 1.2V power pin, VDDC, VDDA, VDDAP. It is recommended the pin should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.
25	NC	—	No connect
26	EEEN	Ipd	***EEPROM Enable*** EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	***Port 1 LED Indicator*** See the description in pins 3, 4, and 5.
28	EEDO	Opd	***EEPROM Data Out*** This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	***EEPROM Serial Clock*** 4μs serial clock to load configuration data from the serial EEPROM.
30	EEDI	Ipd	***EEPROM Data In*** This pin is connected to DO output of the serial EEPROM.
31	NC	—	No connect
32	VDDIO	P	3.3V digital I/O V_{DD}.
33	VDDIO	P	3.3V digital I/O V_{DD}.
34	DGND	Gnd	Digital ground
35	DGND	Gnd	Digital ground
36	PWRDN	Ipu	Full-chip power-down input. Active Low.
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD}
39	AGND	Gnd	Analog ground
40	NC	—	No connect
41	NC	—	No connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD}
44	NC	—	No connect

Pin Number	Pin Name	Type	Pin Function
45	RXP1	I/O	Physical receive (MDI) or transmit (MDIX)signal (+ differential)
46	RXM1	I/O	Physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	NC	—	No connect
53	NC	—	No connect
54	AGND	Gnd	Analog ground
55	NC	—	No connect
56	NC	—	No connect
57	VDDA	P	1.2 analog V_{DD}
58	AGND	Gnd	Analog ground
59	NC	—	No connect
60	NC	—	No connect
61	ISET	O	***Set physical transmit output current*** Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL
64	AGND	Gnd	Analog ground
65	X1	I	***25MHz crystal/oscillator clock connections*** Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is no connected. Note: Clock is □ 50ppm for both crystal and oscillator.
66	X2	O	
67	RSTN	Ipu	***Hardware Reset, Active Low*** RSTN will cause the KSZ8841-PMQL to reset all of its functional blocks. RSTN must be asserted for a minimum duration of 10 ms.
68	PAR	I/O	***PCI Parity*** Even parity computed for PAD[31:0] and CBE[3:0]N, master drives PAR for address and write data phase, target drives PAR for read data phase.
69	FRAMEN	I/O	***PCI Cycle Frame*** This signal is asserted low to indicate the beginning of the address phase of the bus transaction and de-asserted before the final transfer of the data phase of the transaction in a bus master mode. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
70	IRDYN	I/O	***PCI Initiator Ready*** As a bus master, this signal is asserted low to indicate valid data phases on PAD[31:0] during write data phases, indicates it is ready to accept data during read data phases. As a target, it'll monitor this IRDYN signal that indicates the master has put the data on the bus.
71	TRDYN	I/O	***PCI Target Ready*** As a bus target, this signal is asserted low to indicate valid data phases on PAD[31:0] during read data phases, indicates it is ready to accept data during write data phases. As a master, it will monitor this TRDYN signal that indicates the target is ready for data

Pin Number	Pin Name	Type	Pin Function
			during read/write operation.
72	STOPN	I/O	***PCI Stop*** This signal is asserted low by the target device to request the master device to stop the current transaction.
73	IDSEL	I/O	***PCI Initialization Device Select*** This signal is used to select the KSZ8841-PMQL during configuration read and write transactions. Active high.
74	DEVSELN	I/O	***PCI Device Select*** This signal is asserted low when it is selected as a target during a bus transaction. As a bus master, the KSZ8841-PMQL samples this signal to insure that a PCI target recognizes the destination address for the data transfer.
75	REQN	O	***PCI Bus Request*** The KSZ8841-PMQL will assert this signal low to request PCI bus master operation.
76	GNTN	I	***PCI Bus Grant*** This signal is asserted low to indicate to the KSZ8841-PMQL that it has been granted the PCI bus master operation.
77	PERRN	I/O	***PCI Parity Error*** The KSZ8841-PMQL as a master or target will assert this signal low to indicate a parity error on any incoming data. As a bus master, it will monitor this signal on all write operations.
78	DGND	Gnd	Digital ground
79	VDDIO	P	3.3V digital I/O V_{DD}
80	SERRN	O	***PCI System Error*** This system error signal is asserted low by the KSZ8841-PMQL. This signal is used to report address parity errors.
81	NC	—	No connect
82	NC	—	No connect
83	NC	—	No connect
84	NC	—	No connect
85	CBE3N	I/O	***Command and Byte Enable*** These signals are multiplexed on the same PCI pins. During the address phase, these lines define the bus command. During the data phase, these lines are used as Byte Enables, The Byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
86	CBE2N	I/O	
87	CBE1N	I/O	
88	CBE0N	I/O	
89	PAD31	I/O	***PCI Address / Data 31*** Address and data are multiplexed on the all of the PAD pins. The PAD pins carry the physical address during the first clock cycle of a transaction, and carry data during the subsequent clock cycles.
90	DGND	Gnd	Digital core ground
91	VDDC	P	1.2V digital core V_{DD}
92	VDDIO	P	3.3V digital I/O V_{DD}
93	PAD30	I/O	PCI Address / Data 30
94	PAD29	I/O	PCI Address / Data 29
95	PAD28	I/O	PCI Address / Data 28
96	PAD27	I/O	PCI Address / Data 27

Pin Number	Pin Name	Type	Pin Function
97	PAD26	I/O	PCI Address / Data 26
98	PAD25	I/O	PCI Address / Data 25
99	PAD24	I/O	PCI Address / Data 24
100	PAD23	I/O	PCI Address / Data 23
101	PAD22	I/O	PCI Address / Data 22
102	PAD21	I/O	PCI Address / Data 21
103	PAD20	I/O	PCI Address / Data 20
104	PAD19	I/O	PCI Address / Data 19
105	PAD18	I/O	PCI Address / Data 18
106	PAD17	I/O	PCI Address / Data 17
107	DGND	Gnd	Digital ground
108	VDDIO	P	3.3V digital I/O V_{DD}
109	PAD16	I/O	PCI Address / Data 16
110	PAD15	I/O	PCI Address / Data 15
111	PAD14	I/O	PCI Address / Data 14
112	PAD13	I/O	PCI Address / Data 13
113	PAD12	I/O	PCI Address / Data 12
114	PAD11	I/O	PCI Address / Data 11
115	PAD10	I/O	PCI Address / Data 10
116	PAD9	I/O	PCI Address / Data 9
117	PAD8	I/O	PCI Address / Data 8
118	PAD7	I/O	PCI Address / Data 7
119	PAD6	I/O	PCI Address / Data 6
120	PAD5	I/O	PCI Address / Data 5
121	PAD4	I/O	PCI Address / Data 4
122	PAD3	I/O	PCI Address / Data 3
123	DGND	Gnd	Digital ground
124	DGND	Gnd	Digital core ground
125	VDDIO	P	3.3V digital I/O V_{DD}
126	PAD2	I/O	PCI Address / Data 2
127	PAD1	I/O	PCI Address / Data 1
128	PAD0	I/O	PCI Address / Data 0

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipd = Input with internal pull-down.
   Ipu = Input with internal pull-up.
   Opd = Output with internal pull-down.
   Opu = Output with internal pull-up.

Functional Description

The KSZ8841-PMQL is a single chip Fast Ethernet MAC controller consisting of a 10/100 physical layer transceiver (PHY), a MAC, and a PCI interface unit that controls the KSZ8841-PMQL via a 32 bit/33MHz PCI processor interface.

The KSZ8841-PMQL is fully compliant to the IEEE802.3u standard.

PCI Bus Interface Unit

PCI Bus Interface

The PCI Bus Interface implements PCI v2.2 bus protocols and configuration space. The KSZ8841-PMQL supports bus master reads and writes to CPU memory, and CPU access to on-chip register space. When the CPU reads and writes the configuration registers of the KSZ8841-PMQL, it is as a slave. So the KSZ8841-PMQL can be either a PCI bus master or slave. The PCI Bus Interface is also responsible for managing the DMA interfaces and the host processors access. Arbitration logic within the PCI Bus Interface unit accepts bus requests from the TXDMA logic and RXDMA logic.

The PCI bus interface also manages interrupt generation for a host processor.

TXDMA Logic and TX Buffer Manager

The KSZ8841-PMQL supports a multi-frame, multi-fragment DMA gather process. Descriptors representing frames are built and linked in system memory by a host processor. The TXDMA logic is responsible for transferring the multi-fragment frame data from the host memory into the TX buffer.

The KSZ8841-PMQL uses 4K bytes of transmit data buffer between the TXDMA logic and transmit MAC. When the TXDMA logic determines there is enough space available in the TX buffer, the TXDMA logic will move any pending frame data into the TX buffer. The management mechanism depends on the transmit descriptor list.

RXDMA Logic and RX Buffer Manager

The KSZ8841-PMQL supports a multi-frame, multi-fragment DMA scatter process. Descriptors representing frames are built and linked in system memory by the host processor. The RXDMA logic is responsible for transferring the frame data from the RX buffer to the host memory.

The KSZ8841-PMQL uses 4K bytes of receive data buffer between the receive MAC and RXDMA logic. The management mechanism depends on the receive descriptor list.

Power Management

Power down

The KSZ8841-PMQL features a port power-down mode. To save power, the user can power-down this port that is not in use by setting bit 11 in either P1CR4 or P1MBCR register for this port. To bring the port back up, reset bit 11 in these registers.

In addition, there is a full chip power-down mode by pulled-down the PWRDN pin 36. When this pin is pulled-down, the entire chip powers down. Transitioning this pin from pull-down to pull-up results in a power up and chip reset.

Wake-on-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. In all of these instances, the network device is pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic.

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state (working).

A wake-up signal is caused by:

1. Detection of a change in the network link state
2. Receipt of a network wake-up frame
3. Receipt of a Magic Packet

Link Change

Link status wake events are useful to indicate a change in the network's availability, especially when this change may impact the level at which the system should re-enter the sleeping state. For example, a change from link off to link on may trigger the system to re-enter sleep at a higher level (D2 versus D3) so that wake frames can be detected. Conversely, a transition from link on to link off may trigger the system to re-enter sleep at a deeper level (D3 versus D2) since the network is not currently available.

Note: References to D0, D1, D2, and D3 are power management states defined in a similar fashion to the way they are defined for PCI. For more information, refer to the PCI specification at www.pcisig.com/specifications/conventional/pcipm1.2.pdf.

Wake-up Packet

Wake-up packets are certain types of packets with specific CRC values that a system recognizes as a 'wake up' frame. The KSZ8841-PMQL supports up to four users defined wake-up frames as below:

1. Wake-up frame 0 is defined in registers 0x0220-0x022A and is enabled by bit 0 in wakeup frame control register.
2. Wake-up frame 1 is defined in registers 0x0230-0x023A and is enabled by bit 1 in wakeup frame control register.
3. Wake-up frame 2 is defined in registers 0x0240-0x024A and is enabled by bit 2 in wakeup frame control register.
4. Wake-up frame 3 is defined in registers 0x0250-0x025A and is enabled by bit 3 in wakeup frame control register

Magic Packet

Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a LAN. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the LAN controller, and when the LAN controller receives a Magic Packet frame, it will alert the system to wake up.

Magic Packet is a standard feature integrated into the KSZ8841-PMQL. The chip implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ8841-PMQL has been put into Magic Packet Enable mode (WFCR[7]=1), it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the chip this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as Source Address (SA), Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

EXAMPLE

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE MISC: FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -11 22 33 44 55 66 -11 22 33 44 55 66 -11 22 33 44 55 66 -11 22 33 44 55 66 -11 22 33 44 55 66 -11 22 33 44 55 66 -11 22 33 44 55 66 -11 22 33 44 55 66 -11 22 33 44 55 66 - MISC -CRC.

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the controller (KSZ8841-PMQL) detects the data sequence, however, it then alerts the PC's power management circuitry (asserted the PMEN pin) to wake up the system.

Physical Layer Transceiver (PHY)

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the 25MHz 4-bit nibbles into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 1% 3.01KΩ resistor for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

PLL Clock Synthesizer (Recovery)

The internal PLL clock synthesizer generates 125MHz, 62.5MHz, 41.66MHz, and 25MHz clocks by setting the on-chip bus speed control register OBCR for KSZ8841-PMQL system timing. These internal clocks are generated from an external 25MHz crystal or oscillator.

Note: Default setting is 25MHz in OBCR register, recommends the software driver to set it to 125MHz for best performance.

Scrambler/De-scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

10BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with typical 2.4V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering

the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8841-PMQL decodes a data frame.

The receiver clock is maintained active during idle periods in between data reception.

MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8841-PMQL supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8841-PMQL device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

The IEEE 802.3u standard MDI and MDI-X definitions are:

MDI		MDI-X	
RJ45 Pins	**Signals**	**RJ45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 1. MDI/MDI-X Pin Definitions

Straight Cable

A straight cable connects an MDI device to an MDI-X device or an MDI-X device to an MDI device. The following diagram shows a typical straight cable connection between a network interface card (NIC) (MDI) and a switch (MDIX) or a hub (MDI-X).

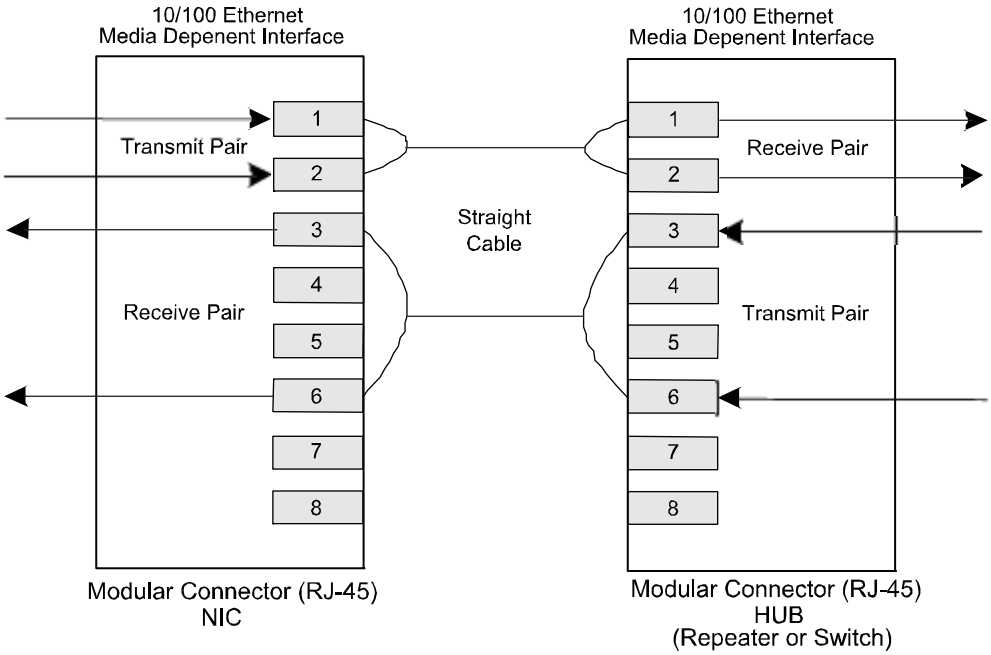

Figure 3. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

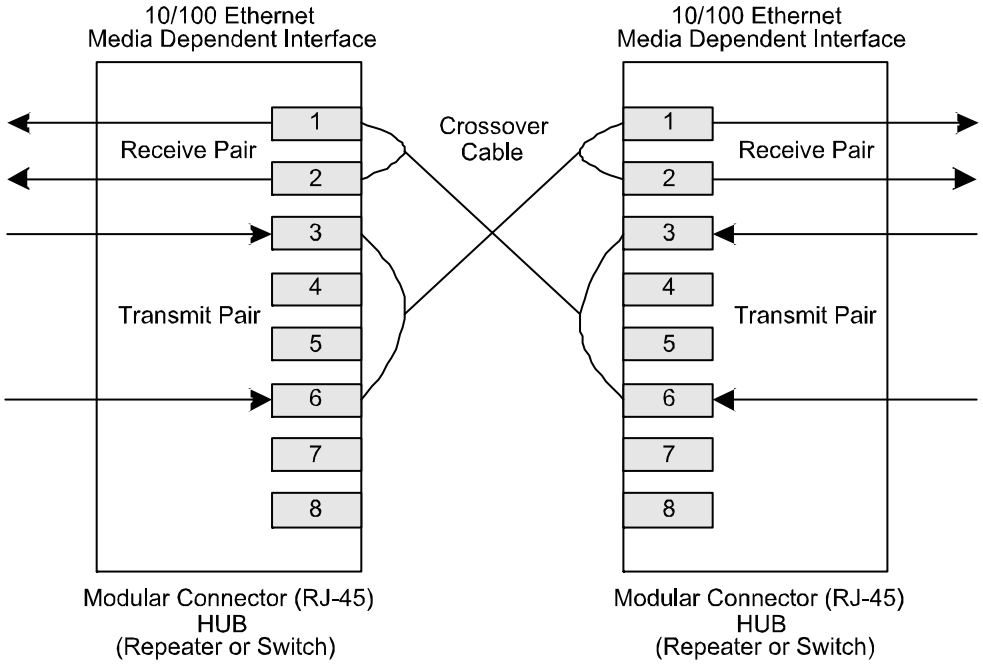

Figure 4. Typical Crossover Cable Connection

Auto Negotiation

The KSZ8841-PMQL conforms to the auto negotiation protocol as described by the 802.3 committee.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8841-PMQL is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link setup is shown in the following flow diagram (Figure 3).

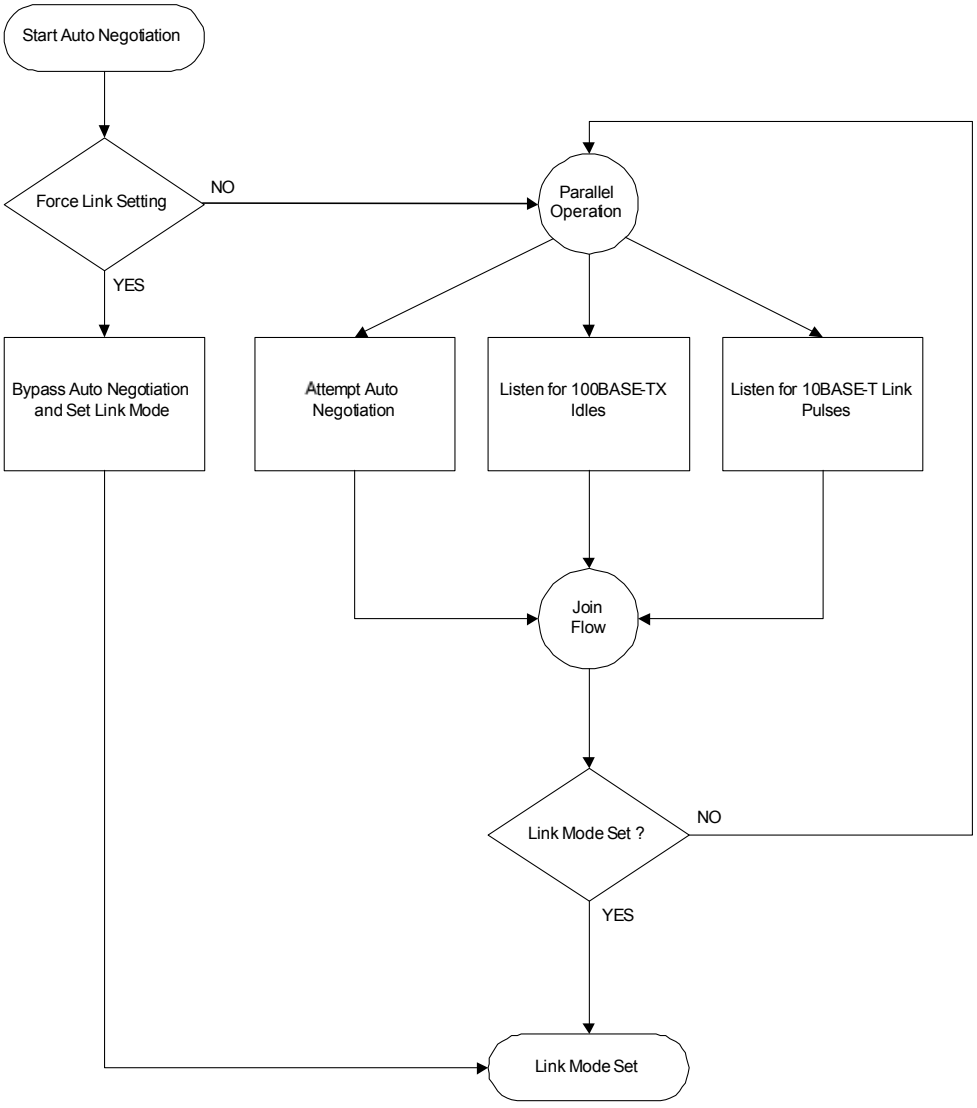

Figure 5. Auto Negotiation and Parallel Operation

LinkMD Cable Diagnostics

The KSZ8841-PMQL LinkMD uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of +/–2m.

Access

LinkMD is initiated by accessing register P1VCT, the LinkMD Control/Status register, in conjunction with register P1CR4, the 100BASE-TX PHY Controller register.

Usage

LinkMD can be run at any time. To use LinkMD, disable HP Auto-MDIX by writing a '1' to P1CR4[10] to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P1VCT[15], is set to '1' to start the test on this pair.

When bit P1VCT[15] returns to '0', the test is complete. The test result is returned in bits P1VCT[14-13] and the distance is returned in bits P1VCT[8-0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD failed

If P1VCT[14-13]=11 case, this indicates an invalid test, occurs when the KSZ8841-PMQL is unable to shut down the link partner. In this instance, the test is not run, since it would be impossible for the KSZ8841-PMQL to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance (in meters) can approximately be determined by the following formula:

Distance = P1VCT[8-0] x 0.4m

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

Media Access Control (MAC) and other

The KSZ8841-PMQL strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the minimum 96-bits time for IPG is between the two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bits time for IPG is from carrier sense to the next transmit packet.

Back-Off Algorithm

The KSZ8841-PMQL implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

Flow Control

The KSZ8841-PMQL supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8841-PMQL receives a pause control frame, the KSZ8841-PMQL will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8841-PMQL are transmitted.

On the transmit side, the KSZ8841-PMQL has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources.

The KSZ8841-PMQL issues a flow control frame (XON), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8841-PMQL sends out another flow control frame (XOFF) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

Half-Duplex Backpressure

A half-duplex backpressure option (non-IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as above in full-duplex mode. If backpressure is required, the KSZ8841-PMQL sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8841-PMQL discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further colliding and maintaining carrier sense to prevent packet reception.

The backpressure will take effect automatically in Auto-negotiation enable and half-duplex mode.

Clock Generator

The X1 and X2 pins are connected to a 25MHz crystal. X1 can also serve as the connector to the 3.3V 25MHz oscillator (as described in the pin description).

EEPROM Interface

An external serial EEPROM with a standard microwire bus interface is used for non-volatile storage of information such as the node address and subsystem ID.

As part of the initialization after system reset, the KSZ8841-PMQL reads the external EEPROM and places the data into certain host-accessible registers if the EEEN pin is pulled-up, the KSZ8841-PMQL performs an automatic read of the EEPROM word from 0x0 to 0x6 after the de-assertion of Reset. An EEPROM of 1KB(93C46) or 4KB(93C66) can be used based on application.

The EEPROM read/write function can also be performed by software reading and writing to the EEPCR register.

The KSZ8841-PMQL EEPROM format is given in Table 2.

WORD	15 8	7 0
0x0	Reserved	
0x1	MAC Address Byte 2	MAC Address Byte 1
0x2	MAC Address Byte 4	MAC Address Byte 3
0x3	MAC Address Byte 6	MAC Address Byte 5
0x4	Subsystem ID	
0x5	Subsystem Vendor ID	
0x6	ConfigParam	
0x7-0x3F	Not used by KSZ8841-PMQL (available for user to use)	

Table 2. KSZ8841-PMQL EEPROM Format

The ConfigParam in the EEPROM format is shown below.

Bit	Name	Description
15	NEW_CAP	***New Capabilities*** Indicates whether or not the KSZ8841-PMQL implements a list of new capabilities. When set, this bit indicates the presence of New capabilities. When reset, New capabilities are not implemented. The value of this bit is loaded to the New_cap bit in CFCS register.
14	NO_SRST	***No Soft Reset*** When this bit is set, indicates that KSZ8841-PMQL transitioning from D3_hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3_hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When this bit is clear, KSZ8841-PMQL performs an internal reset upon transitioning from D3_hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3_hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3_hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. This bit is loaded to bit 3 of CPMC register
13	Reserved	
12	PME_D2	***PME -Support D2*** When this bit is set, the KSZ8841-PMQL asserts PME event when the KSZ8841-PMQL is in D2 state and PME_EN is set. Otherwise, the KSZ8841-PMQL does not assert PME event when the KSZ8841-PMQL is in D2 state. This bit is loaded to bit 13 of PMCR register, and bit 29 of CCID register.
11	PME_D1	***PME Support D1*** When this bit is set, the K8841P asserts PME event when the K8841P is in D1 state and PME_EN is set. Otherwise, the KSZ8841-PMQL does not assert PME event when the KSZ8841-PMQL is in D1 state. This bit is loaded to bit 12 of PMCR register, and bit 28 of CCID register.
10	D2_SUP	***D2 support*** When this bit is set, the KSZ8841-PMQL supports D2 power state. This bit is loaded to bit 10 of PMCR register, and bit 26 of CCID register.
9	D1_SUP	***D1 support*** When this bit is set, the KSZ8841-PMQL supports D1 power state. This bit is loaded to bit 9 of PMCR register, and bit 25 of CCID register.
8 - 6	Reserved	
5	DSI	***Device Specific Initialization*** This bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. A “1” indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. This bit is loaded to bit 5 of PMCR register and bit 21 of CCID register.
4	Reserved	

Bit	Name	Description
3	PME_CK	***PME Clock*** When this bit is a “1”, it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a “0”, it indicates that no PCI clock is required for the function to generate PME#. This bit is loaded to bit 3 of PMCR register and bit 19 of CCID register.
2 - 0	PCI: PME_VER	PCI: Power Management PCI Version. These bits are loaded to bits [2-0] of the PMCR register and bits [18-16] of the CCID register.

Table 3. KSZ8841-PMQL ConfigParam in EEPROM Format

Loopback Support

The KSZ8841-PMQL provides loopback support for remote diagnostic failure. In loopback mode, the speed at the PHY port will be set to 100BASE-TX full-duplex mode. The KSZ8841-PMQL only supports Near-end (Remote) Loopback.

Near-end (Remote) loopback is conducted at PHY port 1 of the KSZ8841-PMQL. The loopback path starts at the PHY ports receive inputs (RXPx/RXMx), wraps around at the same PHY port’s PMD/PMA, and ends at the PHY ports transmit outputs (TXPx/TXMx).

Bit [1] of register P1PHYCTRL is used to enable near-end loopback for port 1. Alternatively, Bit [9] of register P1SCSLMD can also be used to enable near-end loopback. The port’s near-end loopback path is illustrated in the following Figure 4.

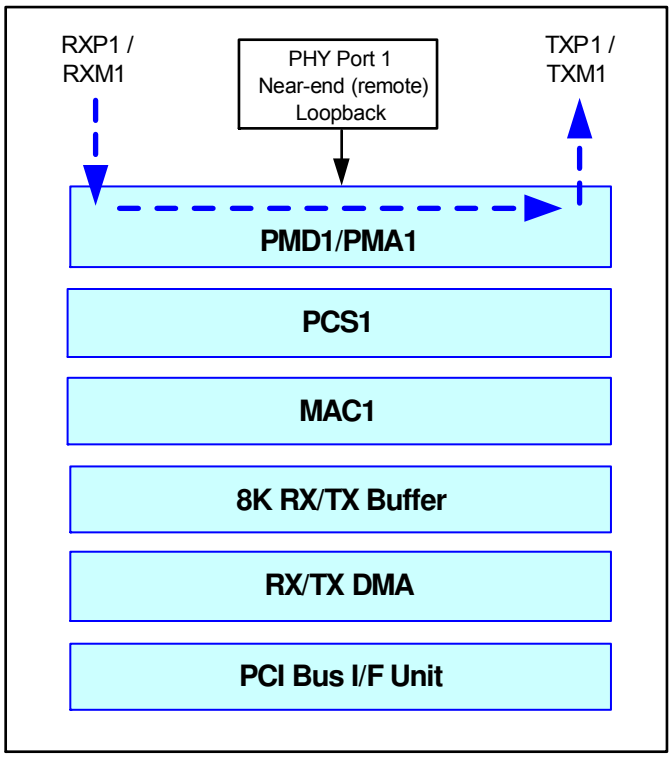

Figure 6. Port 1 Near-End (Remote) Loopback Path

Host Communication

The descriptor lists and data buffers, collectively called the host communication, manage the actions and status related to buffer management. Commands and signals that control the functional operation of the KSZ8841-PMQL are also described.

The KSZ8841-PMQL and the driver communicate through the two data structures: Command and status registers (CSRs) and Descriptor Lists and Data Buffers.

Note: All unused bits of the data structure in this section are reserved and should be written by the driver as zeros.

Host Communication Descriptor Lists and Data Buffers

The KSZ8841-PMQL transfers received data frames to the receive buffer in host memory and transmits data from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers.

There are two descriptor lists (one for receive and one for transmit) for the MAC DMA. The base address of each list is written in the TDLB register and in the RDLB register, respectively. A descriptor list is forward linked. The last descriptor may point back to the first entry to create a ring structure. Descriptors are chained by setting the *next address* to the next buffer in both receive and transmit descriptors.

The descriptor lists reside in the host *physical* memory address space. Each pointer points to one buffer and the second pointer points to the next descriptor. This enables the greatest flexibility for the host to chain any data buffers with discontinuous memory location. This eliminates processor-intensive tasks such as memory copying from the host to memory.

A data buffer contains either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; and buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. Data buffers reside in host physical memory space.

Receive Descriptors (RDES0-RDES3)

Receive descriptor and buffer addresses must be Word aligned. Each receive descriptor provides one frame buffer, one byte count field, and control and status bits.

The following table shows the RDES0 register bit fields.

Bit	Description
31	***OWN Own Bit*** When set, indicates that the descriptor is owned by the KSZ8841-PMQL. When reset, indicates that the descriptor is owned by the host. The KSZ8841-PMQL clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	***FS First Descriptor*** When set, indicates that this descriptor contains the first buffer of a frame. If the buffer size of the first buffer is 0, the next buffer contains the beginning of the frame.
29	***LS Last Descriptor*** When set, indicates that the buffer pointed by this descriptor is the last buffer of the frame.
28	***IPE IP Checksum Error*** When set, indicates that the received frame is an IP packet and its IP checksum field does not match. This bit is valid only when last descriptor is set.
27	***TCPE TCP Checksum Error*** When set, indicates that the received frame is a TCP/IP packet and its TCP checksum field does not match. This bit is valid only when last descriptor is set.

Bit	Description
26	***UDPE UDP Checksum Error*** When set, indicates that the received frame is an UDP/IP packet and its UDP checksum field does not match. This bit is valid only when last descriptor is set.
25	***ES Error Summary*** Indicates the logical OR of the following RDES0 bits: CRC error Frame too long Runt frame This bit is valid only when last descriptor is set.
24	***MF Multicast Frame*** When set, indicates that this frame has a multicast address. This bit is valid only when last descriptor is set.
23 - 20	***SPN Switch Engine Source Port Number*** This field indicates the source port where the packet originated. If bit 20 is set, it indicates the packet was received from port 1. If bit 21 is set, it indicates the packet was received from port 2. This field is valid only when the last descriptor is set. (Bits 23 and 22 are not used, but reserved for backward compatibility and future expansion.)
19	***RE Report on MII Error*** When set, indicates that a receive error in the physical layer was reported during the frame reception.
18	***TL Frame Too Long*** When set, indicates that the frame length exceeds the maximum size of 1518 bytes. This bit is valid only when last descriptor is set. Note: Frame too long is only a frame length indication and does not cause any frame truncation.
17	***RF Runt Frame*** When set, indicates that this frame was damaged by a collision or premature termination before the collision window has passed. Runt frames are passed on to the host only if the pass bad frame bit is set.
16	***CE CRC Error*** When set, indicates that a CRC error occurred on the received frame. This bit is valid only when last descriptor is set.
15	***FT Frame Type*** When set, indicates that the frame is an Ethernet-type frame (frame length field is greater than 1500 bytes). When clear, indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames. This bit is valid only when last descriptor is set.
14 - 11	Reserved
10 - 0	***FL Frame Length*** Indicates the length, in bytes, of the received frame, including the CRC. This field is valid only when last descriptor is set and descriptor error is reset.