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KSZ8842-16/32 MQL/MVL/MVLI/MBL

2-Port Ethernet Switch with Non-PCI Interface

Data Sheet Rev 1.9

General Description

The KSZ8842-series of 2-port switches includes PCI and non-PCI CPU interfaces, and are available in 8/16-bit and 32-bit bus designs (see **Ordering Information**). This datasheet describes the KSZ8842M-series of non-PCI CPU interface chips. For information on the KSZ8842 PCI CPU interface switches, refer to the KSZ8842P datasheet.

The KSZ8842M is the industry's first fully managed, 2-port switch with a non-PCI CPU interface. It is based on a proven, 4th generation, integrated Layer-2 switch, compliant with IEEE 802.3u standards. Also an industrial temperature grade version of the KSZ8842, the KSZ8842MVLI, can be ordered (see **Ordering Information**).

The KSZ8842M can be configured as a switch or as a low-latency (≤ 310 nanoseconds) repeater in latency-critical, embedded or industrial Ethernet applications. For industrial applications, the KSZ8842M can run in half-duplex mode regardless of the application.

LinkMD®

The KSZ8842M offers an extensive feature set that includes tag/port-based VLAN, quality of service (QoS) priority management, management information base (MIB) counters, and CPU control/data interfaces to effectively address Fast Ethernet applications.

The KSZ8842M contains: Two 10/100 transceivers with patented, mixed-signal, low-power technology, two media access control (MAC) units, a direct memory access (DMA) channel, a high-speed, non-blocking, switch fabric, a dedicated 1K entry forwarding table, and an on-chip frame buffer memory.

Functional Diagram

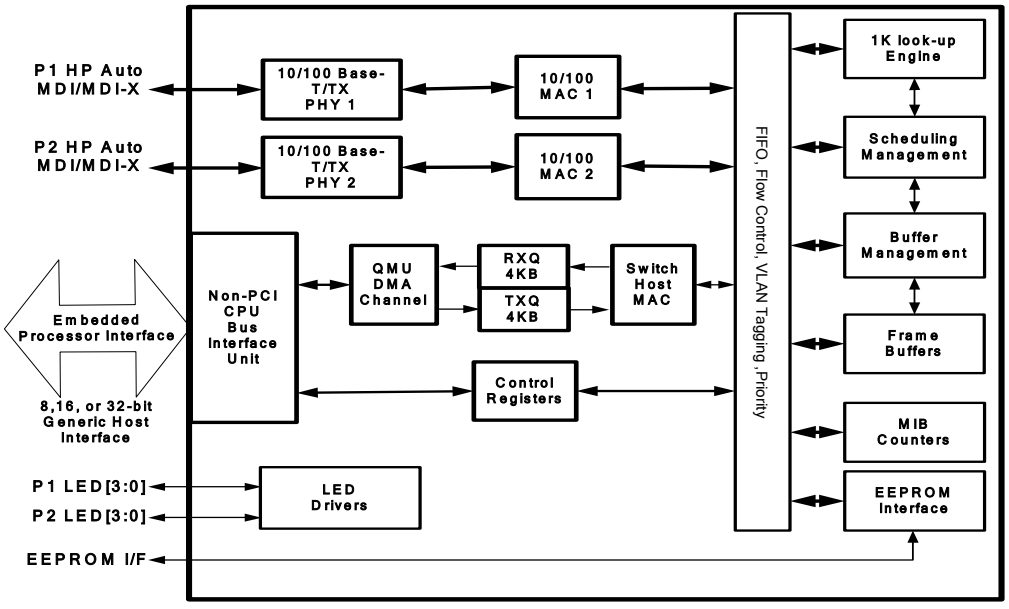

Figure 1. KSZ8842M Functional Diagram

Features

Switch Management

- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K entry forwarding table
- Fully compliant with IEEE 802.3u standards
- Full-duplex IEEE 802.3x flow control (Pause) with force mode option
- Half-duplex back pressure flow control

Advanced Switch Management

- IEEE 802.1Q VLAN support for up to 16 groups (full range of VLAN IDs)
- VLAN ID tag/untag options, on a per port basis
- IEEE 802.1p/Q tag insertion or removal on a per port basis (egress)
- Programmable rate limiting at the ingress and egress ports
- Broadcast storm protection
- IEEE 802.1d spanning tree protocol support
- MAC filtering function to filter or forward unknown unicast packets
- Direct forwarding mode enabling the processor to identify the ingress port and to specify the egress port
- Internet Group Management Protocol (IGMP) v1/v2 snooping support for multicast packet filtering
- IPV6 Multicast Listener Discovery (MLD) snooping support

Monitoring

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- MIB counters for fully compliant statistics gathering – 34 MIB counters per port
- Loopback modes for remote failure diagnostics

Comprehensive Register Access

- Control registers configurable on-the-fly (port-priority, 802.1p/d/Q)

QoS/CoS Packets Prioritization Support

- Per port, 802.1p and DiffServ-based
- Remapping of 802.1p priority field on a per port basis

Power Modes, Packaging, and Power Supplies

- Full-chip hardware power-down (register configuration not saved) allows low power dissipation
- Per port-based, software power-save on PHY (idle link detection, register configuration preserved)
- Single power supply: 3.3V
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C (see **Ordering Information**)
- Available in 128-pin PQFP and 100-ball LFBGA (optional package: 128-pin LQFP)
- Available in –16 version for 8/16-bit bus support and –32 version for 32-bit bus support (see **Ordering Information**).

Additional Features

In addition to offering all of the features of an integrated Layer-2 managed switch, the KSZ8842M offers:

- Repeater mode capabilities to allow for cut through in latency critical industrial Ethernet or embedded Ethernet applications
- Dynamic buffer memory scheme
  – Essential for applications such as Video over IP where image jitter is unacceptable
- 2-port switch with a flexible 8, 16, or 32-bit generic host processor interfaces
- Micrel LinkMD™ cable diagnostics to determine cable length, diagnose faulty cables, and determine distance-to-fault
- Hewlett Packard (HP) Auto-MDIX crossover with disable and enable options
- Four priority queues to handle voice, video, data, and control packets
- Ability to transmit and receive jumbo frame sizes up to 1916 bytes

Applications

- Video Distribution Systems
- High-end Cable, Satellite, and IP set-top boxes
- Video over IP
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Motion Control
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

Ordering Information

Part Number	Temperature Range	Package
KSZ8842-16MQL	0°C to 70°C	128-Pin PQFP
KSZ8842-32MQL	0°C to 70°C	128-Pin PQFP
KSZ8842-16MVL	0°C to 70°C	128-Pin LQFP
KSZ8842-32MVL	0°C to 70°C	128-Pin LQFP
KSZ8842-16MVLI	–40°C to +85°C	128-Pin LQFP
KSZ8842-32MVLI	–40°C to +85°C	128-Pin LQFP
KSZ8842-16MBL	0°C to 70°C	100-Ball LFBGA
KSZ8842-16MBLI	–40°C to +85°C	100-Ball LFBGA
KSZ8842-16MQL-Eval	Evaluation Board for the KSZ8842-16MQL	
KSZ8842-16MBL-Eval	Evaluation Board for the KSZ8842-16MBL	

Revision History

Revision	Date	Summary of Changes
1.0	06/30/05	First released Preliminary Information
1.1	07/19/05	Updated General Description, Functional Diagram, Pin Description and Features. Added this Revision History Table, Repeater mode and Loopback support sections.
1.2	08/08/05	Updated Tables, timing and body text.
1.3	10/04/05	Updated Power Saving bit description in P1/2PHYCTRL and P1/2SCSLMD registers
1.4	11/01/05	Updated Figure 16/17/18 Asynchronous Timing and Table 24/25/26 parameters, PQFP package information
1.5	03/20/06	Added QMU RX Flow Control High Watermark QRFCR register and updated body text
1.6	11/30/06	Improve the ARDY low time in read cycle to 40 ns and in write cycle to 50 ns during QMU data register access
1.7	05/24/07	Updated ordering information and thermal data
1.8	08/09/07	Add 100 ohm resistor between 1.2V and 3.3V in Appendix
1.9	10/22/07	Add KSZ8842-16MBL 100-Ball BGA package information

Content

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List of Tables

Pin Configuration for KSZ8842-16 Switches (8/16-Bit)

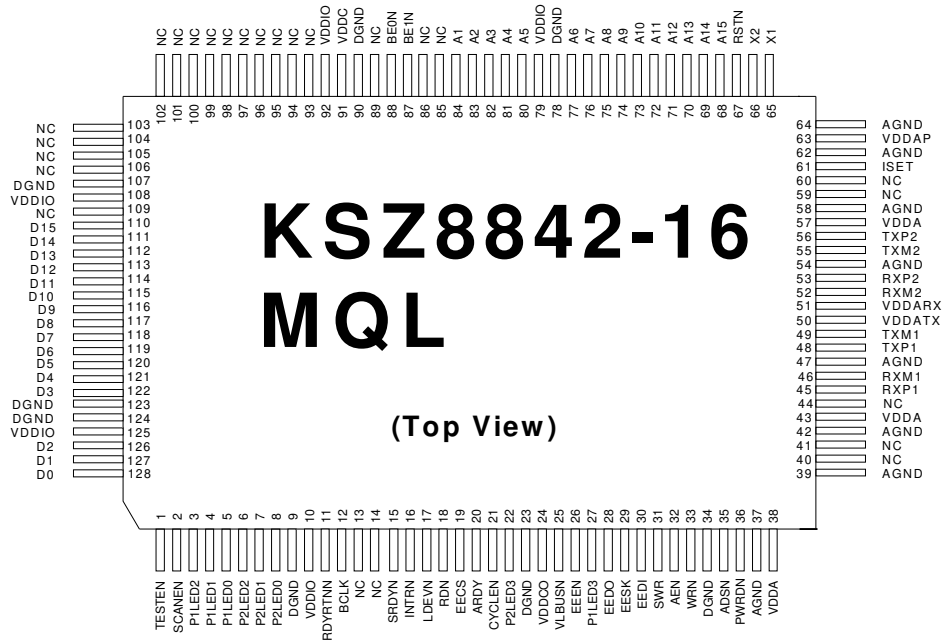

Figure 2. Standard – KSZ8842-16 MQL 128-Pin PQFP (Top View)

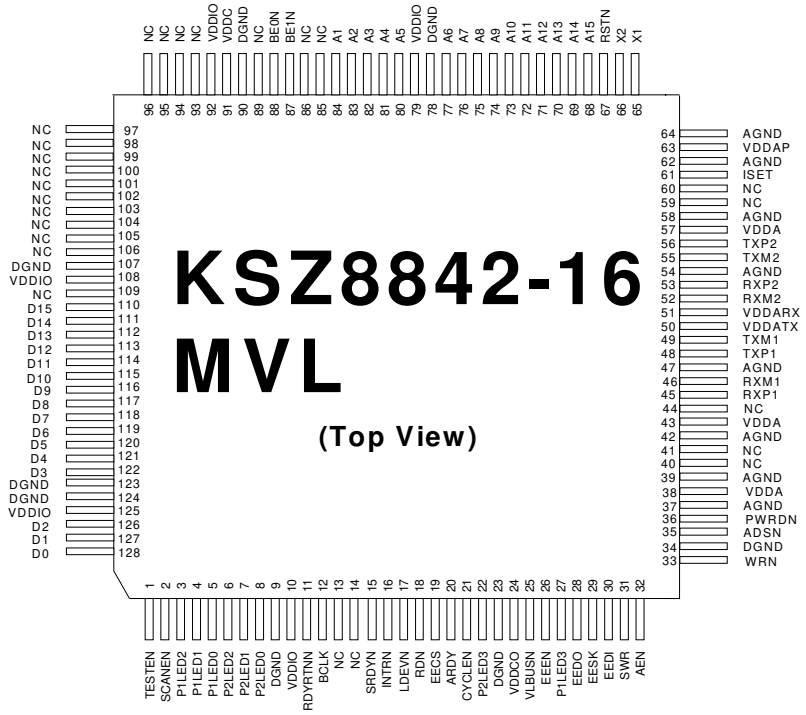

Figure 3. Option – KSZ8842-16 MVL 128-Pin LQFP (Top View)

Ball Configuration for KSZ8842-16 Switches (8/16-Bit)

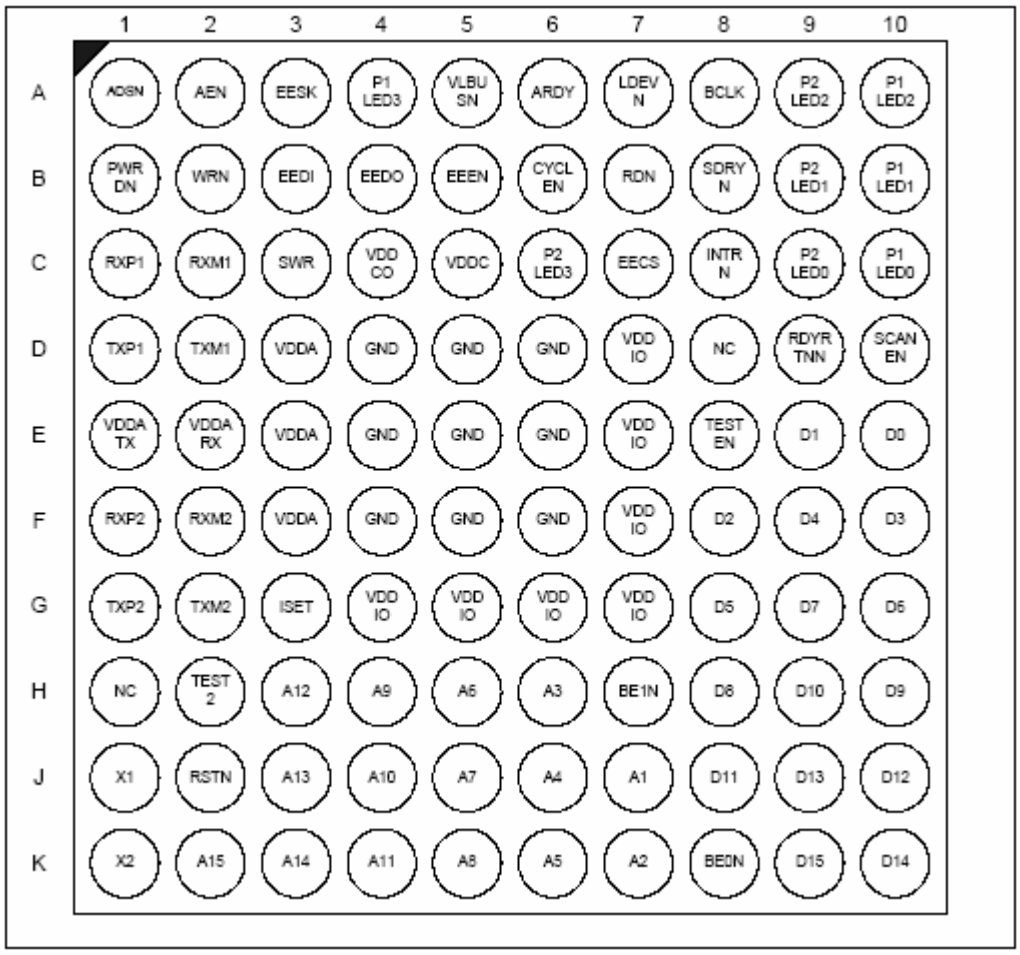

Figure 4. KSZ8842-16MBL 100-Ball LFBGA (Top View)

Pin Description for KSZ8842-16 Switches (8/16-Bit)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>3</td><td>P1LED2</td><td>Opu</td><td rowspan="8">Port 1 and Port 2 LED indicators[1] defined as follows:
<table>
<tr><th></th><th colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1]</th></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><th></th><th colspan="2">Reg. SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[1,0]</th><th>[1,1]</th></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27. P2LED3 is pin 22.
Port 1 and Port 2 LED indicators[3] for Repeater mode defined as follows:
<table>
<tr><th></th><th colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1] [1,0] [1,1]</th></tr>
<tr><td>P1LED3, P2LED3</td><td>RPT_COL, RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2, P2LED2</td><td>RPT_Link3/RX, RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1, P2LED1</td><td>RPT_Link2/RX, RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0, P2LED0</td><td>RPT_Link1/RX, RPT_ERR1</td><td>—</td></tr>
</table>
Note 3: RPT_COL = Blink; RPT_Link3/RX (Host port) = On/Blink;
RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink;
RPT_ACT = on if any activity, RPT_ERR3/2/1 = RX error on port 3, 2, or 1.</td></tr>
<tr><td>4</td><td>P1LED1</td><td>Opu</td></tr>
<tr><td>5</td><td>P1LED0</td><td>Opu</td></tr>
<tr><td>6</td><td>P2LED2</td><td>Opu</td></tr>
<tr><td>7</td><td>P2LED1</td><td>Opu</td></tr>
<tr><td>8</td><td>P2LED0</td><td>Opu</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.
For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
</table>

Pin Number	Pin Name	Type	Pin Function
12	BCLK	Ipd	Bus Interface Clock Local bus clock for synchronous bus systems. Maximum frequency is 50MHz. This pin should be tied Low or unconnected if it is in asynchronous mode.
13	NC	Ipu	No connect.
14	NC	Opu	No connect.
15	SRDYN	Opu	Synchronous Ready Not Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses. For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK. For burst mode (32-bit interface only), the KSZ8842M drives this pin low to signal wait states.
16	INTRN	Opd	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor.
17	LDEVN	Opd	Local Device Not Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8842M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
19	EECS	Opu	EEPROM Chip Select
20	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. This pin need an external 4.7K pull-up resistor.
21	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles.
22	P2LED3	Opd	Port 2 LED indicator See the description in pins 6, 7, and 8.
23	DGND	Gnd	Digital IO ground
24	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins. Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite bead and capacitors). It is recommended this pin should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application.
25	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 8-bit or 16-bit asynchronous mode or EISA-like burst mode.
26	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.

Pin Number	Pin Name	Type	Pin Function
27	P1LED3	Opd	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	Opd	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	EEPROM Serial Clock A 4µs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.
30	EEDI	Ipd	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin can be pull-down for 8-bit bus mode, pull-up for 16-bit bus mode or don't care for 32-bit bus mode when EEEN is pull-down (without EEPROM).
31	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
32	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
33	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
34	DGND	Gnd	Digital IO ground
35	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
36	PWRDN	Ipu	Full-chip power-down. Low = Power down; High or floating = Normal operation.
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
39	AGND	Gnd	Analog ground
40	NC	—	No connect
41	NC	—	No connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
44	NC	—	No connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (- differential)
53	RXP2	I/O	Port 2 physical receive (MDI)or transmit (MDIX) signal (+ differential)
54	AGND	Gnd	Analog ground

Pin Number	Pin Name	Type	Pin Function
55	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (- differential)
56	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential)
57	VDDA	P	1.2 analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
58	AGND	Gnd	Analog ground
59	NC	Ipu	No connect
60	NC	Ipu	No connect
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
64	AGND	Gnd	Analog ground
65	X1	I	25MHz crystal or oscillator clock connection.
66	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ± 50ppm for either crystal or oscillator.
67	RSTN	Ipu	Hardware reset pin (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
68	A15	I	Address 15
69	A14	I	Address 14
70	A13	I	Address 13
71	A12	I	Address 12
72	A11	I	Address 11
73	A10	I	Address 10
74	A9	I	Address 9
75	A8	I	Address 8
76	A7	I	Address 7
77	A6	I	Address 6
78	DGND	Gnd	Digital IO ground
79	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
80	A5	I	Address 5
81	A4	I	Address 4
82	A3	I	Address 3
83	A2	I	Address 2
84	A1	I	Address 1
85	NC	I	No Connect
86	NC	I	No Connect
87	BE1N	I	Byte Enable 1 Not, Active low for Data byte 1 enable (don't care in 8-bit bus mode).
88	BE0N	I	Byte Enable 0 Not, Active low for Data byte 0 enable (there is an internal inverter enabled and connected to the BE1N for 8-bit bus mode).
89	NC	I	No Connect
90	DGND	Gnd	Digital core ground
91	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.

Pin Number	Pin Name	Type	Pin Function
92	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
93	NC	I	No Connect
94	NC	I	No Connect
95	NC	I	No Connect
96	NC	I	No Connect
97	NC	I	No Connect
98	NC	I	No Connect
99	NC	I	No Connect
100	NC	I	No Connect
101	NC	I	No Connect
102	NC	I	No Connect
103	NC	I	No Connect
104	NC	I	No Connect
105	NC	I	No Connect
106	NC	I	No Connect
107	DGND	Gnd	Digital IO ground
108	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
109	NC	I	No Connect
110	D15	I/O	Data 15
111	D14	I/O	Data 14
112	D13	I/O	Data 13
113	D12	I/O	Data 12
114	D11	I/O	Data 11
115	D10	I/O	Data 10
116	D9	I/O	Data 9
117	D8	I/O	Data 8
118	D7	I/O	Data 7
119	D6	I/O	Data 6
120	D5	I/O	Data 5
121	D4	I/O	Data 4
122	D3	I/O	Data 3
123	DGND	Gnd	Digital IO ground
124	DGND	Gnd	Digital core ground
125	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
126	D2	I/O	Data 2
127	D1	I/O	Data 1
128	D0	I/O	Data 0

Legend:

P = Power supply
I/O = Bi-directional
Ipd = Input with internal pull-down
Ipu = Input with internal pull-up
Opd = Output with internal pull-down
Opu = Output with internal pull-up
Gnd = Ground
I = Input O = Output

Ball Description for KSZ8842-16 Switches (8/16-Bit)

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type</th><th>Ball Function</th></tr>
<tr><td>E8</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this ball to ground.</td></tr>
<tr><td>D10</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this ball to ground.</td></tr>
<tr><td>A10
B10
C10</td><td>P1LED2
P1LED1
P1LED0</td><td>Opu</td><td>Port 1 and Port 2 LED indicators[1] defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is ball A4. P2LED3 is ball C6.
Port 1 and Port 2 LED indicators[3] for Repeater mode defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1] [1,0] [1,1]</td></tr>
<tr><td>P1LED3, P2LED3</td><td>RPT_COL, RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2, P2LED2</td><td>RPT_Link3/RX, RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1, P2LED1</td><td>RPT_Link2/RX, RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0, P2LED0</td><td>RPT_Link1/RX, RPT_ERR1</td><td>—</td></tr>
</table>
Note 3: RPT_COL = Blink; RPT_Link3/RX (Host port) = On/Blink;
RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink;
RPT_ACT = on if any activity, RPT_ERR3/2/1 = RX error on port 3, 2, or 1.</td></tr>
<tr><td>A9
B9
C9</td><td>P2LED2
P2LED1
P2LED0</td><td>Opu</td><td></td></tr>
<tr><td>D9</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this ball, assert this ball.
For burst mode (32-bit interface only): Host drives this ball low to signal waiting states.</td></tr>
<tr><td>A8</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock
Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.</td></tr>
</table>

Ball Number	Ball Name	Type	Ball Function
			This ball should be tied Low or unconnected if it is in asynchronous mode.
B8	SRDYN	Opu	Synchronous Ready Not Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses. For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK. For burst mode (32-bit interface only), the KSZ8842M drives this ball low to signal wait states.
C8	INTRN	Opd	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set, this ball need an external 4.7K pull-up resistor.
A7	LDEVN	Opd	Local Device Not Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8842M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
B7	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
C7	EECS	Opu	EEPROM Chip Select
A6	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. This ball needs an external 4.7K pull-up resistor.
B6	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this ball follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this ball stays High for read cycles and Low for write cycles.
C6	P2LED3	Opd	Port 2 LED indicator See the description in balls A9, B9, and C9.
A5	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 8-bit or 16-bit asynchronous mode or EISA-like burst mode.
B5	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this ball is pull-up. EEPROM is disabled when this ball is pull-down or no connect.
A4	P1LED3	Opd	Port 1 LED indicator See the description in balls A10, B10, and C10.
B4	EEDO	Opd	EEPROM Data Out This ball is connected to DI input of the serial EEPROM.
A3	EESK	Opd	EEPROM Serial Clock A 4μs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.
B3	EEDI	Ipd	EEPROM Data In This ball is connected to DO output of the serial EEPROM when EEEN is pull-up.

Ball Number	Ball Name	Type	Ball Function
			This ball can be pull-down for 8-bit bus mode, pull-up for 16-bit bus mode or don't care for 32-bit bus mode when EEEN is pull-down (without EEPROM).
C3	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
A2	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
B2	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
A1	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
B1	PWRDN	Ipu	Full-chip power-down. Low = Power down; High or floating = Normal operation.
C1	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
C2	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
D1	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
D2	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
F2	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (- differential)
F1	RXP2	I/O	Port 2 physical receive (MDI)or transmit (MDIX) signal (+ differential)
G2	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (- differential)
G1	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential)
H2	TEST2	Ipu	Test input 2 For normal operation, left this ball open.
G3	ISET	O	Set physical transmits output current. Pull-down this ball with a 3.01K 1% resistor to ground.
J1	X1	I	25MHz crystal or oscillator clock connection.
K1	X2	O	Balls (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ± 50ppm for either crystal or oscillator.
J2	RSTN	Ipu	Hardware reset ball (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
K2	A15	I	Address 15
K3	A14	I	Address 14
J3	A13	I	Address 13
H3	A12	I	Address 12
K4	A11	I	Address 11
J4	A10	I	Address 10
H4	A9	I	Address 9
K5	A8	I	Address 8
J5	A7	I	Address 7
H5	A6	I	Address 6
K6	A5	I	Address 5
J6	A4	I	Address 4
H6	A3	I	Address 3
K7	A2	I	Address 2

Ball Number	Ball Name	Type	Ball Function
J7	A1	I	Address 1
H7	BE1N	I	Byte Enable 1 Not, Active low for Data byte 1 enable (don't care in 8-bit bus mode).
K8	BE0N	I	Byte Enable 0 Not, Active low for Data byte 0 enable (there is an internal inverter enabled and connected to the BE1N for 8-bit bus mode).
K9	D15	I/O	Data 15
K10	D14	I/O	Data 14
J9	D13	I/O	Data 13
J10	D12	I/O	Data 12
J8	D11	I/O	Data 11
H9	D10	I/O	Data 10
H10	D9	I/O	Data 9
H8	D8	I/O	Data 8
G9	D7	I/O	Data 7
G10	D6	I/O	Data 6
G8	D5	I/O	Data 5
F9	D4	I/O	Data 4
F10	D3	I/O	Data 3
F8	D2	I/O	Data 2
E9	D1	I/O	Data 1
E10	D0	I/O	Data 0
C4	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output ball provides power to all VDDC/VDDA balls. Note: Internally generated power voltage. Do not connect an external power supply to this ball. This ball is used for connecting external filter (Ferrite bead and capacitors). It is recommended this ball should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application.
C5	VDDC	P	1.2V digital core V_{DD} input power supply from VDDCO (ball C4) through external Ferrite bead and capacitor.
D3, E3, F3	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (ball C4) through external Ferrite bead and capacitor.
E1	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
E2	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
D7, E7, F7, G4, G5, G6, G7	VDDIO	P	3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
D4, D5, D6, E4, E5, E6, F4, F5, F6	GND	Gnd	All digital and analog grounds
D8, H1	NC	I	No Connect

Pin Configuration for KSZ8842-32 Switches (32-Bit)

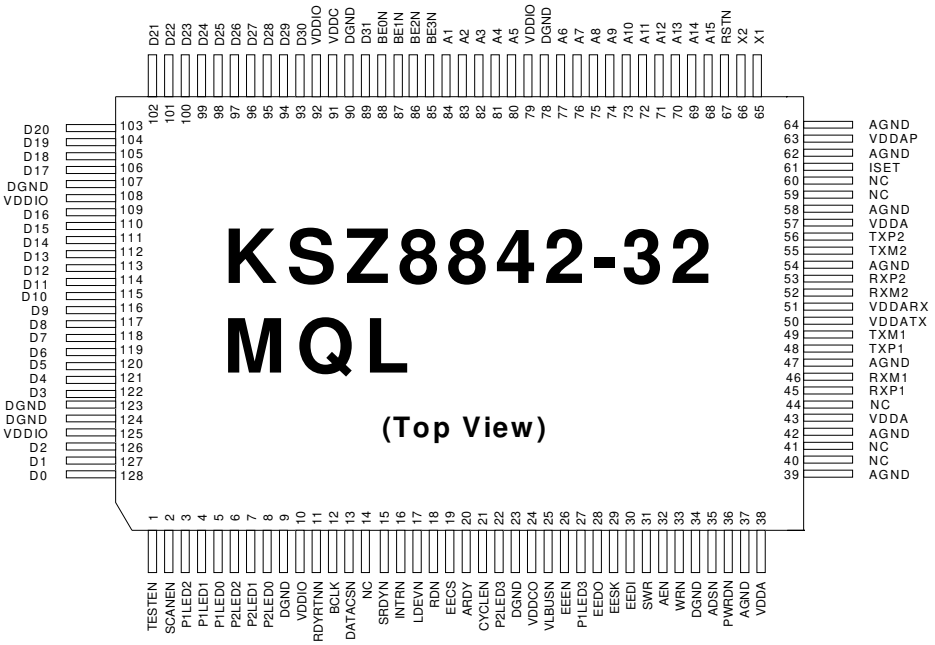

Figure 5. Standard – KSZ8842-32 MQL 128-Pin PQFP (Top View)

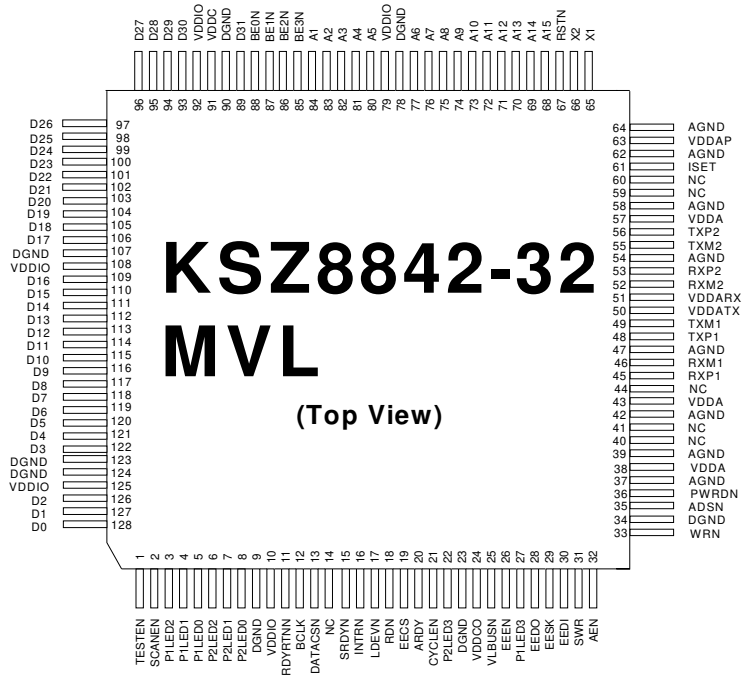

Figure 6. Option – KSZ8842-32 MVL 128-Pin LQFP (Top View)

Pin Description for KSZ8842-32 Switches (32-Bit)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>3</td><td>P1LED2</td><td>Opu</td><td rowspan="8">Port 1 and Port 2 LED indicators[1] defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27. P2LED3 is pin 22.
Port 1 and Port 2 LED indicators[3] for Repeater mode defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1] [1,0] [1,1]</td></tr>
<tr><td>P1LED3; P2LED3</td><td>RPT_COL; RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2; P2LED2</td><td>RPT_Link3/RX; RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1; P2LED1</td><td>RPT_Link2/RX; RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0; P2LED0</td><td>RPT_Link1/RX; RPT_ERR1</td><td>—</td></tr>
</table>
Note 3: RPT_COL = Blink; RPT_Link3/RX (Host port) = On/Blink;
RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink;
RPT_ACT = on if any activity, RPT_ERR3/2/1 = RX error on port 3, 2, or 1.</td></tr>
<tr><td>4</td><td>P1LED1</td><td>Opu</td></tr>
<tr><td>5</td><td>P1LED0</td><td>Opu</td></tr>
<tr><td>6</td><td>P2LED2</td><td>Opu</td></tr>
<tr><td>7</td><td>P2LED1</td><td>Opu</td></tr>
<tr><td>8</td><td>P2LED0</td><td>Opu</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not
For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.
For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
</table>

Pin Number	Pin Name	Type	Pin Function
12	BCLK	Ipd	Bus Interface Clock Local bus clock for synchronous bus systems. Maximum frequency is 50MHz. This pin should be tied Low or unconnected if it is in asynchronous mode.
13	DATACSN	Ipu	DATA Chip Select Not (For KSZ8842-32 Mode only) Chip select signal for QMU data register (QDRH, QDRL), active Low. When DATACSN is Low, the data path can be accessed regardless of the value of AEN, A15-A1, and the content of the BANK select register.
14	NC	Opu	No connect.
15	SRDYN	Opu	Synchronous Ready Not Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses. For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK. For burst mode (32-bit interface only), the KSZ8842M drives this pin low to signal wait states.
16	INTRN	Opd	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor.
17	LDEVN	Opd	Local Device Not Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8842M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	Ipd	Read Strobe Not Asynchronous read strobe, active Low.
19	EECS	Opu	EEPROM Chip Select
20	ARDY	Opd	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. this pin need an external 4.7K pull-up resistor.
21	CYCLEN	Ipd	Cycle Not For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle. For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles.
22	P2LED3	Opd	Port 2 LED indicator. See the description in pins 6, 7, and 8.
23	DGND	Gnd	Digital IO ground
24	VDDCO	P	1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins. Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite Bead and capacitors). It is recommended this pin should be connected to 3.3V power rail by a 100 ohm resistor for the internal LDO application.
25	VLBUSN	Ipd	VLBus-like Mode Pull-down or float: Bus interface is configured for synchronous mode. Pull-up: Bus interface is configured for 32-bit asynchronous mode or EISA-like burst mode.

Pin Number	Pin Name	Type	Pin Function
26	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	Opd	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	EEPROM Serial Clock A 4µs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM.
30	EEDI	Ipd	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin can be pull-down for 8-bit bus mode, pull-up for 16-bit bus mode or don't care for 32-bit bus mode when EEEN is pull-down (without EEPROM).
31	SWR	Ipd	Synchronous Write/Read Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low.
32	AEN	Ipu	Address Enable Address qualifier for the address decoding, active Low.
33	WRN	Ipd	Write Strobe Not Asynchronous write strobe, active Low.
34	DGND	Gnd	Digital IO ground
35	ADSN	Ipd	Address Strobe Not For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN.
36	PWRDN	Ipu	Full-chip power-down. Low = Power down; High or floating = Normal operation.
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
39	AGND	Gnd	Analog ground
40	NC	—	No connect
41	NC	—	No connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD} input power supply from VDDCO (pin24) through external Ferrite bead and capacitor.
44	NC	—	No connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (- differential)
53	RXP2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential)