Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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KSZ8842-PMQL/PMBL

2-Port Ethernet Switch with PCI Interface

Rev.1.5

General Description

The KSZ8842-series of 2-port switches includes PCI and non-PCI CPU interfaces. This datasheet describes the KSZ8842-PMQL/PMBL PCI CPU interface chips. KSZ8842-PMQL is PQFP package chip, KSZ8842-PMBL is LFBGA package chip. For information on the KSZ8842-MQL/MBL CPU non-PCI interface switches, refer to the KSZ8842-MQL/MBL datasheet.

The KSZ8842-PMQL/PMBL is the industry's first fully managed 2-port switch with a 32 bit/33MHz PCI processor interface. It is a proven, 4th generation, integrated Layer 2 switch that is compliant with the IEEE 802.3u standard. An industrial temperature grade version of the KSZ8842-PMQL/PMBL, also can be ordered the KSZ8842-PMQLI/PMBL AM.

The KSZ8842-PMQL/PMBL can be configured as a switch or as a low-latency (<310 nanoseconds) repeater in latency-critical, embedded or industrial Ethernet applications. For industrial automation applications, the KSZ8842-PMQL/PMBL can run in half-duplex mode regardless of the application. The KSZ8842-PMQL/PMBL offers an extensive feature set that includes tag/port-based VLAN, quality of service (QoS) priority management, management information base (MIB) counters, and CPU control/data interfaces to effectively address Fast Ethernet applications.

LinkMD®

The KSZ8842-PMQL/PMBL contains two 10/100 transceivers with patented, mixed-signal, low-power technology three media access control (MAC) units, a direct memory access (DMA) channel, a high-speed, non-blocking, switch fabric, a dedicated 1K entry forwarding table, and an on-chip frame buffer memory.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Diagram

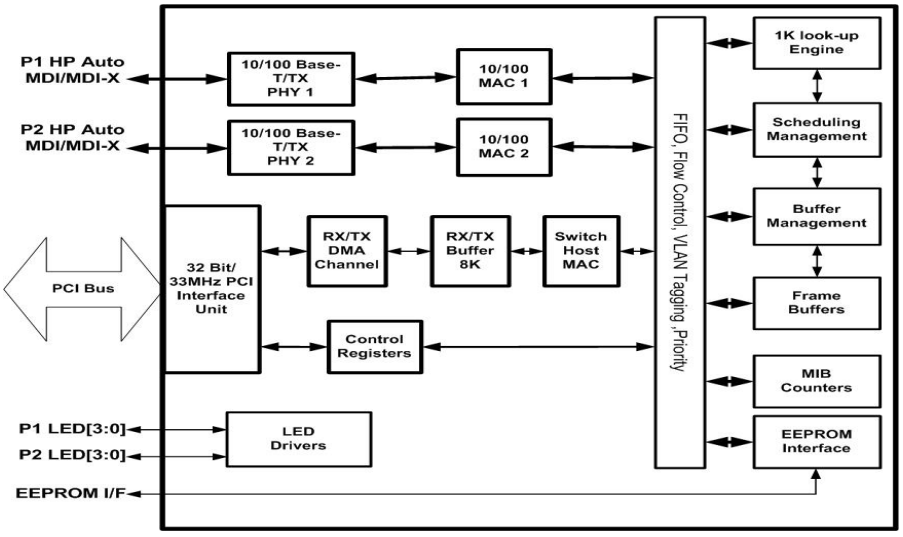

Figure 1. KSZ8842-PMQL/PMBL Functional Diagram

Features

Switch Management

- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K entry MAC Address look-up engine and a store-and-forward architecture
- Fully compliant with IEEE802.3u standards
- Full-duplex IEEE 802.3x flow control (Pause) with force mode option
- Half-duplex back pressure flow control

Advanced Switch Management

- IEEE 802.1Q VLAN support for up to 16 groups (full-range of VLAN IDs)
- VLAN ID tag/untag options, per port basis
- IEEE 802.1p/Q tag insertion or removal on a per-port basis (egress)
- Programmable rate limiting at the ingress and egress port
- Broadcast storm protection
- IEEE 802.1d spanning tree protocol support
- MAC filtering function to filter unicast packets
- Unknown MAC address forwarding function
- Direct forwarding mode enabling the processor to identify the ingress port and to specify the egress port
- IGMP v1/v2 snooping support for multicast packet filtering
- IPV6 Multicast Listener Discovery (MLD) snooping support

Monitoring

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- Management information base (MIB) counters for fully compliant statistics gathering: 32 MIB counters per port
- Loop back modes for remote failure diagnostics

Comprehensive Register Access

- There are three kinds of register groups:
- The PCI configuration registers are used to initialize and configure the PCI interface
- The PCI control/status registers are used to communicate between the host and KSZ8842-PMQL/PMBL
- Switch registers are used to support transceiver control and status. They are configurable on-the-fly (port-priority, 802.1p/d/Q, etc.)

QoS/CoS Packets Prioritization Support

- Per port, 802.1p and DiffServ based
- Re-mapping of 802.1p priority field on a per port basis

Power Modes, Packaging, and Power Supplies

- Full-chip hardware power-down (register configuration not saved) provides for low power dissipation
- Per port-based software power-save on PHY (idle link detection, register configuration preserved)
- Single power supply: 3.3V
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 128-pin PQFP and 100-ball LFBGA

Additional Features

In addition to offering all of the features of an integrated Layer-2 managed switch, the KSZ8842-PMQL/PMBL offers:

- Repeater mode capabilities to allow for cut through in latency critical Industrial Ethernet or Embedded Ethernet applications
- Dynamic buffer memory scheme essential for applications such as Video over IP where image jitter is unacceptable
- 2-Port switch with a 32-bit/33MHz PCI processor interface.
- Micrel LinkMD® cable diagnostics to determine cable length, diagnose faulty cables, and determine distance-to-fault
- Hewlett Packard (HP) Auto MDI-X crossover with disable and enable options
- Four priority queues to handle voice, video, data, and control packets
- Ability to transmit and receive jumbo frame sizes up to 1916 bytes

Applications

- Video Distribution Systems
- High-end Cable, Satellite, and IP set-top boxes
- Video over IP
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Motion Control
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

Ordering Information

Part Number	Operation Temp. Range	Package
KSZ8842-PMQL	0°C to 70°C	128-Pin PQFP
KSZ8842-PMQLI **(Industrial grade)**	-40°C to +85°C	128-Pin PQFP
KSZ8842-PMBL	0°C to 70°C	100-Ball LFBGA
KSZ8842-PMBL AM **(Industrial/Automotive grade)**	-40°C to +85°C	100-Ball LFBGA

Revision History

Revision	Date	Summary of Changes
1.0	09/29/05	Data sheet created.
1.1	01/13/06	Package information updated.
1.2	01/16/07	Update support transformer, table and other.
1.3	04/17/07	Add the base address and range for host MIB, change description for soft reset and other.
1.4	06/01/07	Add the package thermal information in the operating ratings.
1.5	10/02/07	Add the KSZ8842-PMBL BGA device information.

Contents

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Pin Configuration

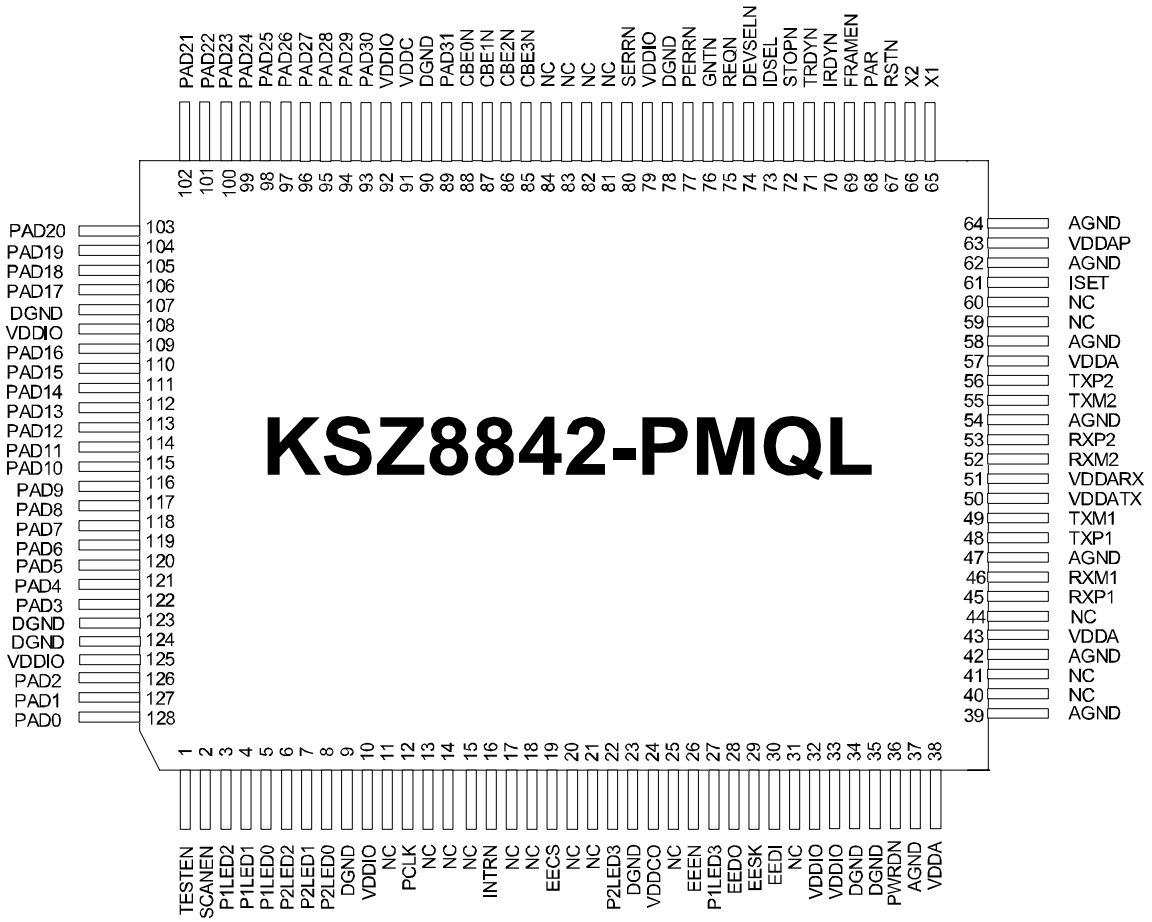

Figure 2. KSZ8842-PMQL 128-Pin PQFP (Top View)

Balls Configuration

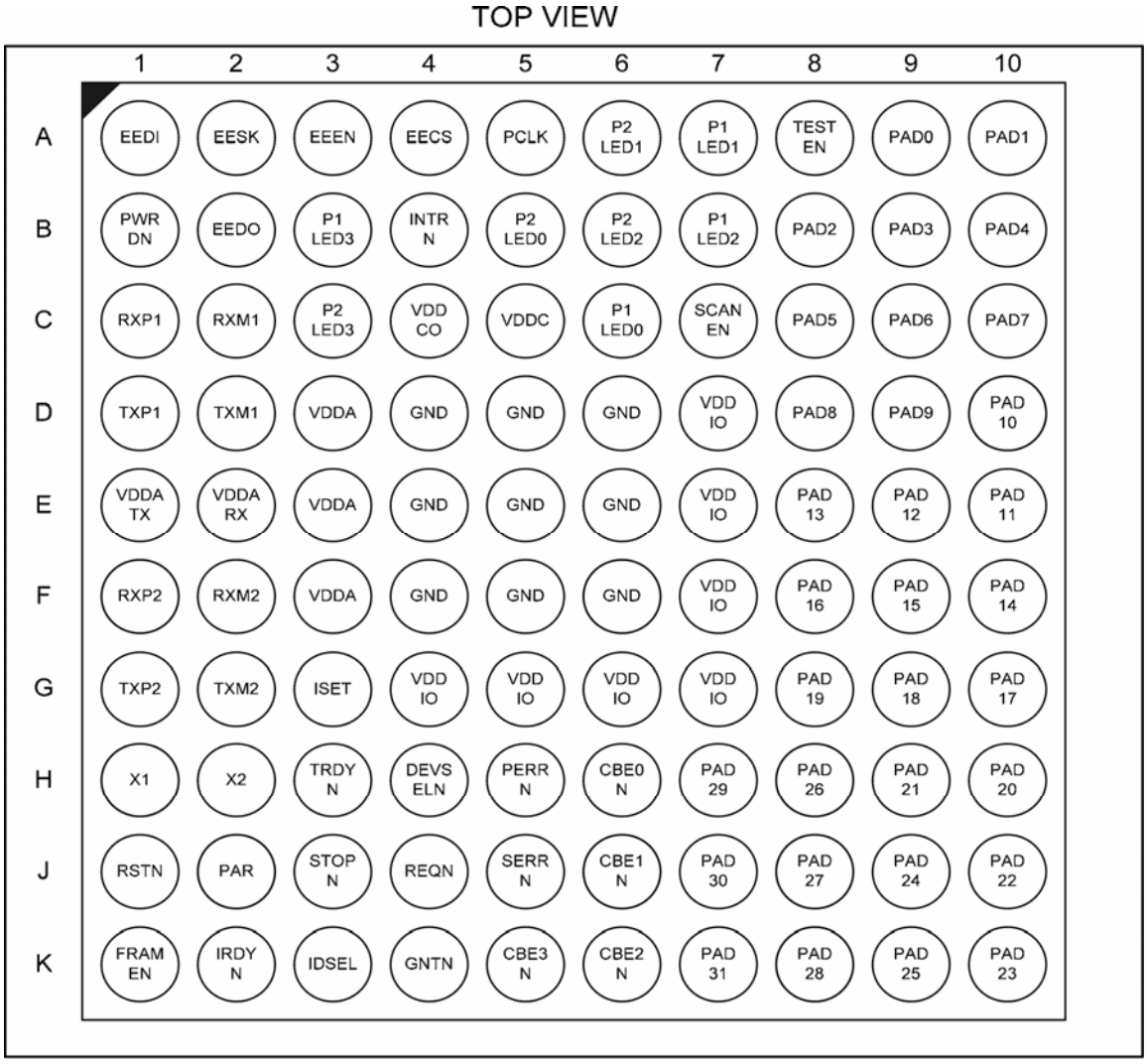

Figure 3. KSZ8842-PMBL 100-Ball LFBGA (Top View)

Pins Description of KSZ8842-PMQL

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>3
4
5
6
7
8</td><td>P1LED2
P1LED1
P1LED0
P2LED2
P2LED1
P2LED0</td><td>Opu
Opu
Opu
Opu
Opu
Opu</td><td>Port 1 and Port 2 LED indicators[1] defined as follows:
LEDs turn on when low.
<table>
<tr><th></th><th colspan="2">Chip Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1]</th></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><th></th><th colspan="2">Reg. SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[1,0]</th><th>[1,1]</th></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27. P2LED3 is pin 22

Port 1 and Port 2 LED indicators[1] for Repeater mode defined as follows:
<table>
<tr><th></th><th colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1] [1,0],[1,1]</th></tr>
<tr><td>P1LED3/P2LED3</td><td>RPT_COL, RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>RPT_Link3/RX, RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>RPT_Link2/RX, RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>RPT_Link1/RX, RPT_ERR1</td><td>—</td></tr>
</table>
Note:
1. RPT_COL = Blink; RPT_Link3/RX (Host port) = On/Blink;
RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink;
RPT_ACT = On if any activity; RPT_ERR3 (Host port) = On if any CRC error;
RPT_ERR2 (port 2) = On if any CRC error; RPT_ERR1 (port 1) = On if any CRC error;</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital I/O V_{DD}</td></tr>
</table>

Pin Number	Pin Name	Type	Pin Function
11	NC	—	No connect
12	PCLK	Ipd	***PCI Bus Clock*** This Clock provides the timing for all PCI bus phases. The rising edge defines the start of each phase. The clock maximum frequency is 33MHz.
13	NC	—	No connect
14	NC	—	No connect
15	NC	—	No connect
16	INTRN	Opd	***Interrupt Request*** Active Low signal to host CPU to request an interrupt when any one of the interrupt conditions occurs in the registers. This pin should be pull-up externally.
17	NC	—	No connect
18	NC	—	No connect
19	EECS	Opu	***EEPROM Chip Select*** This signal is used to select an external EEPROM device
20	NC	—	No connect
21	NC	—	No connect
22	P2LED3	Opd	***Port 2 LED Indicator*** See the description in pins 6, 7, and 8.
23	DGND	Gnd	Digital IO Ground
24	VDDCO	P	***1.2V Core Voltage Output. (Internal 1.2V LDO power supply output)*** This pin is used to provide 1.2V power supply to all 1.2V power VDDC, VDDA and VDDAP. It is recommended the pin should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.
25	NC	—	No connect
26	EEEN	Ipd	***EEPROM Enable*** EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	***Port 1 LED Indicator*** See the description in pins 3, 4, and 5.
28	EEDO	Opd	***EEPROM Data Out*** This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	***EEPROM Serial Clock*** 4µs serial clock to load configuration data from the serial EEPROM.
30	EEDI	Ipd	***EEPROM Data In*** This pin is connected to DO output of the serial EEPROM.
31	NC	—	No connect
32	VDDIO	P	3.3V digital I/O V_{DD}.
33	VDDIO	P	3.3V digital I/O V_{DD}.
34	DGND	Gnd	Digital ground
35	DGND	Gnd	Digital ground
36	PWRDN	Ipu	Full-chip power-down input. Active Low.
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD}
39	AGND	Gnd	Analog ground
40	NC	—	No connect

Pin Number	Pin Name	Type	Pin Function
41	NC	—	No connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD}
44	NC	—	No connect
45	RXP1	I/O	Physical receive (MDI) or transmit (MDIX)signal (+ differential)
46	RXM1	I/O	Physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX)signal (- differential)
53	RXP2	I/O	Port 2 physical receive(MDI) or transmit (MDIX) signal (+ differential)
54	AGND	Gnd	Analog ground
55	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (- differential)
56	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential)
57	VDDA	P	1.2 analog V_{DD}
58	AGND	Gnd	Analog ground
59	NC	—	No connect
60	NC	—	No connect
61	ISET	O	***Set physical transmit output current*** Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL
64	AGND	Gnd	Analog ground
65	X1	I	***25MHz crystal/oscillator clock connections*** Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is not connected. Note: Clock is ±50ppm for both crystal and oscillator.
66	X2	O	
67	RSTN	Ipu	***Hardware Reset, Active Low*** RSTN will cause the KSZ8842-PMQL to reset all of its functional blocks. RSTN must be asserted for a minimum duration of 10 ms.
68	PAR	I/O	***PCI Parity*** Even parity computed for PAD [31:0] and CBE [3:0]N, master drives PAR for address and write data phase, target drives PAR for read data phase.
69	FRAMEN	I/O	***PCI Cycle Frame*** This signal is asserted low to indicate the beginning of the address phase of the bus transaction and de-asserted before the final transfer of the data phase of the transaction in a bus master mode. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
70	IRDYN	I/O	***PCI Initiator Ready*** As a bus master, this signal is asserted low to indicate valid data phases on PAD [31:0] during write data phases, indicates it is ready to accept data during read data phases. As a target, it'll monitor this IRDYN signal that indicates the master has put the data on the bus.

Pin Number	Pin Name	Type	Pin Function
71	TRDYN	I/O	***PCI Target Ready*** As a bus target, this signal is asserted low to indicate valid data phases on PAD [31:0] during read data phases, indicating it is ready to accept data during write data phases. As a master, it will monitor this TRDYN signal that indicates the target is ready for data during read/write operation.
72	STOPN	I/O	***PCI Stop*** This signal is asserted low by the target device to stop the current transaction.
73	IDSEL	I/O	***PCI Initialization Device Select*** This signal is used to select the KSZ8842-PMQL during configuration read and write transactions.
74	DEVSELN	I/O	***PCI Device Select*** This signal is asserted low when it is selected as a target during a bus transaction. As a bus master, the KSZ8842-PMQL samples this signal to insure that the destination address for the data transfer is recognized by a PCI target.
75	REQN	O	***PCI Bus Request*** The KSZ8842-PMQL will assert this signal low to request PCI bus master operation.
76	GNTN	I	***PCI Bus Grant*** This signal is asserted low to indicate to the KSZ8842-PMQL that it has been granted the PCI bus master operation.
77	PERRN	I/O	***PCI Parity Error*** The KSZ8842-PMQL as a master or target will assert this signal low to indicate a parity error on any incoming data. As a bus master, it will monitor this signal on all write operations.
78	DGND	Gnd	Digital I/O ground
79	VDDIO	P	3.3V digital I/O V_{DD}
80	SERRN	O	***PCI System Error*** This system error signal is asserted low by the KSZ8842-PMQL.This signal is used to report address parity errors.
81	NC	—	No connect
82	NC	—	No connect
83	NC	—	No connect
84	NC	—	No connect
85	CBE3N	I	***Command and Byte Enable*** These signals are multiplexed on the same PCI pins. During the address phase, these lines define the bus command. During the data phase, these lines are used as Byte Enables. The Byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
86	CBE2N	I	
87	CBE1N	I	
88	CBE0N	I	
89	PAD31	I/O	***PCI Address / Data 31*** Address and data are multiplexed on the all of the PAD pins. The PAD pins carry the physical address during the first clock cycle of a transaction, and carry data during the subsequent clock cycles.
90	DGND	Gnd	Digital core ground
91	VDDC	P	1.2V digital core V_{DD}
92	VDDIO	P	3.3V digital I/O V_{DD}
93	PAD30	I/O	PCI Address / Data 30
94	PAD29	I/O	PCI Address / Data 29
95	PAD28	I/O	PCI Address / Data 28

Pin Number	Pin Name	Type	Pin Function
96	PAD27	I/O	PCI Address / Data 27
97	PAD26	I/O	PCI Address / Data 26
98	PAD25	I/O	PCI Address / Data 25
99	PAD24	I/O	PCI Address / Data 24
100	PAD23	I/O	PCI Address / Data 23
101	PAD22	I/O	PCI Address / Data 22
102	PAD21	I/O	PCI Address / Data 21
103	PAD20	I/O	PCI Address / Data 20
104	PAD19	I/O	PCI Address / Data 19
105	PAD18	I/O	PCI Address / Data 18
106	PAD17	I/O	PCI Address / Data 17
107	DGND	Gnd	Digital I/O ground
108	VDDIO	P	3.3V digital I/O V_{DD}
109	PAD16	I/O	PCI Address / Data 16
110	PAD15	I/O	PCI Address / Data 15
111	PAD14	I/O	PCI Address / Data 14
112	PAD13	I/O	PCI Address / Data 13
113	PAD12	I/O	PCI Address / Data 12
114	PAD11	I/O	PCI Address / Data 11
115	PAD10	I/O	PCI Address / Data 10
116	PAD9	I/O	PCI Address / Data 9
117	PAD8	I/O	PCI Address / Data 8
118	PAD7	I/O	PCI Address / Data 7
119	PAD6	I/O	PCI Address / Data 6
120	PAD5	I/O	PCI Address / Data 5
121	PAD4	I/O	PCI Address / Data 4
122	PAD3	I/O	PCI Address / Data 3
123	DGND	Gnd	Digital I/O ground
124	DGND	Gnd	Digital core ground
125	VDDIO	P	3.3V digital I/O V_{DD}
126	PAD2	I/O	PCI Address / Data 2
127	PAD1	I/O	PCI Address / Data 1
128	PAD0	I/O	PCI Address / Data 0

Table 1. KSZ8842-PMQL Pin Description

Notes:

P = Power supply.
Gnd = Ground.
I = Input.
O = Output.
I/O = Bi-directional.
Ipd = Input with internal pull-down.
Ipu = Input with internal pull-up.
Opd = Output with internal pull-down.
Opu = Output with internal pull-up.

Balls Description of KSZ8842-PMBL

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type</th><th>Ball Function</th></tr>
<tr><td>A8</td><td>TEST_EN</td><td>I</td><td>Test Enable.
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>C7</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable.
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>B7
A7
C6
B6
A6
B5</td><td>P1LED2
P1LED1
P1LED0
P2LED2
P2LED1
P2LED0</td><td>Opu
Opu
Opu
Opu
Opu
Opu</td><td>Port 1 and Port 2 LED indicators[1] defined as follows:
<table>
<tr><th></th><th colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1]</th></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><th></th><th colspan="2">Reg. SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[1,0]</th><th>[1,1]</th></tr>
<tr><td>P1LED3[2] P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is ball B3. P2LED3 is ball C3.

Port 1 and Port 2 LED indicators[3] for Repeater mode defined as follows:
<table>
<tr><th></th><th colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1] [1,0] [1,1]</th></tr>
<tr><td>P1LED3 , P2LED3</td><td>RPT_COL, RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2, P2LED2</td><td>RPT_Link3/RX, RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1, P2LED1</td><td>RPT_Link2/RX, RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0, P2LED0</td><td>RPT_Link1/RX, RPT_ERR1</td><td>—</td></tr>
</table>
Note 3: RPT_COL = Blink; RPT_Link3/RX (Host port) = On/Blink;
RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink;
RPT_ACT = On if any activity; RPT_ERR3 (Host port) = On if any CRC error;
RPT_ERR2 (port 2) = On if any CRC error; RPT_ERR1 (port 1) = On if any CRC error;</td></tr>
<tr><td>A5</td><td>PCLK</td><td>Ipd</td><td>PCI Bus Clock. This Clock provides the timing for all PCI bus phases. The rising edge</td></tr>
</table>

Ball Number	Ball Name	Type	Ball Function
			defines the start of each phase. The clock maximum frequency is 33MHz.
B4	INTRN	Opd	Interrupt Request. Active Low signal to host CPU to request an interrupt when any one of the interrupt conditions occurs in the registers. This pin should be pull-up externally.
A4	EECS	Opu	EEPROM Chip Select. This signal is used to select an external EEPROM device
C3	P2LED3	Opd	Port 2 LED Indicator See the description in ball B5, B6 and A6.
A3	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
B3	P1LED3	Opd	Port 1 LED indicator See the description in ball C7, A7 and B7.
B2	EEDO	Opd	EEPROM Data Out: This pin is connected to DI input of the serial EEPROM.
A2	EESK	Opd	EEPROM Serial Clock: A 4µs serial output clock to load configuration data from the serial EEPROM.
A1	EEDI	Ipd	EEPROM Data In: This pin is connected to DO output of the serial EEPROM.
B1	PWRDN	Ipu	Full-chip power-down. Active Low.
C1	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
C2	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
D1	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
D2	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
F2	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX)signal (- differential)
F1	RXP2	I/O	Port 2 physical receive(MDI) or transmit (MDIX) signal (+ differential)
G2	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (- differential)
G1	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential)
G3	ISET	O	Set physical transmit output current. Pull-down this ball with a 3.01K 1% resistor.
H1	X1	I	25MHz crystal/oscillator clock connections
H2	X2	O	Balls (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is ± 50ppm for both crystal and oscillator.
J1	RSTN	Ipu	Hardware Reset, Active Low RSTN will cause the KSZ8842-PMBL to reset all of its functional blocks. RSTN must be asserted for a minimum duration of 10 ms.
J2	PAR	O	PCI Parity Even parity computed for PAD [31:0] and CBE[3:0]N, master drives PAR for address and write data phase, target drives PAR for read data phase.
K1	FRAMEN	I/O	PCI Cycle Frame This signal is asserted low to indicate the beginning of the address phase of the bus transaction and de-asserted before the final transfer of the data phase of the transaction in a bus master mode. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.

Ball Number	Ball Name	Type	Ball Function
K2	IRDYN	I/O	PCI Initiator Ready As a bus master, this signal is asserted low to indicate valid data phases on PAD [31:0] during write data phases, indicates it is ready to accept data during read data phases. As a target, it'll monitor this IRDYN signal that indicates the master has put the data on the bus.
H3	TRDYN	I/O	PCI Target Ready As a bus target, this signal is asserted low to indicate valid data phases on PAD [31:0] during read data phases, indicating it is ready to accept data during write data phases. As a master, it will monitor this TRDYN signal that indicates the target is ready for data during read/write operation.
J3	STOPN	I/O	PCI Stop This signal is asserted low by the target device to stop the current transaction
K3	IDSEL	I/O	PCI Initialization Device Select. This signal is used to select the KSZ8842-PMQL/PMBL during configuration read and write transactions.
H4	DEVSELN	I/O	PCI Device Select This signal is asserted low when it is selected as a target during a bus transaction. As a bus master, the KSZ8842-PMBL samples this signal to insure that the destination address for the data transfer is recognized by a PCI target.
J4	REQN	O	PCI Request The KSZ8842-PMBL will assert this signal low to request PCI bus master operation.
K4	GNTN	I	PCI Grant This signal is asserted low to indicate to the KSZ8842-PMBL that it has been granted the PCI bus master operation.
H5	PERRN	I/O	PCI Parity Error The KSZ8842-PMBL as a master or target will assert this signal low to indicate a parity error on any incoming data. As a bus master, it will monitor this signal on all write operations.
J5	SERRN	O	PCI System Error This system error signal is asserted low by the KSZ8842-PMBL.This signal is used to report address parity errors.
K5	CBE3N	I	Command and Byte Enable These signals are multiplexed on the same PCI pins. During the address phase, these lines define the bus command. During the data phase, these lines are used as Byte Enables. The Byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
K6	CBE2N	I	
J6	CBE1N	I	
H6	CBE0N	I	
K7	PAD31	I/O	PCI Address / Data 31 Address and data are multiplexed on the all of the PAD balls. The PAD pins carry the physical address during the first clock cycle of a transaction, and carry data during the subsequent clock cycles.
J7	PAD30	I/O	PCI Address / Data 30
H7	PAD29	I/O	PCI Address / Data 29
K8	PAD28	I/O	PCI Address / Data 28
J8	PAD27	I/O	PCI Address / Data 27
H8	PAD26	I/O	PCI Address / Data 26
K9	PAD25	I/O	PCI Address / Data 25
J9	PAD24	I/O	PCI Address / Data 24
K10	PAD23	I/O	PCI Address / Data 23

Ball Number	Ball Name	Type	Ball Function
J10	PAD22	I/O	PCI Address / Data 22
H9	PAD21	I/O	PCI Address / Data 21
H10	PAD20	I/O	PCI Address / Data 20
G8	PAD19	I/O	PCI Address / Data 19
G9	PAD18	I/O	PCI Address / Data 18
G10	PAD17	I/O	PCI Address / Data 17
F8	PAD16	I/O	PCI Address / Data 16
F9	PAD15	I/O	PCI Address / Data 15
F10	PAD14	I/O	PCI Address / Data 14
E8	PAD13	I/O	PCI Address / Data 13
E9	PAD12	I/O	PCI Address / Data 12
E10	PAD11	I/O	PCI Address / Data 11
D10	PAD10	I/O	PCI Address / Data 10
D9	PAD9	I/O	PCI Address / Data 9
D8	PAD8	I/O	PCI Address / Data 8
C10	PAD7	I/O	PCI Address / Data 7
C9	PAD6	I/O	PCI Address / Data 6
C8	PAD5	I/O	PCI Address / Data 5
B10	PAD4	I/O	PCI Address / Data 4
B9	PAD3	I/O	PCI Address / Data 3
B8	PAD2	I/O	PCI Address / Data 2
A10	PAD1	I/O	PCI Address / Data 1
A9	PAD0	I/O	PCI Address / Data 0
C5	VDDC	P	1.2V digital core V_{DD}
C4	VDDCO	P	1.2V Core Voltage Output. (internal 1.2V LDO power supply output) This ball is used to provide 1.2V power supply to all 1.2V power VDDC and VDDA. It is recommended the ball should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.
D3, E3, F3	VDDA	P	1.2V analog V_{DD}
D7, E7, F7, G4, G5, G6, G7	VDDIO	P	3.3V digital I/O V_{DD}
E1	VDDATX	P	3.3V analog V_{DD}
E2	VDDARX	P	3.3V analog V_{DD}
D4, D5, D6, E4, E5, E6, F4, F5, F6	GND	Gnd	Ground

Table 2. KSZ8842-PMBL Ball Description

Functional Description

The KSZ8842-PMQL/PMBL contains one PCI interface unit, two 10/100 physical layer transceivers (PHYs), three MAC units, and a RX/TX DMA channel all integrated with a Layer-2 switch.

Physical signal transmission and reception are enhanced through the use of analog circuits in the PHY that make the design more efficient and allow for low power consumption.

Functional Overview: PCI Bus Interface Unit

PCI Bus Interface

The PCI Bus Interface implements PCI v2.2 bus protocols and configuration space. The KSZ8842-PMQL/PMBL supports bus master reads and writes to CPU memory, and CPU access to on-chip register space. When the CPU reads and writes the configuration registers of the KSZ8842-PMQL/PMBL, it is as a slave. So the KSZ8842-PMQL/PMBL can be either a PCI bus master or slave. The PCI Bus Interface is also responsible for managing the DMA interfaces and the host processors access. Arbitration logic within the PCI Bus Interface unit accepts bus requests from the TXDMA logic and RXDMA logic.

The PCI bus interface also manages interrupt generation for a host processor.

TXDMA Logic and TX Buffer Manager

The KSZ8842-PMQL/PMBL supports a multi-frame, multi-fragment DMA gather process. Descriptors representing frames are built and linked in system memory by a host processor. The TXDMA logic is responsible for transferring the multi-fragment frame data from the host memory into the TX buffer.

The KSZ8842-PMQL/PMBL uses 4K bytes of transmit data buffer between the TXDMA logic and transmit MAC. When the TXDMA logic determines there is enough space available in the TX buffer, the TXDMA logic will move any pending frame data into the TX buffer. The management mechanism depends on the transmit descriptor list.

RXDMA Logic and RX Buffer Manager

The KSZ8842-PMQL/PMBL supports a multi-frame, multi-fragment DMA scatter process. Descriptors representing frames are built and linked in system memory by the host processor. The RXDMA logic is responsible for transferring the frame data from the RX buffer to the host memory.

The KSZ8842-PMQL/PMBL uses 4K bytes of receive data buffer between the receive MAC and RXDMA logic. The management mechanism depends on the receive descriptor list.

Functional Overview: Physical Layer Transceiver (PHY)

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external1% 3.01KΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial to parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for

optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer (Recovery)

The internal PLL clock synthesizer generates 125MHz, 62.5MHz, 41.66MHz, and 25MHz clocks by setting the on-chip bus speed control register OBCR for KSZ8842-PMQL/PMBL system timing. These internal clocks are generated from an external 25MHz crystal or oscillator.

Note: Default setting is 25MHz in OBCR register, recommends the software driver to set it to 125MHz for best performance.

Scrambler/De-scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

10BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8842-PMQL/PMBL decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

Power Management

The KSZ8842-PMQL/PMBL features a per port power-down mode. To save power, the user can power-down a port that is not in use by setting bit 11 in either P1CR4 or P1MBCR register for port 1, and set bit 11 in either P2CR4 or P2MBCR register for port 2. To bring the port back up, reset bit 11 in these registers.

In addition, there is a full switch power-down mode by PWRDN pin/ball 36. When this pin/ball is pulled-down, the entire chip powers down. Transitioning this pin/ball from pull-down to pull-up results in a power up and chip reset.

MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8842-PMQL/PMBL supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8842-PMQL/PMBL device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

The IEEE 802.3u standard MDI and MDI-X definitions are:

MDI		MDI-X	
RJ45 Pins	**Signals**	**RJ45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 3. MDI/MDI-X Pin Definitions

Straight Cable

A straight cable connects an MDI device to an MDI-X device or an MDI-X device to an MDI device. The following diagram shows a typical straight cable connection between a network interface card (NIC) (MDI) and a switch, or hub (MDI-X).

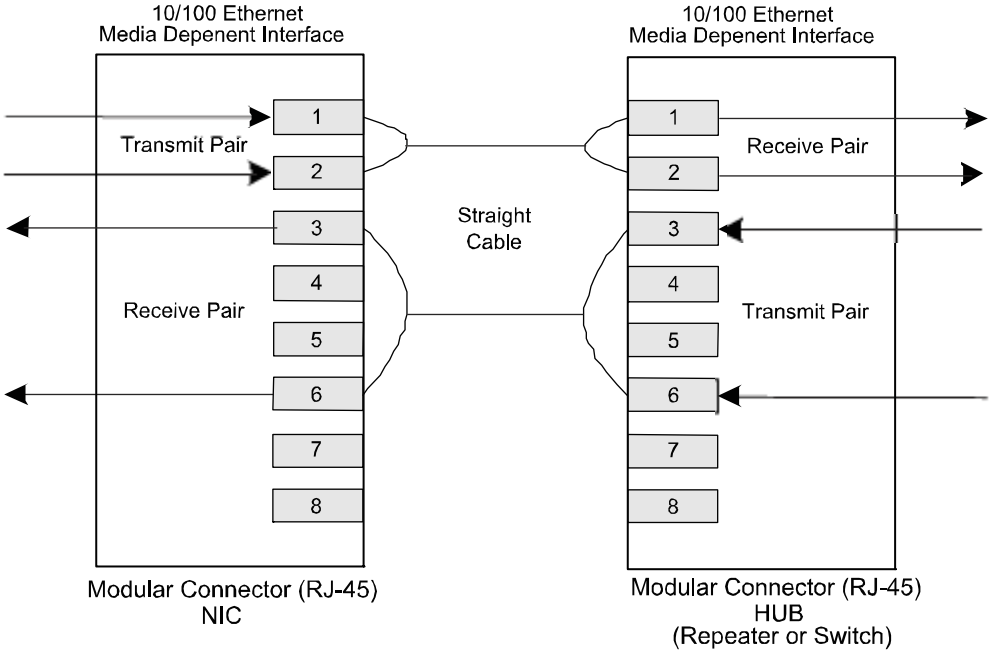

Figure 4. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

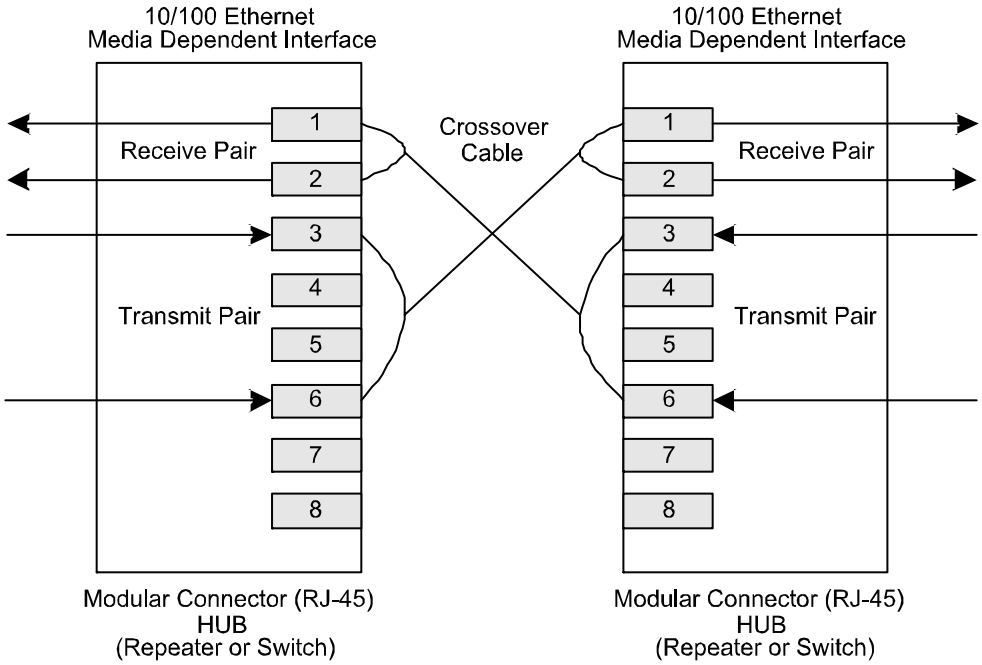

Figure 5. Typical Crossover Cable Connection

Auto Negotiation

The KSZ8842-PMQL/PMBL conforms to the auto negotiation protocol as described by the 802.3 committee to allow the channel to operate at 10Base-T or 100Base-TX.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8842-PMQL/PMBL is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link setup is shown in the following flow diagram (Figure 6).

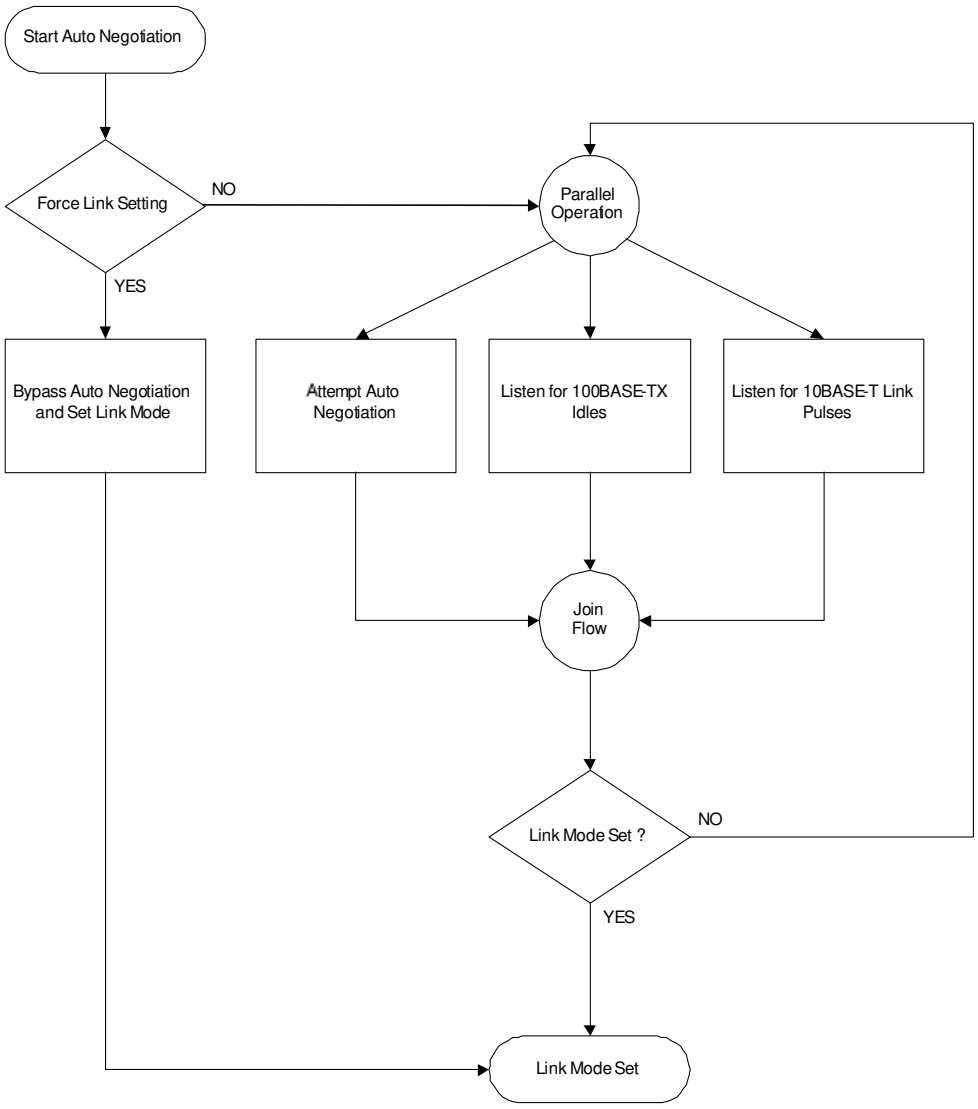

Figure 6. Auto Negotiation and Parallel Operation

LinkMD Cable Diagnostics

The KSZ8842-PMQL/PMBL LinkMD uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format.

Access

LinkMD is initiated by accessing register P1VCT/P2VCT, the LinkMD Control/Status register, in conjunction with register P1CR4/P2CR4, the 100BASE-TX PHY Controller register.

Usage

LinkMD can be used at any time by making sure Auto MDIX has been disabled. To disable Auto-MDIX, write a '1' to P1CR4[10] for port 1 or P2CR4[10] for port 2 to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P1VCT[15] for port 1 or P2VCT[15] for port 2, is set to '1' to start the test on this pair.

When bit P1VCT[15] or P2VCT[15] returns to '0', the test is complete. The test result is returned in bit P1VCT[14-13] or P2VCT[14-13] and the distance is returned in bits P1VCT[8-0] or P2VCT[8-0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD failed

IIf P1VCT[14-13]=11 or P2VCT[14-13]=11, this indicates an invalid test, and occurs when the KSZ8842-PMQL/PMBL is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8842-PMQL/PMBL to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance (in meters) can be approximated by the following formula:

Distance = P1VCT[8-0] x 0.4m

Distance = P1VCT[8-0] x 0.4m

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

Functional Overview: MAC and Switch

Address Lookup

The internal lookup table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information.

The KSZ8842-PMQL/PMBL is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal lookup engine updates its table with a new entry if the following conditions are met:

1. The received packet's Source Address (SA) does not exist in the lookup table.
2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

Migration

The internal lookup engine also monitors whether a station has moved. If a station has moved, it updates the table accordingly. Migration happens when the following conditions are met:

1. The received packet's SA is in the table but the associated source port information is different.
2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine updates the existing record in the table with the new source port information.

Aging

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and continuously removes aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through Global Register SGCR1[10]).