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KSZ8851-16MLL

Single-Port Ethernet MAC Controller with 8-Bit or 16-Bit Non-PCI Interface

Highlights

- Single-Port Controller Chip with Non-PCI CPU Interface
- Mixed Analog/Digital Device Offering Wake-On-LAN Technology for Effectively Addressing Fast Ethernet Applications
- HP Auto-MDIX Support

Target Applications

- Video/Audio Distribution Systems
- High-End Cable, Satellite, and IP Set-Top Boxes
- Video over IP and IPTV
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Home Base Station with Ethernet Connection
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security, Motion Control and Surveillance Cameras
- In-Vehicle Diagnostics (OBD) and Software Download

Features

- Integrated MAC and PHY Ethernet Controller Fully Compliant with IEEE 802.3/802.3u Standards
- Designed for High Performance and High Throughput Applications
- Supports 10BASE-T/100BASE-TX
- Supports IEEE 802.3x Full-Duplex Flow Control and Half-Duplex Backpressure Collision Flow Control
- Supports DMA-Slave Burst Data Read and Write Transfers
- Supports IP Header (IPv4)/TCP/UDP/ICMP Checksum Generation and Checking
- Supports IPv6 TCP/UDP/ICMP Checksum Generation and Checking
- Automatic 32-Bit CRC Generation and Checking
- Simple SRAM-like Host Interface Easily Connects to Most Common Embedded MCUS
- Supports Multiple Data Frames for Receive without Address Bus and Byte-Enable Signals
- Supports Both Big- and Little-Endian Processors
- Larger Internal Memory with 12 kb for RX FIFO and 6 kb for TX FIFO. Programmable Low, High and Overrun Watermark for Flow Control in Rx FIFO
- Shared Data Bus for Data, Address, and Byte Enable
- Efficient Architecture Design with Configurable Host Interrupt Schemes to Minimize Host CPU Overhead and Utilization
- Powerful and Flexible Address Filtering Scheme
- Optional to Use External Serial EEPROM Configuration for MAC Address
- Single 25 MHz Reference Clock for Both PHY and MAC
- HBM ESD Rating 6 kV

Power Modes, Power Supplies, and Packaging

- Single 3.3V Power Supply with Options for 1.8V, 2.5V and 3.3V VDD I/O
- Built-in Integrated 3.3V or 2.5V to 1.8V Low Noise Regulator (LDO) for Core and Analog Blocks
- Enhanced Power Management Feature with Energy Detect Mode and Soft Power-Down Mode to Ensure Low-Power Dissipation During Device Idle Periods
- Comprehensive LED Indicator Support for Link, Activity and 10/100 Speed (2 LEDs) - User Programmable
- Low-Power CMOS Design
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Flexible Package Options Available in 48-Pin QFP KSZ8851-16MLL or 128-Pin PQFP KSZ8851-16/32MQL

Additional Features

In Addition to Offering All the Features of a Layer 2 Controller, the KSZ8851-16MLL Offers:

- Flexible 8-bit and 16-bit Generic Host Processor Interfaces with Same Access Time and Single Bus Timing to any I/O Registers and Rx/Tx FIFO Buffers
- Supports to add Two-Byte Before Frame Header in Order for IP Frame Content with Double Word Boundary
- LinkMD® Cable Diagnostic Capabilities to Determine Cable Length, Diagnose Faulty Cables, and Determine Distance To Fault
- Wake-on-LAN Functionality
  - Incorporates Magic Packet™, Wake-up Frame, Network Link State, and Detection of Energy Signal Technology
- HP Auto MDI-X™ Crossover with Disable/Enable Option
- Ability to Transmit and Receive Frames up to 2000 Bytes

Network Features

- 10BASE-T and 100BASE-TX Physical Layer Support
- Auto-Negotiation: 10/100 Mbps Full- and Half-Duplex
- Adaptive Equalizer
- Baseline Wander Correction

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet
- Embedded Systems
- Automotive Ethernet

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Table of Contents

1.0 INTRODUCTION

1.1 General Terms and Conventions

The following is list of the general terms used throughout this document:

BIU	Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU	Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS	Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC	Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
—	Cut-Through Switch	A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet.
DA	Destination Address	The address to send packets.
DMA	Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EEPROM	Electronically Erasable Programmable Read-only Memory	A design in which memory on a chip can be erased by exposing it to an electrical charge.
EISA	Extended Industry Standard Architecture	A bus architecture designed for PCs using 80x86 processors, or an Intel 80386, 80486 or Pentium microprocessor. EISA buses are 32 bits wide and support multiprocessing.
EMI	Electro-Magnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS	Frame Check Sequence	See CRC.
FID	Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
IGMP	Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG	Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI	Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
ISA	Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
—	Jumbo Packet	A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.

MDI	Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore 'media dependent.
MDI-X	Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB	Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII	Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC	Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID	Non Port VLAN ID	The Port VLAN ID value is used as a VLAN reference.
PLL	Phase-Locked Loop	—
PME	Power Management Event	An occurrence that affects the directing of power to different components of a system.
QMU	Queue Management Unit	Manages packet traffic between MAC/PHY interface and the system host. The QMU has built-in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue).
SA	Source Address	The address from which information has been sent.
TDR	Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal -- or part of the signal -- to return.
UTP	Unshielded Twisted Pair	Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.
VLAN	Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

1.2 General Description

The KSZ8851M-series is a single-port controller chip with a non-PCI CPU interface, and is available in 8-bit and 16-bit bus designs. This datasheet describes the 48-pin LQFP KSZ8851-16MLL functionality for applications requiring high-performance from a single-port Ethernet controller with an 8-bit or 16-bit generic processor interface. The KSZ8851-16MLL offers the most cost-effective solution for adding high-throughput Ethernet connectivity to traditional embedded systems.

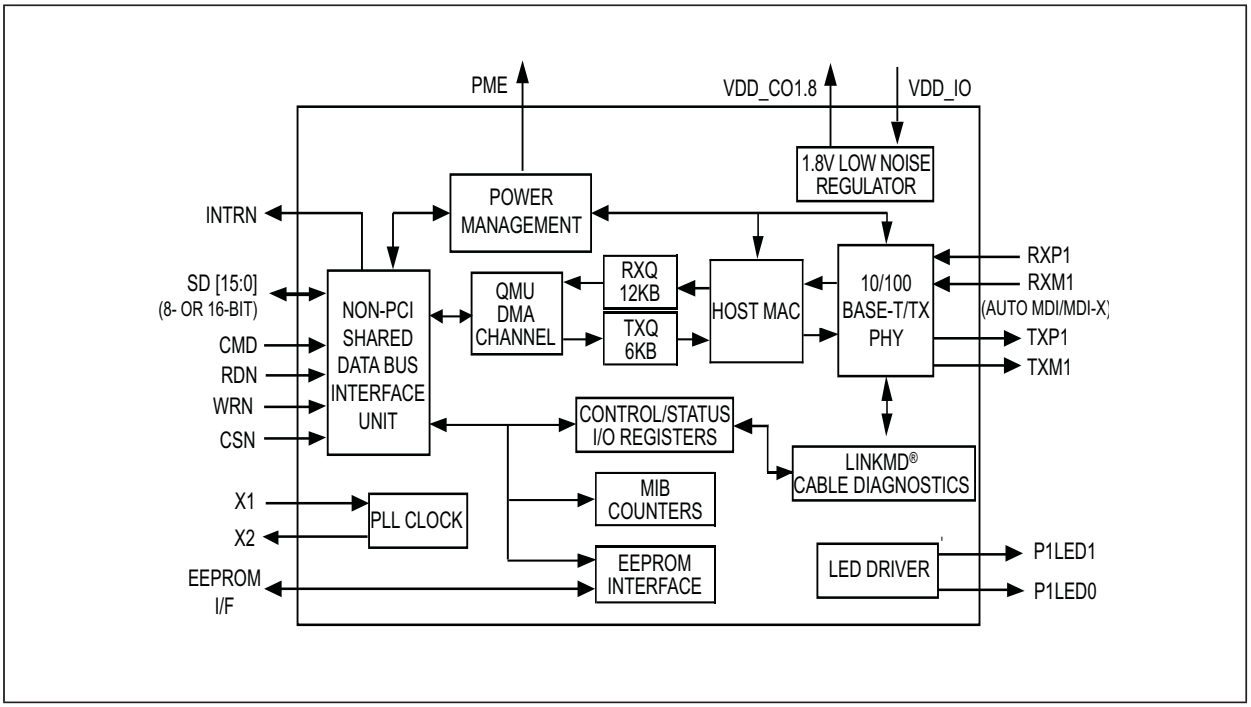
The KSZ8851-16MLL is a single-chip, mixed analog/digital device offering wake-on-LAN technology for effectively addressing fast Ethernet applications. It consists of a fast Ethernet MAC controller, an 8-bit or 16-bit generic host processor interface, and incorporates a unique, dynamic memory pointer with 4-byte buffer boundary and can fully utilize 18 KB for both TX (allocated 6 KB) and RX (allocated 12 KB) directions in the host buffer interface.

The KSZ8851-16MLL is designed to be fully compliant with the appropriate IEEE 802.3 standards. An industrial temperature-grade version of the KSZ8851-16MLLI and a qualified AEC-Q100 automotive version of the KSZ8851-16MLLU are also available.

Physical signal transmission and reception are enhanced through the use of analog circuitry. This makes the design more efficient and allows lower-power consumption. The KSZ8851-16MLL is designed using a low-power CMOS process that features a single 3.3V power supply with options for 1.8V, 2.5V, or 3.3V V_{DD} I/O. The device includes an extensive feature set that offers management information base (MIB) counters and CPU control/data interfaces with single shared data bus timing.

The KSZ8851-16MLL includes a unique cable diagnostics feature called LinkMD®. This feature determines the length of the cabling plant and also ascertains if there is an open or short condition in the cable. Accompanying software enables the cable length and cable conditions to be conveniently displayed. In addition, the KSZ8851-16MLL supports Hewlett Packard (HP) Auto-MDIX thereby eliminating the need to differentiate between straight or crossover cables in applications.

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 48-LQFP PIN ASSIGNMENT (TOP VIEW)

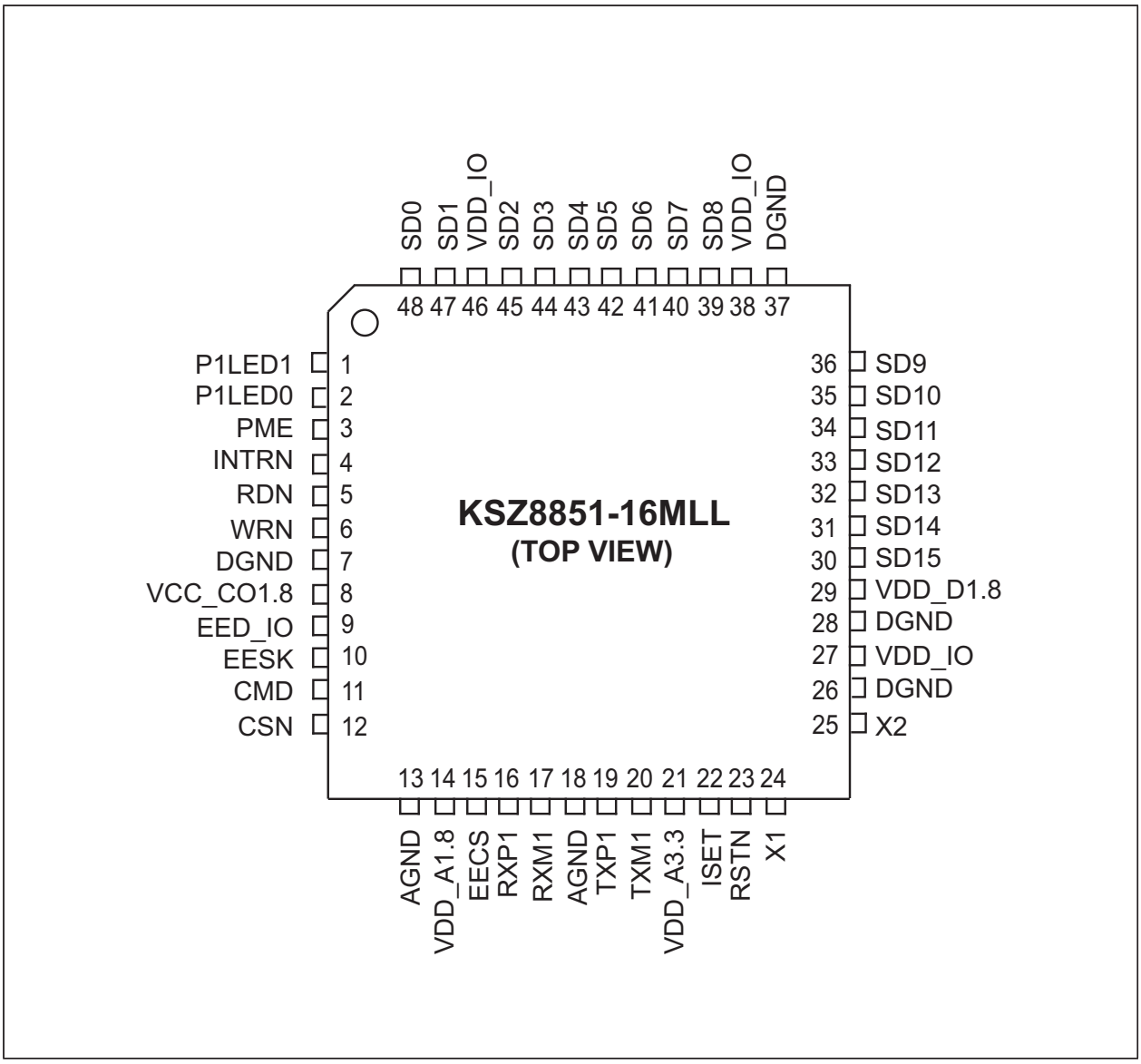


TABLE 2-1: SIGNALS

Num Pins	Name	Buffer Type (Note 2-1)	Description		
1	P1LED1	IPU/O	Programmable LED output to indicate port activity/status. LED is ON when output is LOW; LED is OFF when output is HIGH. Port 1 LED indicators* defined as follows:		
				Chip Global Control Register: CGCR bit [9]	
				0 (Default)	1
			P1LED1	100BT	ACT
			P1LED0	LINK/ACT	LINK
2	P1LED0	OPU	* Link = LED On; Activity = LED Blink; Link/Act = LED On/Blink; Speed = LED On (100BASE-T); LED Off (10BASE-T) Config Mode: The P1LED1 pull-up/pull-down value is latched as 16-/8-bit mode during power-up/reset. See the Pin for strap-in options section for details.		
3	PME	OPU	Power Management Event (default active low): It is asserted (low or high depends on polarity set in PMECR register) when one of the wake-on-LAN events is detected by KSZ8851-16MLL. The KSZ8851-16MLL is requesting the system to wake up from low power mode.		
4	INTRN	OPU	Interrupt: An active low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7 kΩ pull-up resistor.		
5	RDN	IPU	Read Strobe Not Asynchronous read strobe, active low to indicate read cycle.		
6	WRN	IPU	Read Strobe Not Asynchronous read strobe, active low to indicate read cycle.		
7	DGND	GND	Digital Ground.		
8	$V_{DD\_}$-CO1.8	P	1.8V regulator output. This 1.8V output pin provides power to pins 14 (VDD_A1.8) and 29 (VDD_D1.8) for core V_{DD} supply. If VDD_IO is set for 1.8V then this pin should be left floating, pins 14 (VDD_A1.8) and 29 (VDD_D1.8) will be sourced by the external 1.8V supply that is tied to pins 27, 38 and 46 (VDD_IO) with appropriate filtering.		
9	EED_IO	IPD/O	In/Out Data from/to external EEPROM. Config Mode: The pull-up/pull-down value is latched as with/without EEPROM during power-up/reset. See the Pin for strap-in options section for details.		
10	EESK	IPD/O	EEPROM Serial Clock A 4 µs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM. Config Mode: The pull-up/pull-down value is latched as big-/little-Endian mode during power-up/reset. See the Pin for strap-in options section for details.		

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Name	Buffer Type (Note 2-1)	Description
11	CMD	IPD	Command Type This command input decides the SD[15:0] shared data bus access information. When command input is low, the access of shared data bus is for data access in 16-bit mode shared data bus SD[15:0] or in 8-bit mode shared data bus SD[7:0]. When command input is high, the access of shared data bus is for address A[7:2] access at shared data bus SD[7:2], byte enable BE[3:0] at SD[15:12] and the SD[11:8] is “Do Not Care” in 16-bit mode. It is for address A[7:0] access at SD[7:0] in 8-bit mode.
12	CSN	IPU	Chip Select Not Chip select for the shared data bus access enable, active Low.
13	AGND	GND	Analog ground.
14	VDD_A1.8	P	1.8V analog power supply from VDD_CO1.8 (pin 8) with appropriate filtering. If VDD_IO is 1.8V, this pin must be supplied power from the same source as pins 27, 38 and 46 (VDD_IO) with appropriate filtering.
15	EECS	OPD	EEPROM Chip Select This signal is used to select an external EEPROM device.
16	RXP1	I/O	Port 1 physical receive signal (+ differential).
17	RXM1	I/O	Port 1 physical receive signal (– differential).
18	AGND	GND	Analog ground.
19	TXP1	I/O	Port 1 physical transmit signal (+ differential).
20	TXM1	I/O	Port 1 physical transmit signal (– differential).
21	VDD_A3.3	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
22	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01 KΩ 1% resistor to ground.
23	RSTN	IPU	Reset Not Hardware reset pin (active Low). This reset input is required minimum of 10 ms low after stable supply voltage 3.3V.
24	X1	I	25 MHz crystal or oscillator clock connection. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ±50 ppm for either crystal or oscillator.
25	X2	O	
26	DGND	GND	Digital ground
27	VDD_IO	P	3.3V, 2.5V or 1.8V digital V_{DD} input power supply for IO with well decoupling capacitors.
28	DGND	GND	Digital ground
29	VDD_D1.8	P	1.8V digital power supply from VDD_CO1.8 (pin 8) with appropriate filtering. If VDD_IO is 1.8V, this pin must be supplied power from the same source as pins 27, 38, and 46 (VDD_IO) with appropriate filtering.

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Name	Buffer Type (Note 2-1)	Description
30	SD15	I/O (PD)	Shared Data Bus bit 15. Data D15 access when CMD=0. Byte Enable 3 at double-word boundary access (BE3, 4th byte enable and active high) in 16-bit mode when CMD=1. This pin must be tied to GND in 8-bit bus mode.
31	SD14	I/O (PD)	Shared Data Bus bit 14. Data D14 access when CMD=0. Byte Enable 2 at double-word boundary access (BE2, 3rd byte enable and active high) in 16-bit mode when CMD=1. This pin must be tied to GND in 8-bit bus mode.
32	SD13	I/O (PD)	Shared Data Bus bit 13. Data D13 access when CMD=0. Byte Enable 1 at double-word boundary access (BE1, 2nd byte enable and active high) in 16-bit mode when CMD=1. This pin must be tied to GND in 8-bit bus mode.
33	SD12	I/O (PD)	Shared Data Bus bit 12. Data D12 access when CMD=0. Byte Enable 0 at double-word boundary access (BE0, 1st byte enable and active high) in 16-bit mode when CMD=1. This pin must be tied to GND in 8-bit bus mode.
34	SD11	I/O (PD)	Shared Data Bus bit 11. Data D11 access when CMD=0. Do Not Care when CMD=1. This pin must be tied to GND in 8-bit bus mode.
35	SD10	I/O (PD)	Shared Data Bus bit 10. Data D10 access when CMD=0. Do Not Care when CMD=1. This pin must be tied to GND in 8-bit bus mode.
36	SD9	I/O (PD)	Shared Data Bus bit 9. Data D9 access when CMD=0. Do Not Care when CMD=1. This pin must be tied to GND in 8-bit bus mode.
37	DGND	GND	Digital ground.
38	VDD_IO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power supply for IO with well decoupling capacitors.
39	SD8	I/O (PD)	Shared Data Bus bit 8. Data D8 access when CMD=0. Do Not Care when CMD=1. This pin must be tied to GND in 8-bit bus mode.
40	SD7	I/O (PD)	Shared Data Bus bit 7. Data D7 access when CMD=0. Address A7 access when CMD=1.
41	SD6	I/O (PD)	Shared Data Bus bit 6. Data D6 access when CMD=0. Address A6 access when CMD=1.
42	SD5	I/O (PD)	Shared Data Bus bit 5. Data D5 access when CMD=0. Address A5 access when CMD=1.
43	SD4	I/O (PD)	Shared Data Bus bit 4. Data D4 access when CMD=0. Address A4 access when CMD=1.
44	SD3	I/O (PD)	Shared Data Bus bit 3. Data D3 access when CMD=0. Address A3 access when CMD=1.
45	SD2	I/O (PD)	Shared Data Bus bit 2. Data D2 access when CMD=0. Address A2 access when CMD=1.

TABLE 2-1: SIGNALS (CONTINUED)

Num Pins	Name	Buffer Type (Note 2-1)	Description
46	VDD_IO	P	Shared Data Bus bit 2. Data D2 access when CMD=0. Address A2 access when CMD=1.
47	SD1	I/O (PD)	Shared Data Bus bit 1. Data D1 access when CMD=0. In 8-bit mode, this is address A1 access when CMD=1. In 16-bit mode, this is “Do Not Care” when CMD=1.
48	SD0	I/O (PD)	Shared Data Bus bit 0. Data D0 access when CMD=0. In 8-bit mode, this is address A0 access when CMD=1. In 16-bit mode, this is “Do Not Care” when CMD=1.

Note 2-1
P = Power supply
GND = Ground
I/O = Bi-directional
I = Input
O = Output
IPD = Input with internal pull-down (58 kΩ ±30%)
IPU = Input with internal pull-up (58 kΩ ±30%)
OPD = Output with internal pull-down (58 kΩ ±30%)
OPU = Output with internal pull-up (58 kΩ ±30%)
IPU/O = Input with internal pull-up (58 kΩ ±30%) during power-up/reset; output pin otherwise
IPD/O = Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin otherwise
I/O (PD) = Input/Output with internal pull-down (58 kΩ ±30%)

TABLE 2-2: PIN FOR STRAP-IN OPTIONS

Num Pins	Name	Buffer Type (Note 2-2)	Description
1	P1LED1	IPU/IO	8- or 16-bit bus mode select during power-up/reset: NC or Pull-up (default) = 16-bit bus Pull-down = 8-bit bus This pin value is also latched into register CCR, bit 6/7.
9	EED_IO	IPD/O	EEPROM select during power-up/reset: Pull-up = EEPROM present NC or Pull-down (default) = EEPROM not present This pin value is latched into register CCR, bit 9.
10	EESK	IPD/O	Endian mode select during power-up/reset: Pull-up = Big Endian NC or Pull-down (default) = Little Endian This pin value is latched into register CCR, bit 10. When this pin is no connect or tied to GND, the bit 11 (Endian mode selection) in RXFDPR register can be used to program either Little (bit11=0 default) Endian mode or Big (bit11=1) Endian mode.

Note 2-2
IPU/O = Input with internal pull-up (58K ±30%) during power-up/reset; output pin otherwise.
IPD/O = Input with internal pull-down (58K ±30%) during power-up/reset; output pin otherwise.
Pin strap-ins are latched during power-up or reset.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8851-16MLL is a single-chip fast Ethernet MAC/PHY controller consisting of a 10/100 physical layer transceiver (PHY), a MAC, and a Bus Interface Unit (BIU) that controls the KSZ8851-16MLL via an 8-bit or 16-bit host bus interface.

The KSZ8851-16MLL is fully compliant with IEEE802.3u standards.

3.1 Functional Overview

3.1.1 POWER MANAGEMENT

The KSZ8851-16MLL supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are four operation modes under the power management function which is controlled by two bits in PMECR (0xD4) register as shown below:

PMECR[1:0] = 00 Normal Operation Mode

PMECR[1:0] = 01 Energy Detect Mode

PMECR[1:0] = 10 Soft Power-Down Mode

PMECR[1:0] = 11 Power-Saving Mode

TABLE 3-1: INTERNAL FUNCTION BLOCKS STATUSES

KSZ8851-16MLL Function Blocks	Power Management Operation Modes			
	Normal Mode	Power-Saving Mode	Soft Power-Down Mode	Energy Detect Mode
Internal PLL Clock	Enabled	Enabled	Disabled	Disabled
Tx/Rx PHY	Enabled	Rx unused block disabled	Disabled	Energy detect at Rx
MAC	Enabled	Enabled	Disabled	Disabled
Host Interface	Enabled	Enabled	Disabled	Disabled

3.1.2 NORMAL OPERATION MODE

This is the default setting bit[1:0]=00 in PMECR register after the chip power-up or hardware reset (pin 67). When KSZ8851-16MLL is in this normal operation mode, all PLL clocks are running, PHY and MAC are on and the host interface is ready for CPU read or write.

During the normal operation mode, the host CPU can set the bit[1:0] in PMECR register to transit the current normal operation mode to any one of the other three power management operation modes.

3.1.3 POWER SAVING MODE

The power-saving mode is entered when auto-negotiation mode is enabled, cable is disconnected, and by setting bit[1:0]=11 in PMECR register and bit [10]=1 in P1SCLMD register. When KSZ8851M is in this mode, all PLL clocks are enabled, MAC is on, all internal registers value will not change, and host interface is ready for CPU read or write. In this mode, it mainly controls the PHY transceiver on or off based on line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8851M can automatically enabled the PHY power up to normal power state from power-saving mode.

During this power-saving mode, the host CPU can program the bit[1:0] in PMECR register and set bit[10]=0 in P1SCLMD register to transit the current power-saving mode to any one of the other three power management operation modes.

3.1.4 SOFT POWER-DOWN MODE

The soft power-down mode is entered by setting bit[1:0]=10 in PMECR register. When KSZ8851-16MLL is in this mode, all PLL clocks are disabled, the PHY and the MAC are off, all internal registers value will not change, and the host interface is only used to wake-up this device from current soft power-down mode to normal operation mode.

In order to go back the normal operation mode from this soft power-down mode, the only way to leave this mode is through a host wake-up command which the CPU issues to read the Globe Reset Register (GRR at 0x26).

3.1.5 ENERGY DETECT MODE

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8851-16MLL is not connected to an active link partner. For example, if cable is not present or it is connected to a powered down partner, the KSZ8851-16MLL can automatically enter to the low power state in energy detect mode. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8851-16MLL can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8851-16MLL reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit[1:0]=01 in PMECR register. When the KSZ8851-16MLL is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than pre-configured value at bit[7:0] Go-Sleep time in GSWUTR register, KSZ8851-16MLL will go into a low power state. When KSZ8851-16MLL is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable and is continuously presented for a time longer than pre-configured value at bit[15:8] Wake-Up time in GSWUTR register, the KSZ8851-16MLL will enter either the normal power state if the auto-wakeup enable bit[7] is set in PMECR register or the normal operation mode if both auto-wakeup enable bit[7] and wakeup to normal operation mode bit[6] are set in PMECR register.

The KSZ8851-16MLL will also assert PME output pin if the corresponding enable bit[8] is set in PMECR (0xD4) register or generate interrupt to signal an energy detect event occurred if the corresponding enable bit[2] is set in IER (0x90) register. Once the power management unit detects the PME output asserted or interrupt active, it will power up the host CPU and issue a wakeup command which is a read cycle to read the Globe Reset Register (GRR at 0x26) to wake up the KSZ8851-16MLL from the low power state to the normal power state in case the auto-wakeup enable bit[7] is disabled. When KSZ8851-16MLL is at normal power state, it is able to transmit or receive packet from the cable.

3.1.6 WAKE-ON-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. In all of these instances, the network device is pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic. The KSZ8851-16MLL controller can be programmed to notify the host of the wake-up frame detection with the assertion of the interrupt signal (INTRN) or assertion of the power management event signal (PME).

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state (working).

A wake-up signal is caused by:

1. Detection of energy signal over a pre-configured value (bit 2 in ISR register)
2. Detection of a linkup in the network link state (bit 3 in ISR register)
3. Receipt of a Magic Packet (bit 4 in ISR register)
4. Receipt of a network wake-up frame (bit 5 in ISR register)

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own ways.

3.1.7 DETECTION OF ENERGY

The energy is detected from the cable and is continuously presented for a time longer than pre-configured value, especially when this energy change may impact the level at which the system should re-enter to the normal power state.

3.1.8 DETECTION OF LINKUP

Link status wake events are useful to indicate a linkup in the network's connectivity status.

3.1.9 WAKE-UP PACKET

Wake-up packets are certain types of packets with specific CRC values that a system recognizes as a wake-up frame. The KSZ8851-16MLL supports up to four users defined wake-up frames as below:

- Wake-up frame 0 is defined in wakeup frame registers (0x30 – 0x3B) and is enabled by bit 0 in wakeup frame control register (0x2A).
- Wake-up frame 1 is defined in wakeup frame registers (0x40 – 0x4B) and is enabled by bit 1 in wakeup frame control register (0x2A).

- Wake-up frame 2 is defined in wakeup frame registers (0x50 – 0x5B) and is enabled by bit 2 in wakeup frame control register (0x2A).
- Wake-up frame 3 is defined in wakeup frame registers (0x60 – 0x6B) and is enabled by bit 3 in wakeup frame control register (0x2A).

3.1.10 MAGIC PACKET™

Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a LAN. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the LAN controller, and when the LAN controller receives a Magic Packet frame, it will alert the system to wake up.

Magic Packet is a standard feature integrated into the KSZ8851-16MLL. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ8851-16MLL has been put into Magic Packet Enable mode (WFCR[7]=1), it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as Source Address (SA), Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

Example:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE – MISC - FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - MISC - CRC.

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination.

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8851-16MLL controller detects the data sequence, however, it then alerts the PC's power management circuitry (assert the PME pin) to wake up the system.

3.2 Physical Layer Transceiver (PHY)

3.2.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 3.01 kΩ (1%) resistor for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

3.2.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

3.2.3 PLL CLOCK SYNTHESIZER (RECOVERY)

The internal PLL clock synthesizer can generate either 125 MHz, 62.5 MHz, 41.66 MHz, or 25 MHz clocks by setting the on-chip bus control register (0x20) for KSZ8851-16MLL system timing. These internal clocks are generated from an external 25 MHz crystal or oscillator.

3.2.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.2.5 10BASE-T TRANSMIT

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.4V amplitude. The harmonic contents are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.2.6 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP1 or RXM1 input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8851-16MLL decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.2.7 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8851-16MLL supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8851-16MLL device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers. The IEEE 802.3u standard MDI and MDI-X definitions are shown in Table 3-2.

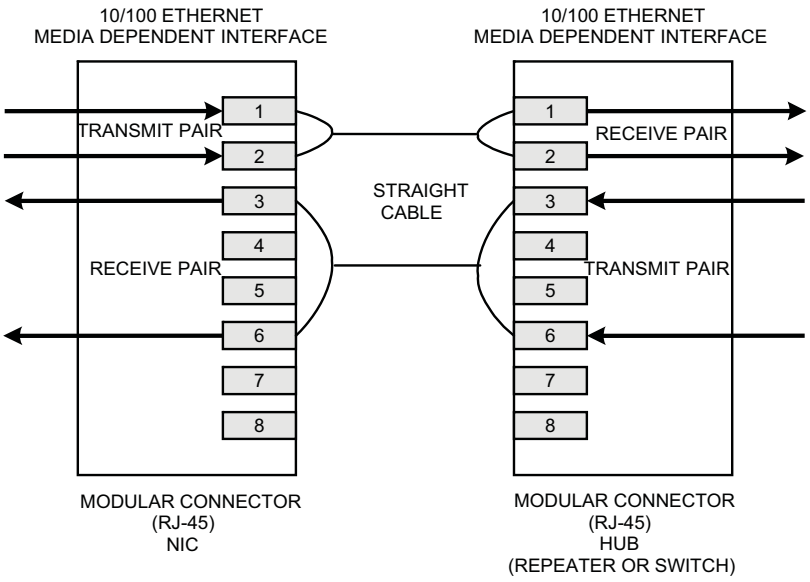
TABLE 3-2: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ45 Pins	**Signals**	**RJ45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.2.8 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device or an MDI-X device to an MDI device. The following diagram shows a typical straight cable connection between a network interface card (NIC) and a switch, or hub (MDI-X).

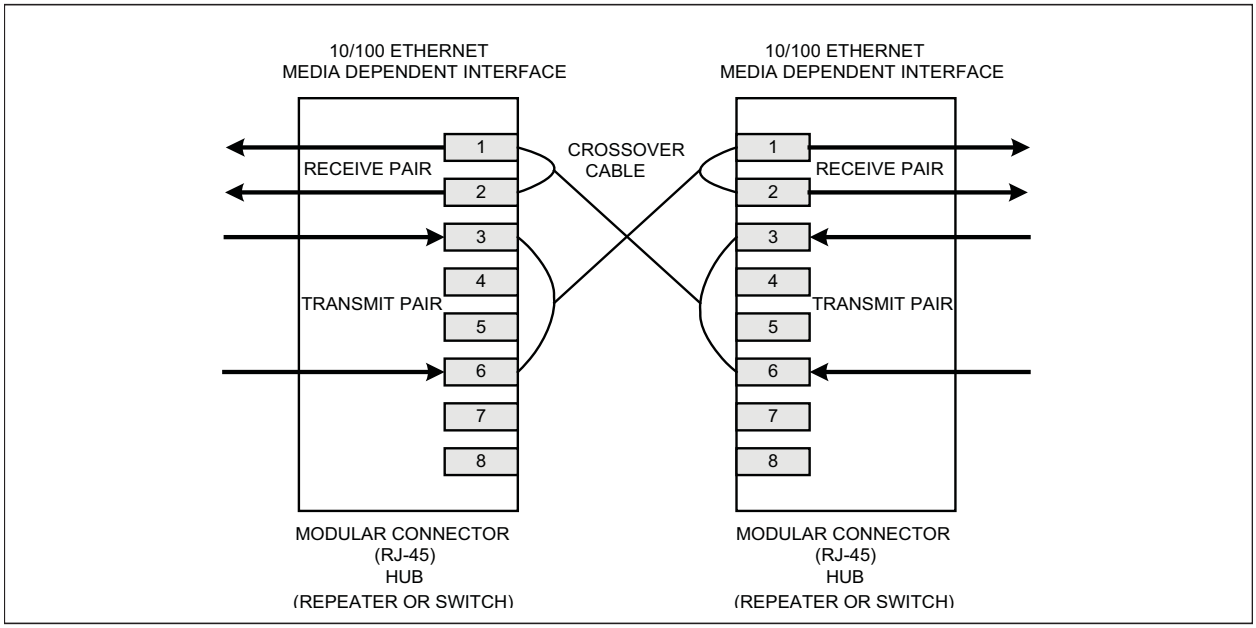
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.2.9 CROSSOVER TABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two chips or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION

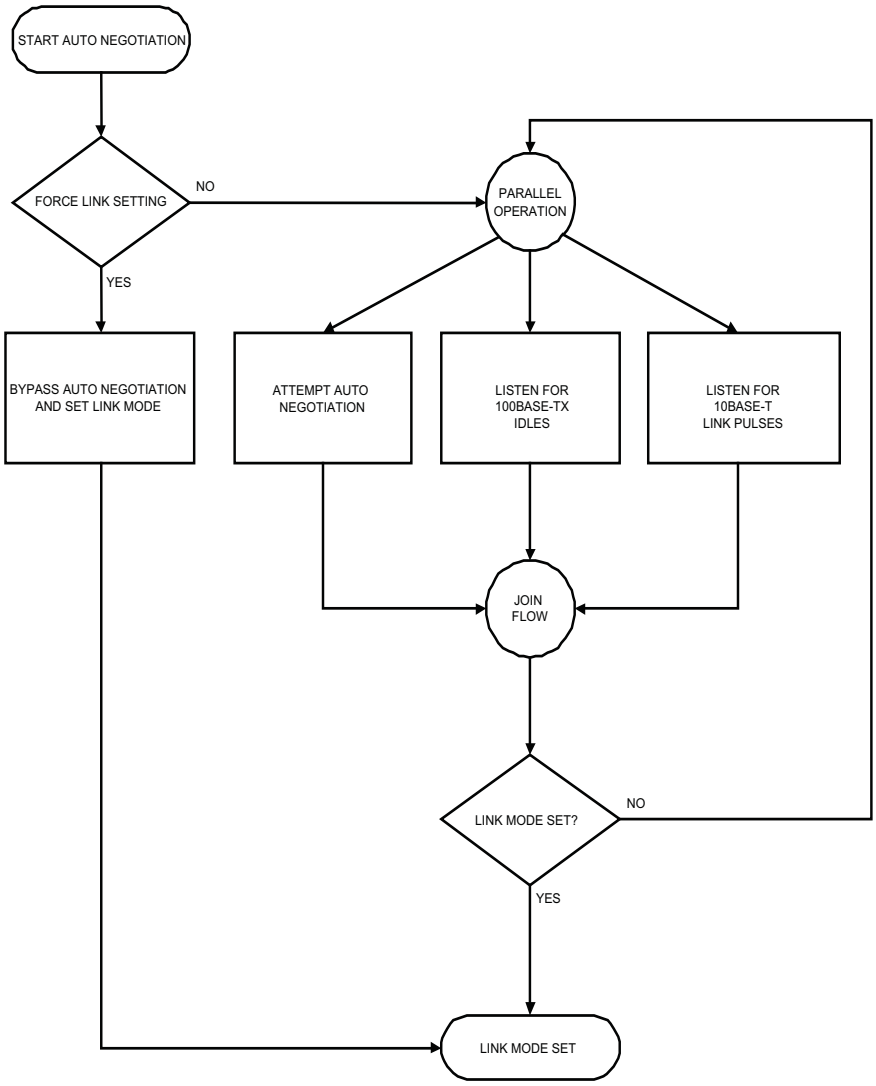


3.2.10 AUTO NEGOTIATION

The KSZ8851-16MLL conforms to the auto negotiation protocol as described by the 802.3 committee to allow the port to operate at either 10BASE-T or 100BASE-TX.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8851-16MLL is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol. The auto negotiation link setup is shown as follows:

FIGURE 3-3: AUTO NEGOTIATION AND PARALLEL OPERATION



3.2.11 LINKMD® CABLE DIAGNOSTICS

The KSZ8851-16MLL LinkMD® uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format in register P1SCLMD[8:0].

Note: cable diagnostics are only valid for copper connections – fiber-optic operation is not supported.

3.2.11.1 Access

LinkMD is initiated by accessing register P1SCLMD, the PHY special control/status and LinkMD register (0xF4).

3.2.11.2 Usage

LinkMD can be run at any time by ensuring that Auto-MDIX has been disabled. To disable Auto-MDIX, write a ‘1’ to P1CR[10] to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P1SCLMD [12], is set to ‘1’ to start the test on this pair.

When bit P1SCLMD[12] returns to ‘0’, the test is complete. The test result is returned in bits P1SCLMD[14:13] and the distance is returned in bits P1SCLMD[8:0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD failed

If P1SCLMD[14:13]=11, this indicates an invalid test, and occurs when the KSZ8851-16MLL is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8851-16MLL to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance can be approximated by the following formula:

P1SCLMD[8:0] x 0.4m for port 1 cable distance

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.3 Media Access Control (MAC) Operation

The KSZ8851-16MLL strictly abides by IEEE 802.3 standards to maximize compatibility.

3.3.1 INTER PACKET GAP (IPG)

If a frame is successfully transmitted, then the minimum 96-bit time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bit time for IPG is measured from carrier sense (CRS) to the next transmit packet.

3.3.2 BACK-OFF ALGORITHM

The KSZ8851-16MLL implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

3.3.3 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

3.3.4 FLOW CONTROL

The KSZ8851-16MLL supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8851-16MLL receives a pause control frame, the KSZ8851-16MLL will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8851-16MLL are transmitted.

On the transmit side, the KSZ8851-16MLL has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources.

There are three programmable low watermark register FCLWR (0xB0), high watermark register FCHWR (0xB2) and overrun watermark register FCOWR (0xB4) for flow control in RXQ FIFO. The KSZ8851-16MLL will send PAUSE frame when the RXQ buffer hit the high watermark level (default 3.072 KB available) and stop PAUSE frame when the RXQ buffer hit the low watermark level (default 5.12 KB available). The KSZ8851-16MLL will drop packet when the RXQ buffer hit the overrun watermark level (default 256 Bytes available).

The KSZ8851-16MLL issues a flow control frame (Xoff, or transmitter off), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8851-16MLL sends out the another flow control frame (Xon, or transmitter on) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

3.3.5 HALF-DUPLEX BACKPRESSURE

A half-duplex backpressure option (non-IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as in full-duplex mode. If backpressure is required, the KSZ8851-16MLL sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8851-16MLL discontinues the carrier sense backpressure and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. The short silent time is about 4 µs and repeat every 1.64 ms in the backpressure jam patter for 10BASE-T. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collision and carrier sense is maintained to prevent packet reception.

3.3.6 ADDRESS FILTERING FUNCTION

The KSZ8851-16MLL supports 11 different address filtering schemes as shown in Table 3-3. The Ethernet destination address (DA) field inside the packet is the first 6-byte field which uses to compare with either the host MAC address registers (0x10 – 0x15) or the MAC address hash table registers (0xA0 – 0xA7) for address filtering operation. The first bit (bit 40) of the destination address (DA) in the Ethernet packet decides whether this is a physical address if bit 40 is “0” or a multicast address if bit 40 is “1”.

TABLE 3-3: ADDRESS FILTERING SCHEME

Item	Address Filtering Mode	Receive Control Register (0x74 – 0x75): RXCR1				Description
		RX All (Bit 4)	RX Inverse (Bit 1)	RX Physical Address (Bit 11)	RX Multicast Address (Bit 8)	
1	Perfect	0	0	1	1	All Rx frames are passed only if the DA exactly matches the MAC address in MARL, MARM and MARH registers.
2	Inverse perfect	0	1	1	1	All Rx frames are passed if the DA is not matching the MAC address in MARL, MARM and MARH registers.
3	Hash only	0	0	0	0	All Rx frames with either multicast or physical destination address are filtering against the MAC address hash table.

Item	Address Filtering Mode	Receive Control Register (0x74 – 0x75): RXCR1				Description
		RX All (Bit 4)	RX Inverse (Bit 1)	RX Physical Address (Bit 11)	RX Multicast Address (Bit 8)	
4	Inverse hash only	0	1	0	0	All Rx frames with either multicast or physical destination address are filtering not against the MAC address hash table. All Rx frames which are filtering out at item 3 (Hash only) only are passed in this mode.
5	Hash perfect (Default)	0	0	1	0	All Rx frames are passed with Physical address (DA) matching the MAC address and to enable receive multicast frames that pass the hash table when Multicast address is matching the MAC address hash table.
6	Inverse hash perfect	0	1	1	0	All Rx frames which are filtering out at item 5 (Hash perfect) only are passed in this mode.
7	Promiscuous	1	1	0	0	All Rx frames are passed without any conditions.
8	Hash only with Multicast address passed	1	0	0	0	All Rx frames are passed with Physical address (DA) matching the MAC address hash table and with Multicast address without any conditions.
9	Perfect with Multicast address passed	1	0	1	1	All Rx frames are passed with Physical address (DA) matching the MAC address and with Multicast address without any conditions.
10	Hash only with Physical address passed	1	0	1	0	All Rx frames are passed with Multicast address matching the MAC address hash table and with Physical address without any conditions.
11	Perfect with Physical address passed	1	0	0	1	All Rx frames are passed with Multicast address matching the MAC address and with Physical address without any conditions.
Note 1: 3.Bit 0 (RX Enable), Bit 5 (RX Unicast Enable) and Bit 6 (RX Multicast Enable) must set to 1 in RXCR1 register. **2:** 4.The KSZ8851-16MLL will discard frame with the same SA as the MAC address if bit[0] is set in RXCR2 register.						

3.3.7 CLOCK GENERATOR

The X1 and X2 pins are connected to a 25 MHz crystal. X1 can also serve as the connector to a 3.3V, 25 MHz oscillator (as described in the Pin Description and Configuration section).

3.4 Bus Interface Unit (BIU)

The BIU host interface is a generic shared data bus interface, designed to communicate with embedded processors. No glue logic is required when it talks to various standard asynchronous buses and processors.

3.4.1 SUPPORTED TRANSFERS

In terms of transfer type, the BIU can support asynchronous transfer or SRAM-like slave mode. To support the data transfers, the BIU provides a group of signals:

Shared Data bus SD[15:0] for Address, Data and Byte Enable, Command (CMD), Chip Select Enable (CSN), Read (RDN), Write (WRN) and Interrupt (INTRN).

3.4.2 PHYSICAL DATA BUS SIZE

The BIU supports an 8-bit or 16-bit host standard data bus. Depending on the size of the physical data bus, the KSZ8851-16MLL can support 8-bit or 16-bit data transfers.

For example:

For a 16-bit data bus mode, the KSZ8851-16MLL allows an 8-bit and 16-bit data transfer.

For an 8-bit data bus mode, the KSZ8851-16MLL only allows an 8-bit data transfer.

The KSZ8851-16MLL supports internal data byte-swap. This means that the system/host data bus HD[7:0] just connect to SD[7:0] for an 8-bit data bus interface. For a 16-bit data bus, the system/host data bus HD[15:8] and HD[7:0] only need to connect to SD[15:8] and SD[7:0] respectively.

Table 3-4 describes the BIU signal grouping.

TABLE 3-4: BUS INTERFACE UNIT SIGNAL GROUPING

Signal	Type	Function
SD[15:0]	I/O	**Shared Data Bus** Data D[15:0] → SD[15:0] access when CMD=0. Address A[7:2] → SD[7:2] and Byte Enable BE[3:0] → SD[15:12] access when CMD=1 in 16-bit mode. Address A[7:0] → SD[7:0] only access when CMD=1 in 8-bit mode (Shared data bus SD[15:8] must be tied to low in 8-bit bus mode).
CMD	Input	**Command Type** This command input decides the SD[15:0] shared data bus access cycle information.
CSN	Input	**Chip Select Enable** Chip Enable asserted (low) indicates that the shared data bus access is enabled.
INTRN	Output	**Interrupt** This pin is asserted to low when interrupt occurred.
RDN	Input	**Asynchronous Read** This pin is asserted to low during read cycle.
WRN	Input	**Asynchronous Write** This pin is asserted to low during write cycle.

3.4.3 LITTLE AND BIG ENDIAN SUPPORT

The KSZ8851-16MLL supports either Little- or Big-Endian microprocessor. The external strap pin 10 (EESK) is used to select between two modes. The KSZ8851-16MLL operates in Little Endian when this pin is pulled-down or in Big Endian when this pin is pulled-up.

When this pin 10 is no connect or tied to GND, the bit 11 (Endian mode selection) in RXFDPR register can be used to program either Little (bit11=0) Endian mode or Big (bit11=1) Endian mode.

3.4.4 ASYNCHRONOUS INTERFACE

For asynchronous transfers, the asynchronous interface uses RDN (read) and WRN (write) signal strobes for data latching. The host utilizes the rising edge of RDN to latch READ data when the host read data from KSZ8851-16MLL. The KSZ8851-16MLL utilizes the internal pulse to latch WRITE data based on the RXFDPR register bit 12 setting.

All asynchronous transfers are either single-data or burst-data transfers. Byte or word data bus access (transfers) is supported. The BIU, however, provides flexible asynchronous interfacing to communicate with various applications and architectures. No additional address latch is required. The BIU qualifies both CSN (Chip Select) pin and WRN (Write Enable) pin to write the Address A[7:2] and BE[3:0] value (in 16-bit mode) or Address A[7:0] value (in 8-bit mode) into KSZ8851-16MLL when CMD (Command type) pin is high. The BIU qualifies both CSN (Chip Select) pin and RDN (Read Enable) or WRN (Write Enable) pin to read or write the SD[15:0] data value from or to KSZ8851-16MLL when CMD (Command type) pin is low.

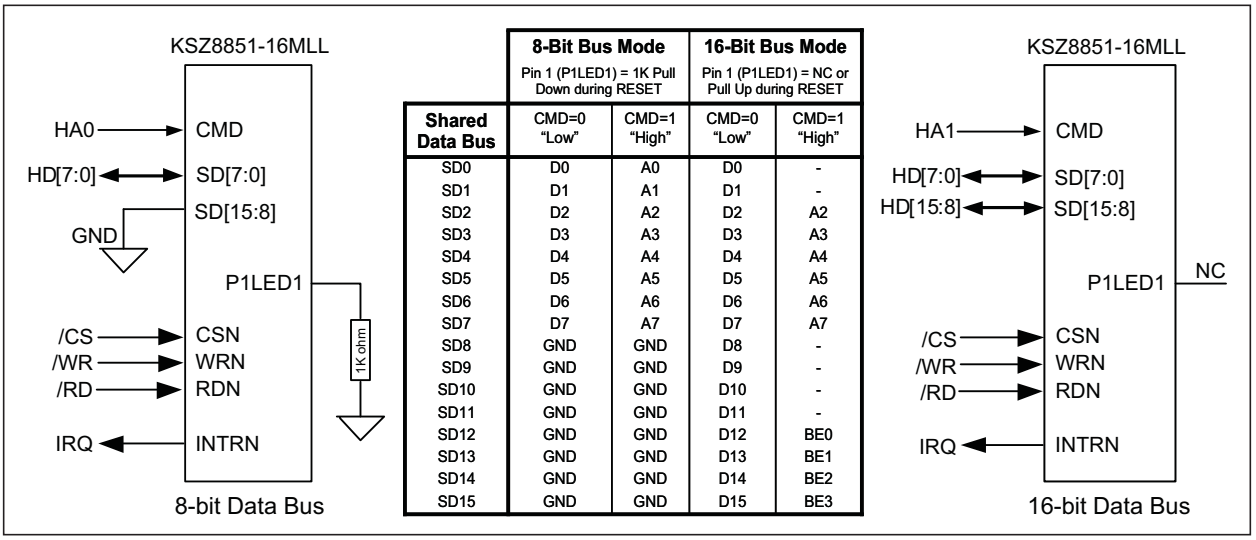
In order for software to read back the previous CMD register write value when CMD is “1”, the BIU qualifies both CSN (Chip Select) pin and RDN (Read Enable) pin to read the Address A[7:2] and BE[3:0] value (in 16-bit mode) or Address A[7:0] value (in 8-bit mode) back from KSZ8851-16MLL when CMD (Command type) pin is high.

3.4.5 BIU SUMMATION

Figure 3-4 shows the connection for different data bus sizes. Note that in 16-bit bus mode, the SD1 bit must be set to “1” when CMD = 1 during DMA access. Refer to reference schematics in hardware design package for further details.

All of control and status registers in the KSZ8851-16MLL are accessed indirectly depending on CMD (Command type) pin. The command sequence to access the specified control or status register is to write the register’s address (when CMD=1) then read or write this register data (when CMD=0). If both RDN and WRN signals in the system are only used for KSZ8851-16MLL, the CSN pin can be forced to active low to simplify the system design. The CMD pin can be connected to host address line HA0 for 8-bit bus mode or HA1 for 16-bit bus mode.

FIGURE 3-4: KSZ8851-16MLL 8-BIT AND 16-BIT DATA BUS CONNECTIONS



Shared Data Bus	8-Bit Bus Mode (Pin 1 (P1LED1) = 1K Pull Down during RESET) CMD=0 “Low”	8-Bit Bus Mode CMD=1 “High”	16-Bit Bus Mode (Pin 1 (P1LED1) = NC or Pull Up during RESET) CMD=0 “Low”	16-Bit Bus Mode CMD=1 “High”
SD0	D0	A0	D0	-
SD1	D1	A1	D1	-
SD2	D2	A2	D2	A2
SD3	D3	A3	D3	A3
SD4	D4	A4	D4	A4
SD5	D5	A5	D5	A5
SD6	D6	A6	D6	A6
SD7	D7	A7	D7	A7
SD8	GND	GND	D8	-
SD9	GND	GND	D9	-
SD10	GND	GND	D10	-
SD11	GND	GND	D11	-
SD12	GND	GND	D12	BE0
SD13	GND	GND	D13	BE1
SD14	GND	GND	D14	BE2
SD15	GND	GND	D15	BE3

3.5 Queue Management Unit (QMU)

The Queue Management Unit (QMU) manages packet traffic between the MAC/PHY interface and the system host. It has built-in packet memory for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue). Each queue contains 12 KB for RXQ and 6 KB for TXQ of memory with back-to-back, non-blocking frame transfer performance. It provides a group of control registers for system control, frame status registers for current packet transmit/receive status, and interrupts to inform the host of the real time TX/RX status.

3.5.1 TRANSMIT QUEUE (TXQ) FRAME FORMAT

The frame format for the transmit queue is shown in Table 3-5. The first word contains the control information for the frame to transmit. The second word is used to specify the total number of bytes of the frame. The packet data follows. The packet data area holds the frame itself. It may or may not include the CRC checksum depending upon whether hardware CRC checksum generation is enabled in TXCR (bit 1) register.