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KSZ8851-16/32MQL

Single-Port Ethernet MAC Controller with 8/16-Bit or 32-Bit Non-PCI Interface

Features

- Integrated MAC and PHY Ethernet Controller Fully Compliant with IEEE 802.3/802.3u Standards
- Designed for High Performance and High Throughput Applications
- Supports 10BASE-T/100BASE-TX
- Supports IEEE 802.3x Full-Duplex Flow Control and Half-Duplex Backpressure Collision Flow Control
- Supports DMA-Slave Burst Data Read and Write Transfers
- Supports IP Header (IPv4)/TCP/UDP/ICMP Checksum Generation and Checking
- Supports IPv6 TCP/UDP/ICMP Checksum Generation and Checking
- Automatic 32-bit CRC Generation and Checking
- Simple SRAM-Like Host Interface Easily Connects to Most Common Embedded MCUs
- Supports Multiple Data Frames for Transmit and Receive without Address Bus and Byte-Enable Signals
- Supports Both Big- and Little-Endian Processors
- Larger Internal Memory with 12K Bytes for RX FIFO and 6K Bytes for TX FIFO. Programmable Low, High, and Overrun Watermark for Flow Control in RX FIFO
- Efficient Architecture Design with Configurable Host Interrupt Schemes to Minimize Host CPU Overhead and Utilization
- Powerful and Flexible Address Filtering Scheme
- Optional to Use External Serial EEPROM Configuration for Both KSZ8851-16MQL and KSZ8851-32MQL
- Single 25 MHz Reference Clock for Both PHY and MAC

Power Modes, Power Supplies, and Packaging

- Single 3.3V Power Supply with Options for 1.8V, 2.5V, and 3.3V VDD I/O
- Built-In Integrated 3.3V or 2.5V to 1.8V Low Noise Regulator (LDO) for Core and Analog Blocks
- Enhanced Power Management Feature with Energy Detect Mode and Power-Down Mode to Ensure Low-Power Dissipation During Device Idle Periods
- Comprehensive LED Indicator Support for Link, Activity and 10/100 Speed (2 LEDs)
  - User Programmable
- Low-Power CMOS Design
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Flexible Package Options Available in 128-pin PQFP: KSZ8851-16/32MQL or 48-pin LQFP KSZ8851-16MLL
- Pin Compatible with Existing 128-pin KSZ8841-16/32MQL and KSZ8842-16/32MQL

Additional Features

In addition to offering all of the features of a Layer 2 controller, the KSZ8851-16/23MQL offers:

- Flexible 8-bit, 16-bit, and 32-bit Generic Host Processor Interfaces with Same Access Time and Single Bus Timing to Any I/O Registers and RX/TX FIFO Buffers
- Supports Adding Two-Bytes Before Frame Header in Order for IP Frame Content with Double Word Boundary
- LinkMD® Cable Diagnostic Capabilities to Determine Cable Length, Diagnose Faulty Cables, and Determine Distance to Fault
- Wake-on-LAN Functionality
  - Incorporates Magic Packet™, Network Link State, and Wake-Up Frame Technology
- HP Auto MDI-X™ Crossover with Disable/Enable Option
- Ability to Transmit and Receive Frames up to 2000 Bytes

Network Features

- 10BASE-T and 100BASE-TX Physical Layer Support
- Auto-Negotiation: 10/100 Mbps Full- and Half-Duplex
- Adaptive Equalizer
- Baseline Wander Correction

Applications

- Video/Audio Distribution Systems
- High-End Cable, Satellite, and IP Set-Top Boxes
- Video over IP and IPTV
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency-Critical Applications
- Home Base Station with Ethernet Connection
- Industrial Control Sensor Devices (Temp., Pressure, Levels, and Valves)
- Security, Motion Control, and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet
- Embedded Systems

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Table of Contents

1.0 INTRODUCTION

1.1 General Terms and Conventions

The following is list of the general terms used throughout this document:

BIU - Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU - Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS - Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC - Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
Cut-Through Switch	A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet.
DA - Destination Address	The address to send packets.
DMA - Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EEPROM - Electronically Erasable Programmable Read-Only Memory	A design in which memory on a chip can be erased by exposing it to an electrical charge.
EISA - Extended Industry Standard Architecture	A bus architecture designed for PCs using 80x86 processors, or an Intel 80386, 80486 or Pentium microprocessor. EISA buses are 32 bits wide and support multiprocessing.
EMI - Electro-Magnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS - Frame Check Sequence	See CRC.
FID - Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
IGMP - Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG - Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI - Inter-Symbol Interface	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.

ISA - Industry Standard Architecture — A bus architecture used in the IBM PC/XT and PC/AT.

Jumbo Packet — A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.

MDI - Medium Dependent Interface — An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore 'media dependent.'

MDI-X - Medium Dependent Interface Crossover — An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.

MIB - Management Information Base — The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).

MII - Media Independent Interface — The MII accesses PHY registers as defined in the IEEE 802.3 specification.

NIC - Network Interface Card — An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.

NPVID - Non-Port VLAN ID — The port VLAN ID value is used as a VLAN reference.

PLL - Phase-Locked Loop — An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.

PME - Power Management Event — An occurrence that affects the directing of power to different components of a system.

QMU - Queue Management Unit — Manages packet traffic between MAC/PHY interface and the system host. The QMU has built-in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue).

SA - Source Address — The address from which information has been sent.

TDR - Time Domain Reflectometry — TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal—or part of the signal—to return.

UTP - Unshielded Twisted Pair — Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.

VLAN - Virtual Local Area Network — A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

1.2 General Description

The KSZ8851M-series is a single-port controller chip with a non-PCI CPU interface and is available in 8/16-bit and 32-bit bus designs. This data sheet describes the 128-pin PQFP KSZ8851-16/32MQL for applications requiring high-performance from single-port Ethernet Controller with 8/16-bit or 32-bit generic processor interface. The KSZ8851M offers the most cost-effective solution for adding high-throughput Ethernet connectivity to traditional embedded systems.

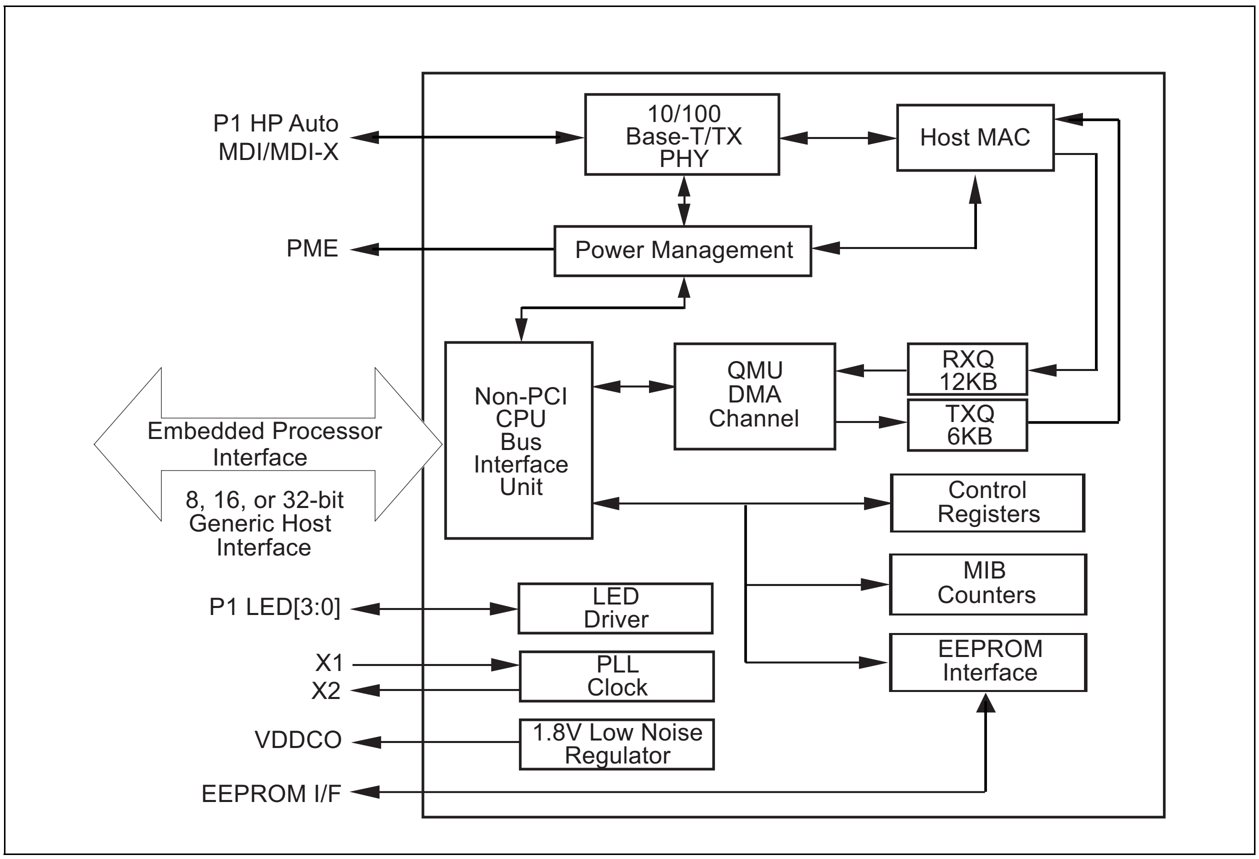
The KSZ8851M is a single-chip, mixed analog/digital device offering Wake-on-LAN technology for effectively addressing Fast Ethernet applications. It consists of a Fast Ethernet MAC controller, an 8-bit, 16-bit, and 32-bit generic host processor interface and incorporates a unique dynamic memory pointer with 4-byte buffer boundary and a fully usable 18KB for both TX (allocated 6KB) and RX (allocated 12KB) directions in host buffer interface.

The KSZ8851M is designed to be fully compliant with the appropriate IEEE 802.3 standards. An industrial temperature-grade version of the KSZ8851M, the KSZ8851MQLI, is also available.

Physical signal transmission and reception are enhanced through the use of analog circuitry, making the design more efficient and allowing for lower-power consumption. The KSZ8851M is designed using a low-power CMOS process that features a single 3.3V power supply with options for 1.8V, 2.5V, or 3.3V VDD I/O. The device includes an extensive feature set that offers management information base (MIB) counters and CPU control/data interfaces with single bus timing.

The KSZ8851M includes unique cable diagnostics feature called LinkMD®. This feature determines the length of the cabling plant and also ascertains if there is an open or short condition in the cable. Accompanying software enables the cable length and cable conditions to be conveniently displayed. In addition, the KSZ8851M supports Hewlett Packard (HP) Auto-MDIX, thereby eliminating the need to differentiate between straight or crossover cables in applications.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 128-PIN PQFP (FOR 16-BIT) ASSIGNMENT, (TOP VIEW)

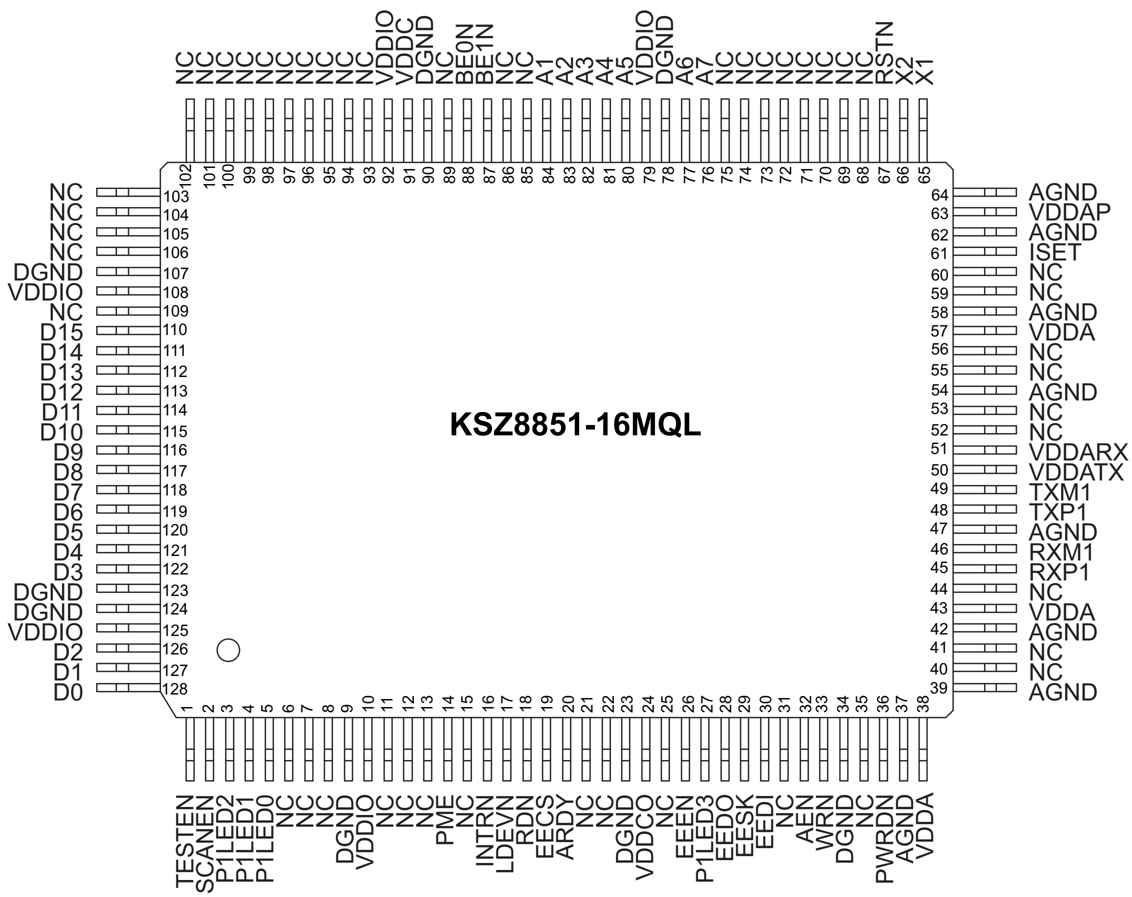


TABLE 2-1: SIGNALS FOR 16-BIT 128-PIN PQFP

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-3</th><th colspan="3">Description</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>Ipd</td><td colspan="3">Test Enable
For normal operation, open or pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>Ipd</td><td colspan="3">Scan Test Scan MUX Enable
For normal operation, open or pull-down this pin to ground.</td></tr>
<tr><td rowspan="5">3</td><td rowspan="5">P1LED2</td><td rowspan="5">Opu</td><td colspan="3">Port 1 LED indicators (Note 2-1) defined as follows:
LED is ON when output is LOW; LED is OFF when output is HIGH.</td></tr>
<tr><td rowspan="2">—</td><td colspan="2">Chip Global Control Register: CGCR bit [15,9]</td></tr>
<tr><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3 (Note 2-2)</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td rowspan="4">4</td><td rowspan="4">P1LED1</td><td rowspan="4">Ipu/O</td><td>P1LED1</td><td>Full-Duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td rowspan="2">—</td><td colspan="2">Reg. CGCR bit [15,9]</td></tr>
<tr><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td rowspan="5">5</td><td rowspan="5">P1LED0</td><td rowspan="5">Ipu/O</td><td>P1LED3 (Note 2-2)</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
<tr><td colspan="3">Note 2-1 Link = On; Activity = Blink; Link/Act = On/Blink; Full-Duplex/Col = On/Blink; Full-Duplex = On (Full-Duplex); Off (Half-Duplex) Speed = On (100BASE-T); Off (10BASE-T).
Note 2-2 P1LED3 is Pin 27.</td></tr>
<tr><td>6</td><td>NC</td><td>—</td><td colspan="3">No connect.</td></tr>
<tr><td>7</td><td>NC</td><td>—</td><td colspan="3">No connect.</td></tr>
<tr><td>8</td><td>NC</td><td>—</td><td colspan="3">No connect.</td></tr>
<tr><td>9</td><td>DGND</td><td>GND</td><td colspan="3">Digital ground.</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td colspan="3">3.3V, 2.5V, or 1.8V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>NC</td><td>—</td><td colspan="3">No connect.</td></tr>
<tr><td>12</td><td>NC</td><td>—</td><td colspan="3">No connect.</td></tr>
<tr><td>13</td><td>NC</td><td>—</td><td colspan="3">No connect.</td></tr>
<tr><td>14</td><td>PME</td><td>Ipu/O</td><td colspan="3">Power Management Event: It is asserted (low or high depends on polarity set in PMECR register) when one of the wake-on-LAN events is detected by KSZ8851M. The KSZ8851M is requesting the system to wake up from low power mode.</td></tr>
</table>

TABLE 2-1: SIGNALS FOR 16-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
15	NC	—	No connect.
16	INTRN	Opu	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set.
17	LDEVN	Opu	Local Device Not Active Low output signal, asserted when AEN is Low and A7-A1 decode to the KSZ8851M right address register. LDEVN is a combinational decode of the Address and AEN signal.
18	RDN	Ipu	Read Strobe Not Asynchronous read strobe, active low.
19	EECS	Opd	EEPROM Chip Select This signal is used to select an external EEPROM device.
20	ARDY	Opu	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. This pin need an external 4.7 kΩ pull-up resistor.
21	NC	—	No connect.
22	NC	—	No connect.
23	DGND	GND	Digital IO ground
24	VDDCO	P	1.8V regulator output. This 1.8V output pin provides power to pins 38, 43, 57 (VDDA), 63 (VDDAP), and 91 (VDDC) for core V_{DD} supply. If VDD_IO is set for 1.8V then this pin should be left floating, pins 38, 43, 57 (VDDA), 63 (VDDAP), and 91 (VDDC) will be sourced by the external 1.8V supply that is tied to pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
25	NC	—	No connect.
26	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	Port 1 LED indicator See the description for pins 3, 4, and 5.
28	EEDO	Opd	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	Ipd/O	EEPROM Serial Clock: A 4 µs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM. Config Mode: The pull-up/pull-down value is latched as big or little endian mode during power-up/reset. See “Strap-In Options” section for details

TABLE 2-1: SIGNALS FOR 16-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
30	EEDI	Ipd	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin has to pull-down for 8-bit bus mode or pull-up for 16-bit mode when the EEEN pin is pull-down (without EEPROM). Config Mode: The pull-up/pull-down value is latched as 16- or 8-bit mode during power-up/reset. See “Strap-In Options” section for details.
31	NC	—	No connect
32	AEN	Ipu	Address Enable Address and chip select qualifier for the address decoding and chip enable, active low.
33	WRN	Ipu	Write Strobe Not Asynchronous write strobe, active low.
34	DGND	GND	Digital IO ground
35	NC	—	No connect.
36	PWRDN	Ipu	Full-chip power-down. Active Low (Low = Power down; High or floating = Normal operation). All I/O pins will tri-state during chip power down.
37	AGND	GND	Analog ground
38	VDDA	P	1.8V analog power supply from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
39	AGND	GND	Analog ground
40	NC	—	No connect
41	NC	—	No connect
42	AGND	GND	Analog ground
43	VDDA	P	1.8V analog power supply from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
44	NC	—	No connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	GND	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	NC	—	No connect

TABLE 2-1: SIGNALS FOR 16-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
53	NC	—	No connect
54	AGND	GND	Analog ground
55	NC	—	No connect
56	NC	—	No connect
57	VDDA	P	1.8V analog power supply from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
58	AGND	GND	Analog ground
59	NC	—	No connect (internal test only)
60	NC	—	No connect (internal test only)
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01 kΩ 1% resistor to ground.
62	AGND	GND	Analog ground
63	VDDAP	P	1.8V analog power supply for PLL from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
64	AGND	GND	Analog ground
65	X1	I	25 MHz crystal or oscillator clock connection. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ±50 ppm for either crystal or oscillator.
66	X2	O	
67	RSTN	Ipu	Reset Not Hardware reset pin (active low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V.
68	NC	—	No connect
69	NC	—	No connect
70	NC	—	No connect
71	NC	—	No connect
72	NC	—	No connect
73	NC	—	No connect
74	NC	—	No connect
75	NC	—	No connect
76	A7	Ipd	Address bus bit 7
77	A6	Ipd	Address bus bit 6
78	DGND	GND	Digital IO ground

TABLE 2-1: SIGNALS FOR 16-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
79	VDDIO	P	3.3V, 2.5V, or 1.8V digital VDDIO input power supply for IO with well decoupling capacitors.
80	A5	Ipd	Address bus bit 5
81	A4	Ipd	Address bus bit 4
82	A3	Ipd	Address bus bit 3
83	A2	Ipd	Address bus bit 2
84	A1	Ipd	Address bus bit 1
85	NC	—	No connect
86	NC	—	No connect
87	BE1N	Ipd	Byte Enable 1 Not, Active low for Data byte 1 enable (don't care in 8-bit bus mode).
88	BE0N	Ipd	Byte Enable 0 Not, Active low for Data byte 0 enable.
89	NC	—	No connect
90	DGND	GND	Digital core ground
91	VDDC	P	1.8V digital core power supply from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
92	VDDIO	P	3.3V, 2.5V, or 1.8V digital VDDIO input power supply for IO with well decoupling capacitors.
93	NC	—	No connect
94	NC	—	No connect
95	NC	—	No connect
96	NC	—	No connect
97	NC	—	No connect
98	NC	—	No connect
99	NC	—	No connect
100	NC	—	No connect
101	NC	—	No connect
102	NC	—	No connect
103	NC	—	No connect
104	NC	—	No connect
105	NC	—	No connect
106	NC	—	No connect

TABLE 2-1: SIGNALS FOR 16-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
107	DGND	GND	Digital I/O ground
108	VDDIO	P	3.3V, 2.5V, or 1.8V digital VDDIO input power supply for IO with well decoupling capacitors.
109	NC	—	No connect
110	D15	I/O (pd)	Data bus bit 15
111	D14	I/O (pd)	Data bus bit 14
112	D13	I/O (pd)	Data bus bit 13
113	D12	I/O (pd)	Data bus bit 12
114	D11	I/O (pd)	Data bus bit 11
115	D10	I/O (pd)	Data bus bit 10
116	D9	I/O (pd)	Data bus bit 9
117	D8	I/O (pd)	Data bus bit 8
118	D7	I/O (pd)	Data bus bit 7
119	D6	I/O (pd)	Data bus bit 6
120	D5	I/O (pd)	Data bus bit 5
121	D4	I/O (pd)	Data bus bit 4
122	D3	I/O (pd)	Data bus bit 3
123	DGND	GND	Digital IO ground
124	DGND	GND	Digital core ground
125	VDDIO	P	3.3V, 2.5V, or 1.8V digital VDDIO input power supply for IO with well decoupling capacitors.
126	D2	I/O (pd)	Data bus bit 2
127	D1	I/O (pd)	Data bus bit 1

TABLE 2-1: SIGNALS FOR 16-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
128	D0	I/O (pd)	Data bus bit 0

Note 2-3 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu/O = Input with internal pull-up (58 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipu = Input with internal pull-up. (58 kΩ ±30%)
Ipd = Input with internal pull-down. (58 kΩ ±30%)
Opu = Output with internal pull-up. (58 kΩ ±30%)
Opd = Output with internal pull-down. (58 kΩ ±30%)
I/O (pd) = Input/Output with internal pull-down. (58 kΩ ±30%)

FIGURE 2-2: 128-PIN PQFP (FOR 32-BIT) ASSIGNMENT, (TOP VIEW)

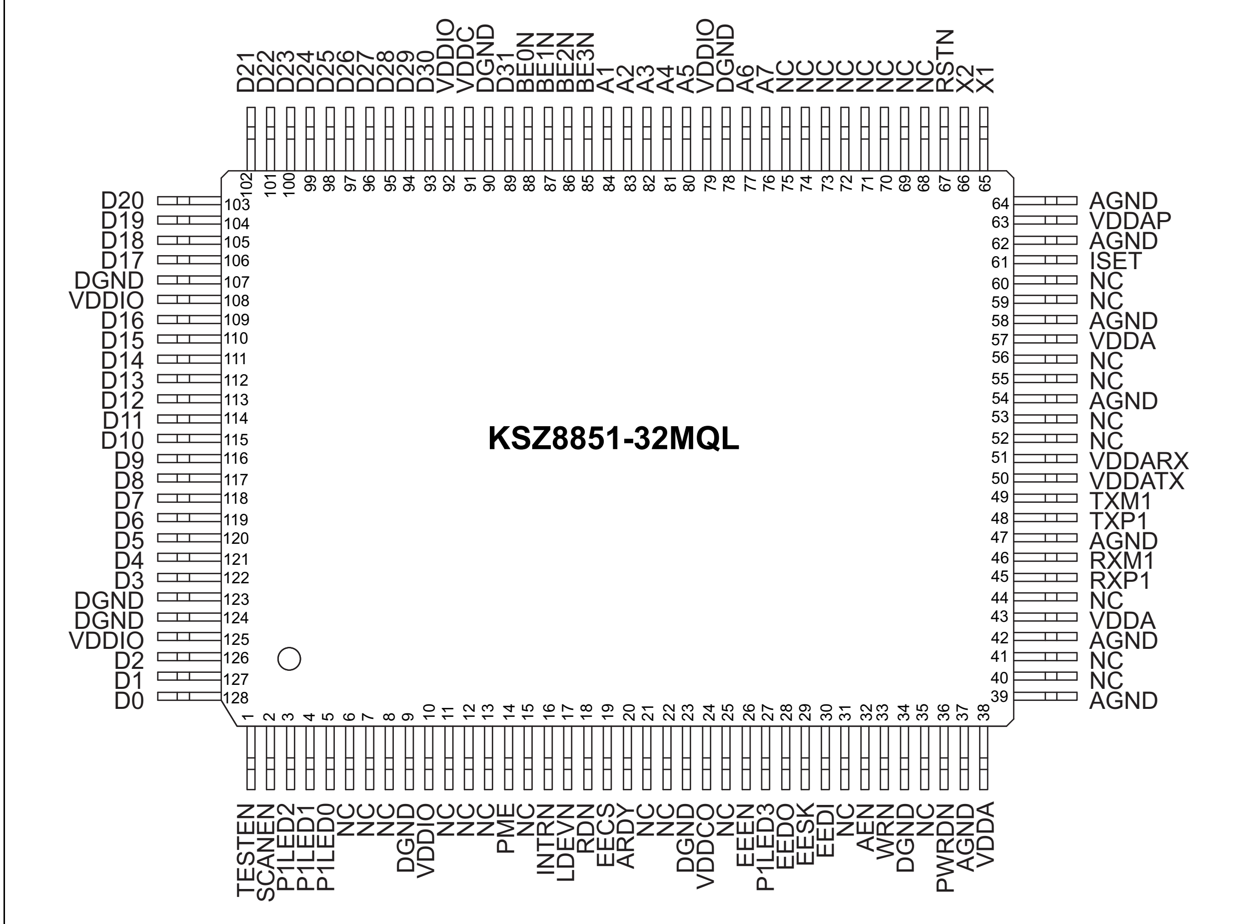


TABLE 2-2: SIGNALS FOR 32-BIT 128-PIN PQFP

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-3</th><th colspan="3">Description</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td colspan="3">Test Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td colspan="3">Scan Test Scan MUX Enable
For normal operation, pull-down this pin-to-ground.</td></tr>
<tr><td rowspan="5">3</td><td rowspan="5">P1LED2</td><td rowspan="5">Opu</td><td colspan="3">Port 1 LED indicators (Note 2-1) defined as follows:
LED is ON when output is LOW; LED is OFF when output is HIGH.</td></tr>
<tr><td rowspan="2">—</td><td colspan="2">Chip Global Control Register: CGCR bit [15,9]</td></tr>
<tr><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3 (Note 2-2)</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td rowspan="4">4</td><td rowspan="4">P1LED1</td><td rowspan="4">Ipu/O</td><td>P1LED1</td><td>Full-Duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td rowspan="2">—</td><td colspan="2">Reg. CGCR bit [15,9]</td></tr>
<tr><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td rowspan="5">5</td><td rowspan="5">P1LED0</td><td rowspan="5">Ipu/O</td><td>P1LED3 (Note 2-2)</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
<tr><td colspan="3">Note 2-1 Link = On; Activity = Blink; Link/Act = On/Blink; Full-Duplex/ Col = On/Blink; Full-Duplex = On (Full-Duplex); Off (Half-Duplex) Speed = On (100BASE-T); Off (10BASE-T)
Note 2-2 P1LED3 is Pin 27.</td></tr>
<tr><td>6</td><td>NC</td><td>—</td><td colspan="3">No connect</td></tr>
<tr><td>7</td><td>NC</td><td>—</td><td colspan="3">No connect</td></tr>
<tr><td>8</td><td>NC</td><td>—</td><td colspan="3">No connect</td></tr>
<tr><td>9</td><td>DGND</td><td>GND</td><td colspan="3">Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td colspan="3">3.3V, 2.5V, or 1.8V digital V_{DDIO} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>NC</td><td>—</td><td colspan="3">No connect</td></tr>
<tr><td>12</td><td>NC</td><td>—</td><td colspan="3">No connect</td></tr>
<tr><td>13</td><td>NC</td><td>—</td><td colspan="3">No connect</td></tr>
<tr><td>14</td><td>PME</td><td>Ipu/O</td><td colspan="3">Power Management Event: It is asserted (low or high depends on polarity set in PMECR register) when one of the wake-on-LAN events is detected by KSZ8851M. The KSZ8851M is requesting the system to wake up from low power mode.</td></tr>
<tr><td>15</td><td>NC</td><td>—</td><td colspan="3">No connect</td></tr>
<tr><td>16</td><td>INTRN</td><td>Opu</td><td colspan="3">Interrupt
Active Low signal to host CPU to indicate an interrupt status bit is set.</td></tr>
<tr><td>17</td><td>LDEVN</td><td>Opu</td><td colspan="3">Local Device Not
Active Low output signal, asserted when AEN is Low and A7-A1 decode to the KSZ8851M right address register. LDEVN is a combinational decode of the Address and AEN signal.</td></tr>
<tr><td>18</td><td>RDN</td><td>Ipu</td><td colspan="3">Read Strobe Not
Asynchronous read strobe, active low.</td></tr>
<tr><td>19</td><td>EECS</td><td>Opd</td><td colspan="3">EEPROM Chip Select
This signal is used to select an external EEPROM device.</td></tr>
</table>

TABLE 2-2: SIGNALS FOR 32-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
20	ARDY	Opu	Asynchronous Ready ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. This pin need an external 4.7 kΩ pull-up resistor.
21	NC	—	No connect
22	NC	—	No connect
23	DGND	GND	Digital IO ground
24	VDDCO	P	1.8V regulator output. This 1.8V output pin provides power to pins 38, 43, 57 (VDDA), 63 (VDDAP), and 91 (VDDC) for core V_{DD} supply. If VDD_IO is set for 1.8V then this pin should be left floating, pins 38, 43, 57 (VDDA), 63 (VDDAP), and 91 (VDDC) will be sourced by the external 1.8V supply that is tied to pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
25	NC	—	No connect
26	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	Opd	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	Ipd/O	EEPROM Serial Clock: A 4 µs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock cycle to load configuration data from the serial EEPROM. Config Mode: The pull-up/pull-down value is latched as big or little endian mode during power-up/reset. See “Strap-In Options” section for details
30	EEDI	Ipd	EEPROM Data In This pin is connected to DO output of the serial EEPROM when EEEN is pull-up. This pin is “don’t care” (no connect) for 32-bit bus mode when EEEN is pull-down (without EEPROM).
31	NC	—	No connect
32	AEN	Ipu	Address Enable Address and chip select qualifier for the address decoding and chip enable, active low.
33	WRN	Ipu	Write Strobe Not Asynchronous write strobe, active low.
34	DGND	GND	Digital IO ground
35	NC	—	No connect
36	PWRDN	Ipu	Full-chip power-down. Active Low (Low = Power down; High or floating = Normal operation). All I/O pins will tri-state during chip power down.
37	AGND	GND	Analog ground
38	VDDA	P	1.8V analog power supply from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
39	AGND	GND	Analog ground
40	NC	—	No connect
41	NC	—	No connect
42	AGND	GND	Analog ground

TABLE 2-2: SIGNALS FOR 32-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
43	VDDA	P	1.8V analog power supply from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
44	NC	—	No connect
45	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	GND	Analog ground
48	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
51	VDDARX	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
52	NC	—	No connect
53	NC	—	No connect
54	AGND	GND	Analog ground
55	NC	—	No connect
56	NC	—	No connect
57	VDDA	P	1.8V analog power supply from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
58	AGND	GND	Analog ground
59	NC	—	No connect
60	NC	—	No connect
61	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01 kΩ 1% resistor to ground.
62	AGND	GND	Analog ground
63	VDDAP	P	1.8V analog power supply for PLL from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
64	AGND	GND	Analog ground
65	X1	I	25 MHz crystal or oscillator clock connection. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ±50 ppm for either crystal or oscillator.
66	X2	O	
67	RSTN	Ipu	Reset Not Hardware reset pin (active low). This reset input is required minimum of 10 ms low after stable supply voltage 3.3V.
68	NC	—	No connect
69	NC	—	No connect
70	NC	—	No connect
71	NC	—	No connect
72	NC	—	No connect
73	NC	—	No connect
74	NC	—	No connect
75	NC	—	No connect
76	A7	Ipd	Address bus bit 7
77	A6	Ipd	Address bus bit 6

TABLE 2-2: SIGNALS FOR 32-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
78	DGND	GND	Digital IO ground
79	VDDIO	P	3.3V, 2.5V, or 1.8V digital VDDIO input power supply for IO with well decoupling capacitors.
80	A5	Ipd	Address bus bit 5
81	A4	Ipd	Address bus bit 4
82	A3	Ipd	Address bus bit 3
83	A2	Ipd	Address bus bit 2
84	A1	Ipd	Address bus bit 1
85	BE3N	Ipd	Byte Enable 3 Not, Active low for Data byte 3 enable.
86	BE2N	Ipd	Byte Enable 2 Not, Active low for Data byte 2 enable.
87	BE1N	Ipd	Byte Enable 1 Not, Active low for Data byte 1 enable.
88	BE0N	Ipd	Byte Enable 0 Not, Active low for Data byte 0 enable.
89	D31	I/O (pd)	Data bus bit 31
90	DGND	GND	Digital core ground
91	VDDC	P	1.8V digital core power supply from VDDCO (pin 24) with appropriate filtering. If VDDIO is 1.8V, this pin must be supplied power from the same source as pins 10, 79, 92, 108, and 125 (VDDIO) with appropriate filtering.
92	VDDIO	P	3.3V, 2.5V, or 1.8V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
93	D30	I/O (pd)	Data bus bit 30
94	D29	I/O (pd)	Data bus bit 29
95	D28	I/O (pd)	Data bus bit 28
96	D27	I/O (pd)	Data bus bit 27
97	D26	I/O (pd)	Data bus bit 26
98	D25	I/O (pd)	Data bus bit 25
99	D24	I/O (pd)	Data bus bit 24
100	D23	I/O (pd)	Data bus bit 23
101	D22	I/O (pd)	Data bus bit 22
102	D21	I/O (pd)	Data bus bit 21
103	D20	I/O (pd)	Data bus bit 20
104	D19	I/O (pd)	Data bus bit 19
105	D18	I/O (pd)	Data bus bit 18
106	D17	I/O (pd)	Data bus bit 17
107	DGND	GND	Digital IO ground
108	VDDIO	P	3.3V, 2.5V, or 1.8V digital V_{DDIO} input power supply for IO with well decoupling capacitors.
109	D16	I/O (pd)	Data bus bit 16
110	D15	I/O (pd)	Data bus bit 15
111	D14	I/O (pd)	Data bus bit 14
112	D13	I/O (pd)	Data bus bit 13
113	D12	I/O (pd)	Data bus bit 12
114	D11	I/O (pd)	Data bus bit 11
115	D10	I/O (pd)	Data bus bit 10
116	D9	I/O (pd)	Data bus bit 9
117	D8	I/O (pd)	Data bus bit 8

TABLE 2-2: SIGNALS FOR 32-BIT 128-PIN PQFP (CONTINUED)

Pin Number	Pin Name	Type Note 2-3	Description
118	D7	I/O (pd)	Data bus bit 7
119	D6	I/O (pd)	Data bus bit 6
120	D5	I/O (pd)	Data bus bit 5
121	D4	I/O (pd)	Data bus bit 4
122	D3	I/O (pd)	Data bus bit 3
123	DGND	GND	Digital IO ground
124	DGND	GND	Digital core ground
125	VDDIO	P	3.3V, 2.5V, or 1.8V digital VDDIO input power supply for IO with well decoupling capacitors.
126	D2	I/O (pd)	Data bus bit 2
127	D1	I/O (pd)	Data bus bit 1
128	D0	I/O (pd)	Data bus bit 0

Note 2-3 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu/O = Input with internal pull-up (58 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipu = Input with internal pull-up. (58 kΩ ±30%)
Ipd = Input with internal pull-down. (58 kΩ ±30%)
Opu = Output with internal pull-up. (58 kΩ ±30%)
Opd = Output with internal pull-down. (58 kΩ ±30%)
I/O (pd) = Input/Output with internal pull-down. (58 kΩ ±30%)

TABLE 2-3: STRAP-IN OPTIONS

Pin Number	Pin Name	Type	Description
29	EESK	Ipd/O	Endian mode select: Pull-up = Big Endian Pull-down (default) = Little Endian During power-up/reset, this pin value is latched into register CCR, bit 10. When this pin is no connect or tied to GND, the bit 11 (Endian mode selection) in RXFDPR register can be used to program either Little (bit11=0 default) Endian mode or Big (bit11=1) Endian mode.
30	EEDI	Ipd	Bus mode select for KSZ8851M when EEEN pin is pull-down without EEPROM Pull-up = 16-bit bus mode Pull-down or No connect (default) = 8-bit bus mode This pin is “don’t care” (no connect) for 32-bit bus mode when EEEN is pull-down (without EEPROM). During power-up/reset, this pin value is latched into register CCR bit 6/7.

Note 2-1 Ipd/O = Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin otherwise. Pin strap-ins are latched during power-up or reset.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8851M is a single-chip Fast Ethernet MAC/PHY controller consisting of a 10/100 physical layer transceiver (PHY), a MAC, and a Bus Interface Unit (BIU) that controls the KSZ8851M via an 8-bit, 16-bit, or 32-bit host bus interface.

The KSZ8851M is fully compliant to IEEE802.3u standards.

3.1 Functional Overview: Power Management

The KSZ8851M supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are four operation modes under the power management function which is controlled by two bits in PMECR (0xD4) register as shown below:

- PMECR[1:0] = 00 Normal Operation Mode
- PMECR[1:0] = 01 Energy Detect Mode
- PMECR[1:0] = 10 Soft Power Down Mode
- PMECR[1:0] = 11 Power Saving Mode

Table 3-1 indicates all internal function blocks status under four different power management operation modes.

TABLE 3-1: INTERNAL FUNCTION BLOCKS STATUS

KSZ8851M Function Blocks	Power Management Operation Modes			
	Normal Mode	Energy Detect Mode	Soft Power Down Mode	Power Saving Mode
Internal PLL Clock	Enabled	Disabled	Disabled	Enabled
Tx/Rx PHY	Enabled	Energy Detect at Rx	Disabled	Rx Unused Block Disabled
MAC	Enabled	Disabled	Disabled	Enabled
SPI	Enabled	Disabled	Disabled	Enabled

3.1.1 NORMAL OPERATION MODE

This is the default setting bit[1:0]=00 in PMECR register after the chip power-up or hardware reset (pin 67). When KSZ8851M is in this normal operation mode, all PLL clocks are running, PHY and MAC are on and the host interface is ready for CPU read or write.

During the normal operation mode, the host CPU can set the bit[1:0] in PMECR register to transit the current normal operation mode to any one of the other three power management operation modes.

3.1.2 ENERGY DETECT MODE

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8851M is not connected to an active link partner. For example, if cable is not present or it is connected to a powered down partner, the KSZ8851M can automatically enter to the low power state in energy detect mode. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8851M can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8851M reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit[1:0]=01 in PMECR register. When the KSZ8851M is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than pre-configured value at bit[7:0] Go-Sleep time in GSWUTR register, KSZ8851M will go into a low power state. When KSZ8851M is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable and is continuously presented for a time longer than pre-configured value at bit[15:8] Wake-Up time in GSWUTR register, the KSZ8851M will enter either the normal power state if the auto-wakeup enable bit[7] is set in PMECR register or the normal operation mode if both auto-wakeup enable bit[7] and wakeup to normal operation mode bit[6] are set in PMECR register.

The KSZ8851M will also assert PME output pin if the corresponding enable bit[8] is set in PMECR (0xD4) register or generate interrupt to signal an energy detect event occurred if the corresponding enable bit[2] is set in IER (0x90) register. Once the power management unit detects the PME output asserted or interrupt active, it will power up the host

CPU and issue a wakeup command which is a read cycle to read the Globe Reset Register (GRR at 0x26) to wake up the KSZ8851M from the low power state to the normal power state in case the auto-wakeup enable bit[7] is disabled. When KSZ8851M is at normal power state, it is able to transmit or receive packet from the cable.

3.1.3 SOFT POWER DOWN MODE

The soft power down mode is entered by setting bit[1:0]=10 in PMECR register. When KSZ8851M is in this mode, all PLL clocks are disabled, the PHY and the MAC are off, all internal registers value will not change, and the host interface is only used to wake-up this device from current soft power down mode to normal operation mode.

In order to go back the normal operation mode from this soft power down mode, the only way to leave this mode is through a host wake-up command which the CPU issues to read the Globe Reset Register (GRR at 0x26).

3.1.4 POWER SAVING MODE

The power saving mode is entered when auto-negotiation mode is enabled, cable is disconnected, and by setting bit[1:0]=11 in PMECR register and bit [10]=1 in P1SCLMD register. When KSZ8851M is in this mode, all PLL clocks are enabled, MAC is on, all internal registers value will not change, and host interface is ready for CPU read or write. In this mode, it mainly controls the PHY transceiver on or off based on line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8851M can automatically enabled the PHY power up to normal power state from power saving mode.

During this power saving mode, the host CPU can program the bit[1:0] in PMECR register and set bit[10]=0 in P1SCLMD register to transit the current power saving mode to any one of the other three power management operation modes.

3.1.5 POWER DOWN

There is a full chip power-down mode if PWRDN (pin 36) is tied to low. When this pin is pulled-down, the entire chip powers down. Transitioning this pin from pull-down to pull-up results in a power up and chip reset. The reset will set all registers to default values. The host CPU will need to re-program all register values again after release of the PWRDN.

3.1.6 WAKE-ON-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. In all of these instances, the network device is pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic. The KSZ8851M controller can be programmed to notify the host of the wake-up frame detection with the assertion of the interrupt signal (INTRN) or assertion of the power management event signal (PME).

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state (working).

A wake-up signal is caused by:

- Detection of energy signal over a pre-configured value (bit 2 in ISR register)
- Detection of a linkup in the network link state (bit 3 in ISR register)
- Receipt of a network wake-up frame (bit 5 in ISR register)
- Receipt of a Magic Packet (bit 4 in ISR register)

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own ways.

3.1.6.1 Detection of Energy

The energy is detected from the cable and is continuously presented for a time longer than pre-configured value, especially when this energy change may impact the level at which the system should re-enter to the normal power state.

3.1.6.2 Detection of Linkup

Link status wake events are useful to indicate a linkup in the network's connectivity status.

3.1.6.3 Wake-Up Packet

Wake-up packets are certain types of packets with specific CRC values that a system recognizes as a 'wake up' frame. The KSZ8851M supports up to four users defined wake-up frames as below:

1. Wake-up frame 0 is defined in wakeup frame registers (0x30 – 0x3B) and is enabled by bit 0 in wakeup frame control register (0x2A).
2. Wake-up frame 1 is defined in wakeup frame registers (0x40 – 0x4B) and is enabled by bit 1 in wakeup frame control register (0x2A).
3. Wake-up frame 2 is defined in wakeup frame registers (0x50 – 0x5B) and is enabled by bit 2 in wakeup frame control register (0x2A).
4. Wake-up frame 3 is defined in wakeup frame registers (0x60 – 0x6B) and is enabled by bit 3 in wakeup frame control register (0x2A).

3.1.6.4 Magic Packet

Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a LAN. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the LAN controller, and when the LAN controller receives a Magic Packet frame, it will alert the system to wake up.

Magic Packet is a standard feature integrated into the KSZ8851M. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ8851M has been put into Magic Packet Enable mode (WFCR[7]=1), it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as Source Address (SA), Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

Example:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE – MISC - FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - MISC - CRC.

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination.

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8851M controller detects the data sequence, however, it then alerts the PC's power management circuitry (assert the PME pin) to wake up the system.

3.2 Physical Layer Transceiver (PHY)

3.2.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 3.01 kΩ (1%) resistor for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

3.2.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

3.2.3 PLL CLOCK SYNTHESIZER (RECOVERY)

The internal PLL clock synthesizer can generate either 125 MHz, 62.5 MHz, 41.66 MHz, or 25 MHz clocks by setting the on-chip bus control register (0x20) for KSZ8851M system timing. These internal clocks are generated from an external 25 MHz crystal or oscillator.

3.2.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.2.5 10BASE-T TRANSMIT

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.4V amplitude. The harmonic contents are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.2.6 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP1 or RXM1 input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8851M decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.2.7 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8851M supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8851M device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers. The IEEE 802.3u standard MDI and MDI-X definitions are in Table 3-2.

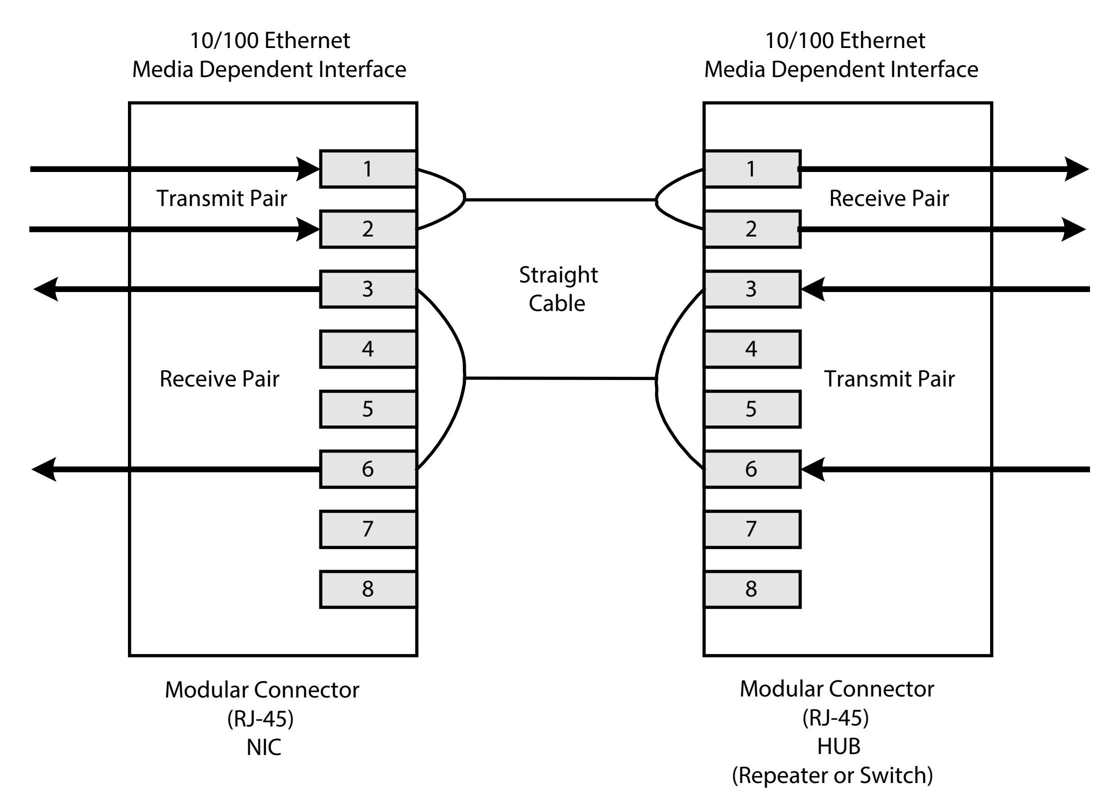
TABLE 3-2: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.2.7.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a network interface card (NIC) and a switch, or hub (MDI-X).

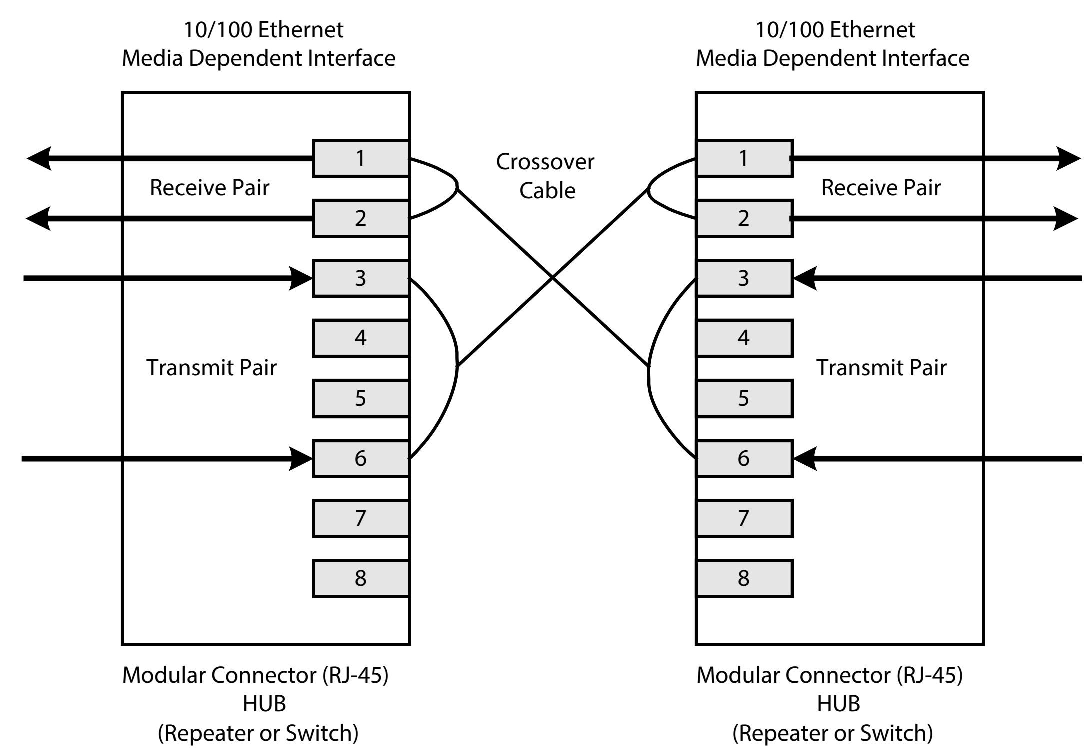
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.2.7.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



3.2.8 AUTO-NEGOTIATION

The KSZ8851M conforms to the auto negotiation protocol as described by the 802.3 committee to allow the port to operate at either 10BASE-T or 100BASE-TX.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8851M is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link up process is shown in Figure 3-3.