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KSZ8851SNL/SNLI

Single-Port Ethernet Controller with SPI

Features

- Integrated MAC and PHY Ethernet Controller Fully Compliant with IEEE 802.3/802.3u Standards
- SPI with Clock Speeds up to 40 MHz for High Throughput Applications
- Supports 10BASE-T/100BASE-TX
- Supports IEEE 802.3x Full-Duplex Flow Control and Half-Duplex Backpressure Collision Flow Control
- Supports RXQ and TXQ FIFO DMA for Fast Data Read and Write Transfers
- Supports IP Header (IPv4)/TCP/UDP/ICMP Checksum Generation and Checking
- Supports IPv6 TCP/UDP/ICMP Checksum Generation and Checking
- Automatic 32-bit CRC Generation and Checking
- Supports Simple Command and Data Phases in SPI Cycle for RXQ/TXQ FIFO and Registers Read/Write
- Supports Multiple Data Frames for TXQ FIFO and RXQ FIFO without Additional Command Phase
- Supports Flexible Byte (8-bit), Word (16-bit) and Double Word (32-bit) Read/Write Access to Internal Registers
- Larger Internal Memory with 12K Bytes for RX FIFO and 6K Bytes for TX FIFO. Programmable Low, High, and Overrun Watermark for Flow Control in RX FIFO
- Efficient Architecture Design with Configurable Host Interrupt Schemes to Minimize Host CPU Overhead and Utilization
- Powerful and Flexible Address Filtering Scheme
- Optional to Use External Serial EEPROM Configuration for MAC Address
- Single 25 MHz Reference Clock for Both PHY and MAC

Power Modes, Power Supplies, and Packaging

- Single 3.3V Power Supply with Options for 1.8V, 2.5V, and 3.3V VDD I/O
- Built-In Integrated 3.3V or 2.5V to 1.8V Low Noise Regulator (LDO) for Core and Analog Blocks
- Enhanced Power Management Feature with Energy Detect Mode and Soft Power-Down Mode to Ensure Low-Power Dissipation During Device Idle Periods
- Comprehensive LED Indicator Support for Link, Activity and 10/100 Speed (2 LEDs)
  - User Programmable
- Low-Power CMOS Design
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 32-pin (5 mm x 5 mm) QFN Package

Additional Features

In addition to offering all of the features of a Layer 2 controller, the KSZ8851SNL offers:

- Supports Adding Two-Bytes Before Frame Header in Order for IP Frame Content with Double Word Boundary
- LinkMD® Cable Diagnostic Capabilities to Determine Cable Length, Diagnose Faulty Cables, and Determine Distance to Fault
- Wake-on-LAN Functionality
  - Incorporates Magic Packet™, Wake-Up Frame, Network Link State, and Detection of Energy Signal Technology
- HP Auto MDI-X™ Crossover with Disable/Enable Option
- Ability to Transmit and Receive Frames up to 2000 Bytes

Network Features

- 10BASE-T and 100BASE-TX Physical Layer Support
- Auto-Negotiation: 10/100 Mbps Full- and Half-Duplex
- Adaptive Equalizer
- Baseline Wander Correction

Applications

- Video/Audio Distribution Systems
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Building Automation
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security, Motion Control, and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet
- Embedded Systems

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Table of Contents

1.0 INTRODUCTION

1.1 General Terms and Conventions

The following is list of the general terms used throughout this document:

BIU - Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU - Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS - Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC - Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
Cut-Through Switch	A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet.
DA - Destination Address	The address to send packets.
DMA - Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EEPROM - Electronically Erasable Programmable Read-Only Memory	A design in which memory on a chip can be erased by exposing it to an electrical charge.
EISA - Extended Industry Standard Architecture	A bus architecture designed for PCs using 80x86 processors, or an Intel 80386, 80486 or Pentium microprocessor. EISA buses are 32 bits wide and support multiprocessing.
EMI - Electro-Magnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS - Frame Check Sequence	See CRC.
FID - Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
IGMP - Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG - Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI - Inter-Symbol Interface	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.

ISA - Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
Jumbo Packet	A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.
MDI - Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore 'media dependent.'
MDI-X - Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB - Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII - Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC - Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID - Non-Port VLAN ID	The port VLAN ID value is used as a VLAN reference.
PLL - Phase Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
PME - Power Management Event	An occurrence that affects the directing of power to different components of a system.
QMU - Queue Management Unit	Manages packet traffic between MAC/PHY interface and the system host. The QMU has built-in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue).
SA - Source Address	The address from which information has been sent.
TDR - Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal—or part of the signal—to return.
UTP - Unshielded Twisted Pair	Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.
VLAN - Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

1.2 General Description

The KSZ8851SNL is a single-chip Fast Ethernet controller consisting of a 10/100 physical layer transceiver (PHY), a MAC, and a Serial Peripheral Interface (SPI). The KSZ8851SNL is designed to enable an Ethernet network connectivity with any host microcontroller equipped with SPI interface. The KSZ8851SNL offers the most cost-effective solution for adding high-throughput Ethernet link to traditional embedded systems with SPI interface.

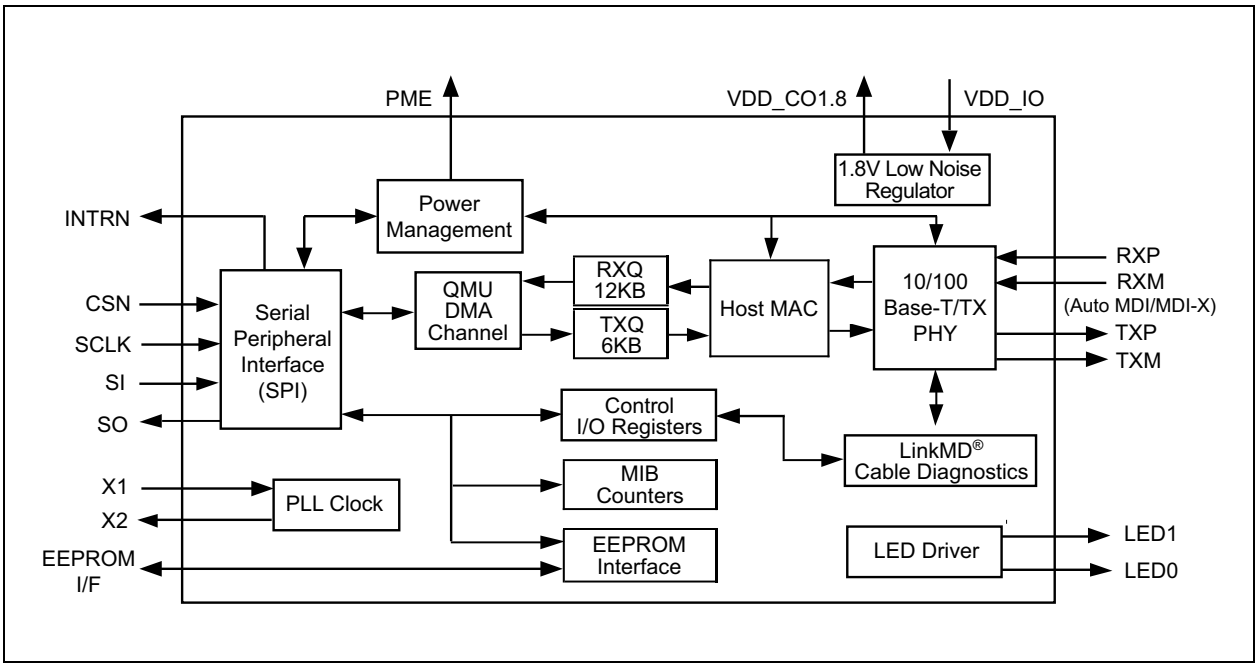
The KSZ8851SNL is a single chip, mixed analog/digital device offering Wake-on-LAN technology for effectively addressing Fast Ethernet applications. It consists of a Fast Ethernet MAC controller, SPI, and incorporates a unique dynamic memory pointer with 4-byte buffer boundary and a fully usable 18 KB for both TX (allocated 6 KB) and RX (allocated 12 KB) directions in host buffer interface.

The KSZ8851SNL is designed to be fully compliant with the appropriate IEEE 802.3 standards. An industrial temperature-grade version, the KSZ8851SNLI, is also available.

Physical signal transmission and reception are enhanced through the use of analog circuitry, making the design more efficient and allowing for lower-power consumption. The KSZ8851SNL features a single 3.3V power supply with options for 1.8V, 2.5V, or 3.3V VDD I/O. The device includes an extensive feature set that offers management information base (MIB) counters and a fast SPI interface with clock speed up to 40 MHz.

The KSZ8851SNL includes unique cable diagnostics feature called LinkMD®. This feature determines the length of the cabling plant and also ascertains if there is an open or short condition in the cable. Accompanying software enables the cable length and cable conditions to be conveniently displayed. In addition, the KSZ8851SNL supports Hewlett Packard (HP) Auto-MDIX thereby eliminating the need to differentiate between straight or crossover cables in applications.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 32-PIN 5 MM X 5 MM QFN ASSIGNMENT, (TOP VIEW)

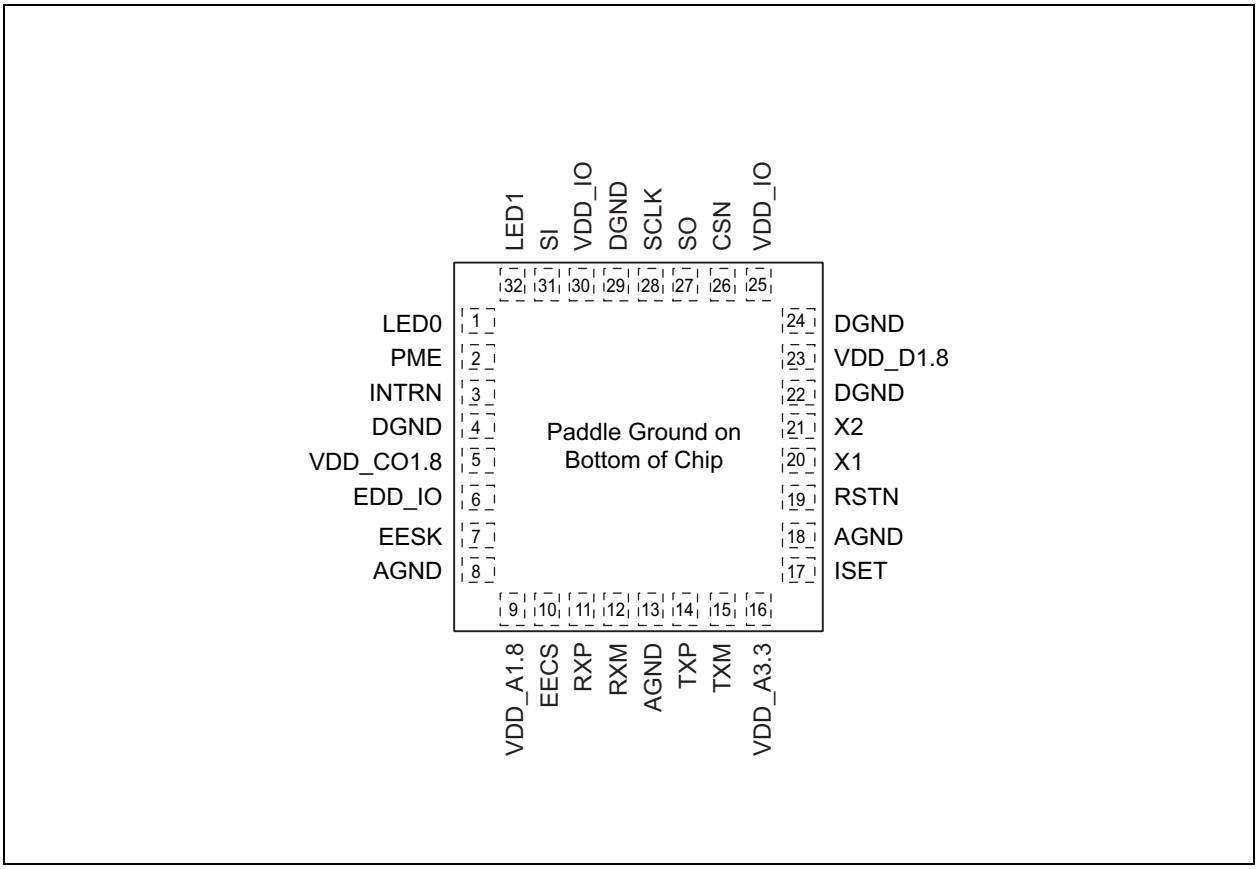


TABLE 2-1: SIGNALS

Pin Number	Pin Name	Type Note 2-1	Description		
1	LED0	Opu	Programmable LED output to indicate PHY activity/status. LED is ON when output is LOW; LED is OFF when output is HIGH. LED indicators are defined as follows:		
			—	Chip Global Control Register: CGCR bit [9]	
			—	0 (default)	1
			LED1 (Pin 32	100BT	ACT
			LED0 (Pin 1)	LINK/ACT	LINK
			Link (up) = LED On; Activity = LED Blink; Link/Act = LED On/Blink; Speed = LED On (100BASE-T); LED Off (10BASE-T)		

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
2	PME	Opu	Power Management Event (default active low) It is asserted (low or high depends on polarity set in PMECR register) when one of the wake-on-LAN events is detected by KSZ8851SNL. The KSZ8851SNL is requesting the system to wake up from low power mode.
3	INTRN	Opu	Interrupt Not An active low signal to host CPU to indicate an interrupt status bit is set. This pin needs an external 4.7 kΩ pull-up resistor.
4	DGND	GND	Digital IO ground.
5	VDD_CO1.8	P	1.8V regulator output . This 1.8V output pin provides power to pins 9 (VDD_A1.8) and 23 (VDD_D1.8) for core V_{DD} supply. If VDD_IO is set for 1.8V then this pin should be left floating, pins 9 (VDDA_1.8) and 23 (VDD_D1.8) will be sourced by the external 1.8V supply that is tied to pins 25 and 30 (VDD_IO) with appropriate filtering.
6	EED_IO	Ipd/O	In/Out Data from/to external EEPROM Config Mode: The pull-up/pull-down value is latched as with/without EEPROM during power-up/reset. See Table 2-2 for details.
7	EESK	Opd	EEPROM Serial Clock A 4 µs (OBCR[1:0]=11 on-chip bus speed @ 25 MHz) or 800 ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock to load configuration data from the serial EEPROM.
8	AGND	GND	Analog ground.
9	VDD_A1.8	P	1.8V analog power supply from VDD_CO1.8 (pin 5) with appropriate filtering. If VDD_IO is 1.8V, this pin must be supplied power from the same source as pins 25 and 30 (VDD_IO) with appropriate filtering.
10	EECS	Opd	EEPROM Chip Select This signal is used to select an external EEPROM device.
11	RXP	I/O	Physical receive (MDI) or transmit (MDIX) signal (+ differential).
12	RXM	I/O	Physical receive (MDI) or transmit (MDIX) signal (– differential).
13	AGND	GND	Analog ground.
14	TXP	I/O	Physical transmit (MDI) or receive (MDIX) signal (+ differential).
15	TXM	I/O	Physical transmit (MDI) or receive (MDIX) signal (– differential).
16	VDD_A3.3	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
17	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01 kΩ 1% resistor to ground.
18	AGND	GND	Analog ground.
19	RSTN	Ipu	Reset Not. Hardware reset pin (active low). This reset input must be held low for a minimum of 10 ms after stable supply voltage 3.3V.

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
20	X1	I	25 MHz crystal or oscillator clock connection. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is ±50 ppm for either crystal or oscillator.
21	X2	O	
22	DGND	GND	Digital IO ground
23	VDD_D1.8	P	1.8V digital power supply from VDD_CO1.8 (pin 5) with appropriate filtering. If VDD_IO is 1.8V, this pin must be supplied power from the same source as pins 25 and 30 (VDD_IO) with appropriate filtering.
24	DGND	GND	Digital IO ground
25	VDD_IO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power supply for IO with well decoupling capacitors.
26	CSN	Ipu	SPI slave mode: Chip Select Not Active low input pin for SPI interface.
27	SO	O	SPI slave mode: Serial data out for SPI interface. This SO is tri-stated output when CSN is negated and this pin must have external 4.7 kΩ pull-up to keep the SO line high while the driver is tri-stated.
28	SCLK	I	SPI slave mode: Serial clock input for SPI interface. This clock speed can run up to 40 MHz.
29	DGND	GND	Digital IO ground
30	VDD_IO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power supply for IO with well decoupling capacitors.
31	SI	Ipd	SPI slave mode: Serial data in for SPI interface.
32	LED1	Opu	Programmable LED1 output to indicate PHY activity/status (see LED0 description at pin 1).

Note 2-1
P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu/O = Input with internal pull-up (58 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin otherwise.
Ipu = Input with internal pull-up. (58 kΩ ±30%)
Ipd = Input with internal pull-down. (58 kΩ ±30%)
Opu = Output with internal pull-up. (58 kΩ ±30%)
Opd = Output with internal pull-down. (58 kΩ ±30%)

TABLE 2-2: STRAP-IN OPTIONS

Pin Number	Pin Name	Type	Description
6	EED_IO	Ipd/O	EEPROM select: Pull-up = EEPROM present Floating (NC) or Pull-down = EEPROM not present (default) During power-up / reset, this pin value is latched into register CCR, bit 9

Note 2-1 Pin strap-ins are latched during power-up or reset. See details about Ipd/O above.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8851SNL is a single-chip Fast Ethernet MAC/PHY controller consisting of a 10/100 physical layer transceiver (PHY), a MAC, and an industry standard Serial Peripheral Interface (SPI). The host CPU is via SPI interface to read/write KSZ8851SNL internal registers either byte (8-bit), word (16-bit) or double word (32-bit) and to access KSZ8851SNL RXQ/TXQ FIFOs for packet receive/transmit.

The KSZ8851SNL is fully compliant with IEEE802.3u standards.

3.1 Functional Overview: Power Management

The KSZ8851SNL supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are four operation modes under the power management function which is controlled by two bits in PMECR (0xD4) register as shown below:

- PMECR[1:0] = 00 Normal Operation Mode
- PMECR[1:0] = 01 Energy Detect Mode
- PMECR[1:0] = 10 Soft Power Down Mode
- PMECR[1:0] = 11 Power Saving Mode

Table 3-1 indicates all internal function blocks status under four different power management operation modes.

TABLE 3-1: INTERNAL FUNCTION BLOCKS STATUS

KSZ8851SNL Function Blocks	Power Management Operation Modes			
	Normal Mode	Energy Detect Mode	Soft Power Down Mode	Power Saving Mode
Internal PLL Clock	Enabled	Disabled	Disabled	Enabled
Tx/Rx PHY	Enabled	Energy Detect at Rx	Disabled	Rx Unused Block Disabled
MAC	Enabled	Disabled	Disabled	Enabled
SPI	Enabled	Disabled	Disabled	Enabled

3.1.1 NORMAL OPERATION MODE

This is the default setting bit[1:0]=00 in PMECR register after the chip power-up or hardware reset (pin 2). When KSZ8851SNL is in this normal operation mode, all PLL clocks are running, PHY and MAC are on and the host interface is ready for CPU read or write.

During the normal operation mode, the host CPU can set the bit[1:0] in PMECR register to transit the current normal operation mode to any one of the other three power management operation modes.

3.1.2 ENERGY DETECT MODE

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8851SNL is not connected to an active link partner. For example, if a cable is not present or it is connected to a powered down partner, the KSZ8851SNL can automatically enter to the low power state in energy detect mode. Once activity resumes due to plugging a cable in or from an attempt by the far end to establish link, the KSZ8851SNL can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8851SNL reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit[1:0]=01 in PMECR register. When the KSZ8851SNL is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than pre-configured value at bit[7:0] Go-Sleep time in GSWUTR register, KSZ8851SNL will go into a low power state. When KSZ8851SNL is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable and is continuously presented for a time longer than pre-configured value at bit[15:8] Wake-Up time in GSWUTR register, the KSZ8851SNL will enter either the normal power state if the auto-wakeup enable bit[7] is set in PMECR register or the normal operation mode if both auto-wakeup enable bit[7] and wakeup to normal operation mode bit[6] are set in PMECR register.

The KSZ8851SNL will also assert PME output pin if the corresponding enable bit[8] is set in PMECR (0xD4) register or generate interrupt to signal an energy detect event occurred if the corresponding enable bit[2] is set in IER (0x90) register. Once the power management unit detects the PME output asserted or interrupt active, it will power up the host

CPU and issue a wakeup command which is any one of registers read or write access to wake up the KSZ8851SNL from the low power state to the normal power state in case the auto-wakeup enable bit[7] is disabled. When KSZ8851SNL is at normal power state, it is able to transmit or receive packet from the cable.

3.1.3 SOFT POWER DOWN MODE

The soft power down mode is entered by setting bit[1:0]=10 in PMECR register. When KSZ8851SNL is in this mode, all PLL clocks are disabled, the PHY and the MAC are off, all internal registers value will not change, and the host interface is only used to wake-up this device from current soft power down mode to normal operation mode.

In order to go back the normal operation mode from this soft power down mode, the only way to leave this mode is through a host wake-up command which the CPU issues any one of registers read or write access.

3.1.4 POWER SAVING MODE

The power saving mode is entered when auto-negotiation mode is enabled, cable is disconnected, and by setting bit[1:0]=11 in PMECR register and bit [10]=1 in P1SCLMD register. When KSZ8851SNL is in this mode, all PLL clocks are enabled, MAC is on, all internal registers value will not change, and host interface is ready for CPU read or write. In this mode, it mainly controls the PHY transceiver on or off based on line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable in or from an attempt by the far end to establish link, the KSZ8851SNL can automatically enabled the PHY power up to normal power state from power saving mode.

During this power saving mode, the host CPU can program the bit[1:0] in PMECR register and set bit[10]=0 in P1SCLMD register to transit the current power saving mode to any one of the other three power management operation modes.

3.1.5 WAKE-ON-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator, or simply network traffic directly targeted to the local system. In all of these instances, the network device is pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic. The KSZ8851SNL controller can be programmed to notify the host of the wake-up frame detection with the assertion of the interrupt signal (INTRN) or assertion of the power management event signal (PME).

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state (working).

A wake-up signal is caused by:

- Detection of energy signal over a pre-configured value (bit 2 in ISR register)
- Detection of a linkup in the network link state (bit 3 in ISR register)
- Receipt of a network wake-up frame (bit 5 in ISR register)
- Receipt of a Magic Packet (bit 4 in ISR register)

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own ways.

3.1.5.1 Detection of Energy

The energy is detected from the cable and is continuously presented for a time longer than pre-configured value, especially when this energy change may impact the level at which the system should re-enter to the normal power state.

3.1.5.2 Detection of Linkup

Link status wake events are useful to indicate a linkup in the network's connectivity status.

3.1.5.3 Wake-Up Packet

Wake-up packets are certain types of packets with specific CRC values that a system recognizes as a 'wake up' frame. The KSZ8851SNL supports up to four user-defined wake-up frames as below:

1. Wake-up frame 0 is defined in wakeup frame registers (0x30 – 0x3B) and is enabled by bit 0 in wakeup frame control register (0x2A).
2. Wake-up frame 1 is defined in wakeup frame registers (0x40 – 0x4B) and is enabled by bit 1 in wakeup frame control register (0x2A).
3. Wake-up frame 2 is defined in wakeup frame registers (0x50 – 0x5B) and is enabled by bit 2 in wakeup frame

control register (0x2A).

4. Wake-up frame 3 is defined in wakeup frame registers (0x60 – 0x6B) and is enabled by bit 3 in wakeup frame control register (0x2A).

3.1.5.4 Magic Packet

Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a LAN. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the LAN controller, and when the LAN controller receives a Magic Packet frame, it will alert the system to wake up.

Magic Packet is a standard feature integrated into the KSZ8851SNL. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ8851SNL has been put into Magic Packet Enable mode (WFCR[7]=1), it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as Source Address (SA), Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

Example:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE – MISC - FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 -11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - MISC - CRC.

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination.

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8851SNL controller detects the data sequence, however, it then alerts the PC's power management circuitry (assert the PME pin) to wake up the system.

3.2 Physical Layer Transceiver (PHY)

3.2.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 3.01 kΩ (1%) resistor is connected to pin 17 (ISET) for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

3.2.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

3.2.3 PLL CLOCK SYNTHESIZER (RECOVERY)

The internal PLL clock synthesizer can generate either 125 MHz, 62.5 MHz, 41.66 MHz, or 25 MHz clocks by setting the on-chip bus control register (0x20) for KSZ8851SNL system timing. These internal clocks are generated from an external 25 MHz crystal or oscillator.

3.2.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.2.5 10BASE-T TRANSMIT

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.2.6 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8851SNL decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.2.7 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8851SNL supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8851SNL device. This feature is extremely useful when end users are unaware of cable types and also saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers or MIIM PHY registers.

The IEEE 802.3u standard MDI and MDI-X definitions are illustrated in Table 3-2.

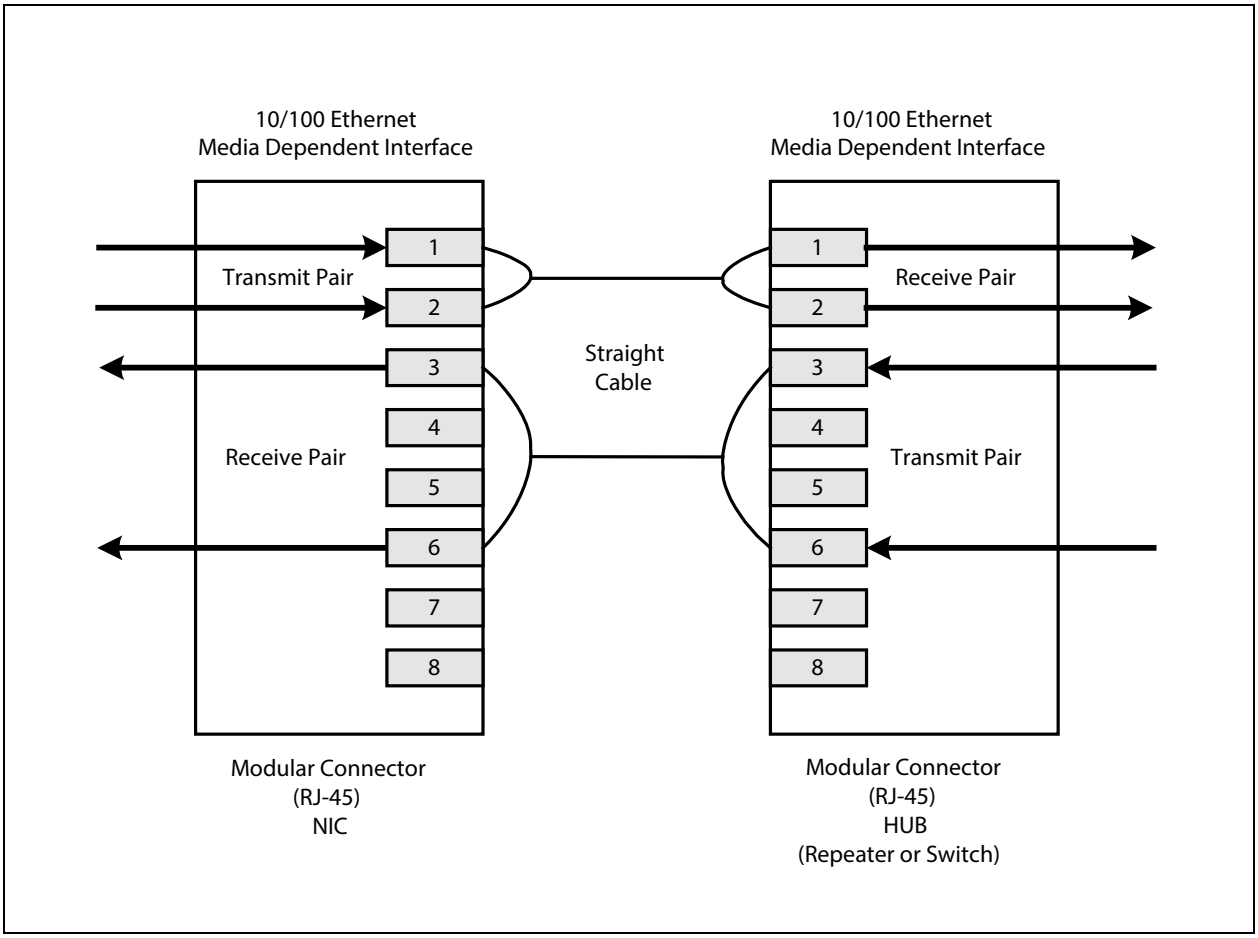
TABLE 3-2: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.2.7.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a network interface card (NIC) and a switch, or hub (MDI-X).

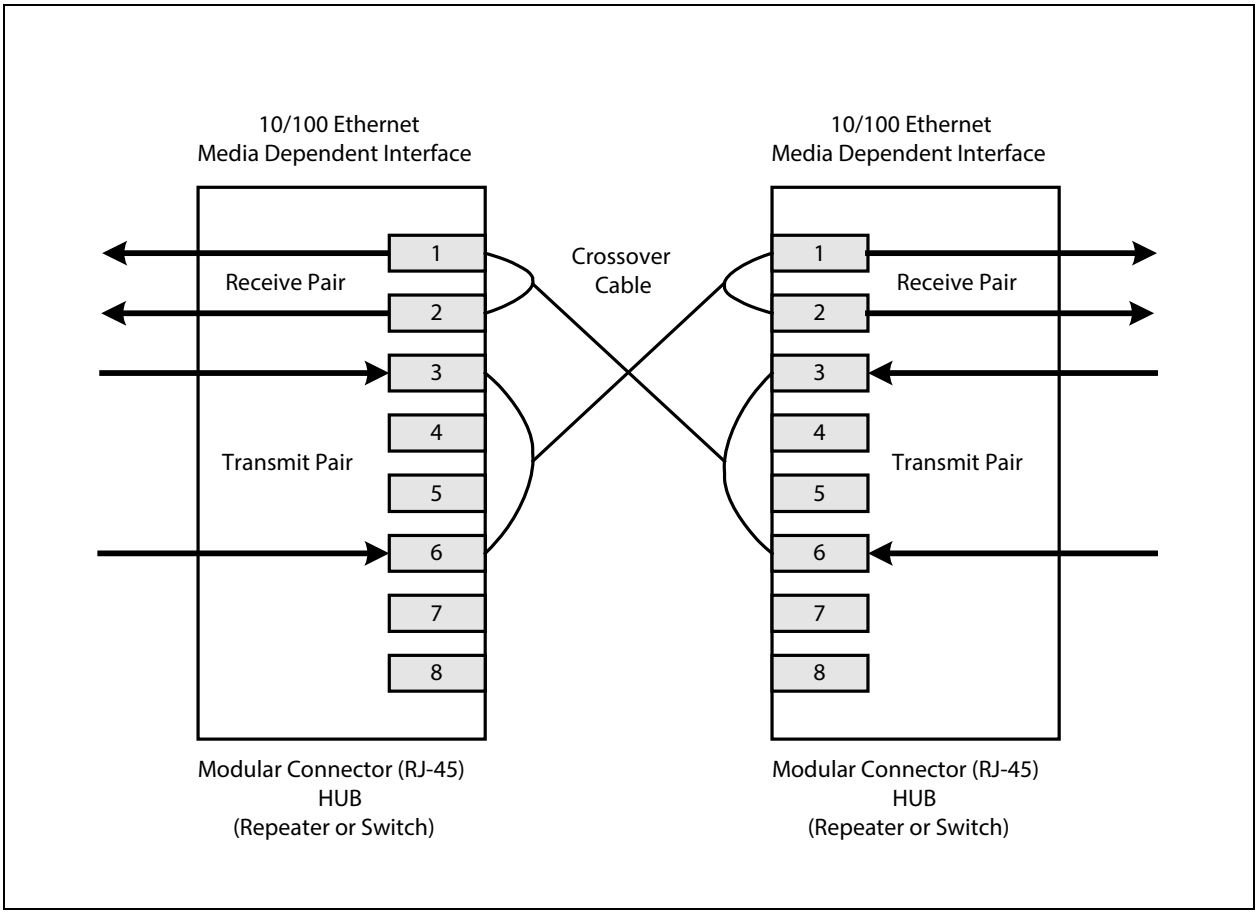
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.2.7.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



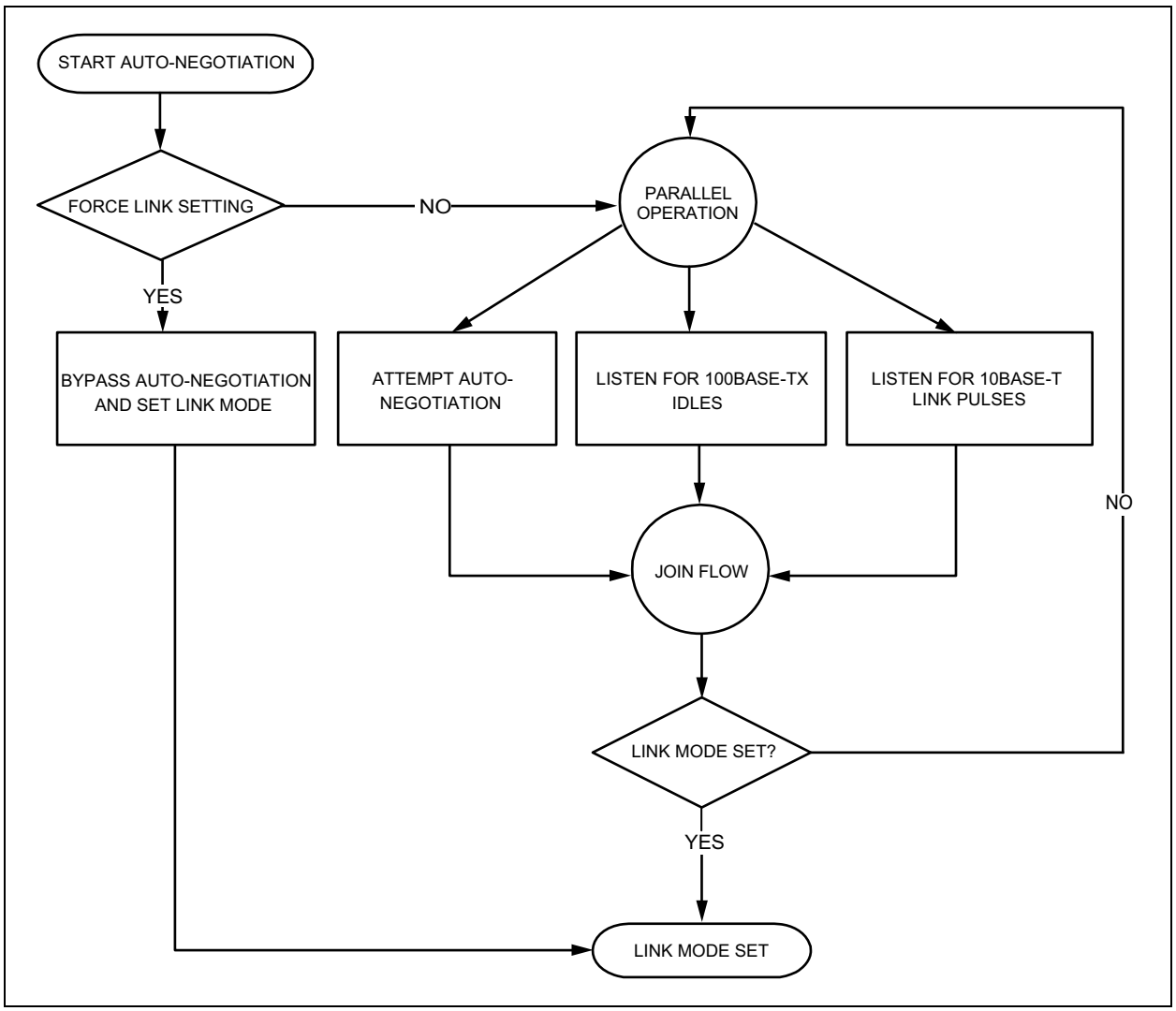
3.2.8 AUTO-NEGOTIATION

The KSZ8851SNL conforms to the auto negotiation protocol as described by the 802.3 committee to allow the port to operate at either 10BASE-T or 100BASE-TX.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8851SNL is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.2.9 LINKMD® CABLE DIAGNOSTICS

The KSZ8851SNL supports LinkMD. The LinkMD feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format in register P1SCLMD[8:0].

Cable diagnostics are only valid for copper connections and do not support fiber optic operation.

3.2.9.1 Access

LinkMD is initiated by accessing register P1SCLMD, the PHY special control/status and LinkMD register (0xF4).

3.2.9.2 Usage

LinkMD can be run at any time by ensuring that Auto-MDIX has been disabled. To disable Auto-MDIX, write a ‘1’ to P1CR[10] to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P1SCLMD [12], is set to ‘1’ to start the test on this pair.

When bit P1SCLMD[12] returns to ‘0’, the test is complete. The test result is returned in bits P1SCLMD[14:13] and the distance is returned in bits P1SCLMD[8:0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD failed

If P1SCLMD[14:13]=11, this indicates an invalid test, and occurs when the KSZ8851SNL is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8851SNL to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance can be approximated by the following formula:

P1SCLMD[8:0] x 0.4m for port 1 cable distance

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.3 Media Access Control (MAC) Operation

The KSZ8851SNL strictly abides by IEEE 802.3 standards to maximize compatibility.

3.3.1 INTER PACKET GAP (IPG)

If a frame is successfully transmitted, then the minimum 96-bit time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bit time for IPG is measured from carrier sense (CRS) to the next transmit packet.

3.3.2 BACK-OFF ALGORITHM

The KSZ8851SNL implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

3.3.3 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

3.3.4 FLOW CONTROL

The KSZ8851SNL supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8851SNL receives a pause control frame, the KSZ8851SNL will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8851SNL are transmitted.

On the transmit side, the KSZ8851SNL has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources.

There are three programmable low watermark register FCLWR (0xB0), high watermark register FCHWR (0xB2) and overrun watermark register FCOWR (0xB4) for flow control in RXQ FIFO. The KSZ8851SNL will send PAUSE frame when the RXQ buffer hit the high watermark level (default 3.072 KByte available) and stop PAUSE frame when the RXQ buffer hit the low watermark level (default 5.12 KByte available). The KSZ8851SNL will drop packet when the RXQ buffer hit the overrun watermark level (default 256-Byte available).

The KSZ8851SNL issues a flow control frame (XOFF, or transmitter off), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8851SNL sends out the another flow control frame (XON, or transmitter on) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

3.3.5 HALF-DUPLEX BACKPRESSURE

A half-duplex backpressure option (non-IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as in full-duplex mode. If backpressure is required, the KSZ8851SNL sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8851SNL discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are trans-

mitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collision and carrier sense is maintained to prevent packet reception.

3.3.6 ADDRESS FILTERING FUNCTION

The KSZ8851SNL supports 11 different address filtering schemes as shown in the following Table 3-3. The Ethernet destination address (DA) field inside the packet is the first 6-byte field which uses to compare with either the host MAC address registers (0x10 – 0x15) or the MAC address hash table registers (0xA0 – 0xA7) for address filtering operation. The first bit (bit 40) of the destination address (DA) in the Ethernet packet decides whether this is a physical address if bit 40 is “0” or a multicast address if bit 40 is “1”.

TABLE 3-3: ADDRESS FILTERING

Item	Address Filtering Mode	Receive Control Register (0x74 – 0x75): RXCR1				Description
		RX All (Bit 4)	RX Inverse (Bit 1)	RX Physical Address (Bit 11)	RX Multicast Address (Bit 8)	
1	Perfect	0	0	1	1	All Rx frames are passed only if the DA exactly matches the MAC address in MARL, MARM, and MARH registers.
2	Inverse perfect	0	1	1	1	All Rx frames are passed if the DA is not matching the MAC address in MARL, MARM, and MARH registers.
3	Hash only	0	0	0	0	All Rx frames with either multicast or physical destination address are filtering against the MAC address hash table.
4	Inverse hash only	0	1	0	0	All Rx frames with either multicast or physical destination address are filtering not against the MAC address hash table. All Rx frames which are filtering out at item 3 (Hash only) only are passed in this mode.
5	Hash perfect (default)	0	0	1	0	All Rx frames are passed with Physical address (DA) matching the MAC address and to enable receive multicast frames that pass the hash table when Multicast address is matching the MAC address hash table.
6	Inverse hash perfect	0	1	1	0	All Rx frames which are filtering out at item 5 (Hash perfect) only are passed in this mode.
7	Promiscuous	1	1	0	0	All Rx frames are passed without any conditions.
8	Hash only with multicast address passed	1	0	0	0	All Rx frames are passed with Physical address (DA) matching the MAC address hash table and with Multicast address without any conditions.
9	Perfect with multicast address passed	1	0	1	1	All Rx frames are passed with Physical address (DA) matching the MAC address and with Multicast address without any conditions.

TABLE 3-3: ADDRESS FILTERING (CONTINUED)

Item	Address Filtering Mode	Receive Control Register (0x74 – 0x75): RXCR1				Description
		RX All (Bit 4)	RX Inverse (Bit 1)	RX Physical Address (Bit 11)	RX Multicast Address (Bit 8)	
10	Hash only with physical address passed	1	0	1	0	All Rx frames are passed with Multicast address matching the MAC address hash table and with Physical address without any conditions.
11	Perfect with physical address passed	1	0	0	1	All Rx frames are passed with Multicast address matching the MAC address and with Physical address without any conditions.

Note 3-1 Bit 0 (RX Enable), Bit 5 (RX Unicast Enable) and Bit 6 (RX Multicast Enable) must be set to 1 in the RXCR1 register.

Note 3-2 The KSZ8851SNL will discard a frame with an SA that is the same as the MAC address if bit[0] is set in RXCR2 register.

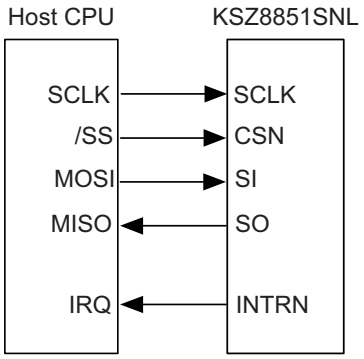
3.3.7 CLOCK GENERATOR

The X1 and X2 pins are connected to a 25 MHz crystal. X1 can also serve as the connector to a 3.3V, 25 MHz oscillator (as described in the pin description).

3.4 Serial Peripheral Interface (SPI)

The KSZ8851SNL supports an SPI in slave mode. In this mode, an external SPI master device (microcontroller or CPU) supplies the operating serial clock (SCLK), chip select (CSN), and serial input data (SI) which is clocked in on the rising edge of SCLK to KSZ8851SNL device. Serial output data (SO) is driven out by the KSZ8851SNL on the falling edge of SCLK to external SPI master device. The falling edge of CSN is starting the SPI operation and the rising edge of CSN is ending the SPI operation. The SCLK stays low state when SPI operation is idle. Figure 3-4 shows the SPI connection for KSZ8851SNL.

FIGURE 3-4: SPI INTERFACE TO KSZ8851SNL



There are four SPI operations depending on the opcode inside the command phase:

- Internal I/O registers read (opcode = 00)
- Internal I/O registers write (opcode = 01)
- RXQ FIFO read to receive packet (opcode = 10)

• TXQ FIFO write to transmit packet (opcode = 11)

As shown in Table 3-4 and Table 3-5, there are two phases in each SPI operation, the first is command phase and the following is data phase. Command phase is two bytes long for internal I/O registers access and one byte long for TXQ/RXQ FIFOs access. Data phase on internal I/O registers access is in the range of one to four bytes long depending on the specified byte enable bits B[3:0] in command phase, and data phase on TXQ or RXQ FIFOs access is limited up to 6 Kbytes for TXQ access or 12 Kbytes for RXQ access.

TABLE 3-4: SPI OPERATION FOR REGISTERS ACCESS

SPI Operation	Command Phase (SI Pin)				Data Phase (SO or SI Pins)
	Byte 0 [7:0]			Byte 1 [7:0]	
	Opcode	Byte Enable	Register Address	Don't Care Bits	
Internal I/O Register Read	0 0	B3 B2 B1 B0	A7 A6 A5 A4 A3 A2	X X X X	1 to 4 Bytes (read data on SO pin)
Internal I/O Register Write	0 1	B3 B2 B1 B0	A7 A6 A5 A4 A3 A2	X X X X	1 to 4 Bytes (write data on SI pin)

Note 3-1 In Command phase, A[7:2] access register address location in double word and B[3:0] enable which byte to access during read or write. In Data phase, the byte 0 is first in/out and byte 3 is last in/out during read or write. B[3:0] = 1: enable byte, = 0: disable byte.

TABLE 3-5: SPI OPERATION FOR TXQ/RXQ FIFO ACCESS

SPI Operation	Command Phase (SI Pin)		Data Phase (SO or SI Pins)
	Byte 0 [7:0]		
	Opcode	Don't Care Bits	
RXQ FIFO Read (12 KByte)	1 0	X X X X X X	1 to 12 KBytes (DMA read data on SO pin)
TXQ FIFO Write (6 KByte)	1 1	X X X X X X	1 to 6 KBytes (DMA write data on SI pin)

Note 3-1 The Start DMA Access bit 3 in RXQCR register must set to "1" before FIFO read/write commands. This bit must be clear to "0" when DMA operation is finished.

3.4.1 SPI INTERNAL I/O REGISTERS ACCESS OPERATION TIMING

As shown in Figure 3-5 and Figure 3-6, the SPI internal I/O registers read and write operation timing, the first two command byte 0/1 contain opcode (00: read command, 01: write command), B[3:0] Byte enable bits to indicate which data byte is available in data phase (1: byte enable, 0: byte disable) and A[7:2] address bits to access register location. The following is data phase either 1, 2, 3, or 4 bytes depending on B[3:0] setting.

FIGURE 3-5: INTERNAL I/O REGISTER READ TIMING

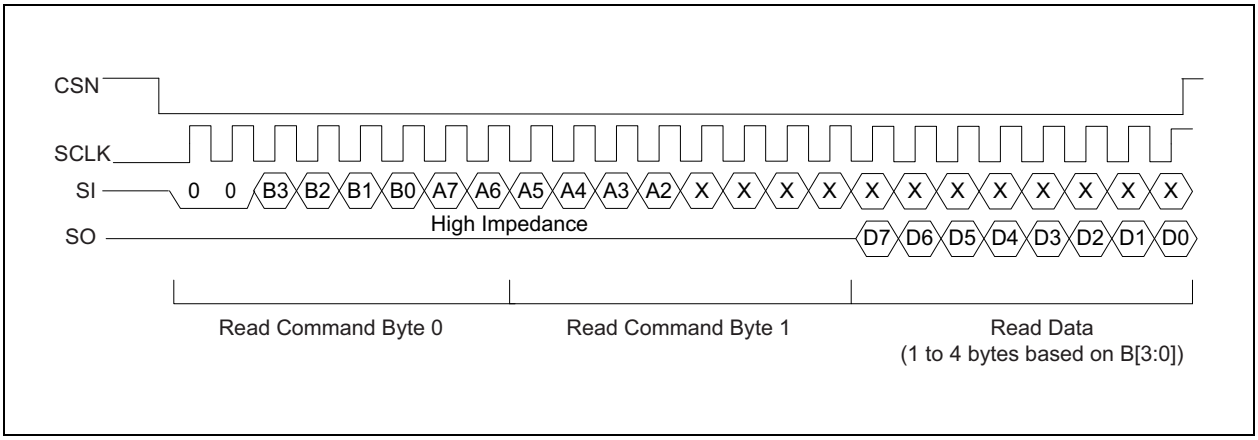
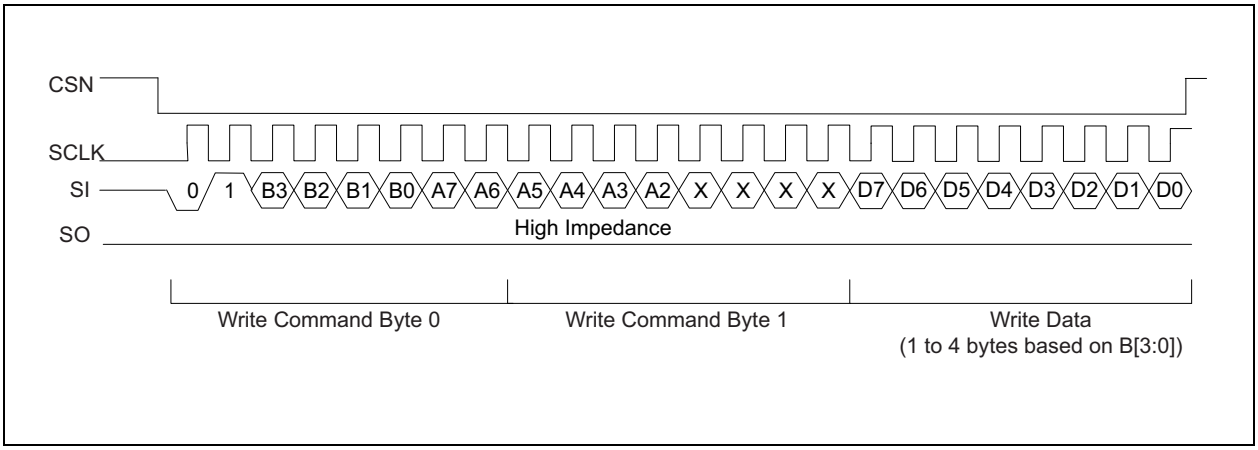


FIGURE 3-6: INTERNAL I/O REGISTER WRITE TIMING



3.4.2 SPI TXQ/RXQ FIFOS ACCESS OPERATION TIMING

Figure 3-7 and Figure 3-8 illustrate the SPI TXQ/RXQ FIFOs write and read operation timing, the first command byte 0 contains only opcode (10: read command, 11: write command) and the following is read/write data phase.

FIGURE 3-7: RXQ FIFO READ TIMING

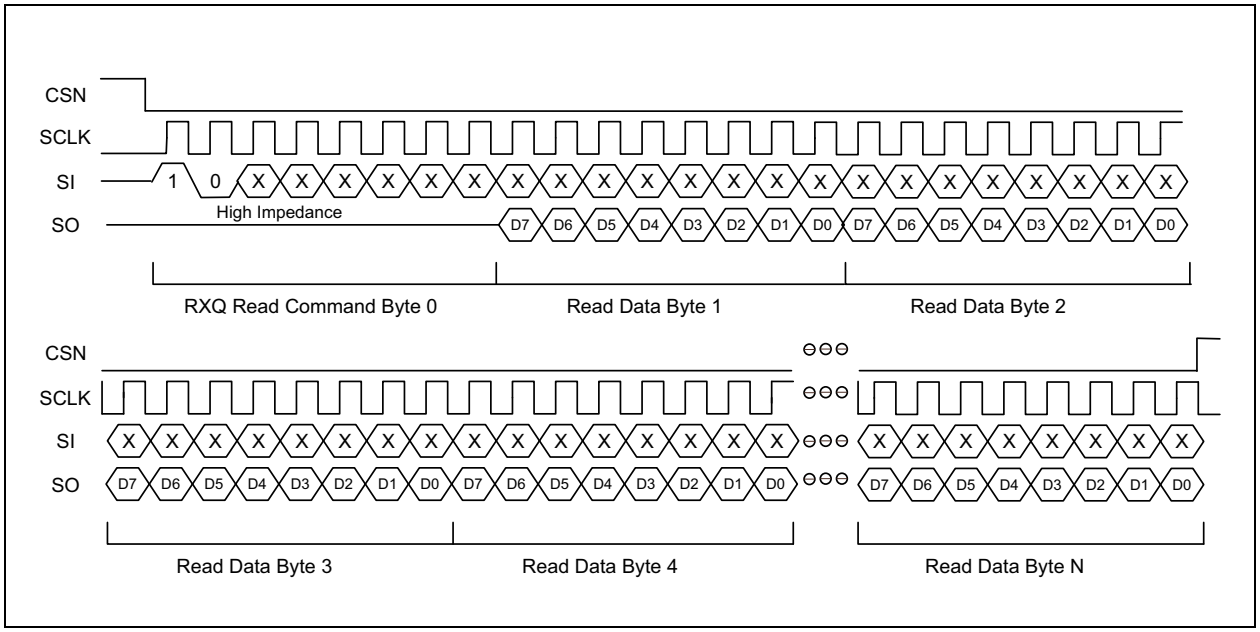
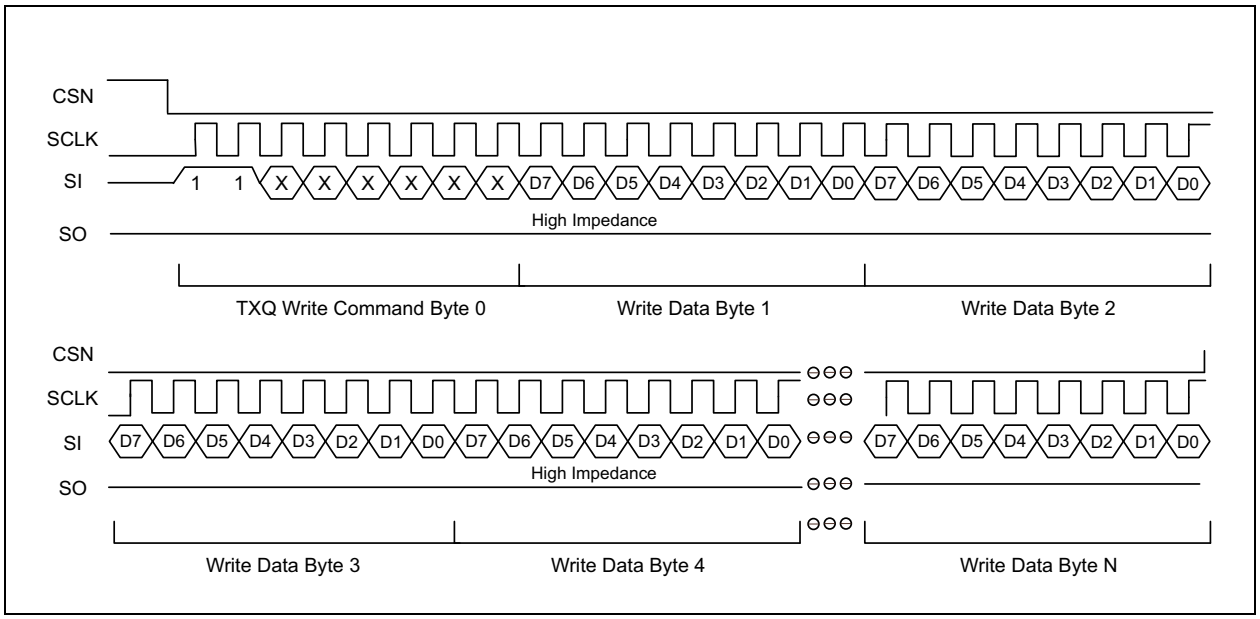


FIGURE 3-8: TXQ FIFO WRITE TIMING



3.5 Queue Management Unit (QMU)

The Queue Management Unit (QMU) manages packet traffic between the MAC/PHY interface and the system host. It has built-in packet memory for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue). Each queue contains 12 KB for RXQ and 6 KB for TXQ of memory with back-to-back, non-blocking frame transfer performance. It provides a group of control registers for system control, frame status registers for current packet transmit/receive status, and interrupts to inform the host of the real time TX/RX status.

3.5.1 TRANSMIT QUEUE (TXQ) FRAME FORMAT

The frame format for the transmit queue is shown in the following Table 3-6. The first word contains the control information for the frame to transmit. The second word is used to specify the total number of bytes of the frame. The packet data follows. The packet data area holds the frame itself. It may or may not include the CRC checksum depending upon whether hardware CRC checksum generation is enabled in TXCR (bit 1) register.

Multiple frames can be pipelined in both the transmit queue and receive queue as long as there is enough queue memory, thus avoiding overrun. For each transmitted frame, the transmit status information for the frame is located in the TXSR (0x72) register.

TABLE 3-6: FRAME FORMAT FOR TRANSMIT QUEUE

Packet Memory Address Offset	Bit 15 2nd Byte Bit 0 1st Byte
0	Control Word
2	Byte Count
4 and Up	Transmit Packet Data (maximum size is 2000)

Because multiple packets can be pipelined into the TX packet memory for transmit, the transmit status reflects the status of the packet that is currently being transferred on the MAC interface, which may or may not be the last queued packet in the TX queue.

The transmit control word is the first 16-bit word in the TX packet memory, followed by a 16-bit byte count. It must be word aligned. Each control word corresponds to one TX packet. Table 3-7 gives the transmit control word bit fields.

TABLE 3-7: TRANSMIT CONTROL WORD BIT FIELDS

Bit	Description
15	**TXIC Transmit Interrupt on Completion** When this bit is set, the KSZ8851SNL sets the transmit interrupt after the present frame has been transmitted.
14-6	Reserved
5-0	**TXFID Transmit Frame ID** This field specifies the frame ID that is used to identify the frame and its associated status information in the transmit status register.

The transmit Byte Count specifies the total number of bytes to be transmitted from the TXQ. Its format is given in Table 3-8.

TABLE 3-8: TRANSMIT BYTE COUNT FORMAT

Bit	Description
15-11	Reserved
10-0	**TXBC Transmit Byte Count** Transmit Byte Count. Hardware uses the byte count information to conserve the TX buffer memory for better utilization of the packet memory. Note: The hardware behavior is unknown if an incorrect byte count information is written to this field. Writing a 0 value to this field is not permitted.

The data area contains six bytes of Destination Address (DA) followed by six bytes of Source Address (SA), followed by a variable-length number of bytes. On transmit, all bytes are provided by the CPU, including the source address. The KSZ8851SNL does not insert its own SA. The 802.3 Frame Length word (Frame Type in Ethernet) is not interpreted by the KSZ8851SNL. It is treated transparently as data both for transmit operations.

3.5.2 FRAME TRANSMITTING PATH OPERATION IN TXQ

This section describes the typical register settings for transmitting packets from host processor to KSZ8851SNL with generic bus interface. Users can use the default value for most of the transmit registers. The following Table 3-9 describes all registers which need to be set and used for transmitting single or multiple frames.

TABLE 3-9: REGISTERS SETTING FOR TRANSMIT FUNCTION BLOCK

Register Name [bit](offset)	Description
TXCR[3:0](0x70) TXCR[8:5](0x70)	Set transmit control function as below: Set bit 3 to enable transmitting flow control. Set bit 2 to enable transmitting padding. Set bit 1 to enable transmitting CRC. Set bit 0 to enable transmitting block operation. Set transmit checksum generation for ICMP, UDP, TCP, and IP packet.
TXMIR[12:0](0x78)	The amount of free transmit memory available is represented in units of byte. The TXQ memory (6 KByte) is used for both frame payload and control word.
TXQCR[0](0x80)	For single frame to transmit, set this bit 0 = 1(manual enqueue). the KSZ8851SNL will enable current TX frame prepared in the TX buffer is queued for transmit, this is only transmit one frame at a time. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before setting up another new TX frame.
TXQCR[1](0x80)	When this bit is written as 1, the KSZ8851SNL will generate interrupt (bit 6 in ISR register) to CPU when TXQ memory is available based upon the total amount of TXQ space requested by CPU at TXNTFSR (0x9E) register. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before set to 1 again
TXQCR[2](0x80)	For multiple frames to transmit, set this bit 2 = 1 (auto-enqueue). the KSZ8851SNL will enable current all TX frames prepared in the TX buffer are queued to transmit automatically.
RXQCR[3](0x82)	Set bit 3 to start DMA access from host CPU either read (receive frame data) or write (transmit data frame)
TXFDPR[14](0x84)	Set bit 14 to enable TXQ transmit frame data pointer register increments automatically on accesses to the data register.
IER[14][6](0x90)	Set bit 14 to enable transmit interrupt in Interrupt Enable Register Set bit 6 to enable transmit space available interrupt in Interrupt Enable Register.
ISR[15:0](0x92)	Write 1 (0xFFFF) to clear all interrupt status bits after interrupt occurred in Interrupt Status Register.
TXNTFSR[15:0](0x9E)	The host CPU is used to program the total amount of TXQ buffer space which is required for next total transmit frames size in double-word count.

3.5.3 DRIVER ROUTINE FOR TRANSMIT PACKET FROM HOST PROCESSOR TO KSZ8851SNL

The transmit routine is called by the upper layer to transmit a contiguous block of data through the Ethernet controller. It is user's choice to decide how the transmit routine is implemented. If the Ethernet controller encounters an error while transmitting the frame, it's the user's choice to decide whether the driver should attempt to retransmit the same frame or discard the data. The following figures show the step-by-step for single and multiple transmit packets from host processor to KSZ8851SNL.

FIGURE 3-9: HOST TX SINGLE FRAME IN MANUAL ENQUEUE FLOW DIAGRAM