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KSZ8852HLE

Two-Port 10/100 Mb/s Ethernet Switch with 8 or 16-Bit Host Interface

Revision 1.1

General Description

The KSZ8852 product line consists of industrial capable Ethernet switches, providing integrated communication for a range of Industrial Ethernet and general Ethernet applications.

The KSZ8852 product enables distributed, daisy-chained topologies preferred for industrial Ethernet networks. Conventional centralized (i.e., star-wired) topologies are also supported for fault tolerant arrangements.

A flexible 8 or 16-bit general bus interface is provided for interfacing to an external host processor.

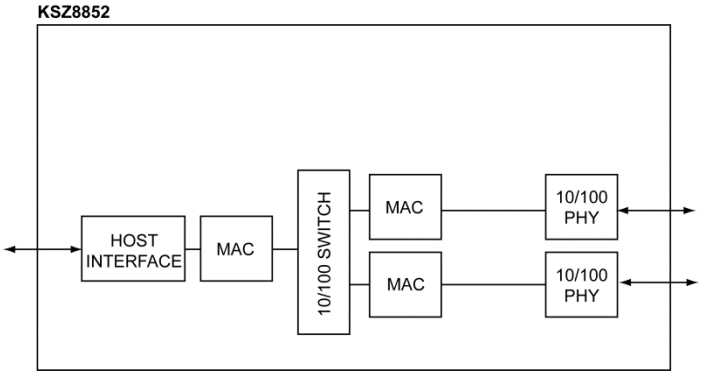
The wire-speed, store-and-forward switching fabric provides a full complement of QoS and congestion control features optimized for real-time Ethernet.

The KSZ8852 product is built upon Micrel's industry-leading Ethernet technology, with features designed to offload host processing and streamline your overall design:

- Wire-speed Ethernet switching fabric with extensive filtering
- Two integrated 10/100BASE-TX PHY transceivers, featuring the industry's lowest power consumption
- Full-featured QoS support
- Flexible management options that support common standard interfaces

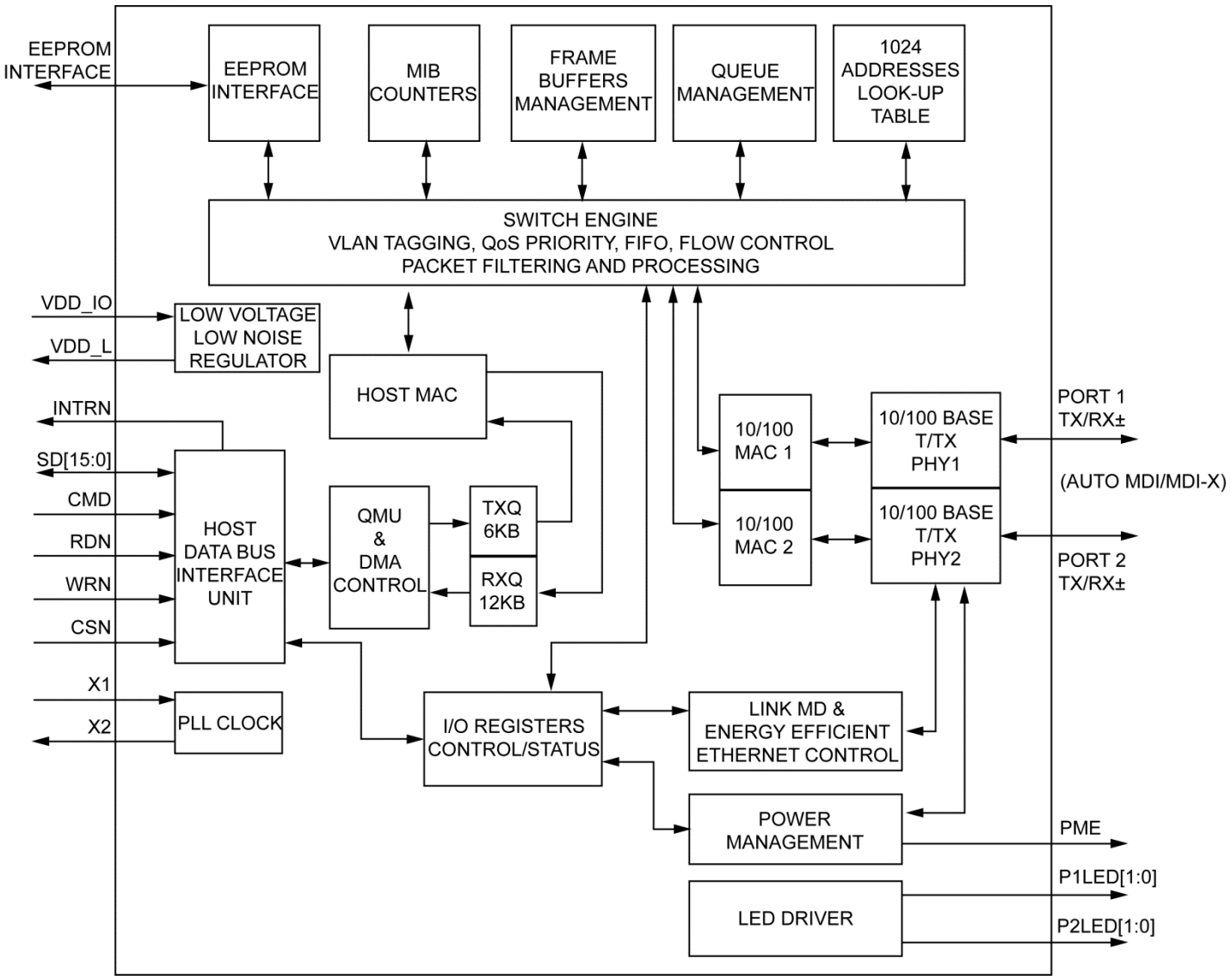
A robust assortment of power management features including energy-efficient Ethernet (EEE) have been designed in to satisfy energy-efficient environments.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.



KSZ8852 Top Level Architecture

Functional Diagram



KSZ8852HLE Functional Diagram

Features

Management Capabilities

- The KSZ8852 includes all the functions of a 10/100BASE-T/TX switch system which combines a switch engine, frame buffer management, address look−up table, queue management, MIB counters, media access controllers (MAC) and PHY transceivers
- Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 1024 entry forwarding table
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- MIB counters for fully compliant statistics gathering − 34 counters per port
- Loopback modes for remote failure diagnostics
- Rapid spanning tree protocol support (RSTP) for topology management and ring/linear recovery

Robust PHY Ports

- Two integrated IEEE 802.3 / 802.3u compliant Ethernet transceivers supporting 10BASE-T and 100BASE-TX
- On-chip termination resistors and internal biasing for differential pairs to reduce power
- HP Auto MDI/MDI-X™ crossover support eliminating the need to differentiate between straight or crossover cables in applications

MAC Ports

- Three internal media access control (MAC) units
- 2Kbyte Jumbo packet support
- Tail tagging mode (one byte added before FCS) support at Port 3 to inform the processor which ingress port receives the packet and its priority
- Programmable MAC addresses for Port 1 and Port 2 and self-address filtering support
- MAC filtering function to filter or forward unknown unicast packets

Advanced Switch Capabilities

- Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 1024 entry forwarding table
- IEEE 802.1Q VLAN for up to 16 groups with a full range of VLAN IDs
- IEEE 802.1p/Q tag insertion or removal on a per-port basis (egress) and support double-tagging
- VLAN ID tag/untag options on per port basis
- Fully compliant with IEEE 802.3 / 802.3u standards
- IEEE 802.3x full-duplex with force mode option and half−duplex backpressure collision flow control
- IEEE 802.1w rapid spanning tree protocol support
- IGMP v1/v2/v3 snooping for multicast packet filtering
- QoS/CoS packets prioritization support: 802.1p, DiffServ-based and re-mapping of 802.1p priority field per port basis on four priority levels
- IPv4/IPv6 QoS support
- IPv6 multicast listener discovery (MLD) snooping support
- Programmable rate limiting at the ingress and egress ports
- Broadcast storm protection
- 1K entry forwarding table with 32K frame buffer
- 4 priority queues with dynamic packet mapping for IEEE 802.1P, IPv4 TOS (DIFFSERV), IPv6 Traffic Class, etc.
- Source address filtering for implementing ring topologies

Comprehensive Configuration Registers Access

- Complete register access via the parallel Host Interface
- Facility to load MAC Address from EEPROM at power up and reset time
- I/O Pin Strapping facility to set certain register bits from I/O pins at reset time
- Control registers configurable on-the-fly

Host Interface

- Selectable 8- or 16-bit wide interface
- Supports Big- and Little-endian processors
- Indirect data bus for data, address and byte enable to access any I/O registers and RX/TX FIFO buffers
- Large internal memory with 12KByte for RX FIFO and 6Kbytes for TX FIFO.
- Programmable low, high and overrun water marks for flow control in RX FIFO
- Efficient architecture design with configurable host interrupt schemes to minimize host CPU overhead and utilization
- Queue management unit (QMU) supervises data transfers across this interface

Power and Power Management

- Single 3.3V power supply with optional VDD I/O for 1.8V, 2.5V or 3.3V
- Integrated low-voltage (~1.3V) low-noise regulator (LDO) output for digital and analog core power
- Supports IEEE P802.3az™ Energy Efficient Ethernet (EEE) to reduce power consumption in transceivers in LPI state
- Full-chip hardware or software power down (all registers value are not saved and strap-in value will re-strap after release the power down)
- Energy detect power down (EDPD), which disables the PHY transceiver when cables are removed
- Wake On LAN supported with configurable packet control
- Dynamic clock tree control to reduce clocking in areas not in use
- Power consumption less than 0.5W

Additional Features

- Single 25MHz +50ppm reference clock requirement
- Comprehensive programmable two LED indicators support for link, activity, full/half duplex and 10/100 speed

Packaging

- Commercial Temperature Range: 0°C to +70°C and Extended Industrial Temperature Ranges: –40°C to +105°C and –40°C to +115°C
- 64−pin (10mm × 10mm) lead free (ROHS) LQFP package with heat exposed ground paddle for low thermal resistance
- 0.11µm technology for lower power consumption

Target Applications

- General and Industrial Ethernet applications
- Wireless LAN Access Point and Gateway
- Set top / Game box
- Test and measurement equipment
- Automotive

Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Description
KSZ8852HLECA[1]	0°C to +70°C	64−Pin 10mm×10mm LQFP with exposed pad	Sn	Commercial Temperature Range Switch
KSZ8852HLEWA	−40°C to +105°C	64−Pin 10mm×10mm LQFP with exposed pad	Sn	Extended (105°C) Industrial Temperature Range Switch
KSZ8852HLEYA	−40°C to +115°C	64−Pin 10mm×10mm LQFP with exposed pad	Sn	Extended (115°C) Industrial Temperature Range Switch
KSZ8852HLE-EVAL	KSZ8852 Evaluation Board			

Note:

1. Contact Micrel for availability.

Revision History

Revision	Date	Summary of Changes
1.0	11/21/13	Initial Draft
1.1	8/31/15	Cleanup: part number on first page; remove table from last page.

Contents

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List of Tables

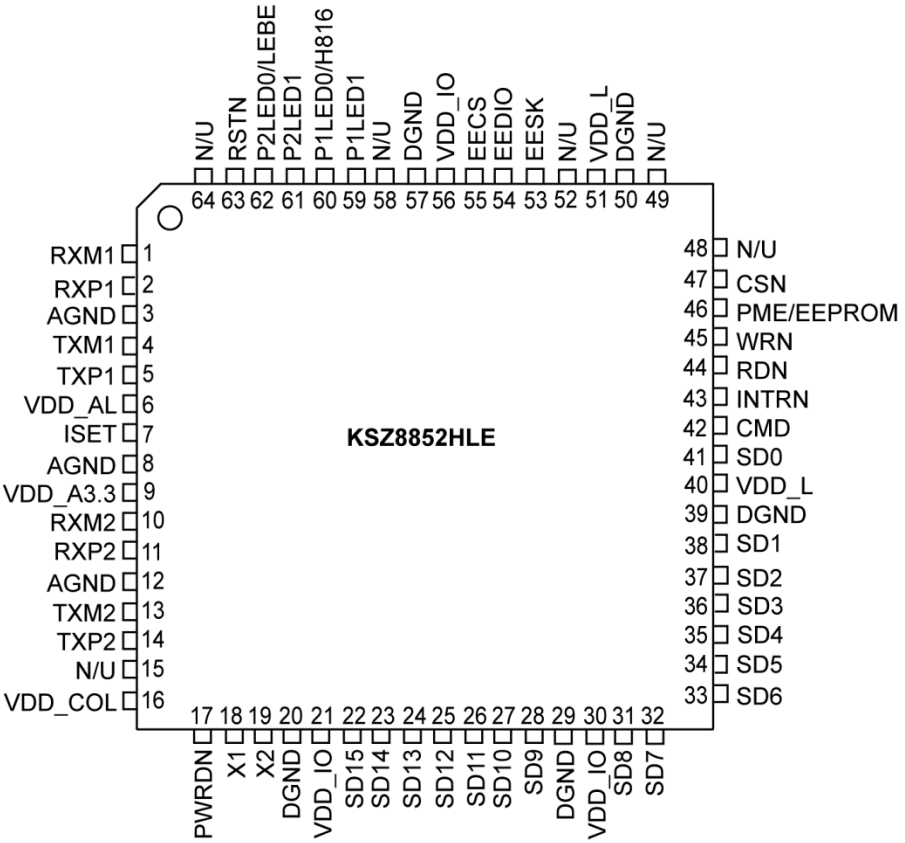
Acronyms

BIU	Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU	Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS	Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC	Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
CUT-THROUGH SWITCH		A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut−through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut−through switches do not store the packet.
DA	Destination Address	The address to send packets.
DMA	Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EMI	Electromagnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS	Frame Check Sequence	See CRC.
FID	Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
IGMP	Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG	Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI	Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
ISA	Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
JUMBO PACKET		A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.
MAC	Media Access Controller	A functional block responsible for implementing the Media Access Control layer which is a sub layer of the Data Link Layer.
MDI	Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null−modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore “media dependent”.

Acronyms (Continued)

MDI-X	Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null−modem, or crossover, cable. For 10/100 full−duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI−X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB	Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII	Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC	Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID	Non-Port VLAN ID	The port VLAN ID value is used as a VLAN reference.
NRZ	Non-Return to Zero	A type of signal data encoding whereby the signal does not return to a zero state in between bits.
PHY		A device or functional block which performs the physical layer interface function in a network.
PLL	Phase-Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
QMU	Queue Management Unit	Manages packet traffic between MAC/PHY interface and the system host. The QMU has built−in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue).
SA	Source Address	The address from which information has been sent.
TDR	Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the whole or part of the signal to return.
VLAN	Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

Pin Configuration



64-Pin LQFP
(Top View)
(Bottom paddle is GND)

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (− differential).
2	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential).
3	AGND	GND	Analog Ground.
4	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (− differential).
5	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential).
6	VDD_AL	P	This pin is used as an input for the low voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
7	ISET	O	**Current Set** Sets the physical transmit output current. Pull-down this pin with a 6.49KΩ (1%) resistor to ground.
8	AGND	GND	Analog Ground.
9	VDD_A3.3	P	3.3V analog VDD input power supply with well decoupling capacitors.
10	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (− differential).
11	RXP2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential).
12	AGND	GND	Analog Ground.
13	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (− differential).
14	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential).
15	N/U	I	This unused input should be connected to GND.
16	VDD_COL	P	This pin is used as a second input for the low voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
17	PWRDN	IPU	**Full Chip Power−Down** Active Low (Low = power down; High or floating = normal operation). While this pin is asserted low, all I/O pins will be tri-stated. All registers will be set to their default state. While this pin is asserted, power consumption will be minimal. When the pin is de-asserted power consumption will climb to nominal and the device will be in the same state as having been reset by the reset pin (RSTN, pin 63).
18	X1	I	**25MHz Crystal or Oscillator Clock Connection** Pins (X1, X2) connect to a crystal or frequency oscillator source. If an oscillator is used, X1 connects to a VDD_IO voltage tolerant oscillator and X2 is a no connect. This clock requirement is ±50ppm.
19	X2	O	
20	DGND	GND	Digital Ground.
21	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power pin for IO logic and the internal Low Voltage regulator.
22	SD15/BE3	I/O (PD)	**Shared Data Bus Bit[15] or BE3** This is data bit (D15) access when CMD = “0”. This is Byte Enable 3 (BE3, 4th byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.
23	SD14/BE2	I/O (PD)	**Shared Data Bus Bit [14] or BE2** This is data bit (D14) access when CMD = “0”. This is Byte Enable 2 (BE2, 3rd byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.
24	SD13/BE1	I/O (PD)	**Shared Data Bus Bit [13] or BE1** This is data bit (D13) access when CMD = “0”. This is Byte Enable 1 (BE1, 2nd byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
25	SD12/BE0	I/O (PD)	**Shared Data Bus Bit [12] or BE0** This is data bit (D12) access when CMD = “0”. This is Byte Enable 0 (BE0, 1st byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.
26	SD11	I/O (PD)	**Shared Data Bus Bit [11]** This is data bit (D11) access when CMD = “0”. Don’t care when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.
27	SD10/A10	I/O (PD)	**Shared Data Bus bit [10]** This is data bit (D10) access when CMD = “0”. In 8-bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A10 access when CMD = “1”.
28	SD9/A9	I/O (PD)	**Shared Data Bus Bit[9] or A9** This is data bit (D9) access when CMD = “0”. In 8−bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A9 access when CMD = “1”.
29	DGND	GND	Digital Ground.
30	VDD_IO	P	3.3V, 2.5V or 1.8V digital VDD input power pin for IO logic and the internal low voltage regulator.
31	SD8/A8	IPU/O	**Shared Data Bus Bit [8] or A8** This is data bit (D8) access when CMD = “0”. In 8-bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A8 access when CMD = “1”.
32	SD7/A7	IPD/O	**Shared Data Bus Bit [7] or A7** This is data bit (D7) access when CMD = “0”. In 8-bit bus mode, this is address A7 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A7 access when CMD = “1”.
33	SD6/A6	IPU/O	**Shared Data Bus Bit [6] or A6** This is data bit (D6) access when CMD = “0”. In 8-bit bus mode, this is address A6 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A6 access when CMD = “1”.
34	SD5/A5	IPU/O	**Shared Data Bus Bit [5] or A5** This is data bit (D5) access when CMD = “0”. In 8-bit bus mode, this is address A5 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A5 access when CMD = “1”.
35	SD4/A4	IPD/O	**Shared Data Bus Bit [4] or A4** This is data bit (D4) access when CMD = “0”. In 8-bit bus mode, this is address A4 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A4 access when CMD = “1”.
36	SD3/A3	I/O (PD)	**Shared Data Bus Bit [3] or A3** This is data bit (D3) access when CMD = “0”. In 8-bit bus mode, this is address A3 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A3 access when CMD = “1”.
37	SD2/A2	I/O (PD)	**Shared Data Bus Bit [2] or A2** This is data bit (D2) access when CMD = “0”. In 8-bit bus mode, this is address A2 (1st write) or A10 (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A2 access when CMD = “1”.
38	SD1/A1/A9	I/O (PD)	**Shared Data Bus Bit [1] or A1 or A9** This is data bit (D1) access when CMD = “0”. In 8-bit bus mode, this is address A1 (1st write) or A9 (2nd write) access when CMD = “1”. In 16-bit bus mode, this is “Don’t care” when CMD = “1”.

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
39	DGND	GND	Digital Ground.
40	VDD_L	P	This pin can be used in two ways; as the pin to input a low voltage to the device if the internal low voltage regulator is not used, or as the low voltage output if the internal low voltage regulator is used.
41	SD0/A0/A8	IPU/O	**Shared Data Bus Bit [0] or A0 or A8** This is data bit (D0) access when CMD = “0”. In 8-bit bus mode, this is address A0 (1st write) or A8 (2nd write) access when CMD = “1”. In 16−bit bus mode, this is “Don’t care” when CMD = “1”.
42	CMD	IPD	**Command Type** This command input decides the SD[15:0] shared data bus access information. When command input is low, the access of shared data bus is for data access either SD[15:0] −> DATA[15:0] in 16−bit bus mode or SD[7:0] −> DATA[7:0] in 8-bit bus mode. When command input is high, in 16−bit bus mode: The access of shared data bus is for address A[10:2] access at shared data bus SD[10:2] and SD[1:0] is “don’t care". Byte enable BE[3:0] at SD[15:12] and the SD[11] is “don’t care”. in 8-bit bus mode: It is for address A[7:0] during 1st write access at shared data bus SD[7:0] or A[10:8] during 2nd write access at shared data bus SD[2:0] (SD[7:3] is don’t care).
43	INTRN	OPU	**Interrupt Output** This is an active low signal going to the host CPU to indicate an interrupt status bit is set. This pin needs an external 4.7KΩ pull-up resistor.
44	RDN	IPU	**Read Strobe** This signal is an active low signal used as the asynchronous read strobe during read access cycles by the host processor. It is recommended that it be pulled up with a 4.7KΩ resistor.
45	WRN	IPU	**Write Strobe** This is an asynchronous write strobe signal used during write cycles from the external host processor. It is a low active signal.
46	PME/EEPROM	IPD/O	**Power Management Event** This output signal indicates that a Wake On LAN event has been detected. The KSZ8852 is requesting the system to wake up from low power mode. Its assertion polarity is programmable with the default polarity to be active low. **Config Mode: (EEPROM)** At the end of the power up/reset period, this pin is sampled and the pull-up/pull-down value is latched. The value latched will indicate if a Serial EEPROM is present or not. See the Strapping Options section for details.
47	CSN	IPU	**Chip Select** This signal is the Chip Select signal that is used by the external host processor for accesses to the device. It is an active low signal.
48	N/U	O(PU)	This unused output should be unconnected.
49	N/U	O(PU)	This unused output should be unconnected.
50	DGND	GND	Digital Ground.
51	VDD_L	P	This pin can be used in two ways; as the pin to input a low voltage to the device if the internal low voltage regulator is not used, or as the low voltage output if the internal low voltage regulator is used.
52	N/U	O(PU)	This unused output should be unconnected.

Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>53</td><td>EESK</td><td>O(PD)</td><td>EEPROM Serial Clock Output
A serial output clock is used to load configuration data into the KSZ8852 from the external EEPROM when it is present.</td></tr>
<tr><td>54</td><td>EEDIO</td><td>I/O(PD)</td><td>EEPROM Data Input/Output
Serial data input/output is from/to external EEPROM when it is present.</td></tr>
<tr><td>55</td><td>EECS</td><td>O(PD)</td><td>EEPROM Chip Select Output
This signal is used to select an external EEPROM device when it is present.</td></tr>
<tr><td>56</td><td>VDD_IO</td><td>P</td><td>3.3V, 2.5V or 1.8V digital VDD input power pin for IO logic and the internal Low Voltage regulator.</td></tr>
<tr><td>57</td><td>DGND</td><td>GND</td><td>Digital Ground.</td></tr>
<tr><td>58</td><td>N/U</td><td>O(PU)</td><td>This unused output should be unconnected.</td></tr>
<tr><td>59</td><td>P1LED1</td><td>IPU/O</td><td rowspan="3">Programmable LED Outputs to Indicate Port 1 and Port 2 Activity/Status
The LED is ON (active) when output is LOW; the LED is OFF (inactive) when output is HIGH.
The Port 1 LED pins outputs are determined by the table below if Reg. 0x06C – 0x06D, bits [14:12] are set to ‘000’. Otherwise, the Port 1 LED pins are controlled via the processor by setting Reg. 0x06C – 0x06D, bits [14:12] to a non-zero value.
The Port 2 LED pins outputs are determined by the table below if Reg. 0x084 – 0x085, bits [14:12] are set to ‘000’. Otherwise, the Port 2 LED pins are controlled via the processor by setting Reg. 0x084 – 0x085, bits [14:12] to a non-zero value.
Automatic Port 1 and Port 2 indicators are defined as follows:
<table>
<tr><td></td><td colspan="4">Two bits [9:8] in SGCR7 Control Register</td></tr>
<tr><td></td><td>00 (Default)</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Speed</td><td>ACT</td><td>Duplex</td><td>Duplex</td></tr>
<tr><td>P1LED0/P2LED0</td><td>LINK/ACT</td><td>LINK</td><td>LINK/ACT</td><td>LINK</td></tr>
</table>
LINK = LED ON ACT = LED Blink LINK/ACT = LED On/Blink
Speed = LED ON (100BT) LED OFF (10BT)
Duplex = LED ON (Full duplex) LED OFF (Half duplex)
Config Mode: (P1LED1)
At the end of the power up/reset period, this pin is sampled and the pull-up/pull-down value is latched. It must be at a logic high level at this time. See the Strapping Options section for details.
Config Mode: (P1LED0/H816)
At the end of the power up/reset period, this pin is sampled and the pull-up/pull-down value is latched. The value latched will determine if 8-bit or 16-bit mode will be used for the host interface. See the Strapping Options section for details.
Config Mode: (P2LED0/LEBE)
At the end of the power up/reset period, this pin is sampled and the pull-up/pull-down value is latched. The value latched will determine if “Little Endian” or “Big Endian” mode will be used for the host interface. See the Strapping Options section for details.</td></tr>
<tr><td>60</td><td>P1LED0/H816</td><td>IPU/O</td></tr>
<tr><td>61</td><td>P2LED1</td><td>O</td></tr>
<tr><td>62</td><td>P2LED0/LEBE</td><td>IPU/O</td></tr>
</table>

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
63	RSTN	IPU	**Reset** Hardware reset pin (Active Low). This reset input is required to be low for a minimum of 10ms after supply voltages VDD_IO and 3.3V are stable.
64	N/U	I	This unused input should be connected to GND.
65 (Bottom pad)	GND	GND	Ground.

Legend:

P = Power supply.

GND = Ground.

I/O = Bi−directional.

I = Input.

O = Output.

IPD = Input with internal pull-down (58K ±30%).

IPU = Input with internal pull-up (58K ±30%).

OPD = Output with internal pull-down (58K ±30%).

OPU = Output with internal pull-up (58K ±30%).

IPU/O = Input with internal pull-up (58K ±30%) during power-up/reset; output pin otherwise.

IPD/O = Input with internal pull-down (58K ±30%) during power-up/reset; output pin otherwise.

I/O (PD) = Bi-directional Input/Output with internal pull-down (58K ±30%).

I/O (PU) = Bi-directional Input/Output with internal pull-up (58K ±30%).

Strapping Options

Pin Number	Pin Name	Type	Pin Function During Power-up / Reset
46	PME/ EEPROM	IPD/O	**EEPROM Select** Pull-up = EEPROM present NC or pull-down (default) = EEPROM not present This pin value is latched into register CCR, bit [9] at the end of the Power-Up/Reset time.
59	P1LED1	IPU/O	**Reserved** NC or pull-up (default) = Normal Operation Pull-down = Reserved
60	P1LED0/ H816	IPU/O	**8 or 16-Bit Host Interface Mode Select** NC or pull-up (default) = 16-bit bus mode Pull-down = 8-bit bus mode This pin value is also latched into register CCR, bit [7:6] at the end of the Power-Up/Reset time.
62	P2LED0/ LEBE	IPU/O	**Endian Mode Select for 8/16-bit Host Interface** NC or pull-up (default) = Little Endian Pull-down = Big Endian This pin value is latched into register CCR, bit [10] at the end of the power-up/reset time.

Notes:

IPU/O = Input with internal pull-up (58K ±30%) during power−up/reset; output pin otherwise.

IPD/O = Input with internal pull-down (58K ±30%) during power−up/reset; output pin otherwise.

All strap-in pins are latched during power−up or reset as well as re−strap−in when hardware/software power-down and hardware reset.

Functional Description

The KSZ8852 is a highly integrated networking device that incorporates a Layer-2 switch, two 10BT/100BT physical layer transceivers (PHYs) and associated MAC units, and a bus interface unit (BIU) with one general 8/16-bit host interface.

The KSZ8852 operates in a managed mode. In managed mode, a host processor can access and control all PHY, Switch, and MAC related registers within the device via the host interface.

Physical signal transmission and reception are enhanced through the use of analog circuits in the PHY that make the design more efficient and allow for low power consumption. Both power management and Energy Efficient Ethernet (EEE) are designed to save more power while device is in idle state. Wake on LAN is implemented to allow the KSZ8852 to monitor the network for packets intended to wake up the system which is upstream from the KSZ8852.

The KSZ8852 is fully compliant to IEEE802.3u standards.

Direction Terminology

Readers should note that two different terminologies are used in this datasheet to describe the direction of data flow. In the standard terminology that is used for all switches, directions are described from the point of view of the switch core: “transmit” indicates data flow out of the KSZ8852 on any of the three ports, while “receive” indicates data flow into the KSZ8852. This terminology is used for the MIB counters.

When referencing the QMU block, which is located on port 3 between the internal MAC and the external 8/16-bit host interface, directions are revered. They are described from the point of view of the external host processor. “Transmit” indicates data flow from the host into port 3 of the KSZ8852, while “receive” indicates data flow out of the KSZ8852 on port 3. Since both terminologies are used for port 3, it is important to note whether or not a particular section refers to the QMU.

Physical (PHY) Block

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 6.49kΩ (1%) resistor for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

Scrambler/De-Scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then, the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

PLL Clock Synthesizer (Recovery)

The internal PLL clock synthesizer generates 125MHz, 62.5MHz and 31.25MHz clocks for the KSZ8852 system timing. These internal clocks are generated from an external 25MHz crystal or oscillator.

100BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnets. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP1 or RXM1 input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8852 decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.