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# KSZ8862-16/32MQL

## 2-Port Ethernet Switch with Non-PCI Interface and Fiber Support

**Rev 3.1**

## General Description

The KSZ8862M is 2-port switch with non-PCI CPU interface and fiber support, and is available in 8/16-bit and 32-bit bus designs (see Ordering Information). This datasheet describes the KSZ8862M non-PCI CPU interface chip.

The KSZ8862M is the industry's first fully managed, 2-port switch with a non-PCI CPU interface and fiber support. It is based on a proven, 4th generation, integrated Layer-2 switch, compliant with IEEE 802.3u standards.

For industrial applications, the KSZ8862M can run in half-duplex mode regardless of the application.

In fiber mode, port 1 can be configurable to either 100BASE-FX or 100BASE-SX/10BASE-FL.

The LED driver and post amplifier are also included for 10Base-FL and 100Base-SX applications.

**LinkMD®**

In copper mode, port 2 supports 10/100BASE-T/TX with HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables. Micrel's proprietary LinkMD® Time Domain Reflectometry (TDR)-based function is also available for determining the cable length, as well as cable diagnostics for identifying faulty cabling.

The KSZ8862M offers an extensive feature set that includes tag/port-based VLAN, quality of service (QoS) priority management, management information base (MIB) counters, and CPU control/data interfaces to effectively address Fast Ethernet applications.

The KSZ8862M contains: Two 10/100 transceivers with patented, mixed-signal, low-power technology, two media access control (MAC) units, a direct memory access (DMA) channel, a high-speed, non-blocking, switch fabric, a dedicated 1K entry forwarding table, and an on-chip frame buffer memory.

## Functional Diagram

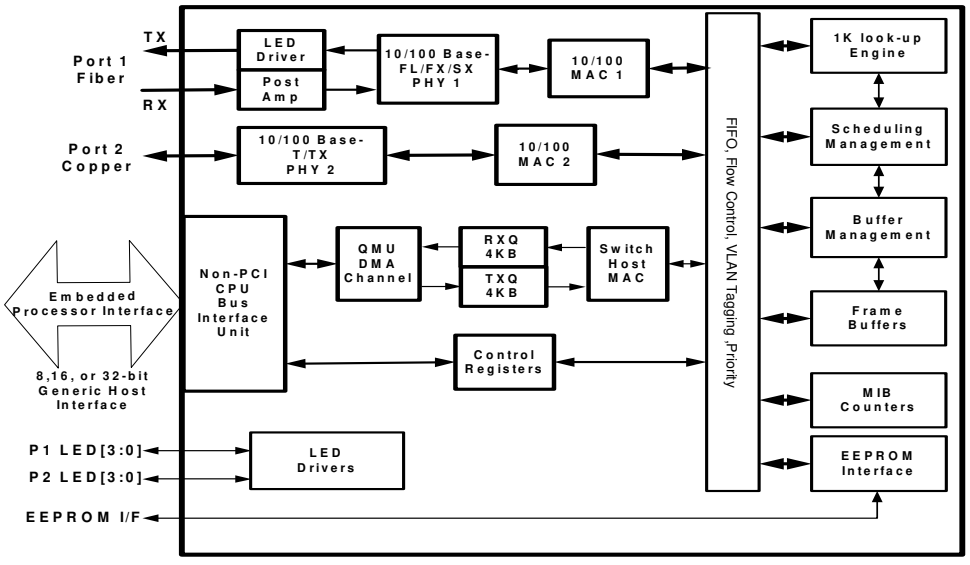


**Figure 1. KSZ8862M Functional Diagram**

LinkMD is a registered trademark of Micrel, Inc.

# Features

**Switch Management**

- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K entry forwarding table and a store-and-forward architecture
- Fully compliant with IEEE 802.3u standards
- Full-duplex IEEE 802.3x flow control (Pause) with force mode option
- Half-duplex back pressure flow control

**Advanced Switch Management**

- IEEE 802.1Q VLAN support for up to 16 groups (full range of VLAN IDs)
- VLAN ID tag/untag options, on a per port basis
- IEEE 802.1p/Q tag insertion or removal on a per port basis (egress)
- Programmable rate limiting at the ingress and egress ports
- Broadcast storm protection
- IEEE 802.1d spanning tree protocol support
- MAC filtering function to filter or forward unknown unicast packets
- Direct forwarding mode enabling the processor to identify the ingress port and to specify the egress port
- Internet Group Management Protocol (IGMP) v1/v2 snooping support for multicast packet filtering
- IPV6 Multicast Listener Discovery (MLD) snooping support

**Fiber Support**

- Integrated LED driver and post amplifier for 10BASE-FL and 100BASE-SX optical modules
- 100BASE-FX/SX and 10BASE-FL fiber support on port 1

**Monitoring**

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- MIB counters for fully compliant statistics gathering – 34 MIB counters per port
- Loopback modes for remote failure diagnostics

**Comprehensive Register Access**

- Control registers configurable on-the-fly (port-priority, 802.1p/d/Q)

**QoS/CoS Packets Prioritization Support**

- Per port, 802.1p and DiffServ-based
- Remapping of 802.1p priority field on a per port basis

**Power Modes, Packaging, and Power Supplies**

- Full-chip hardware power-down (register configuration not saved) allows low power dissipation
- Per port-based, software power-save on PHY (idle link detection, register configuration preserved)
- Single power supply: 3.3V
- Commercial Temperature Range: 0$^{o}$C to +70$^{o}$C
- Industrial Temperature Range: –40$^{o}$C to +85$^{o}$C (see Ordering Information).
- Available in 128-pin PQFP
- Available in –16 version for 8/16-bit bus support and –32 version for 32-bit bus support (see Ordering Information).

**Additional Features**

In addition to offering all of the features of an integrated Layer-2 managed switch, the KSZ8862M offers:

- Dynamic buffer memory scheme
  – Essential for applications such as Video over IP where image jitter is unacceptable
- 2-port switch with a flexible 8, 16, or 32-bit generic host processor interfaces
- Micrel LinkMD® cable diagnostics to determine cable length, diagnose faulty cables, and determine distance-to-fault
- Hewlett Packard (HP) Auto-MDIX crossover with disable and enable options
- Four priority queues to handle voice, video, data, and control packets
- Ability to transmit and receive jumbo frame sizes up to 1916 bytes

# Applications

- Video Distribution Systems
- High-end Cable, Satellite, and IP set-top boxes
- Video over IP
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Motion Control
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security and Surveillance Cameras

# Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

## Ordering Information

| Part Number | Temperature Range | Package | Comment |
|---|---|---|---|
| **KSZ8862-16MQL-FX** | **0°C to 70°C** | **128-Pin PQFP** | **Port 1 operates on 100BASE-FX mode only** |
| **KSZ8862-16MQL** | **0°C to 70°C** | **128-Pin PQFP** | **Port 1 operates on 10BASE-FL or 100BASE-SX mode only** |
| **KSZ8862-32MQL-FX** | **0°C to 70°C** | **128-Pin PQFP** | **Port 1 operates on 100BASE-FX mode only** |
| **KSZ8862-32MQL** | **0°C to 70°C** | **128-Pin PQFP** | **Port 1 operates on 10BASE-FL or 100BASE-SX mode only** |
| KSZ8862-100FX-EVAL | Evaluation Board for the KSZ8862-16MQL at 100FX Mode | | |
| KSZ8862-10FL-EVAL | Evaluation Board for the KSZ8862-16MQL at 100SX_10FL Mode | | |

## Revision History

| Revision | Date | Summary of Changes |
|---|---|---|
| 1.0 | 07/18/06 | First released Information |
| 2.0 | 09/13/06 | Added evaluation ordering info. to Ordering Information Table |
| 3.0 | 04/04/07 | Updated part ordering info. to Ordering Information Table<br>Improve the ARDY low time in read cycle to 40ns and in write cycle to 50 ns during QMU data register access |
| 3.1 | 8/13/10 | Changed the FL/SX part order information |

## Content

## List of Figures

# List of Tables

# Pin Configuration for KSZ8862-16MQL (8/16-Bit)

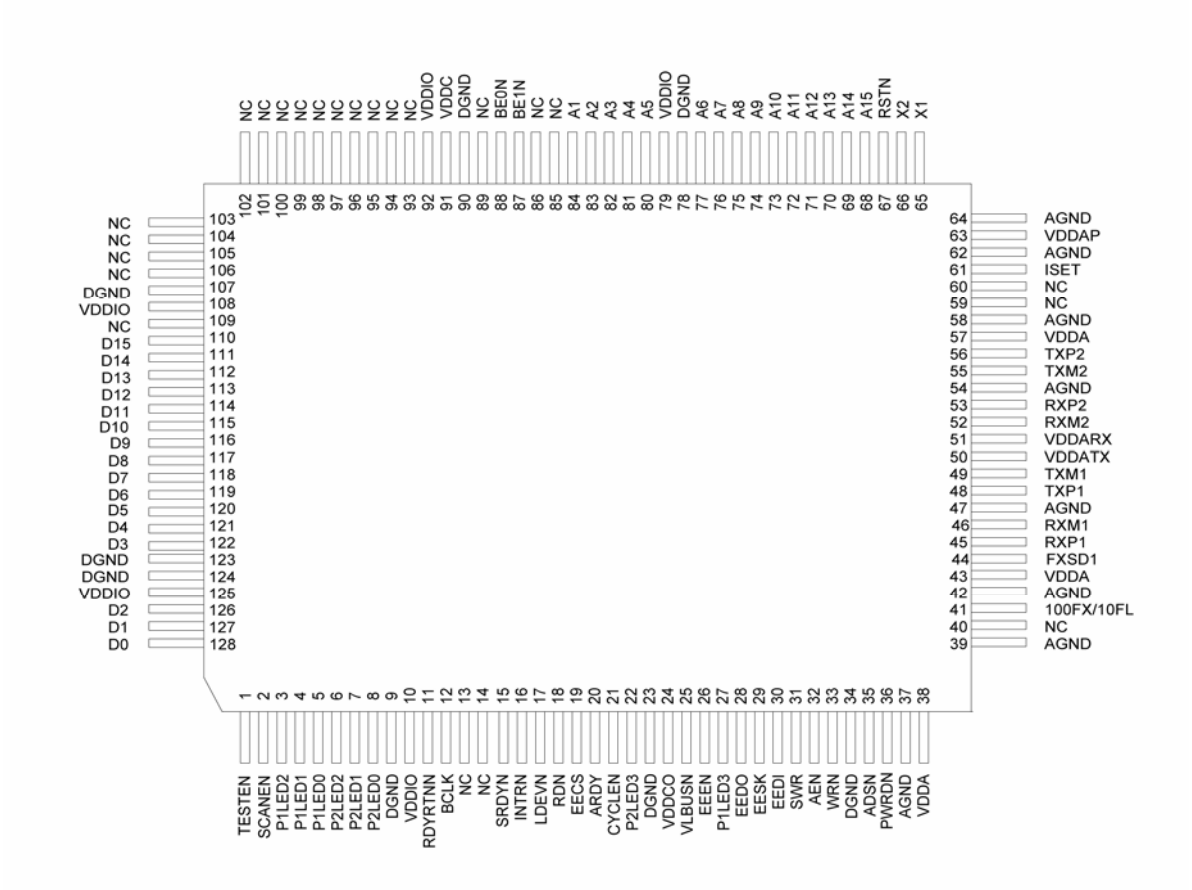


**Figure 2. 128-Pin PQFP**
**(Top View)**

# Pin Description for KSZ8862-16MQL (8/16-Bit)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
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<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
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<tr><td>P1LED3[2] /P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:<br>1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;<br>Full Duplex = On (Full duplex); Off (Half duplex)<br>Speed = On (100BASE-T); Off (10BASE-T)<br>2. P1LED3 is pin 27. P2LED3 is pin 22.</td></tr>
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<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not:<br>For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn’t connect to this pin, assert this pin.<br>For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
<tr><td>12</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock<br>Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.<br>This pin should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>13</td><td>NC</td><td>Ipu</td><td>No connect.</td></tr>
<tr><td>14</td><td>NC</td><td>Opu</td><td>No connect.</td></tr>
<tr><td>15</td><td>SRDYN</td><td>Opu</td><td>Synchronous Ready Not<br>Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extended accesses.<br>For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK.<br>For burst mode (32-bit interface only), the KSZ8862M drives this pin low to signal wait states.</td></tr>
</table>

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 16 | INTRN | Opd | Interrupt<br>Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor. |
| 17 | LDEVN | Opd | Local Device Not<br>Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8862M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal. |
| 18 | RDN | Ipd | Read Strobe Not<br>Asynchronous read strobe, active Low. |
| 19 | EECS | Opu | EEPROM Chip Select |
| 20 | ARDY | Opd | Asynchronous Ready<br>ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. This pin needs an external 4.7K pull-up resistor. |
| 21 | CYCLEN | Ipd | Cycle Not<br>For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle.<br>For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles. |
| 22 | P2LED3 | Opd | Port 2 LED indicator<br>See the description in pins 6, 7, and 8. |
| 23 | DGND | Gnd | Digital IO ground |
| 24 | VDDCO | P | 1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins.<br>Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite bead and capacitors). |
| 25 | VLBUSN | Ipd | VLBus-like Mode<br>Pull-down or float: Bus interface is configured for synchronous mode.<br>Pull-up: Bus interface is configured for 8-bit or 16-bit asynchronous mode or EISA-like burst mode. |
| 26 | EEEN | Ipd | EEPROM Enable<br>EEPROM is enabled and connected when this pin is pull-up.<br>EEPROM is disabled when this pin is pull-down or no connect. |
| 27 | P1LED3 | Opd | Port 1 LED indicator. See the description in pins 3, 4, and 5. |
| 28 | EEDO | Opd | EEPROM Data Out<br>This pin is connected to DI input of the serial EEPROM. |
| 29 | EESK | Opd | EEPROM Serial Clock<br>A 4μs serial output clock to load configuration data from the serial EEPROM. |
| 30 | EEDI | Ipd | EEPROM Data In<br>This pin is connected to DO output of the serial EEPROM when EEEN is pull-up.<br>This pin can be pull-down for 8-bit bus mode, pull-up for 16-bus mode or don't care for 32-bus mode when EEEN is pull-down (without EEPROM). |
| 31 | SWR | Ipd | Synchronous Write/Read<br>Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low. |
| 32 | AEN | Ipu | Address Enable<br>Address qualifier for the address decoding, active Low. |

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 33 | WRN | Ipd | Write Strobe Not<br>Asynchronous write strobe, active Low. |
| 34 | DGND | Gnd | Digital IO ground |
| 35 | ADSN | Ipd | Address Strobe Not<br>For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN. |
| 36 | PWRDN | Ipu | Full-chip power-down. Low = Power down; High or floating = Normal operation. |
| 37 | AGND | Gnd | Analog ground |
| 38 | VDDA | P | 1.2V analog $V_{DD}$ input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 39 | AGND | Gnd | Analog ground |
| 40 | NC | — | No connect |
| 41 | 100FX/10FL | Ipu | Fiber mode select for port 1. 1K ohm pull-up to 3.3V for 100Base-FX, 100 ohm pull-down to GND for 100Base-SX or 10Base-FL. |
| 42 | AGND | Gnd | Analog ground |
| 43 | VDDA | P | 1.2V analog $V_{DD}$ input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 44 | FXSD1 | I | Fiber signal detect input for port 1 in 100Base-FX fiber mode. 1K ohm pull-up to 3.3V for port 1 in 100Base-SX or 10Base-FL fiber modes. |
| 45 | RXP1 | I/O | Port 1 physical receive (MDI) signal (+ differential) from external fiber module |
| 46 | RXM1 | I/O | Port 1 physical receive (MDI) signal (– differential) from external fiber module |
| 47 | AGND | Gnd | Analog ground |
| 48 | TXP1 | I/O | Port 1 physical transmit (MDI) signal (+ differential) to external fiber module |
| 49 | TXM1 | I/O | Port 1 physical transmit (MDI) signal (– differential) to external fiber module |
| 50 | VDDATX | P | 3.3V analog $V_{DD}$ input power supply with well decoupling capacitors. |
| 51 | VDDARX | P | 3.3V analog $V_{DD}$ input power supply with well decoupling capacitors. |
| 52 | RXM2 | I/O | Port 2 physical receive (MDI) or transmit (MDIX) signal (- differential) |
| 53 | RXP2 | I/O | Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential) |
| 54 | AGND | Gnd | Analog ground |
| 55 | TXM2 | I/O | Port 2 physical transmit (MDI) or receive (MDIX) signal (- differential) |
| 56 | TXP2 | I/O | Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential) |
| 57 | VDDA | P | 1.2 analog $V_{DD}$ input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 58 | AGND | Gnd | Analog ground |
| 59 | NC | Ipu | No connect |
| 60 | NC | Ipu | No connect |
| 61 | ISET | O | Set physical transmits output current.<br>Pull-down this pin with a 3.01K 1% resistor to ground. |
| 62 | AGND | Gnd | Analog ground |
| 63 | VDDAP | P | 1.2V analog $V_{DD}$ for PLL input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 64 | AGND | Gnd | Analog ground |

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 65 | X1 | I | 25MHz crystal or oscillator clock connection. |
| 66 | X2 | O | Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect.<br>Note: Clock requirement is 50ppm for either crystal or oscillator. |
| 67 | RSTN | Ipu | Hardware reset pin (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V. |
| 68 | A15 | I | Address 15 |
| 69 | A14 | I | Address 14 |
| 70 | A13 | I | Address 13 |
| 71 | A12 | I | Address 12 |
| 72 | A11 | I | Address 11 |
| 73 | A10 | I | Address 10 |
| 74 | A9 | I | Address 9 |
| 75 | A8 | I | Address 8 |
| 76 | A7 | I | Address 7 |
| 77 | A6 | I | Address 6 |
| 78 | DGND | Gnd | Digital IO ground |
| 79 | VDDIO | P | 3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors. |
| 80 | A5 | I | Address 5 |
| 81 | A4 | I | Address 4 |
| 82 | A3 | I | Address 3 |
| 83 | A2 | I | Address 2 |
| 84 | A1 | I | Address 1 |
| 85 | NC | I | No Connect |
| 86 | NC | I | No Connect |
| 87 | BE1N | I | Byte Enable 1 Not, Active low for Data byte 1 enable (don't care in 8-bit bus mode). |
| 88 | BE0N | I | Byte Enable 0 Not, Active low for Data byte 0 enable (there is an internal inverter enabled and connected to the BE1N for 8-bit bus mode). |
| 89 | NC | I | No Connect |
| 90 | DGND | Gnd | Digital core ground |
| 91 | VDDC | P | 1.2V digital core $V_{DD}$ input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 92 | VDDIO | P | 3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors. |
| 93 | NC | I | No Connect |
| 94 | NC | I | No Connect |
| 95 | NC | I | No Connect |
| 96 | NC | I | No Connect |
| 97 | NC | I | No Connect |
| 98 | NC | I | No Connect |
| 99 | NC | I | No Connect |
| 100 | NC | I | No Connect |
| 101 | NC | I | No Connect |
| 102 | NC | I | No Connect |
| 103 | NC | I | No Connect |

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 104 | NC | I | No Connect |
| 105 | NC | I | No Connect |
| 106 | NC | I | No Connect |
| 107 | DGND | Gnd | Digital IO ground |
| 108 | VDDIO | P | 3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors. |
| 109 | NC | I | No Connect |
| 110 | D15 | I/O | Data 15 |
| 111 | D14 | I/O | Data 14 |
| 112 | D13 | I/O | Data 13 |
| 113 | D12 | I/O | Data 12 |
| 114 | D11 | I/O | Data 11 |
| 115 | D10 | I/O | Data 10 |
| 116 | D9 | I/O | Data 9 |
| 117 | D8 | I/O | Data 8 |
| 118 | D7 | I/O | Data 7 |
| 119 | D6 | I/O | Data 6 |
| 120 | D5 | I/O | Data 5 |
| 121 | D4 | I/O | Data 4 |
| 122 | D3 | I/O | Data 3 |
| 123 | DGND | Gnd | Digital IO ground |
| 124 | DGND | Gnd | Digital core ground |
| 125 | VDDIO | P | 3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors. |
| 126 | D2 | I/O | Data 2 |
| 127 | D1 | I/O | Data 1 |
| 128 | D0 | I/O | Data 0 |

**Legend:**

P = Power supply Gnd = Ground

I/O = Bi-directional I = Input O = Output

Ipd = Input with internal pull-down

Ipu = Input with internal pull-up

Opd = Output with internal pull-down

Opu = Output with internal pull-up

# Pin Configuration for KSZ8862-32MQL (32-Bit)

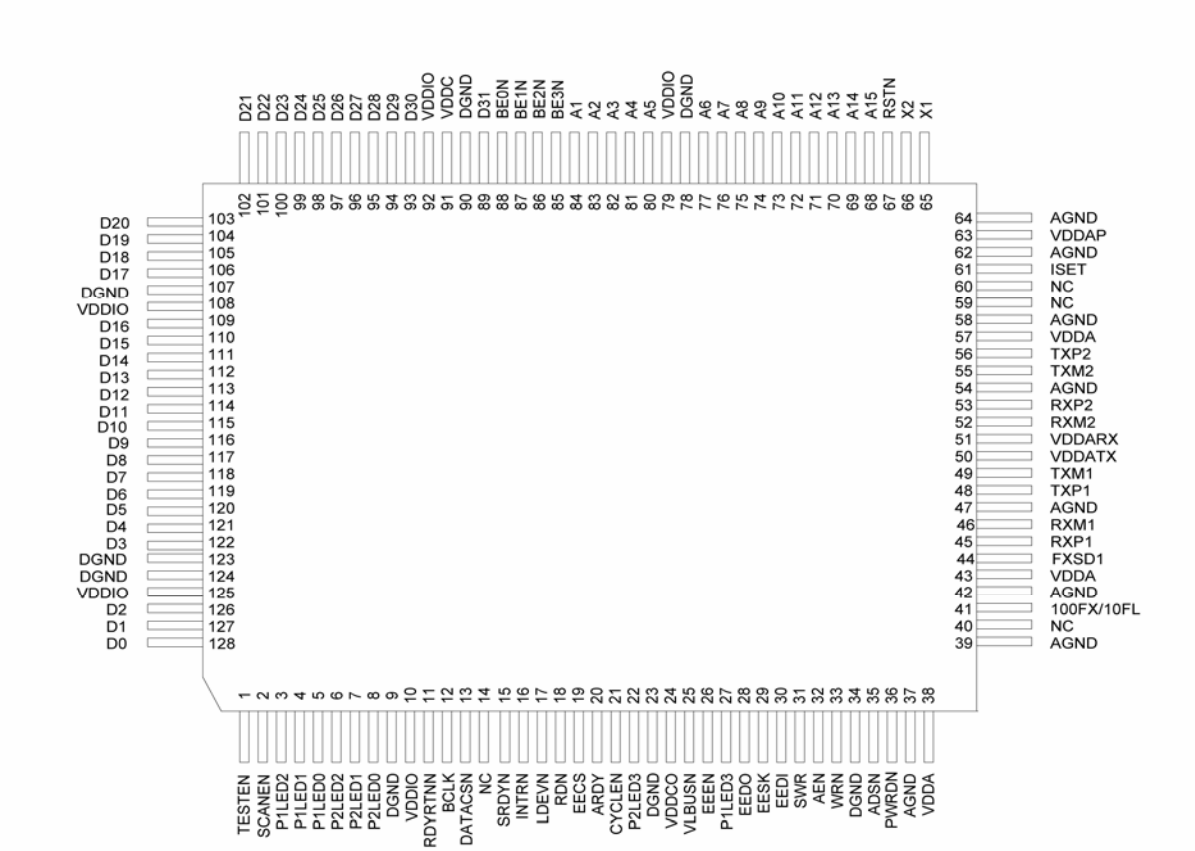


**Figure 3. 128-Pin PQFP**
**(Top View)**

# Pin Description for KSZ8862-32 MQL (32-Bit)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable<br>For normal operation, 1K ohm pull-down this pin-to-ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable<br>For normal operation, 1K ohm pull-down this pin-to-ground.</td></tr>
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<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
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<tr><td>P1LED3[2] /P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
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<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>11</td><td>RDYRTNN</td><td>Ipd</td><td>Ready Return Not<br>For VLBus-like mode: Asserted by the host to complete synchronous read cycles. If the host doesn't connect to this pin, assert this pin.<br>For burst mode (32-bit interface only): Host drives this pin low to signal waiting states.</td></tr>
<tr><td>12</td><td>BCLK</td><td>Ipd</td><td>Bus Interface Clock<br>Local bus clock for synchronous bus systems. Maximum frequency is 50MHz.<br>This pin should be tied Low or unconnected if it is in asynchronous mode.</td></tr>
<tr><td>13</td><td>DATACSN</td><td>Ipu</td><td>DATA Chip Select Not (For KSZ8862-32 Mode only)<br>Chip select signal for QMU data register (QDRH, QDRL), active Low.<br>When DATACSN is Low, the data path can be accessed regardless of the value of AEN, A15-A1, and the content of the BANK select register.</td></tr>
<tr><td>14</td><td>NC</td><td>Opu</td><td>No connect.</td></tr>
<tr><td>15</td><td>SRDYN</td><td>Opu</td><td>Synchronous Ready Not<br>Ready signal to interface with synchronous bus for both EISA-like and VLBus-like extend accesses.<br>For VLBus-like mode, the falling edge of this signal indicates ready. This signal is synchronous to the bus clock signal BCLK.<br>For burst mode (32-bit interface only), the KSZ8862M drives this pin low to signal wait states.</td></tr>
</table>

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 16 | INTRN | Opd | Interrupt<br>Active Low signal to host CPU to indicate an interrupt status bit is set, this pin need an external 4.7K pull-up resistor. |
| 17 | LDEVN | Opd | Local Device Not<br>Active Low output signal, asserted when AEN is Low and A15-A4 decode to the KSZ8862M address programmed into the high byte of the base address register. LDEVN is a combinational decode of the Address and AEN signal. |
| 18 | RDN | Ipd | Read Strobe Not<br>Asynchronous read strobe, active Low. |
| 19 | EECS | Opu | EEPROM Chip Select |
| 20 | ARDY | Opd | Asynchronous Ready<br>ARDY may be used when interfacing asynchronous buses to extend bus access cycles. It is asynchronous to the host CPU or bus clock. This pin needs an external 4.7K pull-up resistor. |
| 21 | CYCLEN | Ipd | Cycle Not<br>For VLBus-like mode cycle signal; this pin follows the addressing cycle to signal the command cycle.<br>For burst mode (32-bit interface only), this pin stays High for read cycles and Low for write cycles. |
| 22 | P2LED3 | Opd | Port 2 LED indicator. See the description in pins 6, 7, and 8. |
| 23 | DGND | Gnd | Digital IO ground |
| 24 | VDDCO | P | 1.2V digital core voltage output (internal 1.2V LDO power supply output), this 1.2V output pin provides power to VDDC, VDDA and VDDAP pins.<br>Note: Internally generated power voltage. Do not connect an external power supply to this pin. This pin is used for connecting external filter (Ferrite Bead and capacitors). |
| 25 | VLBUSN | Ipd | VLBus-like Mode<br>Pull-down or float: Bus interface is configured for synchronous mode.<br>Pull-up: Bus interface is configured for 32-bit asynchronous mode or EISA-like burst mode. |
| 26 | EEEN | Ipd | EEPROM Enable<br>EEPROM is enabled and connected when this pin is pull-up.<br>EEPROM is disabled when this pin is pull-down or no connect. |
| 27 | P1LED3 | Opd | Port 1 LED indicator<br>See the description in pins 3, 4, and 5. |
| 28 | EEDO | Opd | EEPROM Data Out<br>This pin is connected to DI input of the serial EEPROM. |
| 29 | EESK | Opd | EEPROM Serial Clock<br>A 4μs serial output clock to load configuration data from the serial EEPROM. |
| 30 | EEDI | Ipd | EEPROM Data In<br>This pin is connected to DO output of the serial EEPROM when EEEN is pull-up.<br>This pin can be pulled-down for 8-bit bus mode, pulled-up for 16-bus mode or either way for 32-bus mode when EEEN is pulled-down (without EEPROM). |
| 31 | SWR | Ipd | Synchronous Write/Read<br>Write/Read signal for synchronous bus accesses. Write cycles when high and Read cycles when low. |
| 32 | AEN | Ipu | Address Enable<br>Address qualifier for the address decoding, active Low. |
| 33 | WRN | Ipd | Write Strobe Not Asynchronous write strobe, active Low. |

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 34 | DGND | Gnd | Digital IO ground |
| 35 | ADSN | Ipd | Address Strobe Not<br>For systems that require address latching, the rising edge of ADSN indicates the latching moment of A15-A1 and AEN. |
| 36 | PWRDN | Ipu | Full-chip power-down. Low = Power down; High or floating = Normal operation. |
| 37 | AGND | Gnd | Analog ground |
| 38 | VDDA | P | 1.2V analog $V_{DD}$ input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 39 | AGND | Gnd | Analog ground |
| 40 | NC | — | No connect |
| 41 | 100FX/10FL | Ipu | Fiber mode select for port 1. 1K ohm pull-up to 3.3V for 100Base-FX, 100 ohm pull-down to GND for 100Base-SX or 10Base-FL. |
| 42 | AGND | Gnd | Analog ground |
| 43 | VDDA | P | 1.2V analog $V_{DD}$ input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 44 | FXSD1 | I | Fiber signal detect input for port 1 in 100Base-FX fiber mode. 1K ohm pull-up to 3.3V for port 1 in 100Base-SX or 10Base-FL fiber modes. |
| 45 | RXP1 | I/O | Port 1 physical receive (MDI) signal (+ differential) from external fiber module |
| 46 | RXM1 | I/O | Port 1 physical receive (MDI) signal (– differential) from external fiber module |
| 47 | AGND | Gnd | Analog ground |
| 48 | TXP1 | I/O | Port 1 physical transmit (MDI) signal (+ differential) to external fiber module |
| 49 | TXM1 | I/O | Port 1 physical transmit (MDI) signal (– differential) to external fiber module |
| 50 | VDDATX | P | 3.3V analog $V_{DD}$ input power supply with well decoupling capacitors. |
| 51 | VDDARX | P | 3.3V analog $V_{DD}$ |
| 52 | RXM2 | I/O | Port 2 physical receive (MDI) or transmit (MDIX) signal (- differential) |
| 53 | RXP2 | I/O | Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential) |
| 54 | AGND | Gnd | Analog ground |
| 55 | TXM2 | I/O | Port 2 physical transmit (MDI) or receive (MDIX) signal (- differential) |
| 56 | TXP2 | I/O | Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential) |
| 57 | VDDA | P | 1.2 analog $V_{DD}$ input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 58 | AGND | Gnd | Analog ground |
| 59 | NC | Ipu | No connect |
| 60 | NC | Ipu | No connect |
| 61 | ISET | O | Set physical transmits output current.<br>Pull-down this pin with a 3.01K 1% resistor to ground. |
| 62 | AGND | Gnd | Analog ground |
| 63 | VDDAP | P | 1.2V analog $V_{DD}$ for PLL input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 64 | AGND | Gnd | Analog ground |
| 65 | X1 | I | 25MHz crystal or oscillator clock connection.<br>Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect.<br>Note: Clock is 50ppm for either crystal or oscillator. |
| 66 | X2 | O | |
| 67 | RSTN | Ipu | Hardware reset pin (active Low). This reset input is required minimum of 10ms low after stable supply voltage 3.3V. |

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 68 | A15 | I | Address 15 |
| 69 | A14 | I | Address 14 |
| 70 | A13 | I | Address 13 |
| 71 | A12 | I | Address 12 |
| 72 | A11 | I | Address 11 |
| 73 | A10 | I | Address 10 |
| 74 | A9 | I | Address 9 |
| 75 | A8 | I | Address 8 |
| 76 | A7 | I | Address 7 |
| 77 | A6 | I | Address 6 |
| 78 | DGND | Gnd | Digital IO ground |
| 79 | VDDIO | P | 3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors. |
| 80 | A5 | I | Address 5 |
| 81 | A4 | I | Address 4 |
| 82 | A3 | I | Address 3 |
| 83 | A2 | I | Address 2 |
| 84 | A1 | I | Address 1 |
| 85 | BE3N | I | Byte Enable 3 Not, Active low for Data byte 3 enable. |
| 86 | BE2N | I | Byte Enable 2 Not, Active low for Data byte 2 enable. |
| 87 | BE1N | I | Byte Enable 1 Not, Active low for Data byte 1 enable. |
| 88 | BE0N | I | Byte Enable 0 Not, Active low for Data byte 0 enable. |
| 89 | D31 | I/O | Data 31 |
| 90 | DGND | Gnd | Digital core ground |
| 91 | VDDC | P | 1.2V digital core $V_{DD}$ input power supply from VDDCO (pin24) through external Ferrite bead and capacitor. |
| 92 | VDDIO | P | 3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors. |
| 93 | D30 | I/O | Data 30 |
| 94 | D29 | I/O | Data 29 |
| 95 | D28 | I/O | Data 28 |
| 96 | D27 | I/O | Data 27 |
| 97 | D26 | I/O | Data 26 |
| 98 | D25 | I/O | Data 25 |
| 99 | D24 | I/O | Data 24 |
| 100 | D23 | I/O | Data 23 |
| 101 | D22 | I/O | Data 22 |
| 102 | D21 | I/O | Data 21 |
| 103 | D20 | I/O | Data 20 |
| 104 | D19 | I/O | Data 19 |
| 105 | D18 | I/O | Data 18 |
| 106 | D17 | I/O | Data 17 |
| 107 | DGND | Gnd | Digital IO ground |
| 108 | VDDIO | P | 3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors. |

| Pin Number | Pin Name | Type | Pin Function |
|---|---|---|---|
| 109 | D16 | I/O | Data 16 |
| 110 | D15 | I/O | Data 15 |
| 111 | D14 | I/O | Data 14 |
| 112 | D13 | I/O | Data 13 |
| 113 | D12 | I/O | Data 12 |
| 114 | D11 | I/O | Data 11 |
| 115 | D10 | I/O | Data 10 |
| 116 | D9 | I/O | Data 9 |
| 117 | D8 | I/O | Data 8 |
| 118 | D7 | I/O | Data 7 |
| 119 | D6 | I/O | Data 6 |
| 120 | D5 | I/O | Data 5 |
| 121 | D4 | I/O | Data 4 |
| 122 | D3 | I/O | Data 3 |
| 123 | DGND | Gnd | Digital IO ground |
| 124 | DGND | Gnd | Digital core ground |
| 125 | VDDIO | P | 3.3V digital $V_{DDIO}$ input power supply for IO with well decoupling capacitors. |
| 126 | D2 | I/O | Data 2 |
| 127 | D1 | I/O | Data 1 |
| 128 | D0 | I/O | Data 0 |

**Legend:**

P = Power supply Gnd = Ground

I/O = Bi-directional I = Input O = Output

Ipd = Input with internal pull-down

Ipu = Input with internal pull-up

Opd = Output with internal pull-down

Opu = Output with internal pull-up

# Functional Description

The KSZ8862M contains two 10/100 physical layer transceivers (PHYs), two MAC units, and a DMA channel integrated with a Layer-2 switch.

The KSZ8862M contains a bus interface unit (BIU), which controls the KSZ8862M via an 8, 16, or 32-bit host interface.

Physical signal transmission and reception are enhanced through the use of analog circuits in the PHY that make the design more efficient and allow for low power consumption.

# Functional Overview: Physical Layer Transceiver

### 100BASE-TX Transmit

The 100BASE-TX transmit function (port 2 only) performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external1% 3.01KΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

### 100BASE-TX Receive

The 100BASE-TX receiver function (port 2 only) performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to- parallel conversion.

The receiving side begins with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based upon comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

### Scrambler/De-scrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

### 100BASE-FX Operation

100BASE-FX operation is supported on port 1 and similar to 100BASE-TX operation with the differences being that the scrambler/descrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In addition, auto-negotiation is bypassed and auto MDI/MDI-X is disabled.

### 100BASE-FX Signal Detection

In 100BASE-FX operation, FXSD1 (fiber signal detect), input pin 44, is usually connected to the fiber transceiver

SD (signal detect) output pin. 100BASE-FX mode is activated when the FXSD1 input pin is greater than 1V. When FXSD1 is between 1V and 1.8V, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD1 is over 2.2V, the fiber signal is detected. Alternatively, the designer may choose not to implement the FEF feature. In this case, the FXSD1 input pin is tied high to force 100BASE-FX mode.

The 100BASE-FX signal detection is summarized as below:

When FXSD1 input voltage is less than 0.2V, this is not a fiber mode or there is no fiber connection.

When FXSD1 input voltage is greater than 1.0V but less than 1.8V, this is a FX mode but no signal detected and far-end fault generated.

When FXSD1 input voltage is greater than 2.2V, this is a FX mode with signal detected.

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD1 pin's input voltage threshold.

**100BASE-FX Far-End-Fault (FEF)**

A far-end-fault (FEF) occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8862M detects a FEF when its FXSD1 input on port 1 is between 1V and 1.8V. When a FEF is detected, the KSZ8862M signals its fiber link partner that a FEF has occurred by sending 84 1's followed by a zero in the idle period between frames.

By default, FEF is enabled. FEF can be disabled through register setting at P1MBCR (bit2) or P1CR4 (bit12).

**100BASE-SX Operation**

100BASE-SX operation is supported on port 1 only. It conforms to the TIA/EIA-785 Standard for 100BASE-SX fiber operation. Fiber Link Negotiation Pulse (FLNP) Bursts are used to advertise link capabilities to the link partner during fiber auto-negotiation. FLNP Bursts are equivalent to the Fast Link Pulse (FLP) Bursts used in 10BASE-T and 100BASE-TX auto-negotiation defined by clause 28 of the IEEE802.3 Standard. Refer to respective Standard for details.

***Physical Interface***

For 100BASE-SX operation, port 1 interfaces with an external fiber module to drive 850nm fiber optic links up to a maximum distance of 300m. The interface connections between the KSZ8862M and fiber module are single-ended (common mode). 100BASE-SX signal transmission and reception are done on TXM1 (pin 49) and RXM1 (pin 46), respectively. Refer to Micrel reference schematic for recommended interface circuit and termination.

***Enabling 100BASE-SX Mode***

To enable 100BASE-SX mode, tie FXSD1 (pin 44) to high (+3.3V) and 100FX/10FL (pin 41)-to-ground.

***Enabling Fiber Forced Mode***

In 100BASE-SX mode, the KSZ8862M supports forced mode only.

For forced mode, port 1 has auto-negotiation disabled, is forced to 100Mbps for the speed, and is set to either half or full duplex. Optionally, flow control can be enabled to send out PAUSE frames in full duplex mode.

Forced mode and auto-negotiation disabled mode settings for 100BASE-SX fiber use the same registers (P1MBCR, P1CR4). These registers are summarized in the Register Map section.

**10BASE-FL Operation**

10BASE-FL operation is supported on port 1 only. It conforms to clause 15 and 18 of the IEEE802.3 Standard for 10BASE-FL fiber operation. Fiber Link Negotiation Pulse (FLNP) Bursts are used to advertise link capabilities to the link partner during fiber auto-negotiation. FLNP Bursts are equivalent to the Fast Link Pulse (FLP) Bursts used in 10BASE-T and 100BASE-TX auto-negotiation defined by clause 28 of the IEEE802.3 Standard. Refer to respective Standard for details.

***Physical Interface***

For 10BASE-FL operation, port 1 interfaces with an external fiber module to drive 850nm fiber optic links up to a maximum distance of 2km. The interface connections between the KSZ8862M and fiber module are single-ended (common mode). 10BASE-FL signal transmission and reception are done on TXM1 (pin 49) and RXM1 (pin 46), respectively. Refer to Micrel reference schematic for recommended interface circuit and termination.

***Enabling 10BASE-FL Mode***

To enable 10BASE-FL mode, tie FXSD1 (pin 44) to high (+3.3V) and 100FX/10FL (pin 41)-to-ground.

***Enabling Fiber Forced Mode***

In 10BASE-FL mode, the KSZ8862M supports forced mode only.

For forced mode, port 1 has auto-negotiation disabled, is forced to 10Mbps for the speed, and is set to either half or full duplex. Optionally, flow control can be enabled to send out PAUSE frames in full duplex mode.

Forced mode and auto-negotiation disabled mode settings for 10BASE-FL fiber use the same registers (P1MBCR, P1CR4). These registers are summarized in the Register Map section.

**10BASE-T Transmit**

The 10BASE-T driver (port 2 only) is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with typically 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

**10BASE-T Receive**

On the receive side (port 2 only), input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8862M decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

**LED Driver**

The device provides a current mode fiber LED driver (port 1 only). The edge-enhanced current mode does not require any output wave shaping. The drive current of the LED driver can be programmed through ATCR0 [7:6] register in Bank 44.

**Post Amplifier**

The chip also includes a post amplifier (port 1 only). The post amplifier is intended for interfacing the output of the pre-amplifier of the PIN diode module. The minimum sensitivity of the amplifier is 2.5 mV (rms) for 10Base-FL receive on pin RXM1 or 16mV (rms) for 100Base-SX receive on pin RXM1.

**Power Management**

The KSZ8862M features per port power-down mode. To save power, the user can power-down the port that is not in use by setting bit 11 in either P1CR4 or P1MBCR register for port 1 and setting bit 11 in either P2CR4 or P2MBCR register for port 2. To bring the port back up, reset bit 11 in these registers.

In addition, there is a full switch power-down mode. This mode shuts the entire switch down, when the PWRDN (pin 36) is pulled down to low.

**MDI/MDI-X Auto Crossover**

To eliminate the need for crossover cables between similar devices, the KSZ8862M supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover on port 2. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8862M device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

The IEEE 802.3u standard MDI and MDI-X definitions are:

| **MDI** | | **MDI-X** | |
|---|---|---|---|
| **RJ45 Pins** | **Signals** | **RJ45 Pins** | **Signals** |
| 1 | TD+ | 1 | RD+ |
| 2 | TD- | 2 | RD- |
| 3 | RD+ | 3 | TD+ |
| 6 | RD- | 6 | TD- |

**Table 1. MDI/MDI-X Pin Definitions**