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KSZ8864CNX/RMNUB

Integrated 4-Port 10/100 Managed Switch with Two MACs MII or RMII Interfaces

Features

Advanced Switch Features

- IEEE 802.1q VLAN Support for up to 128 VLAN Groups (Full-Range 4096 of VLAN IDs)
- Static MAC Table Supports up to 32 Entries
- VLAN ID Tag/Untagged Options, Per Port Basis
- IEEE 802.1p/q Tag Insertion or Removal on a Per Port Basis Based on Ingress Port (Egress)
- Programmable Rate Limiting at the Ingress and Egress on a Per Port Basis
- Jitter-Free Per Packet Based Rate Limiting Support
- Broadcast Storm Protection with Percentage Control (Global and Per Port Basis)
- IEEE 802.1d Rapid Spanning Tree Protocol RSTP Support
- Tail Tag Mode (1 Byte Added Before FCS) Support at Port 4 to Inform the Processor Which Ingress Port Receives the Packet
- 1.4 Gbps High-Performance Memory Bandwidth and Shared Memory Based Switch Fabric with Fully Non-Blocking Configuration
- Dual MII/RMII with MAC 3 SW3-MII/RMII and MAC 4 SW4-MII/RMII Interfaces
- Enable/Disable Option for Huge Frame Size up to 2000 Bytes Per Frame
- IGMP v1/v2 Snooping (IPv4) Support for Multicast Packet Filtering
- IPv4/IPv6 QoS Support
- Support Unknown Unicast/Multicast Address and Unknown VID Packet Filtering
- Self-Address Filtering

Comprehensive Configuration Register Access

- Serial Management Interface (MDC/MDIO) to All PHYs Registers and SMI Interface (MDC/MDIO) to All Registers
- High-Speed SPI (up to 25 MHz) and I^2C Master Interface to all Internal Registers
- I/O Pins Strapping and EEPROM to Program Selective Registers in Unmanaged Switch Mode
- Control Registers Configurable on the Fly (Port-Priority, 802.1p/d/q, AN…)

QoS/CoS Packet Prioritization Support

- Per Port, 802.1p and DiffServ-Based
- 1/2/4-Queue QoS Prioritization Selection
- Programmable Weighted Fair Queuing for Ratio Control
- Re-Mapping of 802.1p Priority Field Per Port Basis

Integrated 4-Port 10/100 Ethernet Switch

- New Generation Switch with Four MACs and Four PHYs that are Fully Compliant with the IEEE 802.3u Standard
- Non-Blocking Switch Fabric Ensures Fast Packet Delivery by Utilizing a 1K MAC Address Lookup Table and a Store-and-Forward Architecture
- On-Chip 64Kbyte Memory for Frame Buffering (Not Shared with 1K Unicast Address Table)
- Full-Duplex IEEE 802.3x Flow Control (PAUSE) with Force Mode Option
- Half-Duplex Back Pressure Flow Control
- HP Auto MDI/MDI-X and IEEE Auto Crossover Support
- LinkMD® TDR-Based Cable Diagnostics to Identify Faulty Copper Cabling
- MII Interface of MAC Supports Both MAC Mode and PHY Mode
- Per Port LED Indicators for Link, Activity, and 10/100 Speed
- Register Port Status Support for Link, Activity, Full-/Half-Duplex and 10/100 Speed
- On-Chip Terminations and Internal Biasing Technology for Cost Down and Lowest Power Consumption

Switch Monitoring Features

- Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port or MII/RMII
- MIB Counters for Fully Compliant Statistics Gathering 34 MIB Counters Per Port
- Loopback Support for MAC, PHY, and Remote Diagnostic of Failure
- Interrupt for the Link Change on Any Ports

Low-Power Dissipation

- Full-Chip Software Power-Down and Per Port Software Power-Down
- Energy-Detect Mode Support <0.1W Full-Chip Power Consumption When All Ports Have No Activity
- Very-Low Full-Chip Power Consumption (~0.3W), without Extra Power Consumption on Transformers

- Dynamic Clock Tree Shutdown Feature
- Voltages:
  - Analog VDDAT 3.3V Only
  - VDDIO Support 3.3V, 2.5V, and 1.8V
  - Low 1.2V Core Power
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Automotive AEC-Q100 Grade 3 Temperature Range: –40°C to +85°C
- Available in 64-pin QFN, Lead-Free Small Package

Target Applications

- VoIP Phone
- Set-Top/Game Box
- Automotive Ethernet
- Industrial Control
- IPTV POF
- SOHO Residential Gateway
- Broadband Gateway/Firewall/VPN
- Integrated DSL/Cable Modem
- Wireless LAN Access Point + Gateway
- Standalone 10/100 Switch
- Embedded System

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8864CNX/RMNUB is a highly-integrated, Layer 2-managed 4-port switch with optimized design, plentiful features and smallest package size. It is designed for cost-sensitive 10/100 Mbps 4-port switch systems with on-chip termination, lowest-power consumption, and small package to save system cost. It has 1.4 Gbps high-performance memory bandwidth, shared memory-based switch fabric with full non-blocking configuration. It also provides an extensive feature set such as the power management, programmable rate limiting and priority ratio, tag/port-based VLAN, packet filtering, quality-of-service (QoS), four queue prioritization, management interface, MIB counters. Port 3 and Port 4 support either MII or RMII interfaces with SW3-MII/RMII and SW4-MII/RMII (see Figure 1-1) for KSZ8864CNX/RMNUB data interface. An industrial temperature-grade version of the KSZ8864CNXIA and a qualified AEC-Q100 Automotive version of the KSZ8864RMNUB are also available (see the Product Information System section).The KSZ8864CNX/RMNUB provides multiple CPU control/data interfaces to effectively address both current and emerging fast Ethernet applications.

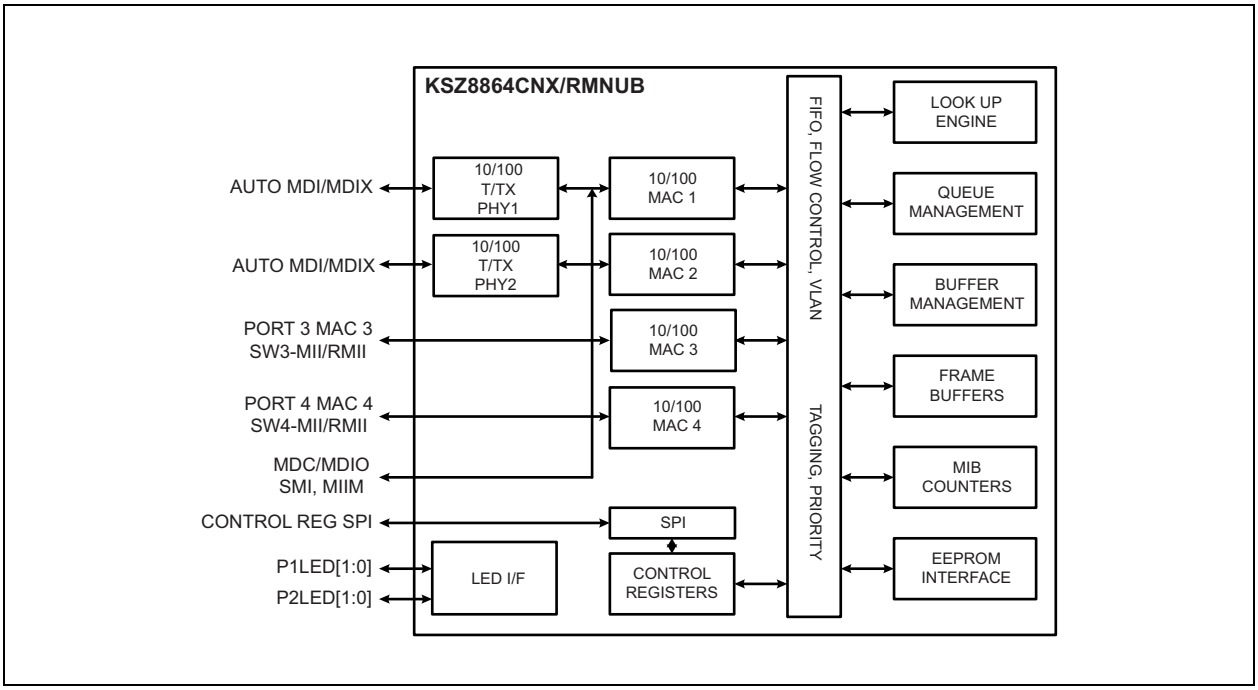
The KSZ8864CNX/RMNUB consists of 10/100 fast Ethernet PHYs with patented and enhanced mixed-signal technology, media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

The KSZ8864CNX/RMNUB contains four MACs and two PHYs. The two PHYs support the 10/100Base-T/TX.

All registers of MACs and PHYs units can be managed by the control interface of SPI or the SMI. MIIM registers of the PHYs can be accessed through the MDC/MDIO interface. EEPROM can set all control registers by I^2C controller interface for the unmanaged mode.

KSZ8864CNX/RMNUB is a 0.11 µm technical device and adding Microchip's LinkMD® feature, KSZ8864CNX/RMNUB is completely pin-compatible with the KSZ8864RMN device.

FIGURE 1-1: FUNCTIONAL DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 64-QFN PIN ASSIGNMENT (TOP VIEW)

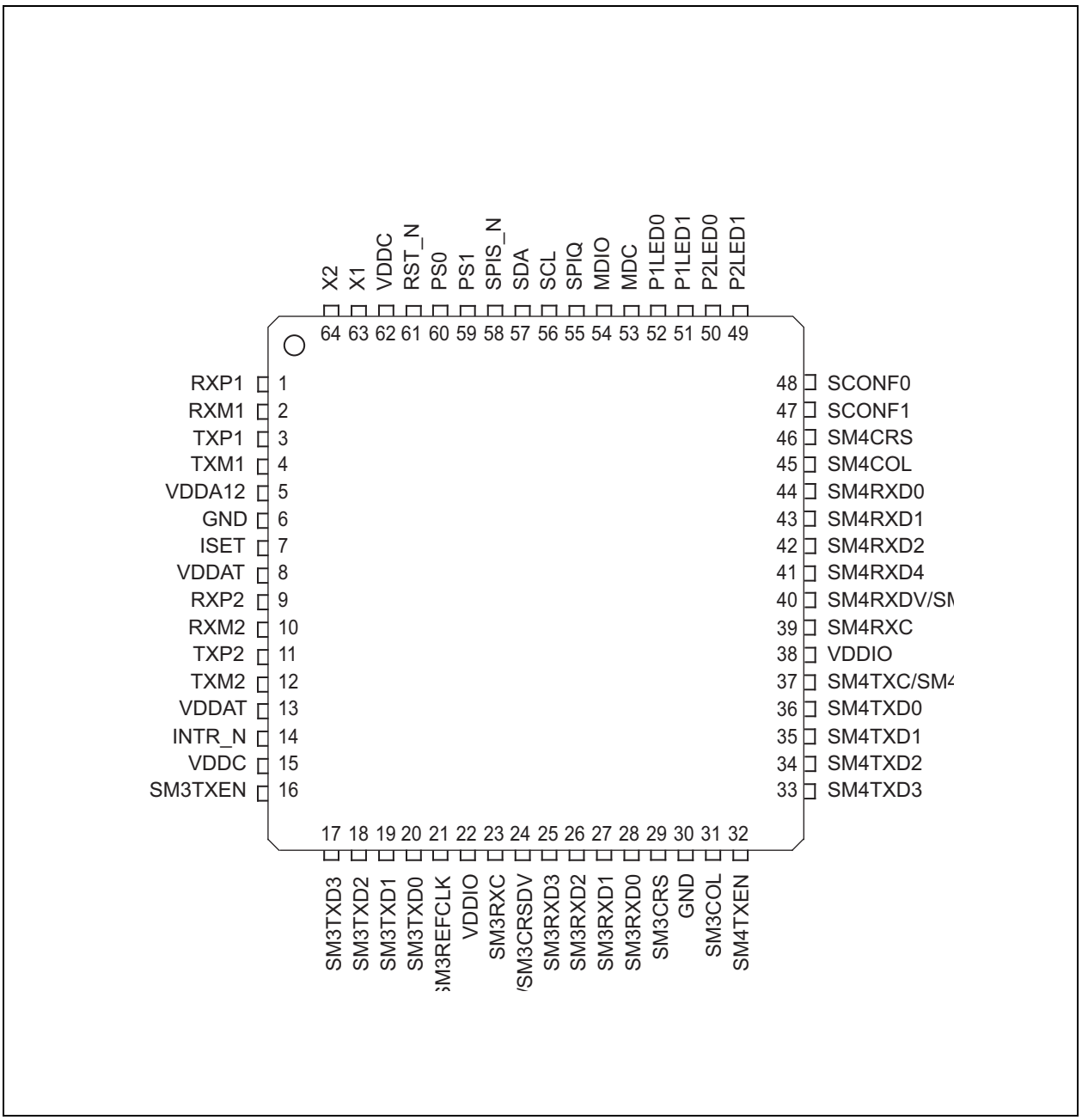


TABLE 2-1: SIGNALS - KSZ8864CNX/RMNUB

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
1	RXP1	I	1	Physical receive signal + (differential)
2	RXM1	I	1	Physical receive signal – (differential)
3	TXP1	O	1	Physical transmit signal + (differential)
4	TXM1	O	1	Physical transmit signal – (differential)
5	VDDA12	P	—	1.2V analog power
6	GND	GND	—	Ground with all grounding of die bottom
7	ISET	—	—	Set physical transmit output current. Pull-down with a 12.4 kΩ 1% resistor.
8	VDDAT	P	—	3.3V analog V_{DD}
9	RXP2	I	2	Physical receive signal + (differential)
10	RXM2	I	2	Physical receive signal – (differential)
11	TXP2	O	2	Physical transmit signal + (differential)
12	TXM2	O	2	Physical transmit signal – (differential)
13	VDDAT	P	—	3.3V analog V_{DD}
14	INTR_N	OPU	—	Interrupt. This pin is the Open-Drain output pin.
15	VDDC	P	—	1.2V digital core V_{DD}
16	SM3TXEN	IPD	3	MAC3 switch MII/RMII transmit enable
17	SM3TXD3	IPD	3	MAC3 switch MII transmit bit 3
18	SM3TXD2	IPD	3	MAC3 switch MII transmit bit 2
19	SM3TXD1	IPD	3	MAC3 switch MII/RMII transmit bit 1
20	SM3TXD0	IPD	3	MAC3 switch MII/RMII transmit bit 0
21	SM3TXC/ SM3REFCLK	I/O	3	MAC3 switch MII transmit clock: Input: SW3-MII MAC mode Output: SW3-MII PHY mode Input: SW3-RMII reference clock
22	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry
23	SM3RXC	I/O	3	MAC3 switch MII receive clock: Input: SW3-MII MAC mode Output: SW3-MII PHY mode Output: SW3-RMII reference clock Unused RMII clock can be pull-down or disable by Register 87.
24	SM3RXDV/ SM3CRSDV	IPD/O	3	SM3RXDV: MAC3 switch SW3-MII receives data valid. SM3CRSDV: MAC3 switch SW3-RMII carrier sense/receive data valid.

TABLE 2-1: SIGNALS - KSZ8864CNX/RMNUB (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
25	SM3RXD3	IPD/O	3	MAC3 switch MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
26	SM3RXD2	IPD/O		MAC3 switch MII receive bit 2 and strap option: PD (default) = disable back pressure; PU = enable back pressure.
27	SM3RXD1	IPD/O		MAC3 switch MII/RMII receive bit 1 Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
28	SM3RXD0	IPD/O		MAC3 switch MII/RMII receive bit 0 Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
29	SM3CRS	IPD/O		MAC3 switch MII carrier sense
30	GND	GND		Ground with all grounding of die bottom
31	SM3COL	IPD/O		MAC3 switch MII collisions detect
32	SM4TXEN	IPD		MAC4 switch MII/RMII transmit enable
33	SM4TXD3	IPD		MAC4 switch MII transmit bit 3
34	SM4TXD2	IPD		MAC4 switch MII transmit bit 2
35	SM4TXD1	IPD		MAC4 switch MII/RMII transmit bit 1
36	SM4TXD0	IPD		MAC4 switch MII/RMII transmit bit 0
37	SM4TXC/ SM4REFCLK	I/O		MAC4 switch MII transmit clock: Input: SW4-MII MAC mode clock. Input: SW4-RMII reference clock, please also see the strap-in pin P1LED1 for the clock mode and normal mode. Output: SW4-MII PHY modes.
38	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry
39	SM4RXC	I/O	4	MAC4 switch MII receive clock: Input: SW4-MII MAC mode. Output: SW4-MII PHY mode. Output: SW4-RMII 50 MHz reference clock (the device is default clock mode; the clock source comes from X1/X2 pins 25 MHz crystal). When the device is set in normal mode, (the chip's clock source comes from SM4TXC), the SM4RXC reference clock output should be disabled by the Register 87. Please also see the strap-in pin P1LED1 for the selection of the clock mode and normal mode.

TABLE 2-1: SIGNALS - KSZ8864CNX/RMNUB (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
40	SM4RXDV/ SM4CRSDV	IPD/O	4	SM4RXDV: MAC4 switch SW4-MII receives data valid. SM4CRSDV: MAC4 switch SW4-RMII carrier sense/receive data valid.
41	SM4RXD3	IPD/O	4	MAC4 switch MII receive bit 3 Strap option: PD (default) = disable switch MII/RMII full-duplex flow control; PU = enable switch MII/RMII full-duplex flow control.
42	SM4RXD2	IPD/O	4	MAC4 switch MII receive bit 2 Strap option: PD (default) = switch MII/RMII in full-duplex mode; PU = switch MII/RMII in half-duplex mode.
43	SM4RXD1	IPD/O	4	MAC4 switch MII/RMII receive bit 1 Strap option: PD (default) = MAC4 switch SW4-MII/RMII in 100 Mbps mode; PU = MAC4 switch SW5-MII/RMII in 10 Mbps mode.
44	SM4RXD0	IPD/O	4	MAC4 Switch MII/RMII receive bit 0. Strap option: LED mode PD (default) = mode 0; PU = Mode 1. See “Register 11.”
				— / Mode 0 / Mode 1 PxLED1 / Link/Activity / 100Link/Activity PxLED0 / Speed / Full-duplex
45	SM4COL	IPD/O	4	MAC4 Switch MII collision detect: Input: SW4-MII MAC modes. Output: SW4-MII PHY modes.
46	SM4CRS	IPD/O	4	MAC4 Switch MII modes carrier sense: Input: SW4-MII MAC modes. Output: SW4-MII PHY modes.
47	SCONF1	IPD	—	MAC4 Switch SW4-MII enabled with PHY mode or MAC mode, have to configure SCONF1 Pin 47 with SCONF0 Pin 48 together. See pins configuration table below:
				Pin# (47, 48) / Port 4 Switch MAC4 SW4-MII 00 (default) / Port 4 SW4-MII PHY mode 01 / Disable port 3 and port 4 10 / Disable port 4 only 11 / Port 4 SW4-MII MAC mode
48	SCONF0	IPD	—	Port 4 Switch SW4-MII enabled with PHY mode or MAC mode, have to configure SCONF0 pin 48 with SCONF1 Pin 47 together. See Pin 47 description.

TABLE 2-1: SIGNALS - KSZ8864CNX/RMNUB (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
49	P2LED1	IPU/O	2	LED indicator for Port 2. This pin has to be pulled down by a 1 kΩ resistor in the design for KSZ8864CNX/RMNUB.
50	P2LED0	IPU/O	2	LED indicator for Port 2. Strap option: Switch MAC3 used only. PU (default) = Select MII interface for the Switch MAC3 SW3-MII. PD = Select RMII interface for the Switch MAC3 SW3-RMII.
51	P1LED1	IPU/O	1	LED indicator for Port 1. Strap option: Switch RMII used only. PU (default) = Select the device as clock mode, when use RMII interface, all clock source come from pin x1/x2 crystal 25 MHz. PD = Select the device as normal mode when use RMII interface. All clock sources come from SW4-RMII SM4TXC pin with an external input 50 MHz clock. In the normal mode, the 25 MHz crystal clock from pin X1/X2 doesn't take affect and should disable SW4-RMII SW4RXC 50 MHz clock output by the register 87. The normal mode is used when SW4-RMII receive an external 50 MHz RMII reference clock from pin SM4TXC.
52	P1LED0	IPU/O	1	LED indicator for Port 1. Strap option: for Switch MAC4 only. PU (default) = Select MII interface for the Switch MAC4 SW4-MII. PD = Select RMII interface for the Switch MAC4 SW4-RMII.
53	MDC	IPU	All	MII management interface clock. Or SMI interface clock
54	MDIO	IPU/O	All	MII management data I/O. Or SMI interface data I/O Features internal pull-down to define pin state when not driven. Note: Need an external pull-up when driven.
55	SPIQ	IPU/O	All	SPI serial data output in SPI slave mode. Note: Need an external pull-up when driven.
56	SPIC/SCL	IPU/O	All	(1) Input clock up to 25 MHz in SPI slave mode, (2) Output clock at 61 kHz in I^2C master mode. Note: Need an external pull-up when driven.
57	SPID/SDA	IPU/O	All	(1) Serial data input in SPI slave mode; (2) Serial data input/output in I^2C master mode. Note: Need an external pull-up when driven.
58	SPIS_N	IPU	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the device is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer. (2) Not used in I^2C master mode.

TABLE 2-1: SIGNALS - KSZ8864CNX/RMNUB (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2	
59	PS1	IPD	—	Serial bus configuration pin. For this case, if the EEPROM is not present, the Switch will start itself with the PS [1.0] = 00 default register values.	
				Pin Configuration	Serial Bus Configuration
				PS[1.0]=00	I^2C Master Mode for EEPROM
				PS[1.0]=01	SMI Interface Mode
				PS[1.0]=10	SPI Slave Mode for CPU Interface
				PS[1.0]=11	Factory Test Mode (BIST)
60	PS0	IPD	—	Serial bus configuration pin.	
61	RST_N	IPU	—	Reset the device. Active low.	
62	VDDC	P	—	1.2V digital core V_{DD}.	
63	X1	I	—	25 MHz crystal clock connection or 3.3V oscillator input. Crystal/ oscillator should be ≤ ±50 ppm tolerance.	
64	X2	O	—	25 MHz crystal clock connection.	

Note 2-1 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
IPD = Input with internal pull-down.
IPU = Input with internal pull-up.
IPU/O = Input with internal pull-up during reset; output pin otherwise.
IPD/O = Input with internal pull-down during reset; output pin otherwise.

Note 2-2 PU = strap pin pull-up
PD = strap pin pull-down

The KSZ8864CNX/RMNUB can function as a managed switch or unmanaged switch. If no EEPROM or microcontroller exists, the KSZ8864CNX/RMNUB will operate from its default setting. The strap-in option pins can be configured by external pull-up/down resistors and take effect after power-up reset or warm reset. The functions are described in the following table.

TABLE 2-2: STRAP-IN OPTIONS - KSZ8864CNX/RMNUB

Pin Number	Pin Name	Type, Note 2-3	Port	Description, Note 2-4
25	SM3RXD3	IPD/O	—	MAC3 Switch MII receive bit 3 Strap option: PD (default) = enable flow control; PU = disable flow control.
26	SM3RXD2	IPD/O	—	MAC3 Switch MII receive bit 2 and Strap option: PD (default) = disable back pressure; PU = enable back pressure.
27	SM3RXD1	IPD/O	—	MAC3 Switch MII/RMII receive bit 1 Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
28	SM3RXD0	IPD/O	—	MAC3 Switch MII/RMII receive bit 0 Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
41	SM4RXD3	IPD/O	—	MAC4 Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII/RMII full-duplex flow control; PU = Enable Switch MII/RMII full-duplex flow control.
42	SM4RXD2	IPD/O	—	MAC4 Switch MII receive bit 2. Strap option: PD (default) = Switch MII/RMII in full-duplex mode; PU = Switch MII/RMII in half-duplex mode.
43	SM4RXD1	IPD/O	—	MAC4 Switch MII/RMII receive bit 1. Strap option: PD (default) =MAC4 Switch SW4-MII/RMII in 100 Mbps mode; PU = MAC4 Switch SW-5MII/RMII in 10 Mbps mode.
44	SM4RXD0	IPD/O	—	MAC4 Switch MII/RMII receive bit 0. Strap option: LED mode PD (default) = mode 0; PU = mode 1. See “Register 11.”

—	Mode 0	Mode 1
PxLED1	Link/Activity	100Link/Activity
PxLED0	Speed	Full-duplex

TABLE 2-2: STRAP-IN OPTIONS - KSZ8864CNX/RMNUB (CONTINUED)

Pin Number	Pin Name	Type, Note 2-3	Port	Description, Note 2-4	
47	SCONF1	IPD	—	MAC4 Switch SW4-MII enabled with PHY mode or MAC mode, have to configure SCONF1 Pin 47 with SCONF0 Pin 48 together. See pins configuration table below:	
				Pin# (47, 48)	Switch MAC4 SW4-MII/RMII
				00 (default)	Port 4 SW4-MII PHY mode
				01	Disable port 3 and port 4
				10	Disable port 4 only
				11	Port 4 SW4-MII MAC mode
48	SCONF0	IPD	—	Port 4 Switch SW4-MII enabled with PHY mode or MAC mode, have to configure SCONF0 Pin 48 with SCONF1 Pin 47 together. See pin 47 description.	
49	P2LED1	IPU/O	2	LED indicator for Port 2. This pin has to be pulled down by 1 kΩ resistor in the design for KSZ8864CNX/RMNUB.	
50	P2LED0	IPU/O	2	LED indicator for Port 2. Strap option: Switch MAC3 used only. PU (default) = Select MII interface for the Switch MAC3 SW3-MII. PD = Select RMII interface for the Switch MAC3 SW3-RMII.	
51	P1LED1	IPU/O	1	LED indicator for Port 1. Strap option: Switch RMII used only. PU (default) = Select the device as clock mode. When use RMII interface, all clock source come from Pin x1/x2 crystal 25 MHz. PD = Select the device as normal mode when use RMII interface. All clock sources come from SW4-RMII SM4TXC pin with an external input 50 MHz clock. In the normal mode, the 25 MHz crystal clock from pin X1/X2 doesn't take affect and should disable SW4-RMII SW4RXC 50 MHz clock output by the Register 87. The normal mode is used when SW4-RMII receive an external 50 MHz RMII reference clock from pin SM4TXC.	
52	P1LED0	IPU/O	1	LED indicator for Port 1. Strap option: for Switch MAC4 only. PU (default) = Select MII interface for the Switch MAC4 SW4-MII. PD = Select RMII interface for the Switch MAC4 SW4-RMII.	
59	PS1	IPD	—	Serial bus configuration pin. For this case, if the EEPROM is not present, the Switch will start itself with the PS [1.0] = 00 default register values.	
				Pin Configuration	Serial Bus Configuration
				PS[1.0]=00	I^2C Master Mode for EEPROM
				PS[1.0]=01	SMI Interface Mode
				PS[1.0]=10	SPI Slave Mode for CPU Interface
				PS[1.0]=11	Factory Test Mode (BIST)

Note 2-3 IPU = Input with internal pull-up
IPD = Input with internal pull-down

IPU/O = Input with internal pull-up during reset; output pin otherwise
IPD/O = Input with internal pull-down during reset; output pin otherwise

Note 2-4 PU = Strap pin pull-up
PD = Strap pin pull-down

3.0 FUNCTIONAL DESCRIPTION

The KSZ8864CNX/RMNUB contains two 10/100 physical layer transceivers and four media access control (MAC) units with an integrated Layer 2 managed switch. The device runs in multiple modes. They are two copper plus two MAC MII, two copper plus two MAC RMII, two copper plus 1 MAC MII plus 1 MAC RMII, and two copper plus 1 MAC MII or 1 MAC RMII. These are useful for implementing multiple products in many applications.

The KSZ8864CNX/RMNUB has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the KSZ8864CNX/RMNUB via the SPI bus, or partial control via the MDC/MDIO interface. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KSZ8864CNX/RMNUB supports IEEE 802.3 10BASE-T/100BASE-TX on all ports with Auto MDI/MDIX. The KSZ8864CNX/RMNUB can be used as fully managed 4-port switch through two microprocessors by its two MII interface or RMII interface for an advance management application.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry with enhanced mixed signal technology that makes the design more efficient and allows for lower power consumption and smaller chip die size.

Major enhancements from the KS8864RMN to the KSZ8864CNX/RMNUB include further power saving, adding Microchip's LinkMD® feature and 0.11 µm silicon process technology. The KSZ8864CNX/RMNUB is completely pin-compatible with the KSZ8864RMN.

3.1 Physical Layer Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversions, 4B/5B coding, scrambling, NRZ-to-NRZI conversions, MLT3 encoding, and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 12.4 kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and it can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler, followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.1.3 PLL CLOCK SYNTHESIZER

The KSZ8864CNX/RMNUB generates 125 MHz, 83 MHz, 41 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator.

3.1.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

3.1.5 10BASE-T TRANSMIT

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

3.1.6 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8864CNX/RMNUB decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.7 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8864CNX/RMNUB supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the switch device. This feature is extremely useful when end users are unaware of cable types and saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers or MIIM PHY registers. The IEEE 802.3u standard MDI and MDI-X definitions are:

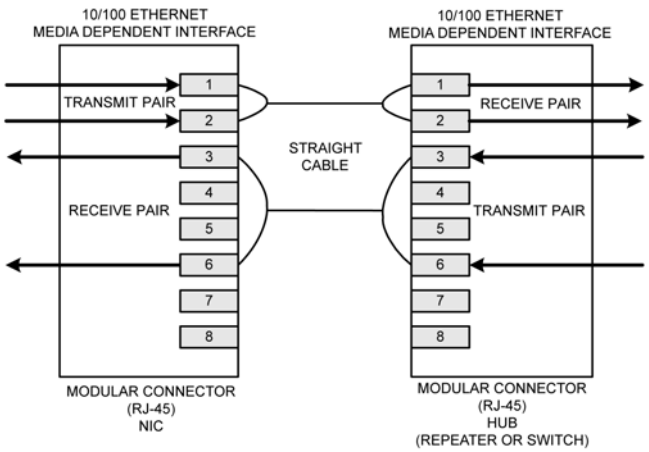
TABLE 3-1: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.1.7.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

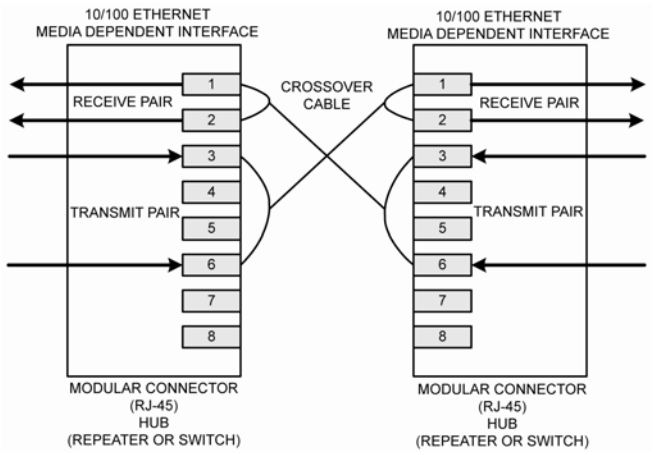
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.1.7.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



3.1.8 AUTO-NEGOTIATION

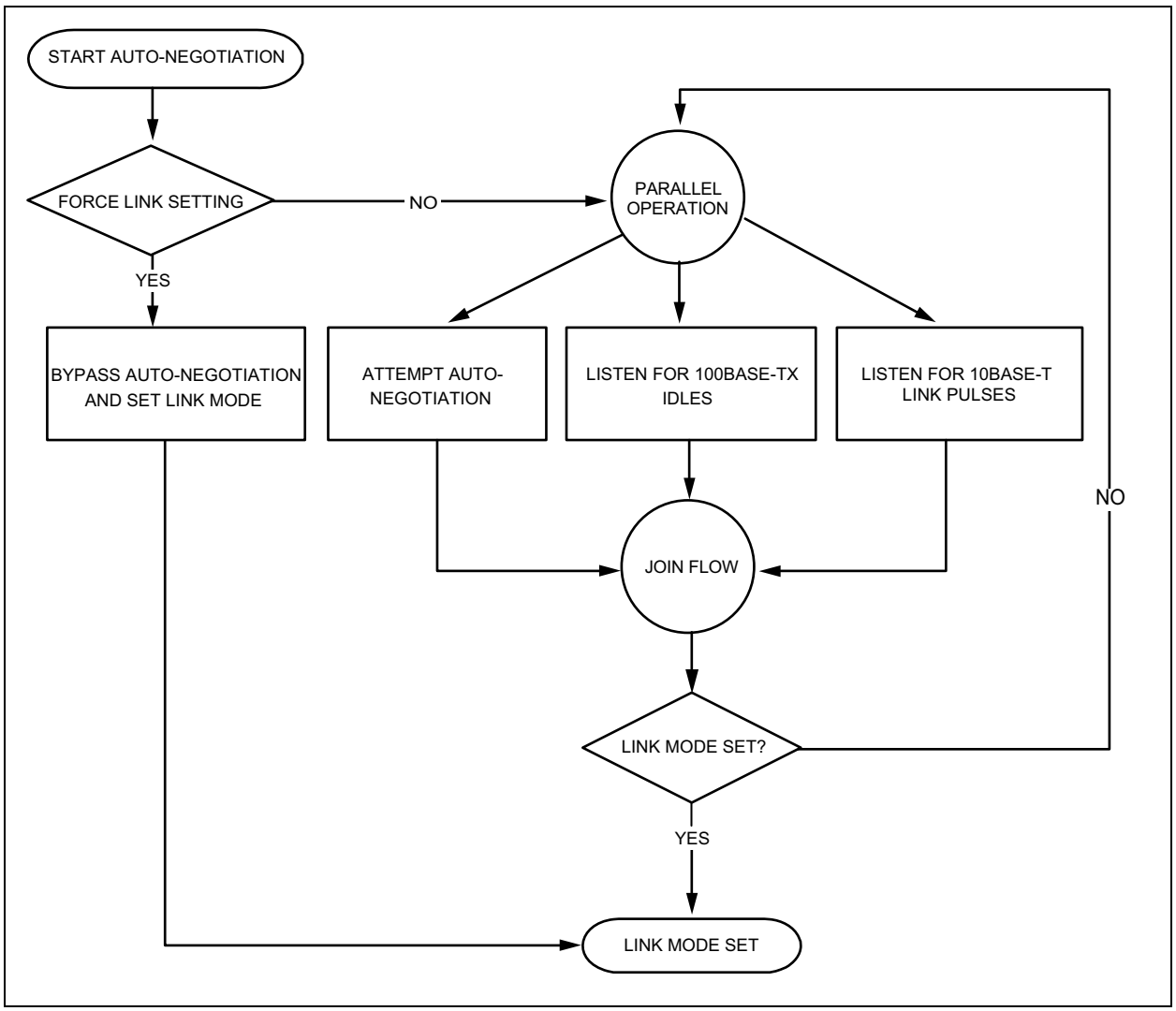
The KSZ8864CNX/RMNUB conforms to the auto-negotiation protocol as described by the IEEE 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ8864CNX/RMNUB link partner is forced to bypass auto-negotiation, then the KSZ8864CNX/RMNUB sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8864CNX/RMNUB to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. The auto-negotiation link up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION FLOW CHART



3.1.9 LINKMD® CABLE DIAGNOSTICS

The LinkMD® feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with maximum distance of 200m and accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format.

Note: Cable diagnostics are only valid for copper connections and do not support fiber optic operation.

3.1.9.1 Access

LinkMD is initiated by accessing the PHY special control/status Registers {42, 58} and the LinkMD result Registers {43, 59} for ports 1 and 2 respectively; and in conjunction with the registers port control 12 and 13 for ports 1 and 2 respectively to disable auto-negotiation and Auto MDI/MDIX.

Alternatively, the MIIM PHY Registers 0 and 1d can also be used for LinkMD access.

3.1.9.2 Usage

The following is a sample procedure for using LinkMD with Registers {42, 43, 44, 45} on port 1.

1. Disable Auto-Negotiation by writing a '1' to Register 44 (0x2c), bit [7].
2. Disable auto MDI/MDI-X by writing a '1' to Register 45 (0x2d), bit [2] to enable manual control over the differential pair used to transmit the LinkMD pulse.
3. A software sequence set up to the internal registers for LinkMD only, see an example below.
4. Start cable diagnostic test by writing a '1' to Register 42 (0x2a), bit [4]. This enable bit is self-clearing.
5. Wait (poll) for Register 42 (0x2a), bit [4] to return a '0', and indicating cable diagnostic test is completed.
6. Read cable diagnostic test results in Register 42 (0x2a), bits [6:5]. The results are as follows:

   00 = normal condition (valid test)

   01 = open condition detected in cable (valid test)

   10 = short condition detected in cable (valid test)

   11 = cable diagnostic test failed (invalid test)

The '11' case, invalid test, occurs when the KSZ8864 is unable to shut down the link partner. In this instance, the test is not run, since it would be impossible for the KSZ8864 to determine if the detected signal is a reflection of the signal generated or a signal from another source.

7. Get distance to fault by concatenating Register 42 (0x2a), bit [0] and Register 43 (0x2b), bits [7:0]; and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

   D (distance to cable fault) = 0.4 x (Register 42, bit [0], Register 43, bits [7:0])

D (distance to cable fault) is expressed in meters.

Concatenated value of Registers 42 bit [0] and 43 bit [7:0] should be converted to decimal before decrease 26 and multiplying by 0.4.

The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

For port 2 and for the MIIM PHY registers, LinkMD usage is similar.

3.1.9.3 A LinkMD Example

The following is a sample procedure for using LinkMD on port 1.

```
//Set Force 100/Full and Force MDI-X mode
//W is WRITE the register. R is READ register
W 2c ff
W 2d 04
//Set Internal Registers Temporary Adjustment for LinkMD
W 47 b0
W 27 00
W 37 04 (value=04 for port1, value=05 for port2)
W 47 40 (bit6=1 for port1, bit5=1 for port2)
W 27 00
W 37 00
//Enable LinkMD Testing with Fault Cable for port 1
W 2a 10
R 2a
R 2b
//Result analysis based on the values of the Register 0x2a and 0x2b for port 1:
//The Register 0x2a bits [6-5] are for the open or the short detection.
//The Register 0x2a bit [0] + the Register 0x2b bits [7-0] = Vct_Fault [8-0]
//The distance to fault is about 0.4 x {Vct_Fault [8-0]}
```

Note: After end the testing, set all registers above to their default values. The default values are ‘00’ for the Register (0x37) and the Register (0x47)

3.1.10 ON-CHIP TERMINATION RESISTORS

The KSZ8864CNX/RMNUB reduces the board cost and simplifies the board layout by using on-chip termination resistors for all ports and RX/TX differential pairs without the external termination resistors. The combination of the on-chip termination and internal biasing will save the power consumption as compared to using external biasing and termination resistors, and the transformer will not consume power any more. The center tap of the transformer does not need to be tied to the analog power due to have this feature of the internal biasing.

3.2 Power Management

The KSZ8864CNX/RMNUB can also use multiple power levels of 3.3V, 2.5V, or 1.8V for VDDIO to support different I/O voltages.

The KSZ8864CNX/RMNUB supports an enhanced power management feature in the low power state with energy detection to ensure low power dissipation during device idle periods. There are five operation modes under the power management function, which is controlled by the Register 14 bit [4:3] and the Register Port Control 6 bit3 as shown below:

Register 14 bit [4:3] = 00 Normal Operation Mode

Register 14 bit [4:3] = 01 Energy Detect Mode

Register 14 bit [4:3] = 10 Soft Power Down Mode

Register 14 bit [4:3] = 11 Power Saving Mode

The Register Port Control 6 bit 3 =1 is for the Port-Based Power-Down Mode

Table 3-2 indicates all internal function blocks status under four different power management operation modes.

TABLE 3-2: INTERNAL FUNCTION BLOCK STATUS

Function Blocks	Power Management Operation Modes			
	Normal Mode	Power Saving Mode	Energy Detect Mode	Soft Power-Down Mode
Internal PLL Clock	Enabled	Enabled	Disabled	Disabled
TX/RX PHY	Enabled	RX unused block disabled	Energy detect at RX	Disabled
MAC	Enabled	Enabled	Disabled	Disabled
Host Interface	Enabled	Enabled	Disabled	Disabled

3.2.1 NORMAL OPERATION MODE

This is the default setting bit [4:3] = 00 in Register 14 after the chip powers-up or experiences a hardware reset. When KSZ8864CNX/RMNUB is in this normal operation mode, all PLL clocks are running, PHY and MAC are on, and the host interface is ready for CPU read or write.

During the normal operation mode, the host CPU can set the bit [4:3] in Register 14 to transit the current normal operation mode to any one of the other three power management operation modes.

3.2.2 ENERGY DETECT MODE

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8864CNX/RMNUB is not connected to an active link partner. In this mode, if the cable is not plugged, then the KSZ8864CNX/RMNUB can automatically enter to a low power state: the energy detect mode. In this mode, KSZ8864CNX/RMNUB will keep transmitting 120 ns width pulses at a rate of one pulse per second. Once activity resumes due to plugging a cable or due to an attempt by the far end to establish link, the KSZ8864CNX/RMNUB can automatically power up to its normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8864CNX/RMNUB reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit [4:3] = 01 in Register 14. When the KSZ8864CNX/RMNUB is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than pre-configured value at bit [7:0] Go-Sleep time in Register 15, then the KSZ8864CNX/RMNUB will go into a low power state. When

KSZ8864CNX/RMNUB is in low power state, it will keep monitoring the cable energy. Once energy is detected from the cable, KSZ8864CNX/RMNUB will enter normal power state. When KSZ8864CNX/RMNUB is at normal power state, it is able to transmit or receive packets from the cable.

3.2.3 SOFT POWER-DOWN MODE

The soft power-down mode is entered by setting bit [4:3] = 10 in Register 14. When KSZ8864CNX/RMNUB is in this mode, all PLL clocks are disabled, also all of the PHYs and the MACs are off. Any dummy host access will wake-up this device from its current soft power-down mode to normal operation mode and internal reset will be issued to make all internal registers go to the default values.

3.2.4 POWER SAVING MODE

The power saving mode is entered when auto-negotiation mode is enabled, the cable is disconnected, and by setting bit [4:3] =11 in Register 14. When KSZ8864CNX/RMNUB is in this mode, all PLL clocks are enabled, MAC is on, all internal register values will not change, and the host interface is ready for CPU read or write. This mode mainly controls the PHY transceiver on or off based on the line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable or an attempt by the far end to establish a link, the KSZ8864CNX/RMNUB can automatically enable the PHY to power up to its normal power state from power saving mode.

During this power saving mode, the host CPU can set bit [4:3] in Register 14 to transit the current power saving mode to any one of the other three power management operation modes.

3.2.5 PORT-BASED POWER-DOWN MODE

In addition, the KSZ8864CNX/RMNUB features a per-port power-down mode. To save power, a PHY port that is not in use can be powered down by the Registers Port Control 13 bit3, or MIIM PHY Registers 0 bit11.

3.3 Switch Core

3.3.1 ADDRESS LOOK-UP

The internal look-up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KSZ8864CNX/RMNUB is guaranteed to learn 1K addresses and distinguishes itself from a hash-based look-up table that, depending upon the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.3.2 LEARNING

The internal look-up engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted first to make room for the new entry.

3.3.3 MIGRATION

The internal look-up engine also monitors whether a station is moved. If this occurs, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

3.3.4 AGING

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 ±75 seconds. This feature can be enabled or disabled through Register 3. See "Register 3" section for more information.

3.3.5 FORWARDING

The KSZ8864CNX/RMNUB will forward packets using an algorithm that is depicted in the following flowcharts. Figure 3-4 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by the spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 3-5. This is where the packet will be sent.

KSZ8864CNX/RMNUB will not forward the following packets:

- Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
- 802.3x pause frames. The KSZ8864CNX/RMNUB will intercept these packets and perform the appropriate actions.
- “Local” packets. Based on destination address (DA) look-up. If the destination port from the look-up table matches the port where the packet was from, the packet is defined as “local.”

3.3.6 SWITCHING ENGINE

The KSZ8864CNX/RMNUB features a high-performance switching engine to move data to and from the MACs, packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency. The KSZ8864CNX/RMNUB has a 64KB internal frame buffer. This resource is shared between all five ports. There are a total of 512 buffers available. Each buffer is sized at 128 bytes.

3.3.7 MEDIA ACCESS CONTROL (MAC) OPERATION

The KSZ8864CNX/RMNUB strictly abides by IEEE 802.3 standards to maximize compatibility.

3.3.8 INTER-PACKET GAP (IPG)

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

3.3.9 BACK-OFF ALGORITHM

The KSZ8864CNX/RMNUB implements the IEEE 802.3 binary exponential back-off algorithm and optional “aggressive mode” back-off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration in Register 3. See “Register 3” for additional information.

3.3.10 LATE COLLISION

If a transmit packet experiences collisions after 512-bit times of the transmission, the packet will be dropped.

3.3.11 ILLEGAL FRAMES

The KSZ8864CNX/RMNUB discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Register 4. For special applications, the KSZ8864CNX/RMNUB can also be programmed to accept frames up to 1916 bytes in Register 4. Because the KSZ8864CNX/RMNUB supports VLAN tags, the maximum sizing is adjusted when these tags are present.

3.3.12 FLOW CONTROL

The KSZ8864CNX/RMNUB supports IEEE 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8864CNX/RMNUB receives a pause control frame, the KSZ8864CNX/RMNUB will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KSZ8864CNX/RMNUB will be transmitted.

On the transmit side, the KSZ8864CNX/RMNUB has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on the availability of system resources, including available buffers, available transmit queues, and available receive queues.

The KSZ8864CNX/RMNUB flow controls a port that has just received a packet if the destination port resource is busy. The KSZ8864CNX/RMNUB issues a flow control frame (XOFF), containing the maximum pause time defined in IEEE 802.3x. Once the resource is freed up, the KSZ8864CNX/RMNUB sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is also provided to prevent over-activation and deactivation of the flow control mechanism.

The KSZ8864CNX/RMNUB flow controls all ports if the receive queue becomes full.

FIGURE 3-4: DESTINATION ADDRESS LOOK-UP FLOW CHART - STAGE 1

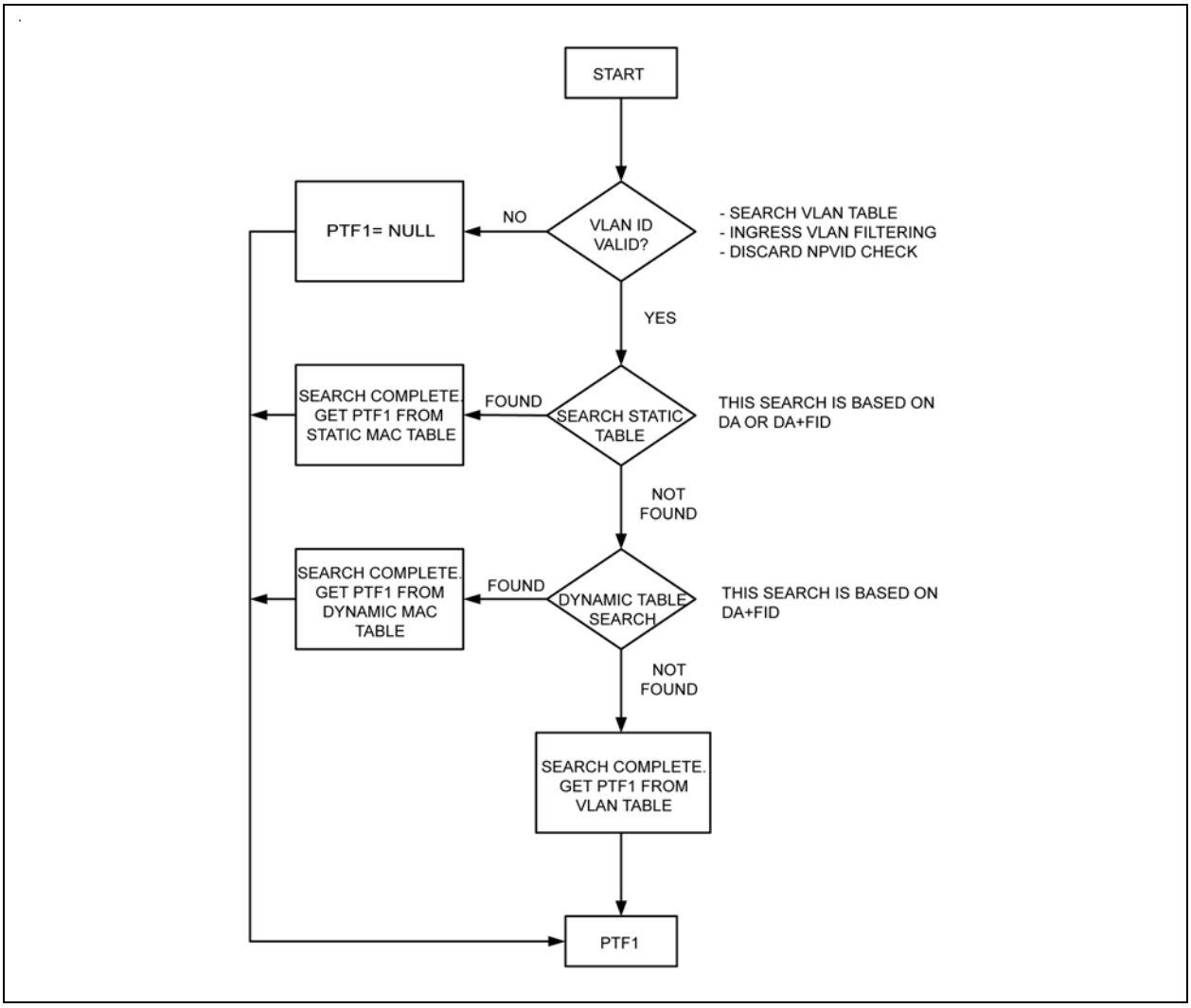
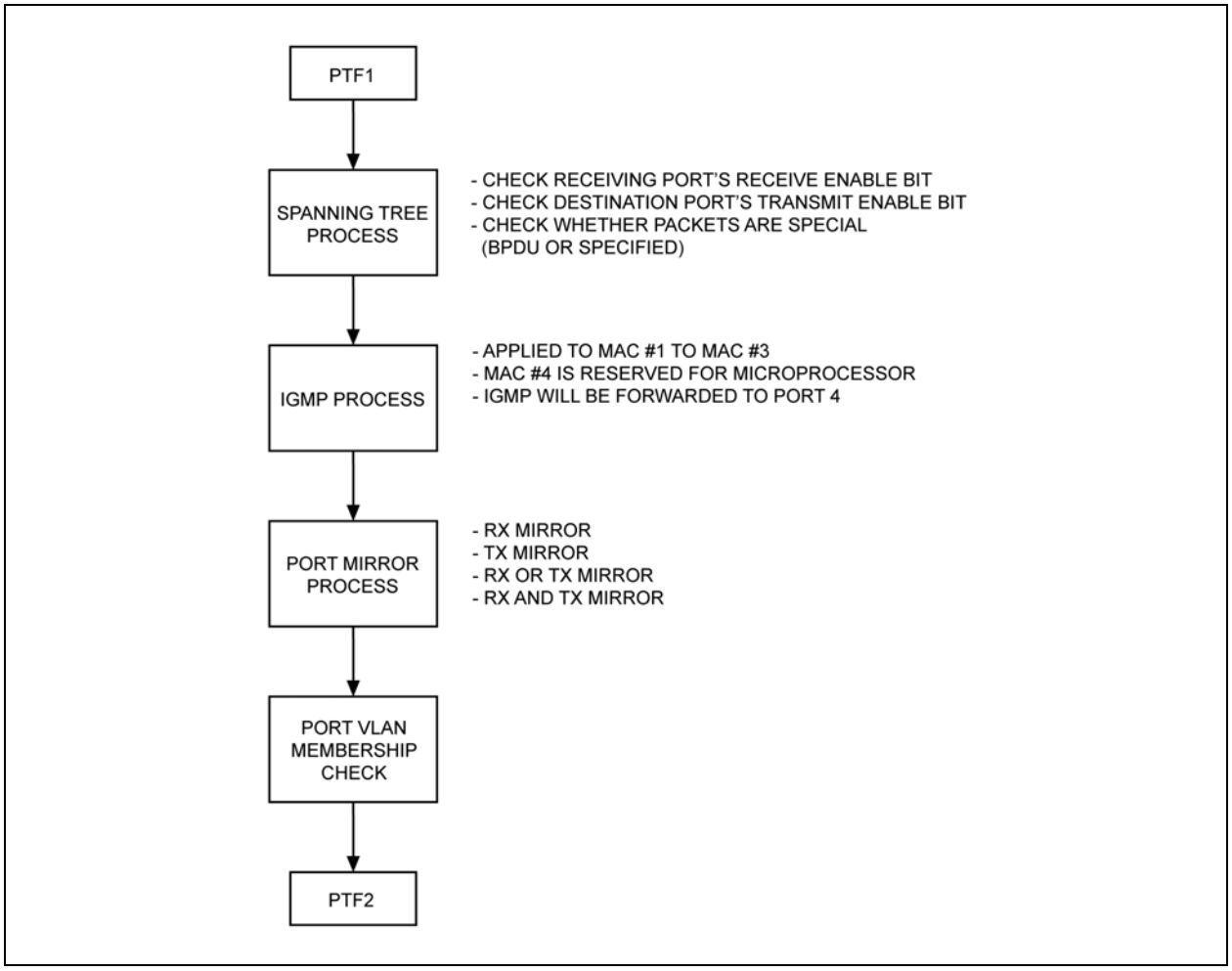


FIGURE 3-5: DESTINATION ADDRESS RESOLUTION FLOW CHART - STAGE 2



The KSZ8864CNX/RMNUB will not forward the following packets:

- Error packets. These include framing errors, frame check sequence (FCS) errors, alignment errors, and illegal size packet errors.
- IEEE 802.3x PAUSE frames. KSZ8864CNX/RMNUB intercepts these packets and performs full-duplex flow control accordingly.
- “Local” packets. Based on destination address (DA) look-up, if the destination port from the look-up table matches the port from which the packet originated, the packet is defined as local.

3.3.13 HALF-DUPLEX BACK PRESSURE

The KSZ8864CNX/RMNUB also provides a half-duplex back pressure option (note: this is not listed in IEEE 802.3 standards). The activation and deactivation conditions are the same as the ones given for full-duplex mode. If back pressure is required, the KSZ8864CNX/RMNUB sends preambles to defer the other station's transmission (carrier sense deference). To avoid jabber and excessive deference as defined in IEEE 802.3 standard, after a certain period of time, the KSZ8864CNX/RMNUB discontinues carrier sense but raises it quickly after it drops packets to inhibit other transmissions. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in a carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier-sense-type back pressure is interrupted and those packets are transmitted instead. If there are no more packets to send, carrier-sense-type back pressure becomes active again until switch resources are free. If a collision occurs, the binary exponential backoff algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets. To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive backoff (Register 3, bit 0)
- No excessive collision drop (Register 4, bit 3)
- Back pressure (Register 4, bit 5

These bits are not set as the default because they are not the IEEE standard.

3.3.14 BROADCAST STORM PROTECTION

The KSZ8864CNX/RMNUB has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets are normally forwarded to all ports except the source port and thus use too many switch resources (bandwidth and available space in transmit queues). The KSZ8864CNX/RMNUB has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally and can be enabled or disabled on a per port basis. The rate is based on a 50 ms (0.05s) interval for 100BT and a 500 ms (0.5s) interval for 10BT. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Global Registers 6 and 7. The default setting for Global Registers 6 and 7 is 0x4A (74 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec × 50 ms (0.05s)/interval × 1% = 74 frames/interval (approx.) = 0x4A.

3.3.15 MII INTERFACE OPERATION

The media independent interface (MII) is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. The KSZ8864CNX/RMNUB provides two MAC layer interfaces for MAC 3 and MAC 4. Each of these MII/RMII interfaces contains two distinct groups of signals, one for transmission and the other for receiving.

3.3.16 SWITCH MAC3/MAC4 SW3/SW4-MII INTERFACE

Table 3-3 shows two connection manners. The first is an external MAC connects to SW3/SW4-MII PHY mode. The second is an external PHY connects to SW3/SW4-MII MAC mode.

Please see the pins [47, 48] description for detail configuration for the MAC mode and PHY mode of the port 4 MAC4 SW4-MII, the default is SW4-MII with PHY mode. Please see the strap pin P2LED0 and the Register 223 bit 6 for the MAC mode and PHY mode of the port 3 MAC3 SW3-MII, the default is SW3-MII with PHY mode also.

TABLE 3-3: SWITCH MAC3 SW3-MII AND MAC4 SW4-MII SIGNALS

KSZ8864CNX/RMNUB PHY Mode Connections			Description	KSZ8864CNX/RMNUB MAC Mode Connections		
External MAC	SW3/4-MII Signal (Note 3-1)	Type		External PHY	SW3/4-MII Signal (Note 3-1)	Type
MTXEN	SMxTXEN	Input	Transmit Enable	MTXEN	SMxRXDV	Output
MTXD3	SMxTXD[3]	Input	Transmit Data Bit 3	MTXD3	SMxRXD[3]	Output
MTXD2	SMxTXD[2]	Input	Transmit Data Bit 2	MTXD2	SMxRXD[2]	Output
MTXD1	SMxTXD[1]	Input	Transmit Data Bit 1	MTXD1	SMxRXD[1]	Output
MTXD0	SMxTXD[0]	Input	Transmit Data Bit 0	MTXD0	SMxRXD[0]	Output
MTXC	SMxTXC	Output	Transmit Clock	MTXC	SMxRXC	Input
MCOL	SMxCOL	Output	Collision Detection	MCOL	SMxCOL	Input
MCRS	SMxCRS	Output	Carrier Sense	MCRS	SMxCRS	Input
MRXDV	SMxRXDV	Output	Receive Data Valid	MRXDV	SMxTXEN	Input
MRXD3	SMxRXD[3]	Output	Receive Data Bit 3	MRXD3	SMxTXD[3]	Input
MRXD2	SMxRXD[2]	Output	Receive Data Bit 2	MRXD2	SMxTXD[2]	Input
MRXD1	SMxRXD[1]	Output	Receive Data Bit 1	MRXD1	SMxTXD[1]	Input
MRXD0	SMxRXD[0]	Output	Receive Data Bit 0	MRXD0	SMxTXD[0]	Input
MRXC	SMxRXC	Output	Receive Clock	MRXC	SMxTXC	Input

Note 3-1 “x” represents “3” or “4” for SW3 or SW4 in the table.