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KSZ8873MML

Integrated 3-Port 10/100 Managed Switch with PHY

Features

- **Advanced Switch Features**
  - IEEE 802.1q VLAN Support for Up to 16 Groups (Full Range of VLAN IDs)
  - VLAN ID Tag/Untag Options, Per Port Basis
  - IEEE 802.1p/q Tag Insertion or Removal on a Per Port Basis (Egress)
  - Programmable Rate Limiting at the Ingress and Egress on a Per Port Basis
  - Broadcast Storm Protection with Percent Control (Global and Per Port Basis)
  - IEEE 802.1d Rapid Spanning Tree Protocol Support
  - Tail Tag Mode (1 byte Added before FCS) Support at Port 3 to Inform the Processor which Ingress Port Receives the Packets
  - Bypass Feature that Automatically Sustains the Switch Function between Port 1 and Port 2 when CPU (Port 3 Interface) Goes into Sleep Mode
  - Self-Address Filtering Support
  - Individual MAC Address for Port 1 and Port 2
  - IGMP Snooping (IPv4) Support for Multicast Packet Filtering
  - IPv4/IPv6 QoS Support
  - MAC Filtering Function to Forward Unknown Unicast Packets to Specified Port
- **Comprehensive Configuration Register Access**
  - Serial Management Interface (SMI) to All Internal Registers
  - MII Management (MIIM) Interface to PHY Registers
  - High Speed SPI and I^2C Interface to All Internal Registers
  - I/O Pins Strapping and EEPROM to Program Selective Registers in Unmanaged Switch Mode
  - Control Registers Configurable on the Fly (Port-Priority, 802.1p/d/q, AN…)
- **QoS/CoS Packet Prioritization Support**
  - Per Port, 802.1p and DiffServ-Based
  - Re-Mapping of 802.1p Priority Field Per Port Basis, Four Priority Levels
- **Proven Integrated 3-Port 10/100 Ethernet Switch**
  - 3rd Generation Switch with Three MACs and One PHY Fully Compliant with IEEE 802.3u Standard
  - Non-Blocking Switch Fabric Ensures Fast Packet Delivery by Utilizing a 1k MAC Address Lookup Table and a Store-and-Forward Architecture
  - Full-Duplex IEEE 802.3x Flow Control (PAUSE) with Force Mode Option
  - Half-Duplex Back Pressure Flow Control
  - HP Auto MDI-X for Reliable Detection of and Correction for Straight-Through and Crossover Cables with Disable and Enable Option
  - MAC MII Interface Supports both MAC Mode and PHY Mode
  - LinkMD® TDR-Based Cable Diagnostics Permit Identification of Faulty Copper Cabling
  - Comprehensive LED Indicator Support for Link, Activity, Full-/Half-Duplex, and 10/100 Speed
  - HBM ESD Rating 3 kV
- **Switch Monitoring Features**
  - Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port or MII
  - MIB Counters for Fully Compliant Statistics Gathering, 34 MIB Counters Per Port
  - Loopback Modes for Remote Diagnostic of Failure
- **Low Power Dissipation**
  - Full-Chip Software Power-Down (Register Configuration Not Saved)
  - Full-Chip Hardware Power-Down (Register Configuration Not Saved)
  - Energy-Detect Mode Support
  - Dynamic Clock Tree Shutdown Feature
  - Per Port Based Software Power-Save on PHY (Idle Link Detection, Register Configuration Preserved)
  - Voltages: Single 3.3V Supply with Internal 1.8V LDO for 3.3V VDDIO
  - Optional 3.3V, 2.5V, and 1.8V for VDDIO
  - Transceiver Power 3.3V for VDDA_3.3
- **Industrial Temperature Range: –40°C to +85°C**
- **Available in a 64-Pin LQFP, Lead-Free Package**

Applications

- VoIP Phone
- Set-Top/Game Box
- Automotive Ethernet
- Industrial Control
- IPTV POF
- SOHO Residential Gateway
- Broadband Gateway/Firewall/VPN
- Integrated DSL/Cable Modem
- Wireless LAN Access Point + Gateway
- Standalone 10/100 Switch

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8873MML is a highly integrated 3-port switch on a chip IC in the industry's smallest footprint. It is designed to enable a new generation of low-port-count, cost-sensitive, and power efficient 10/100 Mbps switch systems. Low power consumption, advanced power management, and sophisticated QoS features (e.g., IPv6 priority classification support) make this device ideal for IPTV, IP-STB, VoIP, automotive, and industrial applications.

The KSZ8873MML is designed to support the GREEN requirement in today's switch systems. Advanced power management schemes include hardware power down, software power down, per port power down, and energy detect mode that shuts downs the transceiver when a port is idle.

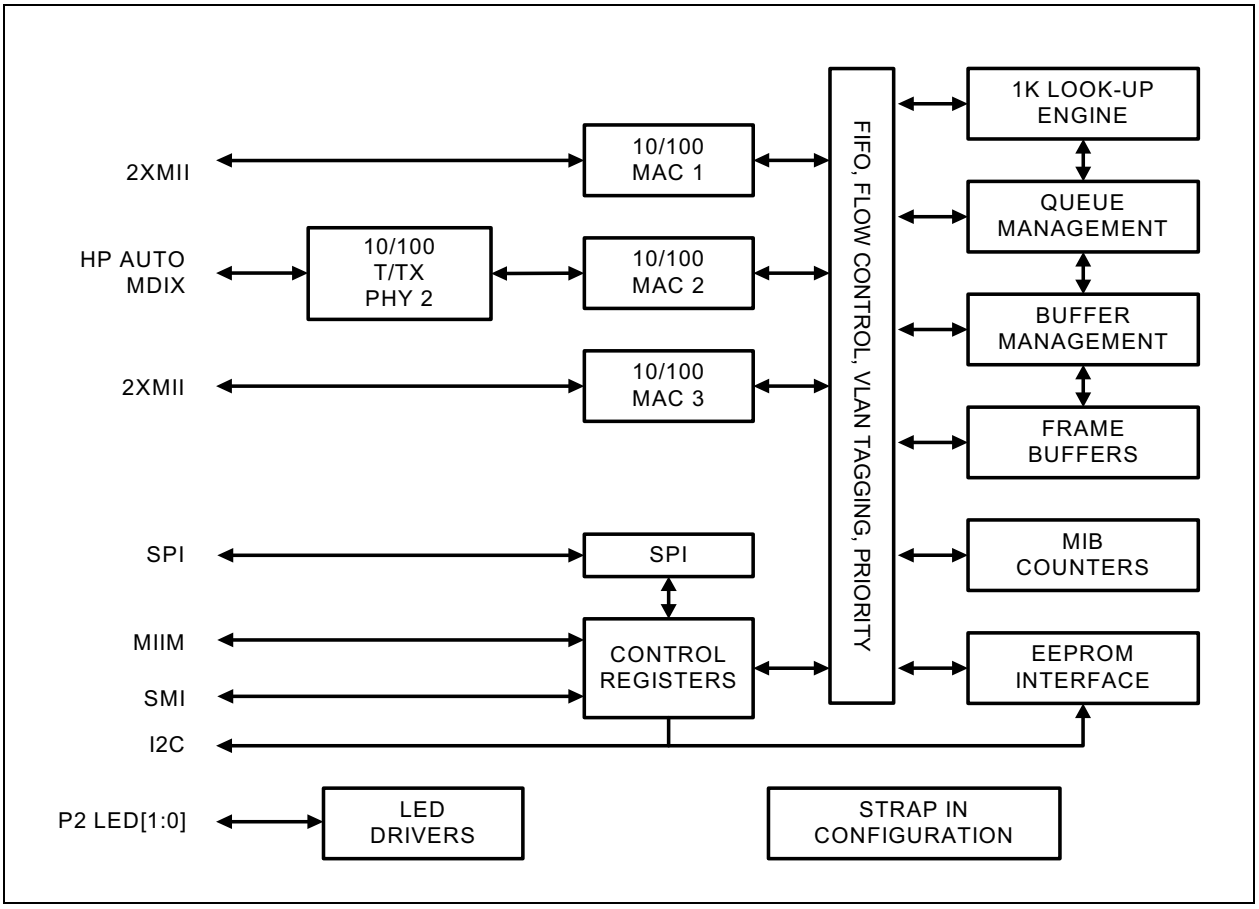
KSZ8873MML also offers a bypass mode that enables system-level power saving. In this mode, the processor connected to the switch through the MII interface can be shut down without impacting the normal switch operation.

The configuration provided by the KSZ8873MML enables the flexibility to meet requirements of different applications:

- KSZ8873MML: One 10/100BASE-T/TX transceiver and two MII interfaces.

The device is available in a RoHS-compliant 64-pin LQFP package. An industrial-grade temperature version is also available.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 64-PIN 10 MM X 10 MM LQFP ASSIGNMENT, (TOP VIEW)

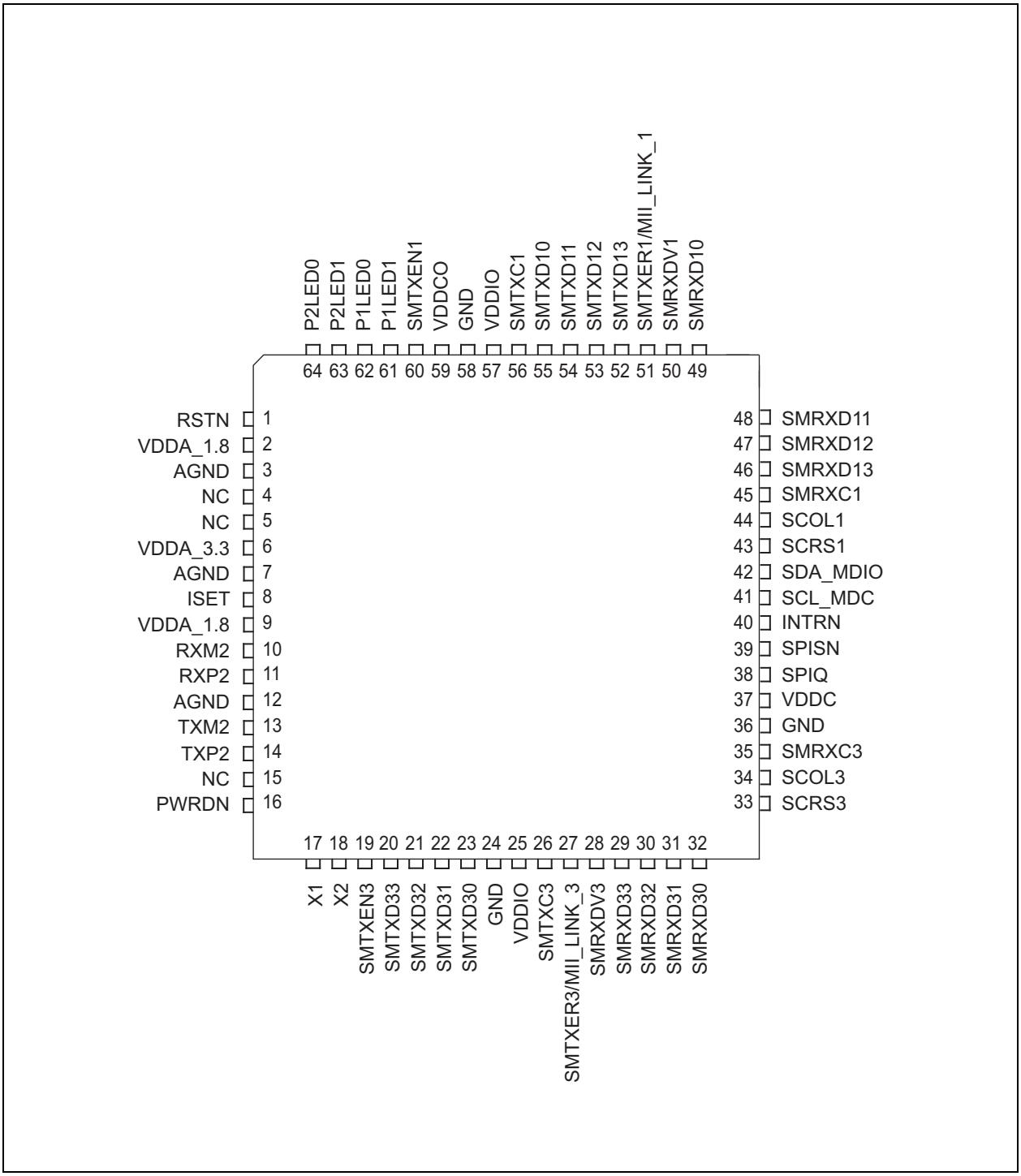


TABLE 2-1: SIGNALS

Pin Number	Pin Name	Type Note 2-1	Description
1	RSTN	IPU	Hardware reset pin (active low)
2	VDDA_1.8	P	1.8V analog core power input from VDDCO (pin 59)
3	AGND	GND	Analog ground
4	NC	NC	Unused pin. No external connection.
5	NC	NC	Unused pin. No external connection.
6	VDDA_3.3	P	3.3V analog V_{DD}
7	AGND	GND	Analog ground.
8	ISET	O	Set physical transmit output current. Pull-down this pin with an 11.8 kΩ 1% resistor to ground.
9	VDDA_1.8	P	1.8 analog V_{DD} input power supply from VDDCO (pin 59) through external Ferrite bead and capacitor.
10	RXM2	I/O	Physical receive or transmit signal (– differential)
11	RXP2	I/O	Physical receive or transmit signal (+ differential)
12	AGND	GND	Analog ground.
13	TXM2	I/O	Physical transmit or receive signal (– differential)
14	TXP2	I/O	Physical transmit or receive signal (+ differential)
15	NC	NC	No Connection
16	PWRDN	IPU	Chip power down input (active low).
17	X1	I	25 MHz or 50 MHz crystal/oscillator clock connections. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is ±50 ppm for both crystal and oscillator, the clock should be applied to X1 pin before reset voltage goes high.
18	X2	O	
19	SMTXEN3	IPU	Switch MII transmit enable
20	SMTXD33	IPU	Switch MII transmit data bit 3
21	SMTXD32	IPU	Switch MII transmit data bit 2
22	SMTXD31	IPU	Switch MII transmit data bit 1
23	SMTXD30	IPU	Switch MII transmit data bit 0
24	GND	GND	Digital ground
25	VDDIO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power supply for IO with well decoupling capacitors.
26	SMTXC3	I/O	Switch MII transmit clock (MII modes only) Output in PHY MII mode Input in MAC MII.

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
27	SMTXER3/ MII_LINK_3	IPU	Switch port 3 MII transmit error in MII mode 0 = MII link indicator from host in MII PHY mode. 1 = No link on port 3 MII PHY mode and enable Bypass mode.
28	SMRXDV3	IPU/O	Switch MII receive data valid Strap option: MII mode selection for port 3 PU = PHY mode. PD = MAC mode (In MAC mode, port 3 MII has to connect to a powered active external PHY for the normal operation)
29	SMRXD33	IPU/O	Switch MII receive data bit 3 Strap option: enable auto-negotiation on port 2 (P2ANEN) PU = Enable PD = Disable
30	SMRXD32	IPU/O	Switch MII receive data bit 2 Strap option: Force the speed on port 2 (P2SPD) PU = Force port 2 to 100BT if P2ANEN = 0 PD = Force port 2 to 10BT if P2ANEN = 0
31	SMRXD31	IPU/O	Switch MII receive data bit 1 Strap option: Force duplex mode (P2DPX) PU = Port 2 default to full-duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in full-duplex mode if P2ANEN = 0. PD = Port 2 set to half-duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in half-duplex mode if P2ANEN = 0.
32	SMRXD30	IPU/O	Switch MII receive data bit 0 Strap option: Force flow control on port 2 (P2FFC) PU = Always enable (force) port 2 flow control feature. PD = Port 2 flow control feature enable is determined by auto-negotiation result.
33	SCRS3	IPU/O	Switch MII carrier sense
34	SCOL3	IPU/O	Switch MII collision detect
35	SMRXC3	I/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
36	GND	GND	Digital ground
37	VDDC	P	1.8V digital core power input from VDDCO (pin 59).
38	SPIQ	IPU/O	SPI slave mode: serial data output Note: an external pull-up is needed on this pin when it is in use.
39	SPISN	IPU	SPI slave mode: chip select (active low) When SPISN is high, the KSZ8873MML is deselected and SPIQ is held in high impedance state. A high-to-low transition is used to initiate SPI data transfer. Note: An external pull-up is needed on this pin when it is in use.
40	INTRN	OPU	Interrupt Active Low signal to host CPU to indicate an interrupt status bit is set. Refer to register 187 and 188.

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
41	SCL_MDC	I/O	SPI slave mode/I^{2}C slave mode: Clock input I^{2}C master mode: Clock output MIIM: Clock input
42	SDA_MDIO	IPU/O	SPI slave mode: serial data input I^{2}C master/slave mode: Serial data input/output MIM: Data input/out Note: An external pull-up is needed on this pin when it is in use.
43	SCRS1	I/O	Switch MII carrier sense
44	SCOL1	I/O	Switch MII collision detect
45	SMRXC1	I/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
46	SMRXD13	IPU/O	Switch MII receive data bit 3 Strap option: MII mode selection for port 1 PU = PHY mode. PD = MAC mode (In MAC mode, port 1 MII has to connect to an powered active external PHY for the normal operation)
47	SMRXD12	IPU/O	Switch MII receive data bit 2 Strap option: Force the speed on port 1 (P1SPD) PU = Force port 1 to 100BT PD = Force port 1 to 10BT
48	SMRXD11	IPU/O	Switch MII receive data bit 1 Strap option: Force duplex mode on port 1 (P1DPX) PU = Port 1 default to full-duplex mode. PD = Port 1 set to half-duplex mode.
49	SMRXD10	IPU/O	Switch MII receive data bit 0 Strap option: Force flow control on port 1 (P1FFC) PU = Always enable (force) port 1 flow control feature. PD = Disable.
50	SMRXDV1	IPD/O	Switch MII receive data valid Strap option: Force the speed on port 3 (P3SPD) PU = Force port 3 to 10BT PD = Force port 3 to 100BT
51	SMTXER1/ MII_LINK_1	IPD	Switch port 1 MII transmit error in MII mode 0 = MII link indicator from host in MII PHY mode. 1 = No link on port 1 MII PHY mode and enable Bypass mode.
52	SMTXD13	I	Switch MII transmit data bit 3
53	SMTXD12	I	Switch MII transmit data bit 2
54	SMTXD11	I	Switch MII transmit data bit 1
55	SMTXD10	I	Switch MII transmit data bit 0

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td>56</td><td>SMTXC1</td><td>I/O</td><td>Switch MII transmit clock (MII modes only)
Output in PHY MII mode
Input in MAC MII.</td></tr>
<tr><td>57</td><td>VDDIO</td><td>P</td><td>3.3V, 2.5V, or 1.8V digital V_{DD} input power supply for IO with well decoupling capacitors.</td></tr>
<tr><td>58</td><td>GND</td><td>GND</td><td>Digital ground</td></tr>
<tr><td>59</td><td>VDDCO</td><td>P</td><td>1.8V core power voltage output (internal 1.8V LDO regulator output), this 1.8V output pin provides power to both VDDA_1.8 and VDDC input pins.
Note: Internally 1.8V LDO regulator input comes from VDDIO. Do not connect an external power supply to VDDCO pin. The ferrite bead is requested between analog and digital 1.8V core power.</td></tr>
<tr><td>60</td><td>SMTXEN1</td><td>I</td><td>Switch MII transmit enable</td></tr>
<tr><td>61</td><td>P1LED1</td><td>IPU/O</td><td>Port 1 LED Indicators: (Not used)
Strap option: Port 3 flow control selection(P3FFC)
PU = Always enable (force) port 3 flow control feature
PD = Disable</td></tr>
<tr><td>62</td><td>P1LED0</td><td>IPD/O</td><td>Port 1 LED Indicators: (Not used)
Strap option: Port 3 duplex mode selection(P3DPX)
PU = Port 3 set to half-duplex mode
PD = Port 3 set to full-duplex mode (default)</td></tr>
<tr><td>63</td><td>P2LED1</td><td>IPU/O</td><td>Port 2 LED Indicators:
Default: Speed (refer to register 195 bit[5:4])
Strap option: Serial bus configuration
Port 2 LED Indicators:
Default: Link/Act. (refer to register 195 bit[5:4])
Strap option: Serial bus configuration
Serial bus configuration pins to select mode of access to KSZ8873MML internal registers.
[P2LED1, P2LED0] = [0, 0] — I^2C master (EEPROM) mode
(If EEPROM is not detected, the KSZ8873MML will be configured with the default values of its internal registers and the values of its strap-in pins.)
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr>
<tr><td>SCL</td><td>O</td><td>I^2C clock</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I^2C data I/O</td></tr>
<tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr>
</table></td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td rowspan="12">64</td><td rowspan="12">P2LED0</td><td rowspan="12">IPU/O</td><td>[P2LED1, P2LED0] = [0, 1] — I²C slave mode
The external I²C master will drive the SCL clock.
The KSZ8873MML device addresses are:
1011_1111 <read>
1011_1110 <write></td></tr>
<tr><td>
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr>
<tr><td>SCL</td><td>I</td><td>I²C clock</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr>
<tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr>
</table>
</td></tr>
<tr><td>[P2LED1, P2LED0] = [1, 0] — SPI slave mode</td></tr>
<tr><td>
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr>
<tr><td>SCL</td><td>I</td><td>SPI clock</td></tr>
<tr><td>SDA</td><td>I</td><td>SPI data in</td></tr>
<tr><td>SPIS_N</td><td>I</td><td>SPI chip select</td></tr>
</table>
</td></tr>
<tr><td>[P2LED1, P2LED0] = [1, 1] – SMI/MIIM-mode
In SMI mode, the KSZ8873MML provides access to all its internal 8-bit registers through its SCL_MDC and SDA_MDIO pins.
In MIIM mode, the KSZ8873MML provides access to its 16-bit MIIM registers through its SDC_MDC and SDA_MDIO pins.</td></tr>
</table>

Note 2-1 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu/O = Input with internal pull-up during reset; output pin otherwise.
Ipu = Input with internal pull-up.
Ipd = Input with internal pull-down.
Opu = Output with internal pull-up.
Opd = Output with internal pull-down.
Speed: Low (100BASE-TX), High (10BASE-T)
Full-Duplex: Low (full-duplex), High (half-duplex)
Activity: Toggle (transmit/receive activity)
Link: Low (link), High (no link)

3.0 FUNCTIONAL DESCRIPTION

The KSZ8873MML contains one 10/100 physical layer transceivers and three MAC units with an integrated Layer 2 managed switch.

The KSZ8873MML has the flexibility to reside in either a managed or unmanaged design. In a managed design, the host processor has complete control of the KSZ8873MML via the SMI interface, MIIM interface, SPI bus, or I^2C bus. An unmanaged design is achieved through I/O strapping and/or EEPROM programming at system reset time.

On the media side, the KSZ8873MML supports IEEE 802.3 10BASE-T and 100BASE-TX on both PHY ports. Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

3.1 Physical Layer Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 11.8 kΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.1.3 PLL CLOCK SYNTHESIZER

The KSZ8873MML generates 125 MHz, 62.5 MHz, and 31.25 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz or 50 MHz crystal or oscillator.

3.1.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.1.5 10BASE-T TRANSMIT

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.6 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8873MML decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.7 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8873MML supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8873MML device. This feature is extremely useful when end users are unaware of cable types and also saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers or MIIM PHY registers.

The IEEE 802.3u standard MDI and MDI-X definitions are illustrated in Table 3-1.

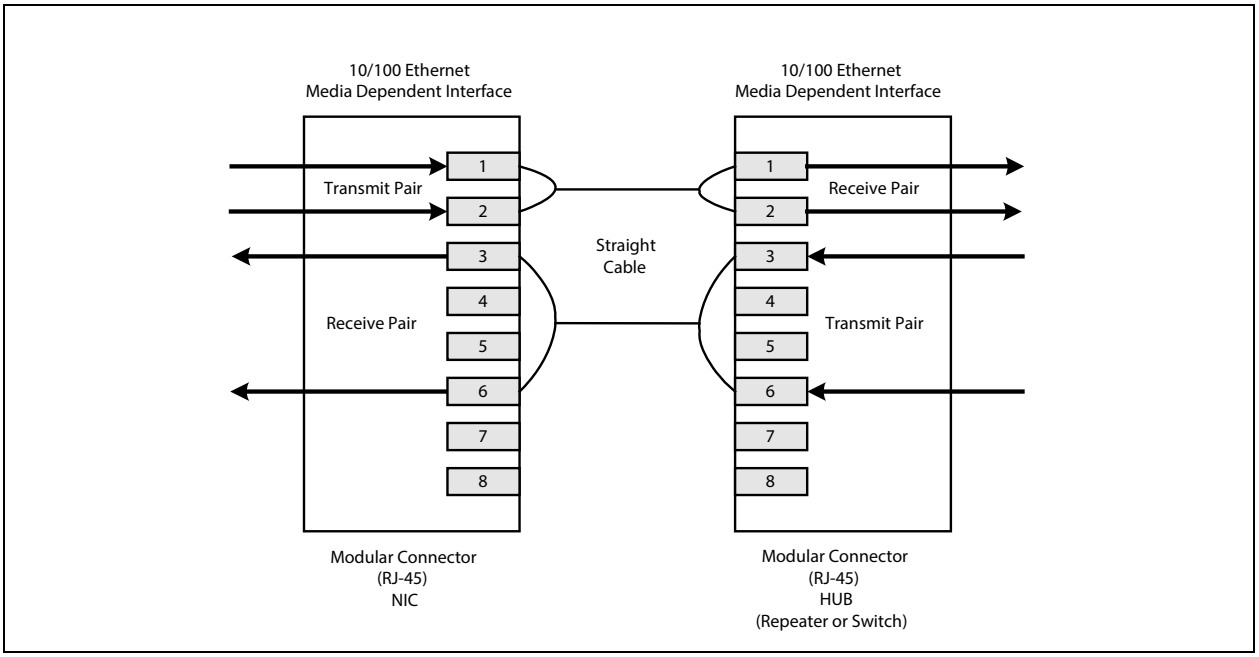
TABLE 3-1: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.1.7.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a NIC card (MDI) and a switch or hub (MDI-X).

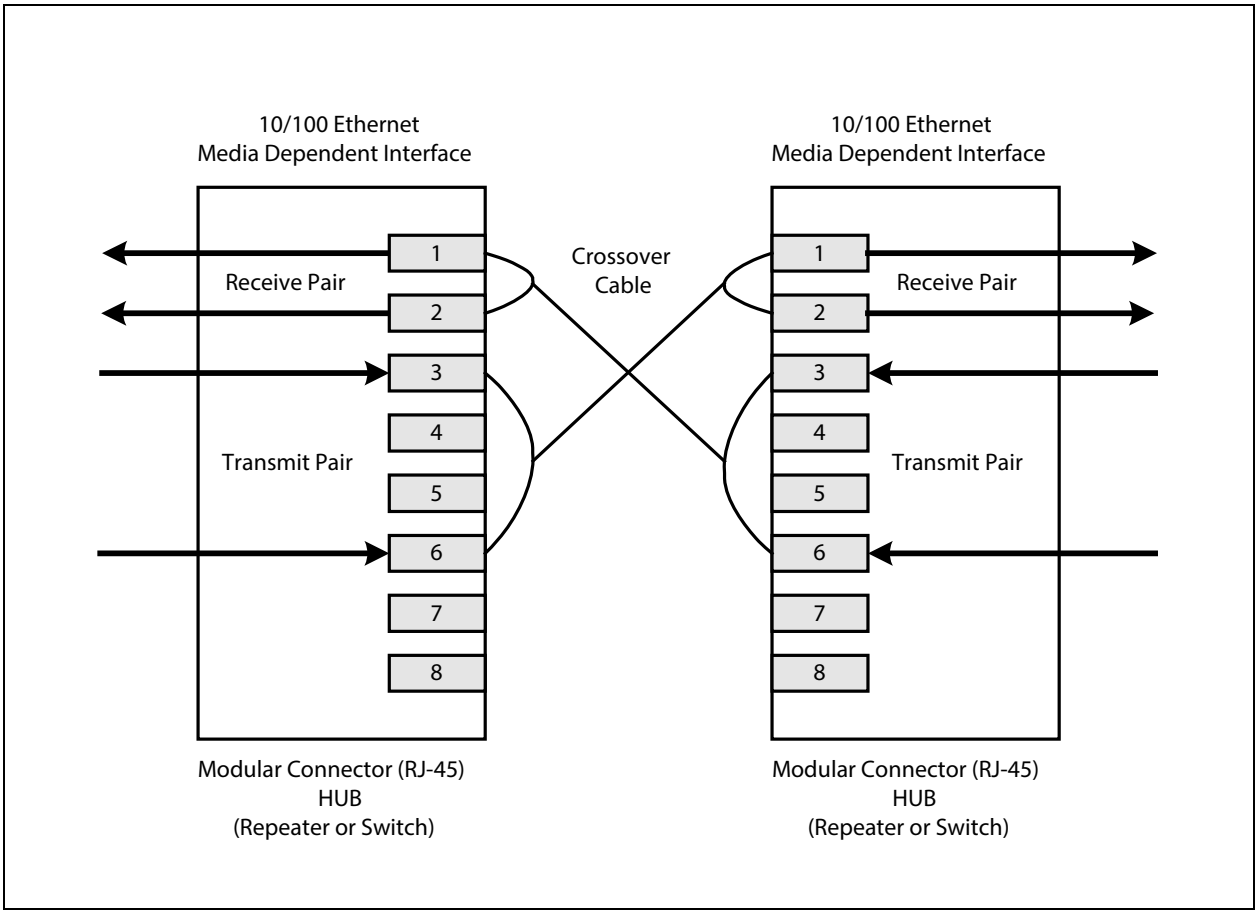
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.1.7.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



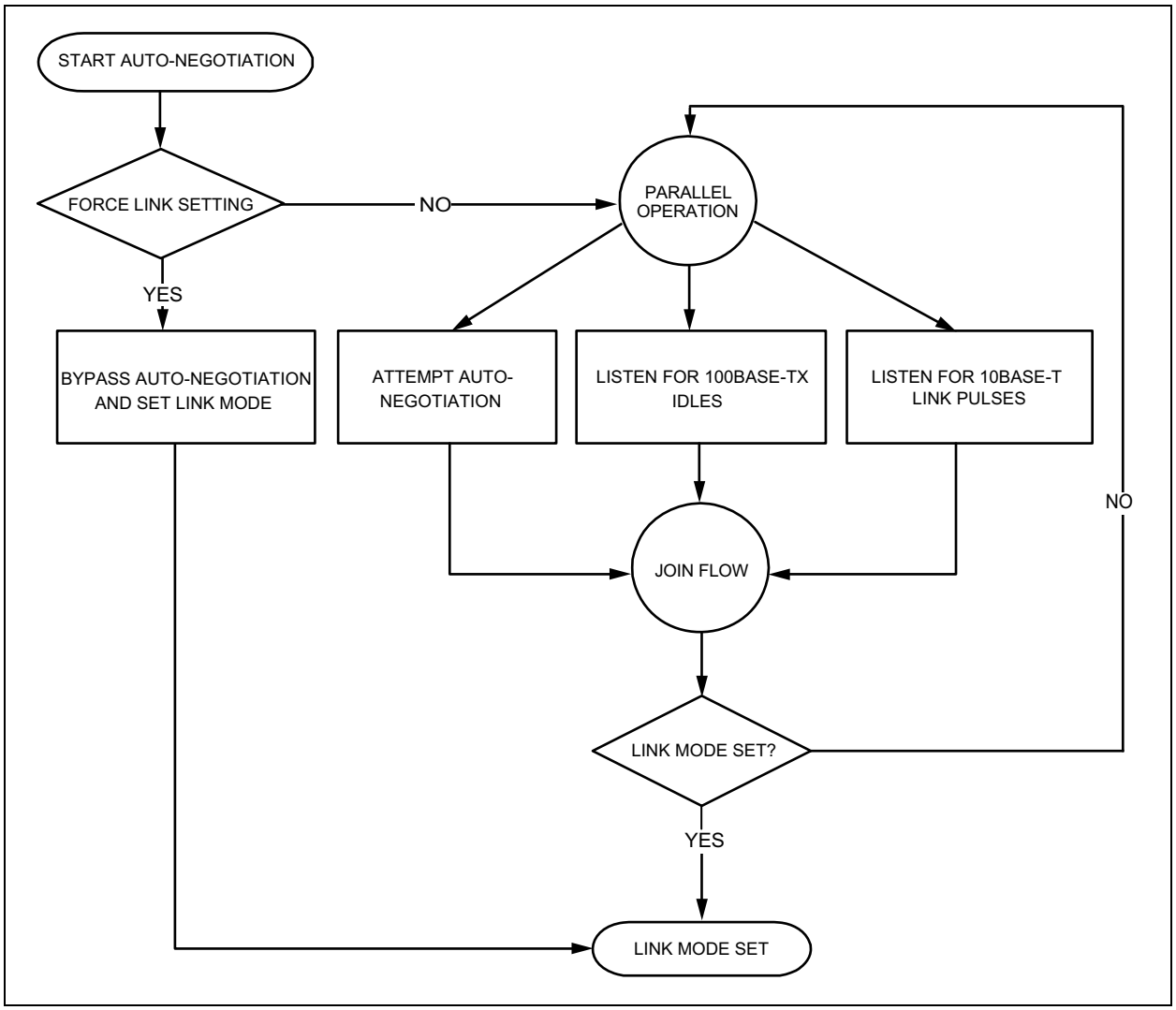
3.1.8 AUTO-NEGOTIATION

The KSZ8873MML conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation, link partners advertise their capabilities across the link to each other. If auto-negotiation is not supported or the KSZ8873MML link partner is forced to bypass auto-negotiation, the KSZ8873MML sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8873MML to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The link up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.1.9 LINKMD® CABLE DIAGNOSTICS

Port 2 of KSZ8873MML supports LinkMD®. The LinkMD® feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD® works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault. Internal circuitry displays the TDR information in a user-readable digital format.

3.1.9.1 Access

LinkMD® is initiated by accessing registers {42, 43}, the LinkMD® Control/Status registers for port 2, and in conjunction with registers 45, Port Control Register 13.

Alternatively, the MIIM PHY registers 0 and 29 can be used for LinkMD® access.

3.1.9.2 Usage

The following is a sample procedure for using LinkMD with registers {42,43,45} on port 2.

1. Disable auto MDI/MDI-X by writing a '1' to register 45, bit [2] to enable manual control over the differential pair used to transmit the LinkMD pulse.
2. Start cable diagnostic test by writing a '1' to register 42, bit [4]. This enable bit is self-clearing.
3. Wait (poll) for register 42, bit [4] to return a '0', indicating cable diagnostic test is complete.
4. Read cable diagnostic test results in register 42, bits [6:5]. The results are as follows:

   00 = normal condition (valid test)

   01 = open condition detected in cable (valid test)

   10 = short condition detected in cable (valid test)

   11 = cable diagnostic test failed (invalid test)

The '11' case, invalid test, occurs when the KSZ8873MML is unable to shut down the link partner. In this instance, the test is not run, because it would be impossible for the KSZ8873MML to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating register 42, bit [0] and register 43, bits [7:0]; and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

EQUATION 3-1:

$$D(Distance\ to\ cable\ fault\ in\ meters) = 0.4 \times (Register\ 26\ bit\ [0] \times Register\ 27\ bits\ [7:0])$$

Concatenated values of registers 42 and 43 are converted to decimal before multiplying by 0.4.

The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.2 Power Management

The KSZ8873MML supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are five operation modes under the power management function which is controlled by two bits in Register 195 (0xC3) and one bit in Register 29 (0x1D), 45(0x2D) as shown below:

Register 195 bit[1:0] = 00 Normal Operation Mode

Register 195 bit[1:0] = 01 Energy Detect Mode

Register 195 bit[1:0] = 10 Soft Power Down Mode

Register 195 bit[1:0] = 11 Power Saving Mode

Register 29, 45 bit 3 = 1 Port Based Power Down Mode

Table 3-2 indicates all internal function blocks status under four different power management operation modes.

TABLE 3-2: INTERNAL FUNCTION BLOCK STATUS

KSZ8873MML Function Blocks	Power Management Operation Modes			
	Normal Mode	Power Saving Mode	Energy Detect Mode	Soft Power Down Mode
Internal PLL Clock	Enabled	Enabled	Disabled	Disabled
Tx/Rx PHY	Enabled	Rx unused block disabled	Energy detect at Rx	Disabled
MAC	Enabled	Enabled	Disabled	Disabled
Host Interface	Enabled	Enabled	Disabled	Disabled

3.2.1 NORMAL OPERATION MODE

This is the default setting bit[1:0] = 00 in register 195 after the chip power-up or hardware reset. When KSZ8873MML is in this normal operation mode, all PLL clocks are running, PHY and MAC are on, and the host interface is ready for CPU read or write.

During the normal operation mode, the host CPU can set the bit[1:0] in register 195 to transit the current normal operation mode to any one of the other three power management operation modes.

3.2.2 POWER SAVING MODE

The power saving mode is entered when auto-negotiation mode is enabled, cable is disconnected, and by setting bit[1:0] = 11 in register 195. When KSZ8873MML is in this mode, all PLL clocks are enabled, MAC is on, all internal registers value will not change, and host interface is ready for CPU read or write. In this mode, it mainly controls the PHY transceiver on or off based on line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8873MML can automatically enabled the PHY power up to normal power state from power saving mode.

During this power saving mode, the host CPU can set bit[1:0] = 0 in register 195 to transit the current power saving mode to any one of the other three power management operation modes.

3.2.3 ENERGY DETECT MODE

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8873MML is not connected to an active link partner. In this mode, the device will save up to 87% of the power. If the cable is not plugged, the KSZ8873MML can automatically enter to a low power state, a.k.a., the energy detect mode. In this mode, KSZ8873MML will keep transmitting 120 ns width pulses at a rate of one pulse per second. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8873MML can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8873MML reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit[1:0] = 01 in register 195. When the KSZ8873MML is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than pre-configured value at bit[7:0] Go-Sleep time in register 196, KSZ8873MML will go into a low power state. When KSZ8873MML is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable, KSZ8873MML will enter normal power state. When KSZ8873MML is at normal power state, it is able to transmit or receive packet from the cable.

It will save about 87% of the power when MII interface is in PHY mode, pin SMTXER3/MII_LINK_3 or SMTXER1/MII_LINK_1 is connected to High, register 195 bit [1:0] = 01, bit 2 = 1(Disable PLL), not cables are connected.

3.2.4 SOFT POWER DOWN MODE

The soft power down mode is entered by setting bit[1:0] = 10 in register 195. When KSZ8873MML is in this mode, all PLL clocks are disabled, the PHY and the MAC are off, all internal registers value will not change. When the host set bit[1:0] = 00 in register 195, this device will be back from current soft power down mode to normal operation mode.

3.2.5 PORT-BASED POWER DOWN MODE

In addition, the KSZ8873MML features a per-port power down mode. To save power, a PHY port that is not in use can be powered down via port control register 45 bit 3, or MIIM PHY register. It will saves about 15 mA per port.

3.2.6 HARDWARE POWER DOWN

KSZ8873 supports a hardware power down mode. When the pin PWRDN is active-low, the entire chip is powered down.

3.3 MAC and Switch

3.3.1 ADDRESS LOOKUP

The internal lookup table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information.

The KSZ8873MML is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.3.2 LEARNING

The internal lookup engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the lookup table.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

3.3.3 MIGRATION

The internal lookup engine also monitors whether a station has moved. If a station has moved, it will update the table accordingly. Migration happens when the following conditions are met:

- The received packet’s SA is in the table, but the associated source port information is different.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine will update the existing record in the table with the new source port information.

3.3.4 AGING

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and will continuously remove aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through register 3 (0x03) bit [2].

3.3.5 FORWARDING

The KSZ8873MML forwards packets using the algorithm that is depicted in the following flowcharts. Figure 3-4 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 3-5. The packet is sent to PTF2.

FIGURE 3-4: DESTINATION ADDRESS LOOKUP FLOW CHART, STAGE 1

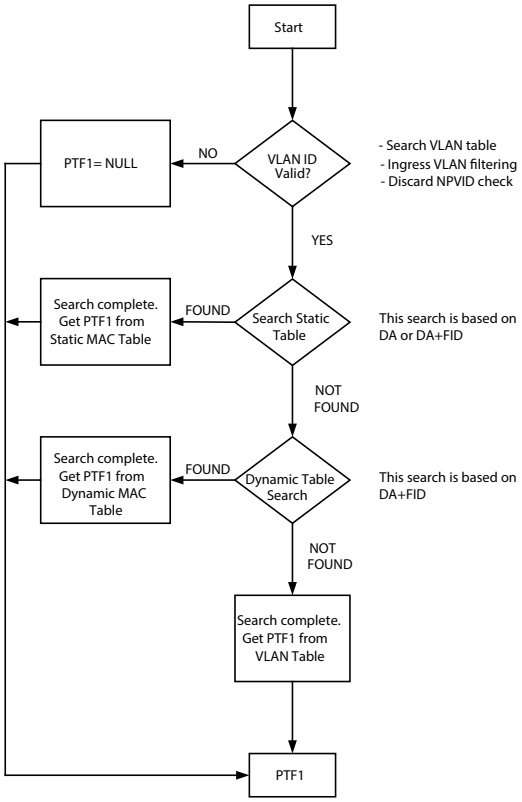
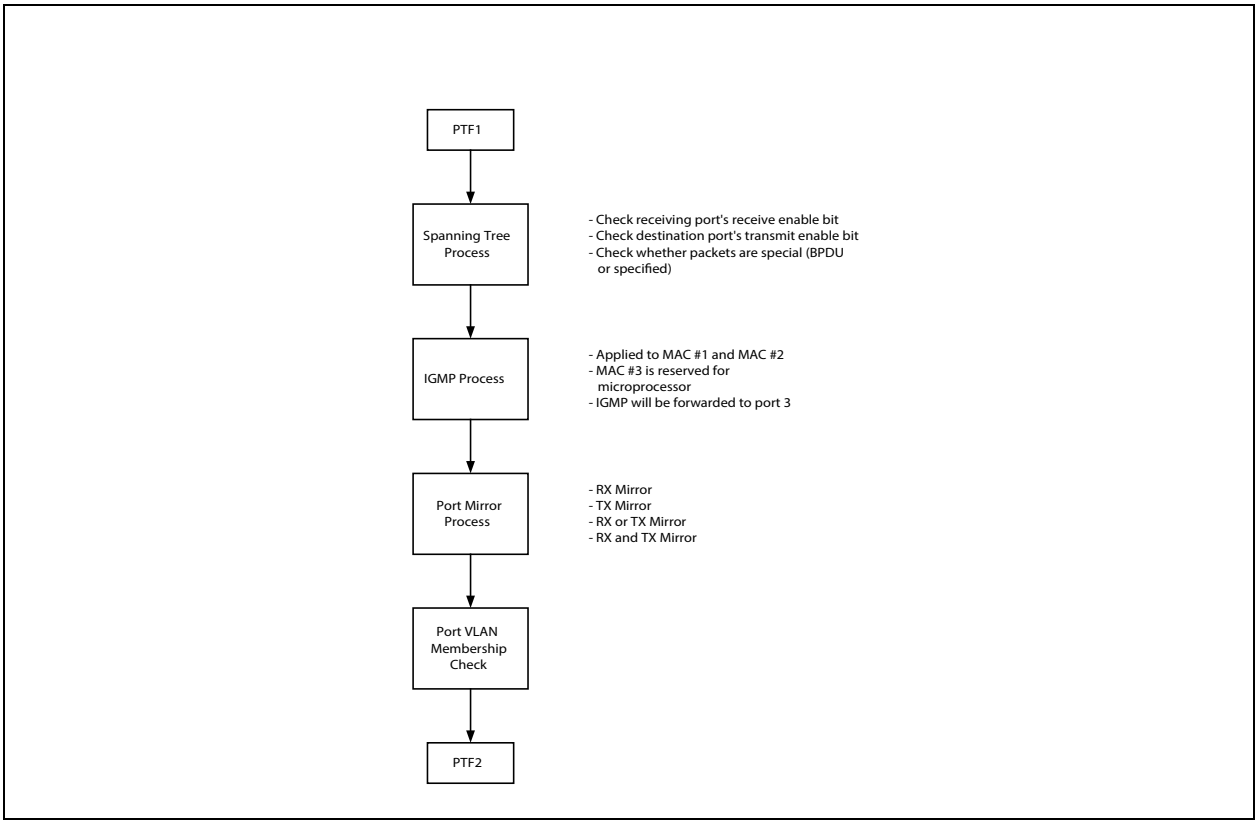


FIGURE 3-5: DESTINATION ADDRESS RESOLUTION FLOW CHART, STAGE 2



The KSZ8873MML will not forward the following packets:

1. Error packets: These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.
2. IEEE802.3x PAUSE frames: KSZ8873MML intercepts these packets and performs full-duplex flow control accordingly.
3. "Local" packets: Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as local.

3.3.6 SWITCHING ENGINE

The KSZ8873MML features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The switching engine has a 32 kB internal frame buffer. This buffer pool is shared between all three ports. There are a total of 256 buffers available. Each buffer is sized at 128 bytes.

3.3.7 MAC OPERATION

The KSZ8873MML strictly abides by IEEE 802.3 standards to maximize compatibility.

3.3.7.1 Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bits time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bits time IPG is measured from MCRS and the next MTXEN.

3.3.7.2 Back-Off Algorithm

The KSZ8873MML implements the IEEE 802.3 standard for the binary exponential back-off algorithm, and optional "aggressive mode" back-off. After 16 collisions, the packet is optionally dropped depending on the switch configuration for register 4 (0x04) bit [3].

3.3.7.3 Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

3.3.7.4 Illegal Frames

The KSZ8873MML discards frames less than 64 bytes and can be programmed to accept frames up to1518 bytes, 1536 bytes, or 1916 bytes. These maximum frame size settings are programmed in register 4 (0x04). Because the KSZ8873MML supports VLAN tags, the maximum sizing is adjusted when these tags are present.

3.3.7.5 Full-Duplex Flow Control

The KSZ8873MML supports standard IEEE 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8873MML receives a pause control frame, the KSZ8873MML will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8873MML are transmitted.

On the transmit side, the KSZ8873MML has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues, and available receive queues.

The KSZ8873MML will flow control a port that has just received a packet if the destination port resource is busy. The KSZ8873MML issues a flow control frame (XOFF), containing the maximum pause time defined by the IEEE 802.3x standard. Once the resource is freed up, the KSZ8873MML sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

The KSZ8873MML flow controls all ports if the receive queue becomes full.

3.3.7.6 Half-Duplex Backpressure

A half-duplex backpressure option (not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as full-duplex flow control. If backpressure is required, the KSZ8873MML sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8873MML discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collisions and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive back-off (register 3 (0x03), bit [0])
- No excessive collision drop (register 4 (0x04), bit [3])

Note that these bits are not set as defaults because this is not the IEEE standard.

3.3.7.7 Broadcast Storm Protection

The KSZ8873MML has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8873MML has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 67 ms interval for 100BT and a 500 ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in register 6 (0x06) and 7 (0x07). The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec × 67 ms/interval × 1% = 99 frames/interval (approx.) = 0x63

Note: 148,800 frames/sec is based on 64-byte block of packets in 100BASE-TX with 12 bytes of IPG and 8 bytes of preamble between two packets.

3.3.7.8 Port Individual MAC Address and Source Port Filtering

The KSZ8873MML provide individual MAC address for port 1 and port 2 respectively. They can be set at register 142-147 and 148-153. The packet will be filtered if its source address matches the MAC address of port 1 or port 2 when the register 21 and 37 bit 6 is set to 1 respectively. For example, the packet will be dropped after it completes the loop of a ring network.

Note that for KSZ8873MML, port 1 means port 1's MII and an external PHY here.

3.3.8 MII INTERFACE OPERATION

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3u Standard. It provides a common interface between physical layer and MAC layer devices. The MII provided by the KSZ8873MML is connected to device's first MAC as port 1 MII and third MAC as port 3 MII. The interface contains two distinct groups of signals: one for transmission and the other for reception. Table 3-3 describes the signals used by the MII bus.

TABLE 3-3: MII SIGNALS

PHY Mode Connections		Pin Description	MAC Mode Connections	
External MAC Controller Signals	**KSZ8873MML Port 1,3 PHY Signals**		**External PHY Signals**	**KSZ8873MML Port 1,3 MAC Signals**
MTXEN	SMTXEN	Transmit Enable	MTXEN	SMRXDV
MTXER	SMTXER	Transmit Error	MTXER	(NOT USED)
MTXD3	SMTXD3	Transmit Data Bit 3	MTXD3	SMRXD3
MTXD2	SMTXD2	Transmit Data Bit 2	MTXD2	SMRXD2
MTXD1	SMTXD1	Transmit Data Bit 1	MTXD1	SMRXD1
MTXD0	SMTXD0	Transmit Data Bit 0	MTXD0	SMRXD0
MTXC	SMTXC	Transmit Clock	MTXC	SMRXC
MCOL	SCOL	Collision Detection	MCOL	SCOL
MCRS	SCRS	Carrier Sense	MCRS	SCRS
MRXDV	SMRXDV	Receive Data Valid	MRXDV	SMTXEN
MRXER	(NOT USED)	Receive Error	MRXER	SMTXER
MRXD3	SMRXD3	Receive Data Bit 3	MRXD3	SMTXD3
MRXD2	SMRXD2	Receive Data Bit 2	MRXD2	SMTXD2
MRXD1	SMRXD1	Receive Data Bit 1	MRXD1	SMTXD1
MRXD0	SMRXD0	Receive Data Bit 0	MRXD0	SMTXD0
MRXC	SMRXC	Receive Clock	MRXC	SMTXC

The MII operates in either PHY mode or MAC mode. The data interface is a nibble wide and runs at ¼ the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Similarly, the receive side has signals that convey when the data is valid and without physical layer errors. For half duplex operation, the SCOL signal indicates if a collision has occurred during transmission. The selection of the PHY mode and MAC mode for port3 MII is by the strap pin SMRXDV3 and the port register 53 bit 7. The selection of the PHY mode and MAC mode for port1 MII is by the strap pin SMRXD13 and the port register 21bit 7.

The KSZ8873MML does not provide the MRXER signal for PHY mode operation and the MTXER signal for MAC mode operation. Normally, MRXER indicates a receive error coming from the physical layer device and MTXER indicates a transmit error from the MAC device. Since the switch filters error frames, these MII error signals are not used by the KSZ8873MML. So, for PHY mode operation, if the device interfacing with the KSZ8873MML has an MRXER input pin, it needs to be tied low. And, for MAC mode operation, if the device interfacing with the KSZ8873MML has an MTXER input pin, it also needs to be tied low.

The KSZ8873MML provides a bypass feature in the MII PHY mode. Pin SMTXER3/MII_LINK is used for MII link status. If the host is power down, pin MII_LINK will go to high. In this case, no new ingress frames from port1 or port 2 will be sent out through port 3, and the frames for port 3 already in packet memory will be flushed out.

3.3.9 MII MANAGEMENT (MIIM) INTERFACE

The KSZ8873MML supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the states of the KSZ8873MML. An external device with MDC/MDIO capability is used to read the PHY status or configure the PHY settings. Further detail on the MIIM interface is found in Clause 22.2.4.5 of the IEEE 802.3u Specification and refer to 802.3 section 22.3.4 for the timing.

The MIIM interface consists of the following:

- A physical connection that incorporates the data line (SDA_MDIO) and the clock line (SCL_MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8873MML device.
- Access to a set of eight 16-bit registers, consisting of six standard MIIM registers [0:5] and two custom MIIM registers [29, 31].

The MIIM Interface can operate up to a maximum clock speed of 5 MHz.

Table 3-4 depicts the MII Management Interface frame format.

TABLE 3-4: MII MANAGEMENT FRAME FORMAT

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.3.10 SERIAL MANAGEMENT INTERFACE (SMI)

The SMI is the KSZ8873MML non-standard MIIM interface that provides access to all KSZ8873MML configuration registers. This interface allows an external device to completely monitor and control the states of the KSZ8873MML.

The SMI interface consists of the following:

- A physical connection that incorporates the data line (SDA_MDIO) and the clock line (SCL_MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8873MML device.
- Access to all KSZ8873MML configuration registers. Register access includes the Global, Port, and Advanced Control Registers 0-198 (0x00 – 0xC6), and indirect access to the standard MIIM registers [0:5] and custom MIIM registers [29, 31].

Table 3-5 depicts the SMI frame format.

TABLE 3-5: SERIAL MANAGEMENT INTERFACE (SMI) FRAME FORMAT

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	00	1xRRR	RRRRR	Z0	0000_0000_DDDD_DDDD	Z
Write	32 1's	01	00	0xRRR	RRRRR	10	xxxx_xxxx_DDDD_DDDD	Z

SMI register read access is selected when OP Code is set to "00" and bit 4 of the PHY address is set to '1'. SMI register write access is selected when OP Code is set to "00" and bit 4 of the PHY address is set to '0'. PHY address bit[3] is undefined for SMI register access, and hence can be set to either '0' or '1' in read/write operations.

To access the KSZ8873MML registers 0-196 (0x00 – 0xC6), the following applies:

- PHYAD[2:0] and REGAD[4:0] are concatenated to form the 8-bit address; that is, {PHYAD[2:0], REGAD[4:0]} = bits [7:0] of the 8-bit address.
- TA bits [1:0] are 'Z0' means the processor MDIO pin is changed to input Hi-Z from output mode and the followed '0' is the read response from device.
- TA bits [1:0] are set to '10' when write registers.
- Registers are 8 data bits wide.
  - For read operation, data bits [15:8] are read back as 0's.
  - For write operation, data bits [15:8] are not defined, and hence can be set to either '0' or '1'.

SMI register access is the same as the MIIM register access, except for the register access requirements presented in this section.

3.4 Advanced Switch Functions

3.4.1 BYPASS MODE

The KSZ8873MML also offers a bypass mode that enables system-level power saving. When the CPU (connected to port 3 or port 1) enters a power saving mode, power down mode or a sleep mode, the CPU can control pin 27 SMTXER3/MII_LINK_3 or pin 51 SMTXER1/MII_LINK_1 which can be tied high so that the KSZ8873MML detects this change and automatically switches to bypass mode in which the switch function between port 2 and port 3/port 1 is sustained. In bypass mode, the packets with DA to port 3 or port 1 will be dropped and bypass the internal buffer memory, making the buffer memory more efficiency for data transfer. Specifically, energy detect mode with bypass mode enabled increases power savings.

3.4.2 IEEE 802.1Q VLAN SUPPORT

The KSZ8873MML supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8873MML provides a 16-entries VLAN table that converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning.

TABLE 3-6: FID+DA LOOKUP IN VLAN MODE

DA Found in Static MAC Table?	Use FID Flag?	FID Match?	FID+DA Found in Dynamic MAC Table?	Action
No	Don’t care	Don’t care	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
No	Don’t care	Don’t care	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	0	Don’t care	Don’t care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	1	Yes	Don’t care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]

TABLE 3-7: FID+SA LOOKUP IN VLAN MODE

FID+SA Found in Dynamic MAC Table?	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table
Yes	Update time stamp

Advanced VLAN features, such as “Ingress VLAN filtering” and “Discard Non PVID packets” are also supported by the KSZ8873MML. These features can be set on a per port basis, and are defined in registers 18, 34, and 50 for ports 1, 2 and 3, respectively.

3.4.3 QOS PRIORITY SUPPORT

The KSZ8873MML provides Quality of Service (QoS) for applications such as VoIP and video conferencing. Offering four priority queues per port, the per-port transmit queue can be split into four priority queues: Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. Bit [0] of registers 16, 32, and 48 is used to enable split transmit queues for ports 1, 2, and 3, respectively. If a port's transmit queue is not split, high priority and low priority packets have equal priority in the transmit queue.

There is an additional option to either always deliver high priority packets first or use weighted fair queuing for the four priority queues. This global option is set and explained in bit [3] of register 5.

3.4.4 PORT-BASED PRIORITY

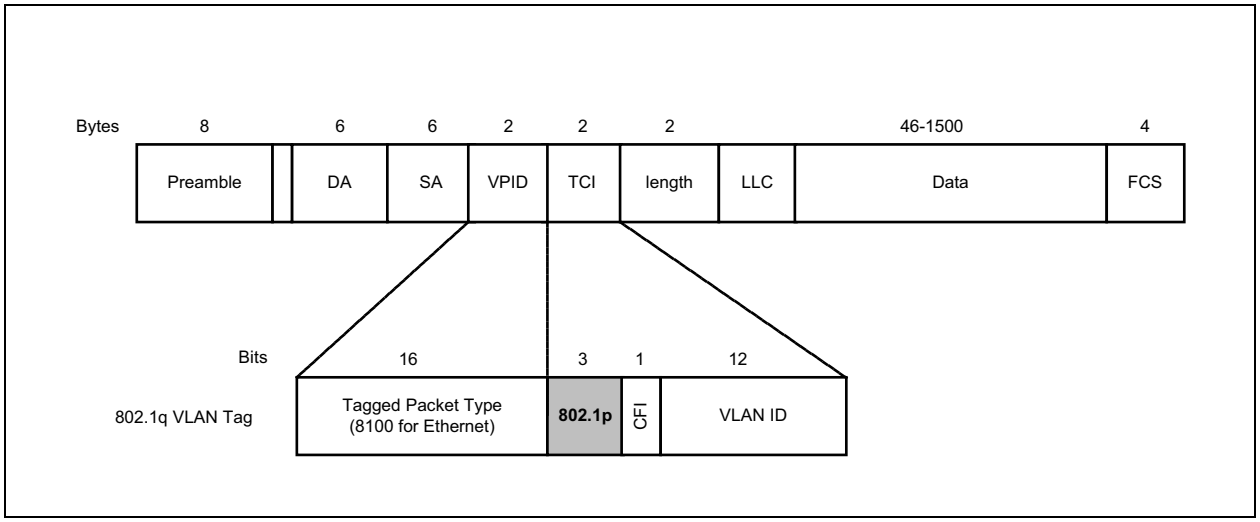
With port-based priority, each ingress port is individually classified as a high priority receiving port. All packets received at the high priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bits [4:3] of registers 16, 32, and 48 are used to enable port-based priority for ports 1, 2, and 3, respectively.

3.4.5 802.1P-BASED PRIORITY

For 802.1p-based priority, the KSZ8873MML examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and compared against the “priority mapping” value, as specified by the registers 12 and 13. The “priority mapping” value is programmable.

Figure 3-6 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

FIGURE 3-6: 802.1P PRIORITY FIELD FORMAT



802.1p-based priority is enabled by bit [5] of registers 16, 32, and 48 for ports 1, 2, and 3, respectively.

The KSZ8873MML provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN Protocol ID (VPID) and the 2-byte Tag Control Information field (TCI), is also referred to as the IEEE 802.1Q VLAN tag.

Tag Insertion is enabled by bit [2] of the port registers control 0 and the register 194 to select which source port (ingress port) PVID can be inserted on the egress port for ports 1, 2, and 3, respectively. At the egress port, untagged packets are tagged with the ingress port’s default tag. The default tags are programmed in register sets {19,20}, {35,36}, and {51,52} for ports 1, 2, and 3, respectively, and the source port VID has to be inserted at selected egress ports by bit[5:0] of register 194. The KSZ8873MML will not add tags to already tagged packets.

Tag Removal is enabled by bit [1] of registers 16, 32, and 48 for ports 1, 2, and 3, respectively. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8873MML will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

802.1p Priority Field Re-mapping is a QoS feature that allows the KSZ8873MML to set the “User Priority Ceiling” at any ingress port. If the ingress packet’s priority field has a higher priority value than the default tag’s priority field of the ingress port, the packet’s priority field is replaced with the default tag’s priority field.

3.4.6 DIFFSERV-BASED PRIORITY

DiffServ-based priority uses the ToS registers (registers 96 to 111) in the Advanced Control Registers section. The ToS priority control registers implement a fully decoded, 64-bit Differentiated Services Code Point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

3.5 Spanning Tree Support

To support spanning tree, port 3 is designated as the processor port.

The other ports (port 1 and port 2) can be configured in one of the five spanning tree states via “transmit enable”, “receive enable”, and “learning disable” register settings in registers 18 and 34 for ports 1 and 2, respectively. The following table shows the port setting and software actions taken for each of the five spanning tree states.

TABLE 3-8: SPANNING TREE STATES

State	Setting	Action
Disable State	**Port Setting**	**Software Action**
The port should not forward or receive any packets. Learning is disabled.	“transmit enable = 0, receive enable = 0, learning disable =1”	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the “static MAC table” with “overriding bit” set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State	**Port Setting**	**Software Action**
Only packets to the processor are forwarded. Learning is disabled.	“transmit enable = 0, receive enable = 0, learning disable =1”	The processor should not send any packets to the port(s) in this state. The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is disabled.	“transmit enable = 0, receive enable = 0, learning disable =1”	The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See **Section 3.7 “Tail Tagging Mode”** for details. Address learning is disabled on the port in this state.
Learning State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is enabled.	“transmit enable = 0, receive enable = 0, learning disable = 0”	The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See **Section 3.7 “Tail Tagging Mode”** for details. Address learning is enabled on the port in this state.