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KSZ8893FQL

Single-Chip 3-Port Switch with Fiber Support

Rev. 1.3

General Description

The KSZ8893FQL, a highly integrated single-chip 3 port Fast Ethernet switch is designed for applications with fiber support such as media converter. It provides two 10/100 transceivers with patented mixed-signal low-power technology, three media access control (MAC) units, a high-speed non-blocking switch fabric, a Layer-2 managed switch and TS-1000 OAM (Operations, Administration and Management) V2 in a compact solution. Backwards compatible to the TS-1000 (2002) specification, TS-1000 V2 is an OAM sub-layer that provides communication between CO (central office) and CPE (customer premises equipment).

In fiber mode, one PHY unit can be configurable to 100Base-FX, 100Base-SX, or 10Base-FL fiber for conversion to 10Base-T and 100Base-TX copper. A fiber LED driver and post amplifier are also included for 10Base-FL and 100Base-SX applications.

LinkMD®

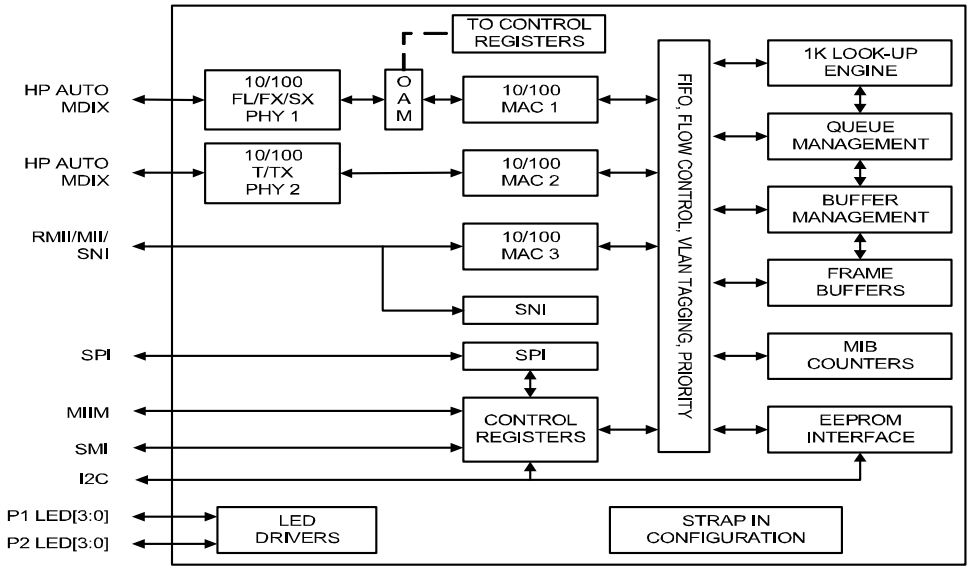
In copper mode, both PHY units support 10Base-T and 100Base-TX with HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables, and LinkMD® TDR-based cable diagnostics for identification of faulty cabling.

The high performance switching engine features an extensive feature set that includes programmable rate limiting, tag/port-based VLAN, 4 priority class, RMII/MII/SNI and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KSZ8893FQL comes in a lead-free package (see Ordering Information).

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Diagram



KSZ8893FQL

Features

Integrated 3-Port 10/100 Ethernet Switch

- Three MACs and two PHYs fully compliant with IEEE 802.3u standard
- Non-blocking switch fabric assures fast packet delivery by utilizing an 1K MAC address lookup table and a store-and-forward architecture
- Full duplex IEEE 802.3x flow control (PAUSE) with force mode option
- Half-duplex back pressure flow control
- HP Auto MDI-X for reliable detection of and correction for straight-through and crossover cables with disable and enable option
- Micrel LinkMD® TDR-based cable diagnostics permit identification of faulty copper cabling
- 100Base-FX, 100Base-SX and 10Base-FL fiber support on port 1
- MII interface supports both MAC mode and PHY mode
- RMII interface support with external 50MHz system clock
- 7-wire serial network interface (SNI) support for legacy MAC
- Comprehensive LED Indicator support for link, activity, full/half duplex and 10/100 speed

Fiber Support

- Integrated LED driver and post amplifier for 10Base-FL and 100Base-SX optical modules

TTC TS-1000 OAM

- Supports OAM sub-layer which conforms to TS-1000 V2 specification from TTC (Telecommunication Technology Committee)
- Sends and receives OAM frames to Center or Terminal side
- Loop back mode to support loop back packet from Center side to Terminal side
- Far-end fault detection with disable and enable
- Link Transparency to indicate link down from link partner
- Unique User Defined Register (UDR) feature brings OAM to low cost/complexity nodes

Comprehensive Configuration Register Access

- SMI, SPI and I^2C management interfaces to all 8-bit internal registers
- MII management (MIIM) interface to PHY registers
- I/O pins strapping and EEPROM to program selective registers in unmanaged switch mode
- Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…)

QoS/CoS Packet Prioritization Support

- Per port, 802.1p and DiffServ-based
- Re-mapping of 802.1p priority field per port basis
- Four priority levels

Advanced Switch Features

- IEEE 802.1q VLAN support for up to 16 groups (full-range of VLAN IDs)
- VLAN ID tag/untag options, per port basis
- IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
- Programmable rate limiting at the ingress and egress on a per port basis
- Broadcast storm protection with % control (global and per port basis)
- IEEE 802.1d spanning tree protocol support
- Special tagging mode to inform the processor which ingress port receives the packet
- IGMP snooping (Ipv4) and MLD snooping (Ipv6) support for multicast packet filtering
- MAC filtering function to forward unknown unicast packets to specified port
- Double-tagging support

Low Latency Support

- Repeater mode

Switch Monitoring Features

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
- MIB counters for fully compliant statistics gathering, 34 MIB counters per port
- Loopback modes for remote diagnostic of failure

Low Power Dissipation

- Full-chip hardware power-down (register configuration not saved)
- Per port based software power-save on PHY (idle link detection, register configuration preserved)
- Voltages:
  - Core 1.2V
  - I/O and Transceiver 3.3V

Available in 128-Pin PQFP, Lead-free package

Applications

- Media Conversion Modules:
  - 10Base-FL <=> 10Base-T
  - 100Base-SX <=> 100Base-TX
  - 100Base-FX <=> 100Base-TX
- FTTx Managed/Unmanaged Media Converters
- Fiber Broadband Gateways

Ordering Information

Part Number	Temp. Range	Package	Lead Finish	Description
KSZ8893FQL	0°C to 70°C	128-Pin PQFP	Pb-Free	Port 1 supports 10Base-FL and 100Base-SX with LED driver and post amp
KSZ8893FQL-FX	0°C to 70°C	128-Pin PQFP	Pb-Free	Port 1 supports 100Base-FX with TS-1000 OAM V2

Revision History

Revision	Date	Summary of Changes
1.0	07/05/06	Data sheet created.
1.1	02/08/07	Modify Table 10. RMII Signal Connections Add TLA-6T718 to Table 37. Qualified Single Port Magnetics Remove KSZ8893FQLI from the datasheet
1.2	06/19/07	Update Ordering Information Add Thermal Resistance (θ_{JC}) to Operating Rating
1.3	10/16/07	Recommend connecting a 100ohm resistor between VDDC and 3.3V power rail.

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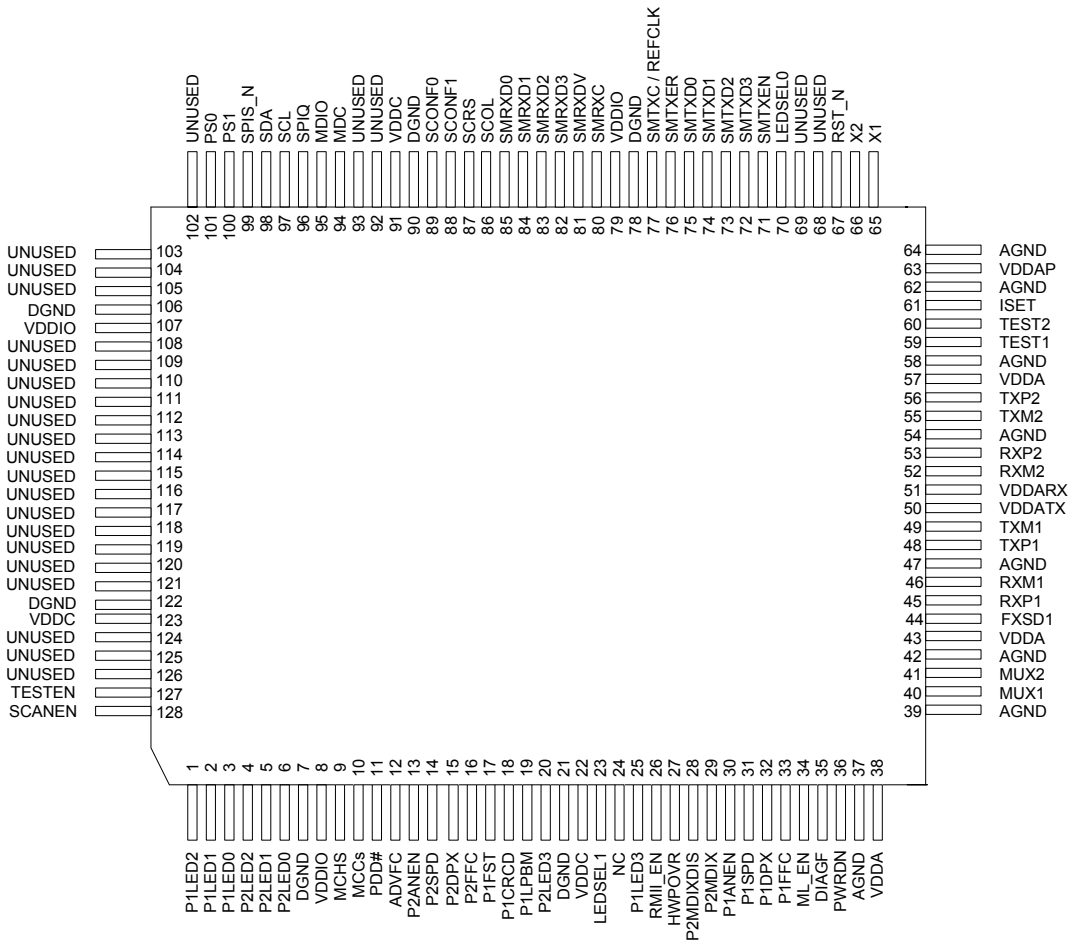
Pin Configuration



128-Pin PQFP (Q)
(Top View)

Pin Description

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>1
2
3</td><td>P1LED2
P1LED1
P1LED0</td><td>Ipu/O
Ipu/O
Ipu/O</td><td>
Port 1LED indicators (active low)
(apply to all modes of operation, except Repeater Mode)
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act:
Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col:
Low (full duplex), High (half duplex), Toggles (collision)
Speed:
Low (100Base-TX), High (10Base-T)
Full duplex:
Low (full duplex), High (half duplex)
Act:
Toggles (transmit / receive activity)
Link:
Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><td></td><td>[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0,0]</td></tr>
<tr><td>P1LED3</td><td>RPT_COL</td></tr>
<tr><td>P1LED2</td><td>RPT_LINK3/RX</td></tr>
<tr><td>P1LED1</td><td>RPT_LINK2/RX</td></tr>
<tr><td>P1LED0</td><td>RPT_LINK1/RX</td></tr>
</table>
RPT_COL:
Low (collision)
RPT_LINK#/RX (# = port):
Low (link), High (no link), Toggles (receive activity)
Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P1LED3 is pin 25.
During reset, P1LED[2:0] are inputs for internal testing.
</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>4
5
6</td><td>P2LED2
P2LED1
P2LED0</td><td>Ipu/O
Ipu/O
Ipu/O</td><td>
Port 2 LED indicators (active low)
(apply to all modes of operation, except Repeater Mode)
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act:
Low (link), High (no link), Toggles (transmit / receive activity)
Full duplex/Col:
Low (full duplex), High (half duplex), Toggles (collision)
Speed:
Low (100Base-TX), High (10Base-T)
Full duplex:
Low (full duplex), High (half duplex)
Act:
Toggles (transmit / receive activity)
Link:
Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><td></td><td>[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0,0]</td></tr>
<tr><td>P2LED3</td><td>RPT_ACT</td></tr>
<tr><td>P2LED2</td><td>RPT_ERR3</td></tr>
<tr><td>P2LED1</td><td>RPT_ERR2</td></tr>
<tr><td>P2LED0</td><td>RPT_ERR1</td></tr>
</table>
RPT_ACT:
Low (activity)
RPT_ERR# (# = port):
Low (error status due to either isolation, partition, jabber, or JK error)
Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P2LED3 is pin 20.
During reset, P2LED[2:0] are inputs for internal testing.
</td></tr>
<tr><td>7</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DD}</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>9
10</td><td>MCHS
MCCS</td><td>Ipd
Ipd</td><td>KSZ8893FQL operating modes (defined below):
<table>
<tr><th>(MCHS, MCCS)</th><th>Description</th></tr>
<tr><td>(0, 0)</td><td>Normal 3 port switch mode (3 MAC + 2 PHY)
MC mode is disabled.
Port 1 is either Fiber or UTP.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr>
<tr><td>(0, 1)</td><td>Center MC mode (3 MAC + 2 PHY)
MC mode is enabled.
Port 1 is Fiber and has Center MC enabled.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr>
<tr><td>(1, 0)</td><td>Terminal MC mode (2 MAC + 2 PHY)
MC mode is enabled.
Port 1 is Fiber and has Terminal MC enabled.
Port 2 is UTP.
Port 3 (MII) is disabled.</td></tr>
<tr><td>(1, 1)</td><td>Terminal MC mode (3 MAC + 2 PHY)
MC mode is enabled.
Port 1 Fiber and has Terminal MC enabled.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr>
</table></td></tr>
<tr><td>11</td><td>PDD#</td><td>Ipu</td><td>Power Down Detect
1 = Normal operation.
0 = Power down detected.

In Terminal MC mode (pin MCHS is ‘1’), a high to low transition to this pin will cause port 1 (fiber) to generate and send out an “Indicate Terminal MC Condition” OAM frame with the S0 status bit set to ‘1’.</td></tr>
<tr><td>12</td><td>ADVFC</td><td>Ipu</td><td>1 = Advertise the switch’s flow control capability via auto-negotiation.
0 = Will not advertise the switch’s flow control capability via auto-negotiation.</td></tr>
<tr><td>13</td><td>P2ANEN</td><td>Ipu</td><td>1 = Enable auto-negotiation on port 2.
0 = Disable auto-negotiation on port 2.</td></tr>
<tr><td>14</td><td>P2SPD</td><td>Ipd</td><td>1 = Force port 2 to 100BT if P2ANEN = 0.
0 = Force port 2 to 10BT if P2ANEN = 0.</td></tr>
<tr><td>15</td><td>P2DPX</td><td>Ipd</td><td>1 = Port 2 default to full duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0.
0 = Port 2 default to half duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0.</td></tr>
<tr><td>16</td><td>P2FFC</td><td>Ipd</td><td>1 = Always enable (force) port 2 flow control feature.
0 = Port 2 flow control feature enable is determine by the auto-negotiation result.</td></tr>
</table>

Pin Number	Pin Name	Type(1)	Pin Function
17	P1FST	Opu	1 = Normal function. 0 = MC in loopback mode, or MC abnormal conditions occur.
18	P1LCRCD	Ipd	In MC loopback mode, 1 = Drop OAM frames and Ethernet frames with the following errors – CRS, undersize, oversize. Loopback Ethernet frames with only good CRC and valid length. 0 = Drop OAM frames only. Loopback all Ethernet frames including those with errors.
19	P1LPBM	Ipd	1 = Perform MC loopback at PHY of port 1. 0 = Perform MC loopback at MAC of port 2
20	P2LED3	Opd	Port 2 LED indicator Note: An external 1K pull-down is needed on this pin if it is connected to an LED. The 1K resistor will not turn ON the LED. See description in pin 4.
21	DGND	Gnd	Digital ground
22	VDDC / VOUT_1V2	P	1.2V digital V_{DD} Provides V_{OUT_1V2} to KSZ8893FQL's input power pins: V_{DDAP} (pin 63), V_{DDC} (pins 91 and 123), and V_{DDA} (pins 38, 43, and 57). It is recommended the pin should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.
23	LEDSEL1	Ipd	LED display mode select. See description in pins 1 and 4.
24	NC	O	No connect
25	P1LED3	Opd	Port 1 LED indicator Note: An external 1K pull-down is needed on this pin if it is connected to an LED. The 1K resistor will not turn ON the LED. See description in pin 1.
26	RMII_EN	Opd	Strap pin for RMII Mode 1 = Enable 0 = Disable After reset, this pin has no meaning and is a no connect.
27	HWPOVR	Ipd	Hardware pin overwrite 1 = Enable: All strap-in pin configurations are overwritten by the EEPROM configuration data, except for P2ANEN (pin 13), P2SPD (pin 14), P2DPX (pin 15) and ML_EN (pin 34). After reset, the pin state for P2ANEN, P2SPD and P2DPX is polled by the KSZ8893FQL. 0 = Disable: All strap-in pin configurations are overwritten by the EEPROM configuration data.
28	P2MDIXDIS	Ipd	Port 2 Auto MDI/MDI-X PD (default) = enable PU = disable
29	P2MDIX	Ipd	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled. PD (default) = MDI-X (transmit on TXP2 / TXM2 pins) PU = MDI, (transmit on RXP2 / RXM2 pins)
30	P1ANEN	Ipu	1 = Enable auto-negotiation on port 1 0 = Disable auto-negotiation on port 1
31	P1SPD	Ipd	1 = Force port 1 to 100BT if P1ANEN = 0 0 = Force port 1 to 10BT if P1ANEN = 0

Pin Number	Pin Name	Type[1]	Pin Function
32	P1DPX	Ipd	1 = Port 1 default to full duplex mode if P1ANEN = 1 and auto-negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0. 0 = Port 1 default to half duplex mode if P1ANEN = 1 and auto-negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0.
33	P1FFC	Ipd	1 = Always enable (force) port 1 flow control feature 0 = Port 1 flow control feature enable is determined by auto-negotiation result.
34	ML_EN	Ipd	1 = Enable missing link 0 = Disable missing link
35	DIAGF	Ipd	1 = Diagnostic fail 0 = Diagnostic normal
36	PWRDN	Ipu	Chip power down input (active low) 1 = Normal operation 0 = The chip is powered down
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD}
39	AGND	Gnd	Analog ground
40	MUX1	I	No connect
41	MUX2	I	10Base-FL/100Base-SX Enable. Active low.
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD}
44	FXSD1	I	Fiber signal detect / factory test pin
45	RXP1	I/O	Physical receive or transmit signal (+ differential)
46	RXM1	I/O	Physical receive or transmit signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Physical transmit or receive signal (+ differential)
49	TXM1	I/O	Physical transmit or receive signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Physical receive or transmit signal (– differential)
53	RXP2	I/O	Physical receive or transmit signal (+ differential)
54	AGND	Gnd	Analog ground
55	TXM2	I/O	Physical transmit or receive signal (– differential)
56	TXP2	I/O	Physical transmit or receive signal (+ differential)
57	VDDA	P	1.2 analog V_{DD}
58	AGND	Gnd	Analog ground
59	TEST1	I	Factory test pin – float for normal operation
60	TEST2	I	Factory test pin – float for normal operation
61	ISET	O	Set physical transmit output current Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL
64	AGND	Gnd	Analog ground

Pin Number	Pin Name	Type[1]	Pin Function
65	X1	I	25MHz crystal/oscillator clock connections
66	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is no connected. Note: Clock is ±50ppm for both crystal and oscillator.
67	RST_N	Ipu	Hardware Reset (active low)
68	UNUSED	I	Unused pin – externally pull down for normal operation
69	UNUSED	I	Unused pin – externally pull down for normal operation
70	LEDSEL0	I	LED display mode select See description in pins 1 and 4.
71	SMTXEN	I	Switch MII transmit enable
72	SMTXD3	I	Switch MII transmit data bit 3
73	SMTXD2	I	Switch MII transmit data bit 2
74	SMTXD1	I	Switch MII transmit data bit 1
75	SMTXD0	I	Switch MII transmit data bit 0
76	SMTXER	I	Switch MII transmit error
77	SMTXC / REFCLK	I/O	Switch MII transmit clock (MII and SNI modes only) Output in PHY MII mode and SNI mode Input in MAC MII mode Reference Clock (RMII mode only) Input for 50MHz ±50ppm system clock Note: In RMII mode, pin X1 is pulled up to VDDIO supply with a 10K resistor and pin X2 is a no connect.
78	DGND	Gnd	Digital ground
79	VDDIO	P	3.3V digital V_{DD}
80	SMRXC	I/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
81	SMRXDV	O	Switch MII receive data valid
82	SMRXD3	Ipd/O	Switch MII receive data bit 3 Strap option: switch MII full-duplex flow control PD (default) = disable PU = enable
83	SMRXD2	Ipd/O	Switch MII receive data bit 2 Strap option: switch MII is in PD (default) = full-duplex mode PU = half-duplex mode
84	SMRXD1	Ipd/O	Switch MII receive data bit 1 Strap option: Switch MII is in PD (default) = 100Mbps mode PU = 10Mbps mode
85	SMRXD0	I/O	Switch MII receive data bit 0 Strap option: switch will accept packet size up to PD = 1536 bytes (inclusive) PU = 1522 bytes (tagged), 1518 bytes (untagged)
86	SCOL	I/O	Switch MII collision detect

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>87</td><td>SCRS</td><td>I/O</td><td>Switch MII carrier sense</td></tr>
<tr><td>88</td><td>SCONF1</td><td>I</td><td rowspan="2">Switch MII interface configuration
<table><tr><th>(SCONF1, SCONF0)</th><th>Description</th></tr><tr><td>(0,0)</td><td>disable, outputs tri-stated</td></tr><tr><td>(0,1)</td><td>PHY mode MII</td></tr><tr><td>(1,0)</td><td>MAC mode MII</td></tr><tr><td>(1,1)</td><td>PHY mode SNI</td></tr></table></td></tr>
<tr><td>89</td><td>SCONF0</td><td>I</td></tr>
<tr><td>90</td><td>DGND</td><td>Gnd</td><td>Digital core ground</td></tr>
<tr><td>91</td><td>VDDC</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>92</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull down for normal operation</td></tr>
<tr><td>93</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull down for normal operation</td></tr>
<tr><td>94</td><td>MDC</td><td>I</td><td>MII management interface: clock input</td></tr>
<tr><td>95</td><td>MDIO</td><td>I/O</td><td>MII management interface: data input/output
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>96</td><td>SPIQ</td><td>O</td><td>SPI slave mode: serial data output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>97</td><td>SCL</td><td>I/O</td><td>SPI slave mode / I^2C slave mode: clock input
I^2C master mode: clock output
See description in pins 100 and 101.</td></tr>
<tr><td>98</td><td>SDA</td><td>I/O</td><td>SPI slave mode: serial data input
I^2C master/slave mode: serial data input/output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>99</td><td>SPIS_N</td><td>I</td><td>SPI slave mode: chip select (active low)
When SPIS_N is high, the KSZ8893FQL is deselected and SPIQ is held in high impedance state.
A high-to-low transition is used to initiate SPI data transfer.
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>100</td><td>PS1</td><td>I</td><td>Serial bus configuration pins to select mode of access to KSZ8893FQL internal</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>101</td><td>PS0</td><td>I</td><td>registers.

[PS1, PS0] = [0, 0] — I²C master (EEPROM) mode
(If EEPROM is not detected, the KSZ8893FQL will be configured with the default values of its internal registers and the values of its strap-in pins.)
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>O</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [0, 1] — I²C slave mode
The external I²C master will drive the SCL clock.
The KSZ8893FQL device addresses are:
1011_1111 <read>
1011_1110 <write>
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>I</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [1, 0] — SPI slave mode
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr><tr><td>SCL</td><td>I</td><td>SPI clock</td></tr><tr><td>SDA</td><td>I</td><td>SPI data In</td></tr><tr><td>SPIS_N</td><td>I</td><td>SPI chip select</td></tr></table>[PS1, PS0] = [1, 1] – SMI-mode
In this mode, the KSZ8893FQL provides access to all its internal 8-bit registers through its MDC and MDIO pins.

Note:
When (PS1, PS0) ≠ (1,1), the KSZ8893FQL provides access to its 16-bit MIIM registers through its MDC and MDIO pins.</td></tr>
<tr><td>102</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull up for normal operation</td></tr>
<tr><td>103</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull up for normal operation</td></tr>
<tr><td>104</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull up for normal operation</td></tr>
<tr><td>105</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull up for normal operation</td></tr>
<tr><td>106</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>107</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DD}</td></tr>
<tr><td>108</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull up for normal operation</td></tr>
<tr><td>109</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull up for normal operation</td></tr>
<tr><td>110</td><td>UNUSED</td><td>I</td><td>Unused pin – externally pull down for normal operation</td></tr>
</table>

Pin Number	Pin Name	Type[1]	Pin Function
111	UNUSED	I	Unused pin – externally pull down for normal operation
112	UNUSED	I	Unused pin – externally pull down for normal operation
113	UNUSED	I	Unused pin – externally pull down for normal operation
114	UNUSED	I	Unused pin – externally pull down for normal operation
115	UNUSED	I	Unused pin – externally pull down for normal operation
116	UNUSED	I	Unused pin – externally pull down for normal operation
117	UNUSED	I	Unused pin – externally pull down for normal operation
118	UNUSED	I	Unused pin – externally pull down for normal operation
119	UNUSED	I	Unused pin – externally pull down for normal operation
120	UNUSED	I	Unused pin – externally pull down for normal operation
121	UNUSED	I	Unused pin – externally pull down for normal operation
122	DGND	Gnd	Digital ground
123	VDDC	P	1.2V digital V_{DD}
124	UNUSED	I	Unused pin – externally pull down for normal operation
125	UNUSED	I	Unused pin – externally pull down for normal operation
126	UNUSED	I	Unused pin – externally pull down for normal operation
127	TESTEN	Ipd	Scan Test Enable For normal operation, pull-down this pin to ground.
128	SCANEN	Ipd	Scan Test Scan Mux Enable For normal operation, pull-down this pin to ground.

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipd = Input with internal pull-down.
   Ipu = Input with internal pull-up.
   Opd = Output with internal pull-down.
   Opu = Output with internal pull-up.
   Ipd/O = Input with internal pull-down during reset; output pin otherwise.
   Ipu/O = Input with internal pull-up during reset; output pin otherwise.

Functional Description

The KSZ8893FQL is a single-chip Fast Ethernet media converter. It contains two 10/100 physical layer transceivers and three Media Access Control (MAC) units with an integrated Layer 2 managed switch.

On the media side, the KSZ8893FQL supports IEEE 802.3 10Base-T and 100Base-TX on both PHY ports. In Media Converter (MC) applications, PHY port 1 is the fiber port and supports 100Base-FX, 100Base-SX and 10Base-FL.

The KSZ8893FQL has the flexibility to reside in either a managed or unmanaged design. In a managed design, the host processor has complete control of the KSZ8893FQL via the SMI interface, MIIM interface, SPI bus, or I^2C bus. An unmanaged design is achieved through I/O strapping and/or EEPROM programming at system reset time.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

Functional Overview: Media Conversion

TS-1000 OAM Operation

The KSZ8893FQL implements Japan's TTC (TELECOMMUNICATION TECHNOLOGY COMMITTEE) TS-1000 version 2, OAM sub-layer, which resides between RS and PCS layer in the IEEE 802.3 Standard. The OAM sub-layer is provided in 100Base-FX mode, and is used by the KSZ8893FQL to send and receive OAM frames. These special frames are used for the transmission of OAM (Operations, Administration, Management) information between center MC and terminal MC. Key TS-1000 OAM features include:

- Private point-to-point communication between two TS-1000 compliant devices
- 96 bits (12 bytes) frames for the transmission of OAM information between center MC and terminal MC
- Transmission of MC status between center MC and terminal MC
- Automatic generation of OAM frame to inform MC link partner of local MC's status change
- Transmission of vendor code and model number information between center MC and terminal MC for device identification
- Inquisition of terminal MC status by center MC
- Remote loop back for diagnostic by center MC

OAM Frame Format

The TS-1000 OAM (Operations, Administration, and Management) Frame Format is shown on the following page.

Bit		Command	Description
F0–F7		Preamble	1010 1010
C0		Conservation Delimiter	0
C1		Direction Delimiter	0: Upstream (from terminal MC to center MC) 1: Downstream (from center MC to terminal MC)
C2–C3		Configuration Delimiter	10: request 11:reponse 01: indication 00:reserved
C4–C7		Version	0000
C8–C15		Control signal	1000 0000: Start loop back test 0000 0000: Stop loop back test 0100 0000: Notify status
S0	Status	Power	0: normal operation 1: power down
S1		Optical	0: normal 1:abnormal
S2		UTP link	0: link up 1: link down
S3		MC	0: normal 1:brake
S4		Way for information	0: use conservation frame 1: use FEFI
S5		Loop mode	0: normal operation 1: in loop mode
S6		Terminal MC Link option	0: Center side MC have to set always “0” 1: Terminal side MC have to set always “1”
S7		Terminal MC Link Speed1	This bit must be set “0”
S8		Terminal MC Link Speed2	0: 10Mbps 1: 100Mbps These bits have to be set “0”, if S2 is “1” (Center side MC have to set always “0”)
S9		Terminal MC Link Duplex	0: Half Duplex 1: Full Duplex This bit have to be set “0”, if S2 is “1” (Center side MC have to set always “0”)
S10		Terminal MC Auto-Negotiation capability	0: Not Support Auto-Negotiation 1: Support Auto-Negotiation (Center side MC have to set always “0”)
S11		Multiple link partner	0: one link partner on UTP side 1: multiple link partner on UTP side
S12–S15		Reserve	All bits must be set “0”
M0–M23		Vendor code	
M24–M47		Model number	
E0–E7		FCS	Create FCS at this sub-layer (C0-M47)

Figure 1. TS-1000 OAM Frame Format

Media Converter Modes

TS-1000 Media Converter (MC) modes are selected and configured using hardware pins: MCHS and MCCS. The MC modes are summarized in the following table and are also shown in the Pin Description and I/O Assignment section.

(MCHS, MCCS)	Description
(0, 0)	Normal 3 port switch mode (3 MAC + 2 PHY) MC mode is disabled. Port 1 is either Fiber or UTP. Port 2 is UTP. Port 3 (MII) is enabled.
(0, 1)	Center MC mode (3 MAC + 2 PHY) MC mode is enabled. Port 1 is Fiber & has Center MC enabled. Port 2 is UTP. Port 3 (MII) is enabled.
(1, 0)	Terminal MC mode (2 MAC + 2 PHY) MC mode is enabled. Port 1 is Fiber & has Terminal MC enabled. Port 2 is UTP. Port 3 (MII) is disabled.
(1, 1)	Terminal MC mode (3 MAC + 2 PHY) MC mode is enabled. Port 1 is Fiber & has Terminal MC enabled. Port 2 is UTP. Port 3 (MII) is enabled.

Table 1. TS-1000 Media Converter Mode Selection

The following figure shows two KSZ8893FQLs connected in a typical center MC to terminal MC application.

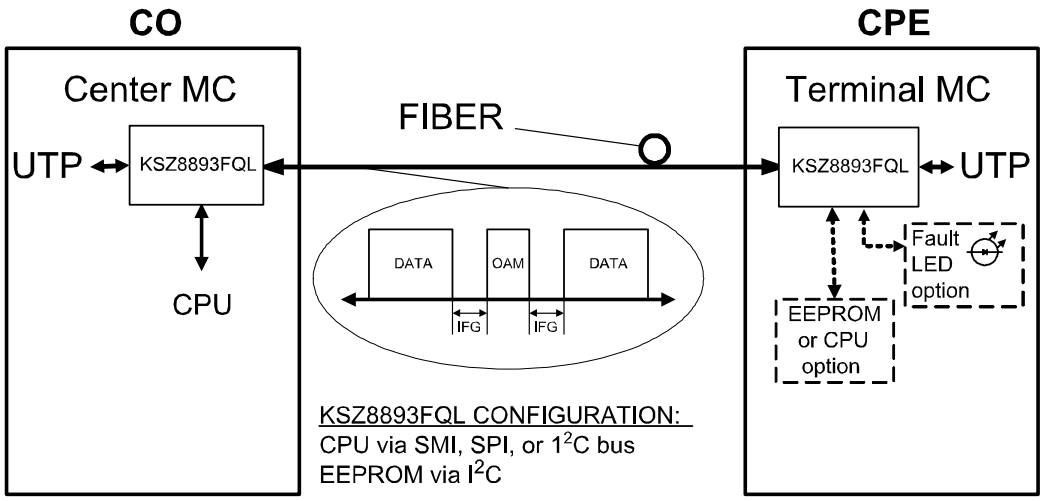


Figure 2. Typical TS-1000 Media Converter Application

MC Loop Back Operation

TS-1000 MC loop back operation is initiated and enabled by the center MC. The terminal MC provides the loop back path to return the loop back packet back to the center MC. The KSZ8893FQL in terminal MC mode provides three loop back path options:

Port 1 OPT

- Receive loop back packet from center MC at RXP1/RXM1 input pins of port 1 (fiber).
- Turn around loop back packet at PMD/PMA of port 1 (fiber).
- Transmit loop back packet back to center MC from TXP1/TXM1 output pins of port 1 (fiber).

Port 2 MAC

- Receive loop back packet from center MC at RXP1/RXM1 input pins of port 1 (fiber).
- Turn around loop back packet at MAC of port 2 (copper).
- Transmit loop back packet back to center MC from TXP1/TXM1 output pins of port 1 (fiber).

Port 2 UTP

- Receive loop back packet from center MC at RXP1/RXM1 input pins of port 1 (fiber).
- Turn around loop back packet at PMD/PMA of port 2 (copper).
- Transmit loop back packet back to center MC from TXP1/TXM1 output pins of port 1 (fiber).

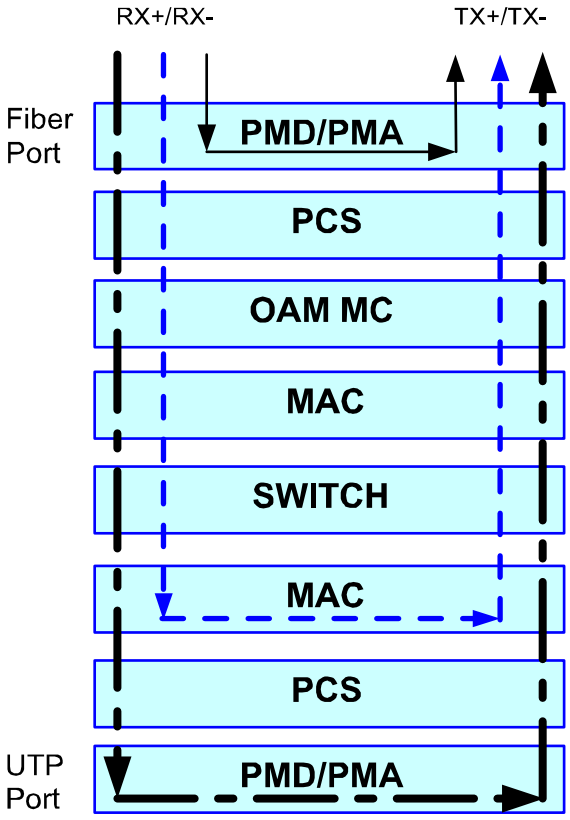


Figure 3. KSZ8893FQL MC Loop Back Paths