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KSZ8893MQL/MBL

Integrated 3-Port 10/100 Managed Switch with PHYs

Rev. 1.6

General Description

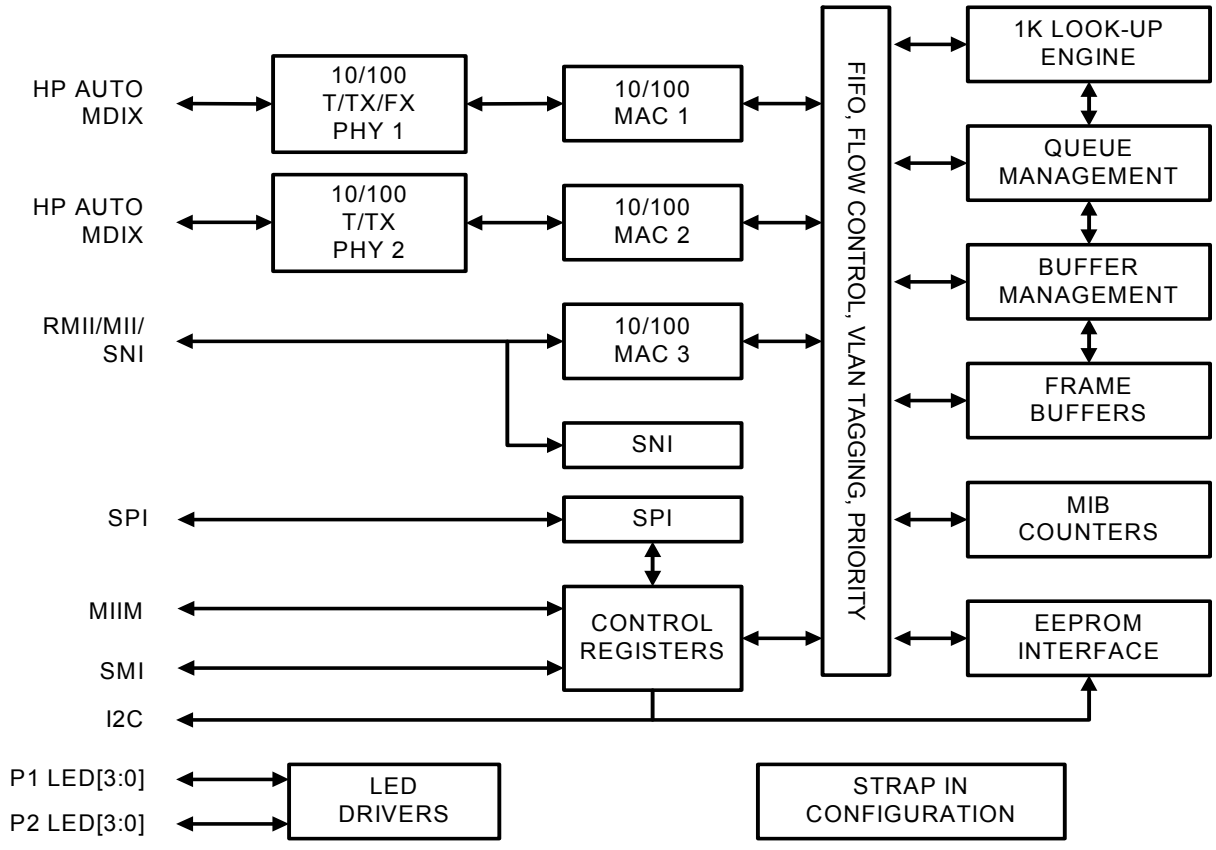
The KSZ8893MQL/MBL, a highly integrated layer 2 managed switch, is designed for low port count, cost-sensitive 10/100 Mbps switch systems. It offers an extensive feature set that includes rate limiting, tag/port-based VLAN, QoS priority, management, management information base (MIB) counters, RMII/MII/SNI, and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KSZ8893MQL/MBL contains two 10/100 transceivers with patented mixed-signal low-power technology, three media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

Both PHY units support 10BASE-T and 100BASE-TX. In addition, one PHY unit supports 100BASE-FX.

The KSZ8893MQL/MBL comes in a lead-free package, and is also available in industrial temperature-grade KS8893MQLI/MBLI and Automotive-grade KSZ8893 MQL AM. (See Ordering Information).

Functional Diagram



Features

- **Proven Integrated 3-Port 10/100 Ethernet Switch**
  – 3rd generation switch with three MACs and two PHYs fully compliant with IEEE 802.3u standard
  – Non-blocking switch fabric assures fast packet delivery by utilizing an 1K MAC address lookup table and a store-and-forward architecture
  – Full duplex IEEE 802.3x flow control (PAUSE) with force mode option
  – Half-duplex back pressure flow control
  – HP Auto MDI-X for reliable detection of and correction for straight-through and crossover cables with disable and enable option
  – Micrel LinkMD™ TDR-based cable diagnostics permit identification of faulty copper cabling
  – 100BASE-FX support on port 1
  – MII interface supports both MAC mode and PHY mode
  – RMII interface support with external 50MHz system clock
  – 7-wire serial network interface (SNI) support for legacy MAC
  – Comprehensive LED Indicator support for link, activity, full/half duplex and 10/100 speed
- **Comprehensive Configuration Register Access**
  – Serial management interface (SMI) to all internal registers
  – MII management (MIIM) interface to PHY registers
  – SPI and I^2C Interface to all internal registers
  – I/0 pins strapping and EEPROM to program selective registers in unmanaged switch mode
  – Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…)
- **QoS/CoS Packet Prioritization Support**
  – Per port, 802.1p and DiffServ-based
  – Re-mapping of 802.1p priority field per port basis
  – Four priority levels
- **Advanced Switch Features**
  – IEEE 802.1q VLAN support for up to 16 groups (full-range of VLAN IDs)
  – VLAN ID tag/untag options, per port basis
  – IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
  – Programmable rate limiting at the ingress and egress on a per port basis
  – Broadcast storm protection with % control (global and per port basis)
  – IEEE 802.1d spanning tree protocol support
  – Special tagging mode to inform the processor which ingress port receives the packet
  – IGMP snooping (Ipv4) and MLD snooping (Ipv6) support for multicast packet filtering
  – MAC filtering function to forward unknown unicast packets to specified port
  – Double-tagging support
  – Support IEEE 802.1w, 802.1t spanning tree
- **Low Latency Support**
  – Repeater mode
- **Switch Monitoring Features**
  – Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
  – MIB counters for fully compliant statistics gathering, 34 MIB counters per port
  – Loopback modes for remote diagnostic of failure
- **Low Power Dissipation**:
  – Full-chip hardware power-down (register configuration not saved)
  – Per port based software power-save on PHY (idle link detection, register configuration preserved)
  – Voltages: Single power supply: 3.3V
- Industrial Temperature Range: –40°C to +85°C
- Available in 128-Pin PQFP and 100-ball LFBGA, Lead- free package

Applications

- **Typical**
  – Media Converter
  – FTTx customer premises equipment
  – VoIP Phone
  – SOHO Residential Gateway
  – Broadband Gateway / Firewall / VPN
  – Integrated DSL/Cable Modem
  – Wireless LAN access point + gateway
  – Set-top/Game Box
  – Standalone 10/100 switch
- **Upgradeable**(1)
  – Unmanaged switch with future option to migrate to a managed solution
  – Single PHY alternative with future expansion option for two ports
- **Industrial**
  – Applications requiring port redundancy and port monitoring
  – Sensor devices in redundant ring topology

Note:
1. Reduces cost and time of PCB re-spin.

Ordering Information

Part Number	Operation Temp. Range	Package	Grade
KSZ8893MQL	0°C to 70°C	128-Pin PQFP, Lead-free	Commercial
KSZ8893MQLI	–40°C to +85°C	128-Pin PQFP, Lead-free	Industrial
KSZ8893MQL AM	-40°C to +85°C	128-Pin PQFP, Lead-free	Automotive grade
KSZ8893MBL	0°C to 70°C	100-Ball LFBGA	Commercial
KSZ8893MBLI	–40°C to +85°C	100-Ball LFBGA	Industrial

Revision History

Revision	Date	Summary of Changes
1.0	6/30/05	Initial release
1.1	11/17/05	Updated ordering information Updated package information Updated default register values Updated current consumption description Changed device reference in datasheet from KS8893M to KSZ8893MQL Added repeater mode description
1.2	02/08/07	Modify Table 5. RMII Signal Connections Add TLA-6T718 to Table 16. Qualified Single Port Magnetics
1.3	06/19/07	Add Thermal Resistance (θ_{JC}) to Operating Rating
1.4	10/16/07	Recommend connecting a 100ohm resistor between VDDC and 3.3V power rail.
1.5	11/05/07 11/26/07 12/10/07 07/30/08 09/16/08 02/12/09	Add the KSZ8893MBL BGA device information. Modify the Hold time, Output valid in table 25, 26 and Figure 25,26 of MII interface timing. Add the I2C timing diagram and parameters in Figure 24 to 27 and Table 28. Add MBLI to order information Modify the paragraph “Unicast MAC Address Filtering” Modify the Table 5 (RMII Signal Connections)

Contents

List of Figures

List of Tables

Pin Description and I/O Assignment of KSZ8893MQL

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>1</td><td>P1LED2</td><td>Ipu/O</td><td rowspan="3">
Port 1 LED Indicators
(apply to all modes of operation, except Repeater Mode)
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P1LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P1LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act : Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col : Low (full duplex), High (half duplex), Toggles (collision)
Speed : Low (100BASE-TX), High (10BASE-T)
Full duplex : Low (full duplex), High (half duplex)
Act : Toggle (transmit / receive activity)
Link : Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><td></td><td>[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td></tr>
<tr><td>P1LED3</td><td>RPT_COL</td></tr>
<tr><td>P1LED2</td><td>RPT_LINK3/RX</td></tr>
<tr><td>P1LED1</td><td>RPT_LINK2/RX</td></tr>
<tr><td>P1LED0</td><td>RPT_LINK1/RX</td></tr>
</table>
RPT_COL : Low (collision)
RPT_LINK#/RX (# = port) : Low (link), High (no link), Toggles (receive activity)

Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P1LED3 is pin 25.
During reset, P1LED[2:0] are inputs for internal testing.
</td></tr>
<tr><td>2</td><td>P1LED1</td><td>Ipu/O</td></tr>
<tr><td>3</td><td>P1LED0</td><td>Ipu/O</td></tr>
</table>

Note:

1. Ipu/O = Input with internal pull-up during reset, output pin otherwise.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>4</td><td>P2LED2</td><td>Ipu/O</td><td rowspan="3">Port 2 LED Indicators
(apply to all modes of operation, except Repeater Mode)

<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>

<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act : Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col : Low (full duplex), High (half duplex), Toggles (collision)
Speed : Low (100BASE-TX), High (10BASE-T)
Full duplex : Low (full duplex), High (half duplex)
Act : Toggle (transmit / receive activity)
Link : Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><td></td><td>[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td></tr>
<tr><td>P2LED3</td><td>RPT_ACT</td></tr>
<tr><td>P2LED2</td><td>RPT_ERR3</td></tr>
<tr><td>P2LED1</td><td>RPT_ERR2</td></tr>
<tr><td>P2LED0</td><td>RPT_ERR1</td></tr>
</table>
RPT_ACT : Low (activity)
RPT_ERR# (# = port) : Low (error status due to either isolation, partition, jabber, or JK error)
Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P2LED3 is pin 20.
During reset, P2LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>5</td><td>P2LED1</td><td>Ipu/O</td></tr>
<tr><td>6</td><td>P2LED0</td><td>Ipu/O</td></tr>
<tr><td>7</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td>3.3V digital V_{DD}</td></tr>
</table>

Note:
1. P = Power supply.
   Gnd = Ground.
   Ipu/O = Input with internal pull-up during reset, output pin otherwise.

Pin Number	Pin Name	Type (1)	Description
9	NC	Ipd	No connect
10	NC	Ipd	No connect
11	NC	Ipu	No connect
12	ADVFC	Ipu	1 = advertise the switch's flow control capability via auto-negotiation. 0 = will not advertise the switch's flow control capability via auto-negotiation.
13	P2ANEN	Ipu	1 = enable auto-negotiation on port 2 0 = disable auto-negotiation on port 2
14	P2SPD	Ipd	1 = force port 2 to 100BT if P2ANEN = 0 0 = force port 2 to 10BT if P2ANEN = 0
15	P2DPX	Ipd	1 = port 2 default to full duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0. 0 = port 2 default to half duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0.
16	P2FFC	Ipd	1 = always enable (force) port 2 flow control feature 0 = port 2 flow control feature enable is determined by auto-negotiation result.
17	NC	Opu	No connect
18	NC	Ipd	No connect
19	NC	Ipd	No connect
20	P2LED3	Opd	Port 2 LED indicator Note: Internal pull-down is weak; it will not turn ON the LED. See description in pin 4.
21	DGND	Gnd	Digital ground
22	VDDCO	P	1.2V digital VDD Provides V_{OUT_1V2} to KSZ8893MQL's input power pins: V_{DDAP} (pin 63), V_{DDC} (pins 91 and 123), and V_{DDA} (pins 38, 43, and 57). It is recommended the pin should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.
23	LEDSEL1	Ipd	LED display mode select See description in pins 1 and 4.
24	NC	O	No connect
25	P1LED3	Opd	Port 1 LED indicator Note: An external 1K pull-down is needed on this pin if it is connected to a LED. The 1K resistor will not turn ON the LED. See description in pin 1.

Note:

1. P = Power supply.
   Gnd = Ground.
   O = Output.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Opu = Output w/ internal pull-up.
   Opd = Output w/ internal pull-down.

Pin Number	Pin Name	Type (1)	Description
26	RMII_EN	Opd	Strap pin for RMII Mode 0 = Disable 1 = Enable After reset, this pin has no meaning and is a no connect.
27	HWPOVR	Ipd	Hardware pin overwrite 0 = Disable. All strap-in pins configurations are overwritten by the EEPROM configuration data 1 = Enable. All strap-in pins configurations are overwritten by the EEPROM configuration data, except for register 0x2C bits [7:5], (port 2: auto-negotiation enable, force speed, force duplex).
28	P2MDIXDIS	Ipd	Port 2 Auto MDI/MDI-X PD (default) = enable PU = disable
29	P2MDIX	Ipd	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled. PD (default) = MDI-X (transmit on TXP2 / TXM2 pins) PU = MDI, (transmit on RXP2 / RXM2 pins)
30	P1ANEN	Ipu	1 = enable auto-negotiation on port 1 0 = disable auto-negotiation on port 1
31	P1SPD	Ipd	1 = force port 1 to 100BT if P1ANEN = 0 0 = force port 1 to 10BT if P1ANEN = 0
32	P1DPX	Ipd	1 = port 1 default to full duplex mode if P1ANEN = 1 and auto-negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0. 0 = port 1 default to half duplex mode if P1ANEN = 1 and auto- negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0.
33	P1FFC	Ipd	1 = always enable (force) port 1 flow control feature 0 = port 1 flow control feature enable is determined by auto negotiation result.
34	NC	Ipd	No connect
35	NC	Ipd	No connect
36	PWRDN	Ipu	Chip power down input (active low)
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD}
39	AGND	Gnd	Analog ground
40	MUX1	I	Factory test pin - float for normal operation
41	MUX2	I	Factory test pin - float for normal operation

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Opd = Output w/ internal pull-down.

Pin Number	Pin Name	Type (1)	Description
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD}
44	FXSD1	I	Fiber signal detect / factory test pin
45	RXP1	I/O	Physical receive or transmit signal (+ differential)
46	RXM1	I/O	Physical receive or transmit signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Physical transmit or receive signal (+ differential)
49	TXM1	I/O	Physical transmit or receive signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Physical receive or transmit signal (– differential)
53	RXP2	I/O	Physical receive or transmit signal (+ differential)
54	AGND	Gnd	Analog ground.
55	TXM2	I/O	Physical transmit or receive signal (– differential)
56	TXP2	I/O	Physical transmit or receive signal (+ differential)
57	VDDA	P	1.2V analog V_{DD}
58	AGND	Gnd	Analog ground
59	TEST1	I	Factory test pin - float for normal operation
60	TEST2	I	Factory test pin - float for normal operation
61	ISET	O	Set physical transmit output current. Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL
64	AGND	Gnd	Analog ground.
65	X1	I	25MHz crystal/oscillator clock connections Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is +/- 50ppm for both crystal and oscillator.
66	X2	O	
67	RST_N	Ipu	Hardware reset pin (active low)
68	UNUSED	I	Unused pin – externally pull down for normal operation
69	UNUSED	I	Unused pin – externally pull down for normal operation

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input w/ internal pull-up.

Pin Number	Pin Name	Type [1]	Description
70	LEDSEL0	I	LED display mode select See description in pins 1 and 4.
71	SMTXEN	I	Switch MII transmit enable
72	SMTXD3	I	Switch MII transmit data bit 3
73	SMTXD2	I	Switch MII transmit data bit 2
74	SMTXD1	I	Switch MII transmit data bit 1
75	SMTXD0	I	Switch MII transmit data bit 0
76	SMTXER	I	Switch MII transmit error
77	SMTXC / REFCLK	I/O	Switch MII transmit clock (MII and SNI modes only) Output in PHY MII mode and SNI mode Input in MAC MII mode Reference Clock (RMII mode only) Input for 50MHz +/- 50ppm system clock Note: In RMII mode, pin X1 is pulled up to VDDIO supply with a 10K resistor and pin X2 is a no connect.
78	DGND	Gnd	Digital ground
79	VDDIO	P	3.3V digital V_{DD}
80	SMRXC	I/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
81	SMRXDV	O	Switch MII receive data valid
82	SMRXD3	Ipd/O	Switch MII receive data bit 3 Strap option: switch MII full-duplex flow control PD (default) = disable PU = enable
83	SMRXD2	Ipd/O	Switch MII receive data bit 2 Strap option: switch MII is in PD (default) = full-duplex mode PU = half-duplex mode
84	SMRXD1	Ipd/O	Switch MII receive data bit 1 Strap option: Switch MII is in PD (default) = 100Mbps mode PU = 10Mbps mode
85	SMRXD0	I/O	Switch MII receive data bit 0 Strap option: switch will accept packet size up to PD = 1536 bytes (inclusive) PU = 1522 bytes (tagged), 1518 bytes (untagged)
86	SCOL	I/O	Switch MII collision detect
87	SCRS	I/O	Switch MII carrier sense

Note:
1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   I/O = Bi-directional.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>88</td><td>SCONF1</td><td>I</td><td rowspan="2">Switch MII interface configuration<table><tr><th>(SCONF1, SCONF0)</th><th>Description</th></tr><tr><td>(0,0)</td><td>disable, outputs tri-stated</td></tr><tr><td>(0,1)</td><td>PHY mode MII</td></tr><tr><td>(1,0)</td><td>MAC mode MII</td></tr><tr><td>(1,1)</td><td>PHY mode SNI</td></tr></table></td></tr>
<tr><td>89</td><td>SCONF0</td><td>I</td></tr>
<tr><td>90</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>91</td><td>VDDC</td><td>P</td><td>1.2V digital VDD</td></tr>
<tr><td>92</td><td>UNUSED</td><td>I</td><td rowspan="2">Unused pins – externally pull down for normal operation</td></tr>
<tr><td>93</td><td>UNUSED</td><td>I</td></tr>
<tr><td>94</td><td>MDC</td><td>I</td><td>MII management interface: clock input</td></tr>
<tr><td>95</td><td>MDIO</td><td>I/O</td><td>MII management interface: data input/output
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>96</td><td>SPIQ</td><td>O</td><td>SPI slave mode: serial data output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>97</td><td>SCL</td><td>I/O</td><td>SPI slave mode / I^2C slave mode: clock input
I^2C master mode: clock output
See description in pins 100 and 101.</td></tr>
<tr><td>98</td><td>SDA</td><td>I/O</td><td>SPI slave mode: serial data input
I^2C master/slave mode: serial data input/output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>99</td><td>SPIS_N</td><td>I</td><td>SPI slave mode: chip select (active low)
When SPIS_N is high, the KSZ8893MQL is deselected and SPIQ is held in high impedance state.
A high-to-low transition is used to initiate SPI data transfer.
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
</table>

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>100</td><td>PS1</td><td>I</td><td rowspan="2">Serial bus configuration pins to select mode of access to KSZ8893MQL internal registers.

[PS1, PS0] = [0, 0] — I²C master (EEPROM) mode
(If EEPROM is not detected, the KSZ8893MQL will be configured with the default values of its internal registers and the values of its strap-in pins.)
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>O</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [0, 1] — I²C slave mode
The external I²C master will drive the SCL clock.
The KSZ8893MQL device addresses are:
1011_1111 <read>
1011_1110 <write>
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>I</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [1, 0] — SPI slave mode
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr><tr><td>SCL</td><td>I</td><td>SPI clock</td></tr><tr><td>SDA</td><td>I</td><td>SPI data In</td></tr><tr><td>SPIS_N</td><td>I</td><td>SPI chip select</td></tr></table>[PS1, PS0] = [1, 1] – SMI-mode
In this mode, the KSZ8893MQL provides access to all its internal 8-bit registers through its MDC and MDIO pins.

Note:
When (PS1, PS0) ≠ (1,1), the KSZ8893MQL provides access to its 16-bit MIIM registers through its MDC and MDIO pins.</td></tr>
<tr><td>101</td><td>PS0</td><td>I</td></tr>
<tr><td>102</td><td>UNUSED</td><td>I</td><td rowspan="2">Unused pins – externally pull up for normal operation</td></tr>
<tr><td>103</td><td>UNUSED</td><td>I</td></tr>
</table>

Note:

1. I = Input.

Pin Number	Pin Name	Type [1]	Description
104	UNUSED	I	Unused pins – externally pull up for normal operation
105	UNUSED	I	
106	DGND	Gnd	Digital ground
107	VDDIO	P	3.3V digital V_{DD}
108	UNUSED	I	Unused pins – externally pull up for normal operation
109	UNUSED	I	
110	UNUSED	I	Unused pin – externally pull down for normal operation
111	UNUSED	I	Unused pin – externally pull down for normal operation
112	UNUSED	I	Unused pin – externally pull down for normal operation
113	UNUSED	I	Unused pin – externally pull down for normal operation
114	UNUSED	I	Unused pin – externally pull down for normal operation
115	UNUSED	I	Unused pin – externally pull down for normal operation
116	UNUSED	I	Unused pin – externally pull down for normal operation
117	UNUSED	I	Unused pin – externally pull down for normal operation
118	UNUSED	I	Unused pin – externally pull down for normal operation
119	UNUSED	I	Unused pin – externally pull down for normal operation
120	UNUSED	I	Unused pin – externally pull down for normal operation
121	UNUSED	I	Unused pin – externally pull down for normal operation
122	DGND	Gnd	Digital ground
123	VDDC	P	1.2V digital V_{DD}
124	UNUSED	I	Unused pin – externally pull down for normal operation
125	UNUSED	I	Unused pin – externally pull down for normal operation
126	UNUSED	I	Unused pin – externally pull down for normal operation
127	TESTEN	Ipd	Scan Test Enable For normal operation, pull-down this pin to ground.
128	SCANEN	Ipd	Scan Test Scan Mux Enable For normal operation, pull-down this pin to ground.

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   Ipd = Input w/ internal pull-down.

Ball Description and I/O Assignment of KSZ8893MBL

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
<tr><td>C10</td><td>P1LED2</td><td>Ipu/O</td><td rowspan="3">Port 1 LED Indicators
(apply to all modes of operation, except Repeater Mode)
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P1LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P1LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act : Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col : Low (full duplex), High (half duplex), Toggles (collision)
Speed : Low (100BASE-TX), High (10BASE-T)
Full duplex : Low (full duplex), High (half duplex)
Act : Toggle (transmit / receive activity)
Link : Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><td></td><td>[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td></tr>
<tr><td>P1LED3</td><td>RPT_COL</td></tr>
<tr><td>P1LED2</td><td>RPT_LINK3/RX</td></tr>
<tr><td>P1LED1</td><td>RPT_LINK2/RX</td></tr>
<tr><td>P1LED0</td><td>RPT_LINK1/RX</td></tr>
</table>
RPT_COL : Low (collision)
RPT_LINK#/RX (# = port) : Low (link), High (no link), Toggles (receive activity)

Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P1LED3 is pin 25.
During reset, P1LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>B10</td><td>P1LED1</td><td>Ipu/O</td></tr>
<tr><td>A10</td><td>P1LED0</td><td>Ipu/O</td></tr>
</table>

Note:

1. Ipu/O = Input with internal pull-up during reset, output pin otherwise.

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
<tr><td>C9</td><td>P2LED2</td><td>Ipu/O</td><td rowspan="3">Port 2 LED Indicators
(apply to all modes of operation, except Repeater Mode)

<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>

<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Link/Act, 100Link/Act, 10Link/Act : Low (link), High (no link), Toggle (transmit / receive activity)
Full duplex/Col : Low (full duplex), High (half duplex), Toggles (collision)
Speed : Low (100BASE-TX), High (10BASE-T)
Full duplex : Low (full duplex), High (half duplex)
Act : Toggle (transmit / receive activity)
Link : Low (link), High (no link)

Repeater Mode (only)
<table>
<tr><td></td><td>[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td></tr>
<tr><td>P2LED3</td><td>RPT_ACT</td></tr>
<tr><td>P2LED2</td><td>RPT_ERR3</td></tr>
<tr><td>P2LED1</td><td>RPT_ERR2</td></tr>
<tr><td>P2LED0</td><td>RPT_ERR1</td></tr>
</table>
RPT_ACT : Low (activity)
RPT_ERR# (# = port) : Low (error status due to either isolation, partition, jabber, or JK error)
Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P2LED3 is pin 20.
During reset, P2LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>B9</td><td>P2LED1</td><td>Ipu/O</td></tr>
<tr><td>A9</td><td>P2LED0</td><td>Ipu/O</td></tr>
<tr><td>C8</td><td>ADVFC</td><td>Ipu</td><td>1 = advertise the switch’s flow control capability via auto-negotiation.
0 = will not advertise the switch’s flow control capability via auto-negotiation.</td></tr>
<tr><td>B8</td><td>P2ANEN</td><td>Ipu</td><td>1 = enable auto-negotiation on port 2
0 = disable auto-negotiation on port 2</td></tr>
</table>

Ball Number	Ball Name	Type [1]	Ball Function Description
A8	P2SPD	Ipd	1 = force port 2 to 100BT if P2ANEN = 0 0 = force port 2 to 10BT if P2ANEN = 0
B7	P2DPX	Ipd	1 = port 2 default to full duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0. 0 = port 2 default to half duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0.
A7	P2FFC	Ipd	1 = always enable (force) port 2 flow control feature 0 = port 2 flow control feature enable is determined by auto-negotiation result.
B6	P2LED3	Opd	Port 2 LED indicator Note: Internal pull-down is weak; it will not turn ON the LED. See description in pin 4.
A6	LEDSEL1	Ipd	LED display mode select See description in pins 1 and 4.
B5	P1LED3	Opd	Port 1 LED indicator Note: An external 1K pull-down is needed on this pin if it is connected to a LED. The 1K resistor will not turn ON the LED. See description in pin 1.
A5	RMII_EN	Opd	Strap pin for RMII Mode 0 = Disable 1 = Enable After reset, this pin has no meaning and is a no connect.
B4	HWPOVR	Ipd	Hardware pin overwrite 0 = Disable. All strap-in pins configurations are overwritten by the EEPROM configuration data 1 = Enable. All strap-in pins configurations are overwritten by the EEPROM configuration data, except for register 0x2C bits [7:5], (port 2: auto-negotiation enable, force speed, force duplex).
A4	P2MDIXDIS	Ipd	Port 2 Auto MDI/MDI-X PD (default) = enable PU = disable
B3	P2MDIX	Ipd	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled. PD (default) = MDI-X (transmit on TXP2 / TXM2 pins) PU = MDI, (transmit on RXP2 / RXM2 pins)
A3	P1ANEN	Ipu	1 = enable auto-negotiation on port 1 0 = disable auto-negotiation on port 1
B2	P1SPD	Ipd	1 = force port 1 to 100BT if P1ANEN = 0 0 = force port 1 to 10BT if P1ANEN = 0
A2	P1DPX	Ipd	1 = port 1 default to full duplex mode if P1ANEN = 1 and auto- negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0. 0 = port 1 default to half duplex mode if P1ANEN = 1 and auto- negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0.

Ball Number	Ball Name	Type [1]	Ball Function Description
A1	P1FFC	Ipd	1 = always enable (force) port 1 flow control feature 0 = port 1 flow control feature enable is determined by auto negotiation result.
B1	PWRDN	Ipu	Chip power down input (active low)
C3	FXSD1	I	Fiber signal detect / factory test pin
C1	RXP1	I/O	Physical receive or transmit signal (+ differential)
C2	RXM1	I/O	Physical receive or transmit signal (– differential)
D1	TXP1	I/O	Physical transmit or receive signal (+ differential)
D2	TXM1	I/O	Physical transmit or receive signal (– differential)
F2	RXM2	I/O	Physical receive or transmit signal (– differential)
F1	RXP2	I/O	Physical receive or transmit signal (+ differential)
G2	TXM2	I/O	Physical transmit or receive signal (– differential)
G1	TXP2	I/O	Physical transmit or receive signal (+ differential)
H2	ISET	O	Set physical transmit output current. Pull-down this pin with a 3.01K 1% resistor to ground.
H1	X1	I	25MHz crystal/oscillator clock connections
J1	X2	O	Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is +/- 50ppm for both crystal and oscillator.
K1	RST_N	Ipu	Hardware reset pin (active low)
J2	LEDSEL0	I	LED display mode select See description in pins 1 and 4.
K2	SMTXEN	I	Switch MII transmit enable
J3	SMTXD3	I	Switch MII transmit data bit 3
K3	SMTXD2	I	Switch MII transmit data bit 2
J4	SMTXD1	I	Switch MII transmit data bit 1
K4	SMTXD0	I	Switch MII transmit data bit 0
J5	SMTXER	I	Switch MII transmit error
K5	SMTXC / REFCLK	I/O	Switch MII transmit clock (MII and SNI modes only) Output in PHY MII mode and SNI mode Input in MAC MII mode Reference Clock (RMII mode only) Input for 50MHz +/- 50ppm system clock Note: In RMII mode, pin X1 is pulled up to VDDIO supply with a 10K resistor and pin X2 is a no connect.
K6	SMRXC	I/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
J6	SMRXDV	O	Switch MII receive data valid
J7	SMRXD3	Ipd/O	Switch MII receive data bit 3 Strap option: switch MII full-duplex flow control PD (default) = disable PU = enable

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
<tr><td>K7</td><td>SMRXD2</td><td>Ipd/O</td><td>Switch MII receive data bit 2
Strap option: switch MII is in
PD (default) = full-duplex mode
PU = half-duplex mode</td></tr>
<tr><td>J8</td><td>SMRXD1</td><td>Ipd/O</td><td>Switch MII receive data bit 1
Strap option: Switch MII is in
PD (default) = 100Mbps mode
PU = 10Mbps mode</td></tr>
<tr><td>K8</td><td>SMRXD0</td><td>I/O</td><td>Switch MII receive data bit 0
Strap option: switch will accept packet size up to
PD = 1536 bytes (inclusive)
PU = 1522 bytes (tagged), 1518 bytes (untagged)</td></tr>
<tr><td>J9</td><td>SCOL</td><td>I/O</td><td>Switch MII collision detect</td></tr>
<tr><td>K9</td><td>SCRS</td><td>I/O</td><td>Switch MII carrier sense</td></tr>
<tr><td>J10</td><td>SCONF1</td><td>I</td><td rowspan="2">Switch MII interface configuration
<table><tr><th>(SCONF1, SCONF0)</th><th>Description</th></tr><tr><td>(0,0)</td><td>disable, outputs tri-stated</td></tr><tr><td>(0,1)</td><td>PHY mode MII</td></tr><tr><td>(1,0)</td><td>MAC mode MII</td></tr><tr><td>(1,1)</td><td>PHY mode SNI</td></tr></table></td></tr>
<tr><td>K10</td><td>SCONF0</td><td>I</td></tr>
<tr><td>H10</td><td>MDC</td><td>I</td><td>MII management interface: clock input</td></tr>
<tr><td>H9</td><td>MDIO</td><td>I/O</td><td>MII management interface: data input/output
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>G9</td><td>SPIQ</td><td>O</td><td>SPI slave mode: serial data output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>G10</td><td>SCL</td><td>I/O</td><td>SPI slave mode / I^2C slave mode: clock input
I^2C master mode: clock output
See description in pins 100 and 101.</td></tr>
<tr><td>F9</td><td>SDA</td><td>I/O</td><td>SPI slave mode: serial data input
I^2C master/slave mode: serial data input/output
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>F10</td><td>SPIS_N</td><td>I</td><td>SPI slave mode: chip select (active low)
When SPIS_N is high, the KSZ8893MBL is deselected and SPIQ is held in high impedance state.
A high-to-low transition is used to initiate SPI data transfer.
See description in pins 100 and 101.
Note: an external pull-up is needed on this pin when it is in use.</td></tr>
</table>

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
<tr><td>E9</td><td>PS1</td><td>I</td><td rowspan="2">Serial bus configuration pins to select mode of access to KSZ8893MBL internal registers.
[PS1, PS0] = [0, 0] — I²C master (EEPROM) mode
(If EEPROM is not detected, the KSZ8893MBL will be configured with the default values of its internal registers and the values of its strap-in pins.)
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>O</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [0, 1] — I²C slave mode
The external I²C master will drive the SCL clock.
The KSZ8893MBL device addresses are:
1011_1111 <read>
1011_1110 <write>
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>I</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>I</td><td>Not used</td></tr></table>[PS1, PS0] = [1, 0] — SPI slave mode
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr><tr><td>SCL</td><td>I</td><td>SPI clock</td></tr><tr><td>SDA</td><td>I</td><td>SPI data In</td></tr><tr><td>SPIS_N</td><td>I</td><td>SPI chip select</td></tr></table>[PS1, PS0] = [1, 1] – SMI-mode
In this mode, the KSZ8893MBL provides access to all its internal 8-bit registers through its MDC and MDIO pins.
Note:
When (PS1, PS0) ≠ (1,1), the KSZ8893MBL provides access to its 16-bit MIIM registers through its MDC and MDIO pins.</td></tr>
<tr><td>E10</td><td>PS0</td><td>I</td></tr>
<tr><td>D9</td><td>TESTEN</td><td>Ipd</td><td>Scan Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>D10</td><td>SCANEN</td><td>Ipd</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>C5, D8, E8, H6, H7</td><td>VDDC</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>C4</td><td>VDDCO</td><td>P</td><td>1.2V digital V_{DD}
Provides V_{OUT_1V2} to KSZ8893MBL’s input power pins: V_{DDA} (pin E3, F3 and G3), V_{DDC} (pins C5, D8, E8, H6 and H7). It is recommended the pin should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.</td></tr>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type (1)</th><th>Ball Function Description</th></tr>
</table>

E3, F3, G3	VDDA	P	1.2V analog V_{DD}
C6, C7, F8, G8, H4, H5	VDDIO	P	3.3V digital V_{DD}
E1	VDDATX	P	3.3V analog V_{DD}
E2	VDDARX	P	3.3V analog V_{DD}
D4, D5, D6, D7, E4, E5, E6, E7, F4, F5, F6, F7, G4, G5, G6, G7	GND	Gnd	Ground
D3, H3, H8	NC	NC	No connect

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input w/ internal pull-up.