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KSZ8895MQ/RQ/FMQ

Integrated 5-Port 10/100 Managed Ethernet Switch with MII/RMII Interface

Revision 1.7

General Description

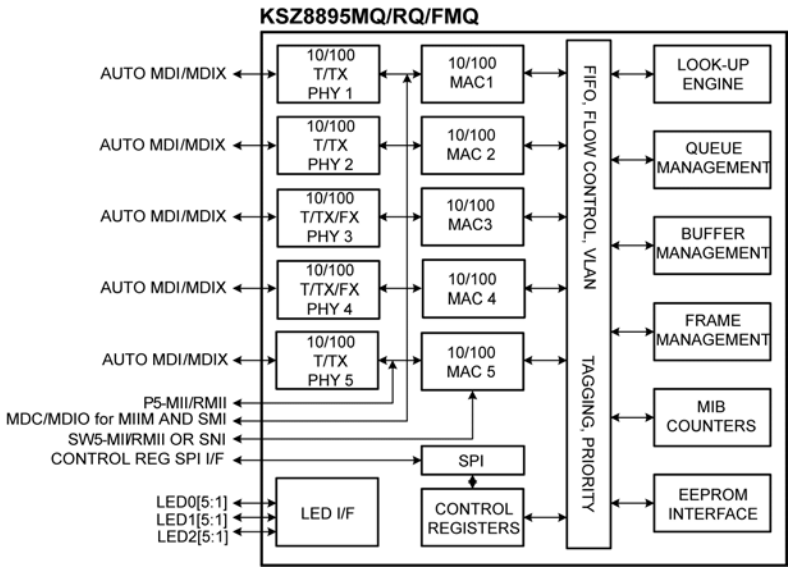
The KSZ8895MQ/RQ/FMQ is a highly-integrated, Layer 2 managed, five-port switch with numerous features designed to reduce system cost. Intended for cost-sensitive 10/100Mbps five-port switch systems with low power consumption, on-chip termination, and internal core power controllers, it supports high-performance memory bandwidth and shared memory-based switch fabric with non-blocking configuration. Its extensive feature set includes power management, programmable rate limit and priority ratio, tag/port-based VLAN, packets filtering, four-queue QoS prioritization, management interfaces, and MIB counters. The KSZ8895 family provides multiple CPU data interfaces to effectively address both current and emerging fast Ethernet applications when port 5 is configured to separate MAC5 with SW5-MII/RMII and PHY5 with P5-MII/RMII interfaces.

The KSZ8895 family offers three configurations, providing the flexibility to meet different requirements:

- KSZ8895MQ: Five 10/100Base-T/TX transceivers, one SW5-MII and one P5-MII interface,
- KSZ8895RQ: Five 10/100Base-T/TX transceivers, one SW5-RMII and one P5-RMII interface
- KSZ8895FMQ: Three 10/100Base-T/TX transceivers on Ports 1, 2, 5 and two 100Base-FX transceivers on Ports 3, 4, one SW5-MII and one P5-MII interface

All registers of MACs and PHYs units can be managed by the SPI or the SMI interface. MIIM registers can be accessed through the MDC/MDIO interface. EEPROM can set all control registers for the unmanaged mode. KSZ8895MQ/RQ/FMQ are 128-pin PQFP packages.

Functional Diagram



Note:
SW5 indicates the MAC5 of the switch side, P5 indicates the PHY5 of the Port 5.

Features

Advanced Switch Features

- IEEE 802.1q VLAN support for up to 128 active VLAN groups (full-range 4096 of VLAN IDs).
- Static MAC table supports up to 32 entries.
- VLAN ID tag/untag options, per port basis
- IEEE 802.1p/q tag insertion or removal on a per port basis based on ingress port (egress).
- Programmable rate limiting at the ingress and egress on a per port basis.
- Jitter-free per packet based rate limiting support.
- Broadcast storm protection with percentage control (global and per port basis).
- IEEE 802.1d rapid spanning tree protocol RSTP support.
- Tail tag mode (1 byte added before FCS) support at Port 5 to inform the processor which ingress port receives the packet.
- 1.4Gbps high-performance memory bandwidth and shared memory-based switch fabric with fully non-blocking configuration.
- Dual MII with MAC5 and PHY5 on port 5, SW5-MII/RMII for MAC 5 and P5-MII/RMII for PHY 5.
- Enable/Disable option for huge frame size up to 2000 Bytes per frame.
- IGMP v1/v2 snooping (Ipv4) support for multicast packet filtering.
- IPv4/IPv6 QoS support.
- Support unknown unicast/multicast address and unknown VID packet filtering.
- Self-address filtering.

Comprehensive Configuration Register Access

- Serial management interface (MDC/MDIO) to all PHYs registers and SMI interface (MDC/MDIO) to all registers.
- High speed SPI (up to 25MHz) and I^2C master Interface to all internal registers.
- I/0 pins strapping and EEPROM to program selective registers in unmanaged switch mode.
- Control registers configurable on the fly (port-priority, 802.1p/d/q, AN).

QoS/CoS Packet Prioritization Support

- Per port, 802.1p and DiffServ-based.
- 1/2/4-queue QoS prioritization selection.
- Programmable weighted fair queuing for ratio control.
- Re-mapping of 802.1p priority field per port basis.

Integrated Five-Port 10/100 Ethernet Switch

- New generation switch with five MACs and five PHYs with fully compliant with IEEE 802.3u standard.
- PHYs designed with patented enhanced mixed-signal technology.
- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K MAC address lookup table and a store-and-forward architecture.
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table).
- Full duplex IEEE 802.3x flow control (PAUSE) with force mode option.
- Half-duplex back pressure flow control.
- HP Auto MDI/MDI-X and IEEE Auto crossover support.
- SW-MII interface supports both MAC mode and PHY mode.
- 7-wire serial network interface (SNI) support for legacy MAC.
- Per port LED Indicators for link, activity, and 10/100 speed.
- Register port status support for link, activity, full/half duplex and 10/100 speed.
- On-chip terminations and internal biasing technology for cost down and lowest power consumption.

Switch Monitoring Features

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII.
- MIB counters for fully compliant statistics gathering 34 MIB counters per port.
- Loop-back support for MAC, PHY and remote diagnostic of failure.
- Interrupt for the link change on any ports.

Low Power Dissipation

- Full-chip hardware power-down.
- Full-chip software power-down and per port software power down.
- Energy-detect mode support < 100mW full chip-power consumption when all ports have no activity.
- Very low full chip power consumption (<0.5W), without extra power consumption on transformers.
- Dynamic clock tree shutdown feature.
- Voltages: Single 3.3V supply with 3.3V VDDIO and Internal 1.2V LDO controller enabled, or external 1.2V LDO solution.
  - Analog VDDAT 3.3V only.
  - VDDIO support 3.3V, 2.5V and 1.8V.
  - Low 1.2V core power .
- 0.13µm CMOS technology.
- Commercial temperature range: 0°C to +70°C.
- Industrial Temperature Range: -40°C to +85°C.
- Available in 128-pin PQFP lead-free package.

Applications

- VoIP phone
- Set-top/game box
- Automotive
- Industrial control
- IPTV POF
- SOHO residential gateway
- Broadband gateway/firewall/VPN
- Integrated DSL/cable modem
- Wireless LAN access point + gateway
- Standalone 10/100 switch

Ordering Information

Part Number	Temperature Range	Package	Lead Finish/Grade
KSZ8895MQ	0°C to 70°C	128-Pin PQFP	Pb-Free/Commercial
KSZ8895MQI	–40°C to +85°C	128-Pin PQFP	Pb-Free/Industrial
KSZ8895RQ	0°C to 70°C	128-Pin PQFP	Pb-Free/Commercial
KSZ8895RQI	–40°C to +85°C	128-Pin PQFP	Pb-Free/Industrial
KSZ8895FMQ	0°C to 70°C	128-Pin PQFP	Pb-Free/Commercial
KSZ8895FMQI	–40°C to +85°C	128-Pin PQFP	Pb-Free/Industrial
KSZ8895MQ-EVAL	Evaluation Board for KSZ8895MQ		
KSZ8895RQ-EVAL	Evaluation Board for KSZ8895RQ		
KSZ8895FMQ-Eval	Evaluation Board for KSZ8895FMQ		

Note:
1. Please consult sales for the availability

Revision History

Revision	Date	Description
1.0	09/13/10	Initial document created
1.1	11/16/10	Remove TMQ part
1.2	01/20/11	Update the ordering information and some data.
1.3	03/18/11	Update the register number, descriptions and correct typo error.
1.4	08/30/11	Correct typo error for package information and update some descriptions for SMI mode and IGMP and update register default values, pins type and some parameters.
1.5	02/24/12	Update descriptions for Pin, register 1 chip ID, port register, VLAN table and I2C master. Update the equation in the broadcast storm protection section. Update table of strap-in pins. Update the ordering information for RQ parts.
1.6	11/28/12	Update the ordering information for FMQ parts available. Correct typos. Update the operation rating to ±5% and TTL min/max I/O voltage in different VDDIO. Add register 165 for FMQ part with fiber mode. Update a note for pin 125 descriptions.
1.7	03/12/14	Change I/O from TTL to CMOS. Update SPI description from 127 to 255 for access registers. Update Register 6 offset. Update register offset mapping index. Correct typos. Updates timing data for MII PHY mode. Update the table of tail tag rules. Update description for Register 1 bits [7:4]. Update Table 8 from bit [57:55] to bit [58:56]. Update the port register control 2 bit [6] description (bits [20:16] change to bits [11:7]). Update Table 33. Add evaluation Board in ordering information table. Update a note for pin 126 descriptions.

Contents

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System Level Applications

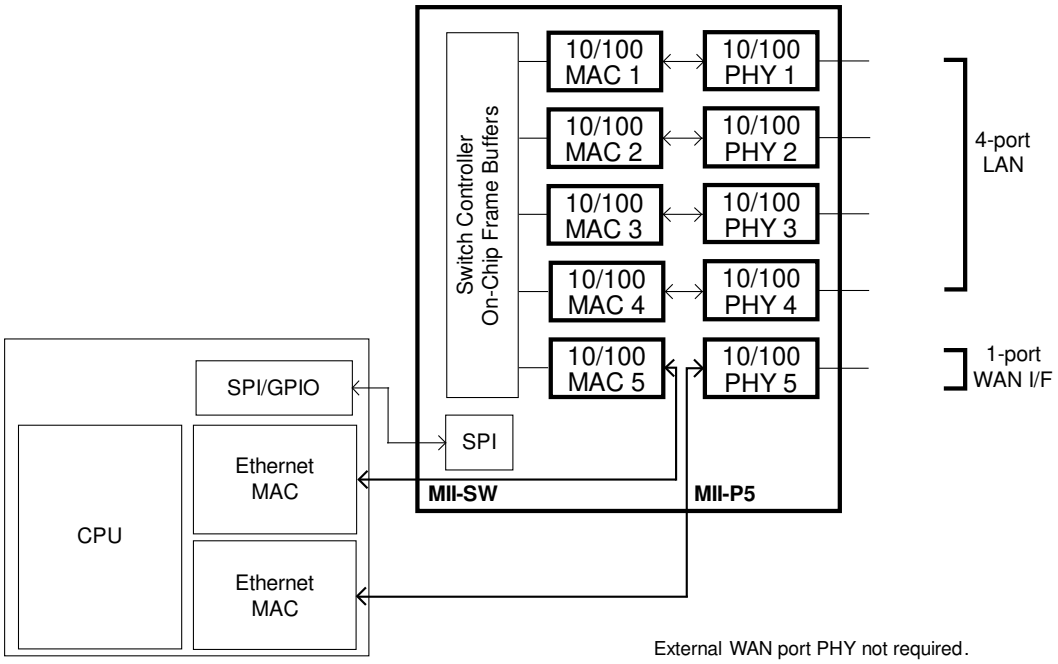

Figure 1. Broadband Gateway

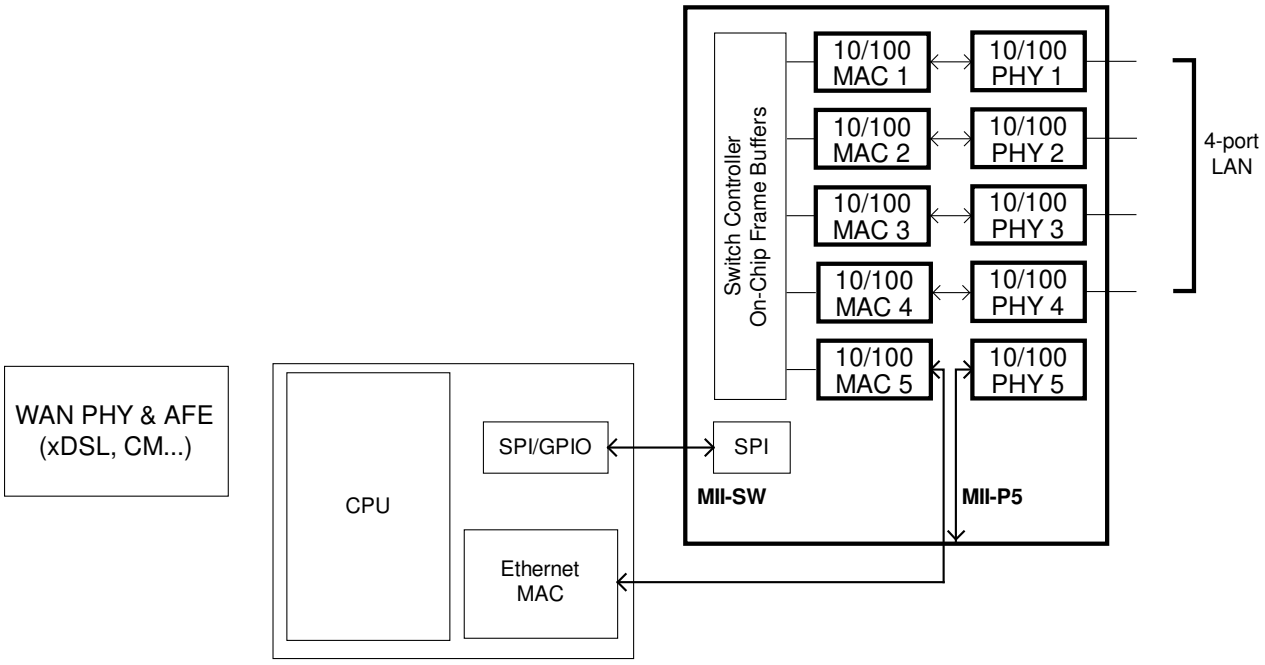

Figure 2. Integrated Broadband Router

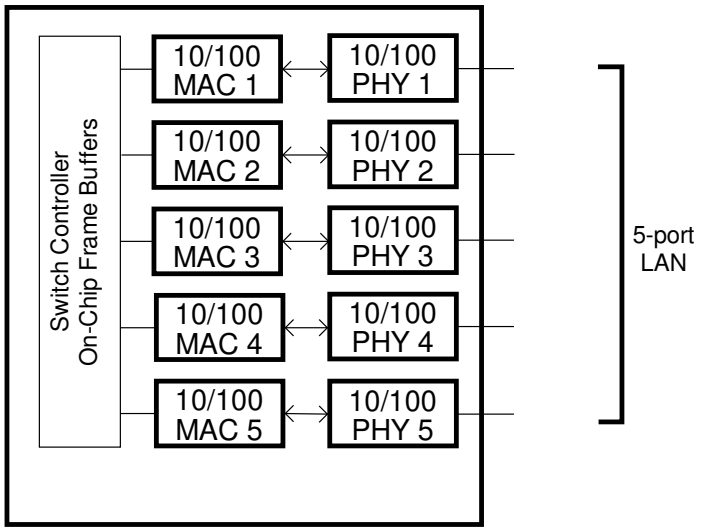

Figure 3. Standalone Switch

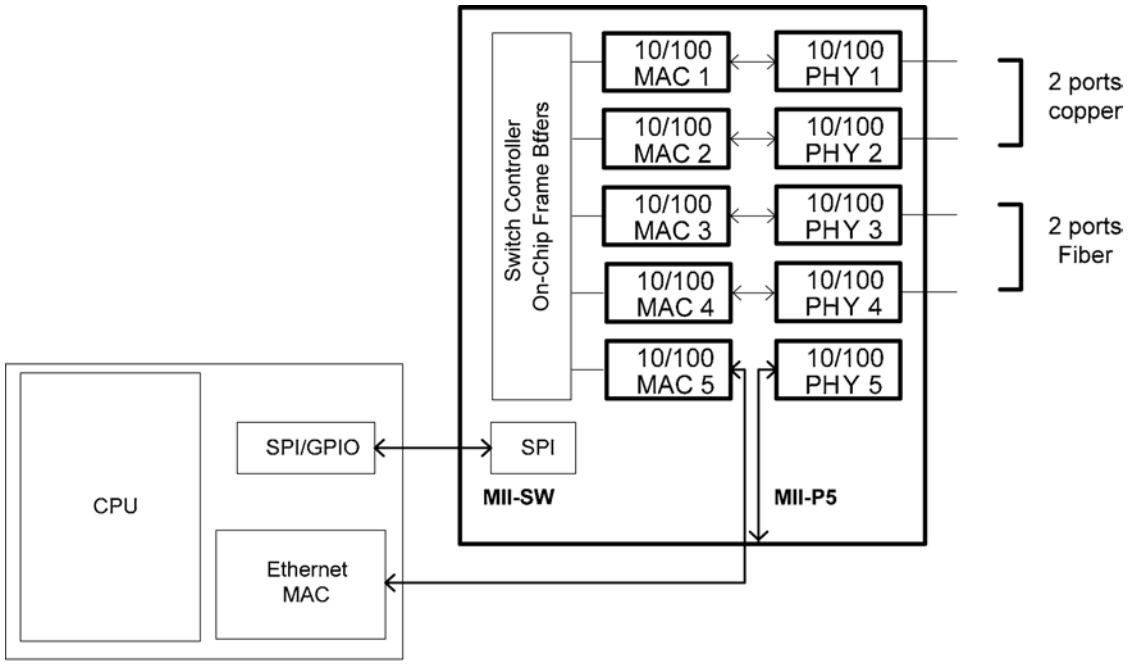

Figure 4. Using KSZ8895FMQ for Dual Media Converter

Pin Configuration

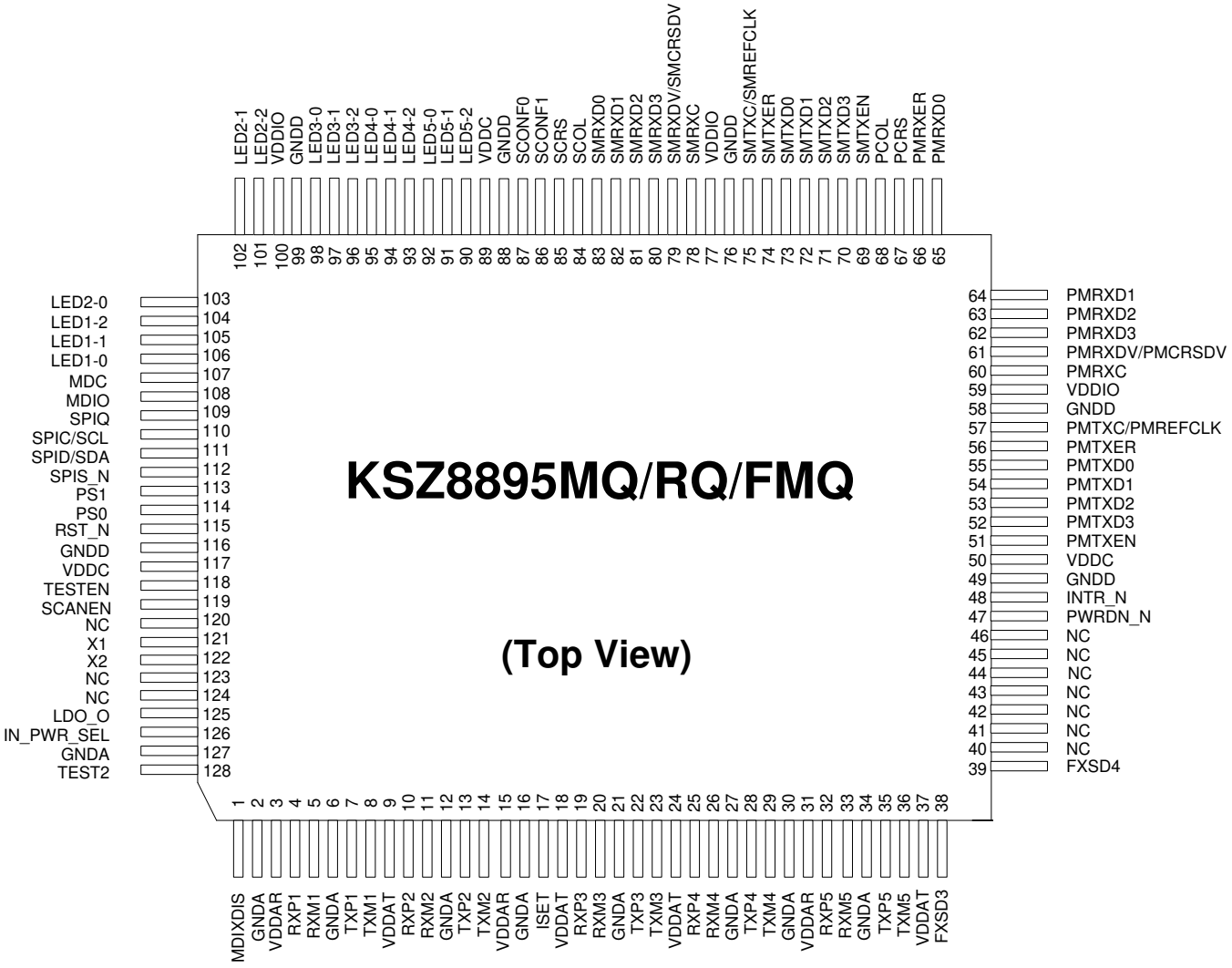

Figure 5. KSZ8895MQ/RQ/FMQ 128-Pin PQFP Pins Configuration

Pin Description

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
1	MDI-XDIS	IPD	1 – 5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GNDA	GND		Analog ground.
3	VDDAR	P		1.2V analog V_{DD}.
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal - (differential).
6	GNDA	GND		Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal - (differential).
9	VDDAT	P		3.3V analog V_{DD}.
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal - (differential).
12	GNDA	GND		Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal - (differential).
15	VDDAR	P		1.2V analog V_{DD}.
16	GNDA	GND		Analog ground.
17	ISET			Set physical transmit output current. Pull-down with a 12.4kΩ1% resistor.
18	VDDAT	P		3.3V analog V_{DD}.
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal - (differential).
21	GNDA	GND		Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
24	VDDAT	P		3.3V analog V_{DD}.
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal - (differential).
27	GNDA	GND		Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal - (differential).
30	GNDA	GND		Analog ground.
31	VDDAR	P		1.2V analog V_{DD}.
32	RXP5	I	5	Physical receive signal + (differential).
33	RXM5	I	5	Physical receive signal - (differential).
34	GNDA	GND		Analog ground.
35	TXP5	O	5	Physical transmit signal + (differential).
36	TXM5	O	5	Physical transmit signal - (differential).
37	VDDAT	P		3.3V analog V_{DD}.
38	FXSD3	IPD	3	FMQ: Fiber signal detect pin for Port 3. MQ/RQ: no connection.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
39	FXSD4	IPD	4	FMQ: Fiber signal detect pin for Port 4. MQ/RQ: no connection.
40	NC	NC		No connect.
41	NC	NC		No connect.
42	NC	NC		No connect.
43	NC	NC		No connect.
44	NC	NC		No connect.
45	NC	NC		No connect.
46	NC	NC		No connect.
47	PWRDN_N	IPU		Full-chip power down. Active low.
48	INTR_N	OPU		Interrupt. This pin is Open-Drain output pin.
49	GNDD	GND		Digital ground.
50	VDDC	P		1.2V digital core V_{DD}.
51	PMTXEN	IPD	5	PHY[5] MII/RMII transmit enable.
52	PMTXD3	IPD	5	MQ/FMQ: PHY[5] MII transmit bit 3. RQ: no connection for RMII.
53	PMTXD2	IPD	5	MQ/FMQ: PHY[5] MII transmit bit 2. RQ: no connection for RMII.
54	PMTXD1	IPD	5	PHY[5] MII/RMII transmit bit 1.
55	PMTXD0	IPD	5	PHY[5] MII/RMII transmit bit 0.
56	PMTXER	IPD	5	MQ/FMQ: PHY[5] MII transmit error. RQ: no connection for RMII.
57	PMTXC/PMREFCLK	I/O	5	MQ/FMQ: Output PHY[5] MII transmit clock RQ: Input PHY[5] RMII reference clock, 50MHz ±50ppm, the 50MHz clock comes from PMRXC Pin 60.
58	GNDD	GND		Digital ground.
59	VDDIO	P		3.3V, 2.5V or 1.8V digital V_{DD} for digital I/O circuitry.
60	PMRXC	I/O	5	MQ/FMQ: Output PHY[5] MII receive clock. RQ: Output PHY[5] RMII reference clock, this clock is used when opposite doesn't provide RMII 50MHz clock or the system doesn't provide an external 50MHz clock for the P5-RMII interface.
61	PMRXDV/PMCRSDV	IPD/O	5	MQ/FMQ: PMRXDV is for PHY[5] MII receive data valid. RQ: PMCRSDV is for PHY[5] RMII Carrier Sense/Receive Data Valid Output.
62	PMRXD3	IPD/O	5	MQ/FMQ: PHY[5] MII receive bit 3. RQ: no connection for RMII. Strap option: PD (default) = enable flow control. PU = disable flow control.
63	PMRXD2	IPD/O	5	MQ/FMQ: PHY[5] MII receive bit 2. RQ: no connection for RMII. Strap option: PD (default) = disable back pressure. PU = enable back pressure.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
64	PMRXD1	IPD/O	5	PHY[5] MII/RMII receive bit 1. Strap option: PD (default) = drop excessive collision packets. PU = does not drop excessive collision packets.
65	PMRXD0	IPD/O	5	PHY[5] MII/RMII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode. PU = enable for performance enhancement.
66	PMRXER	IPD/O	5	MQ/FMQ:PHY[5] MII receive error RQ: no connection for RMII Strap option: PD (default) = packet size 1518/1522 bytes. PU = 1536 bytes.
67	PCRS	IPD/O	5	MQ/FMQ: PHY[5] MII carrier sense. RQ: no connection for RMII. Strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
68	PCOL	IPD/O	5	MQ/FMQ: PHY[5] MII collision detect. RQ: no connection. Strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.
69	SMTXEN	IPD		Port 5 Switch MII/RMII transmit enable.
70	SMTXD3	IPD		MQ/FMQ: Port 5 Switch MII transmit bit 3. RQ: no connection for RMII.
71	SMTXD2	IPD		MQ/FMQ: Port 5 Switch MII transmit bit 2. RQ: no connection for RMII.
72	SMTXD1	IPD		Port 5 Switch MII/RMII transmit bit 1.
73	SMTXD0	IPD		Port 5 Switch MII/RMII transmit bit 0.
74	SMTXER	IPD		MQ/FMQ: Port 5 Switch MII transmit error. RQ: no connection for RMII.
75	SMTXC/SMREFCLK	I/O		MQ/FMQ: Port 5 Switch MII transmit clock, Input: SW5-MII MAC mode, Output: SW5-MII PHY modes. RQ: Input SW5-RMII 50MHz +/-50ppm reference clock. The 50MHz clock comes from SMRXC Pin 78 when the device is the clock mode which the device's clock comes from 25MHz crystal/oscillator from pins X1/X2. Or the 50MHz clock comes from external 50MHz clock source when the device is the normal mode which the device's clock source comes from SMTXC pin not from X1/X2 pins.
76	GNDD	GND		Digital ground.
77	VDDIO	P		3.3V, 2.5V or 1.8V digital V_{DD} for digital I/O circuitry.

Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Port</th><th>Pin Function(2)</th></tr>
<tr><td>78</td><td>SMRXC</td><td>I/O</td><td></td><td>MQ/FMQ: Port 5 Switch MII receive clock,
Input: SW5-MII MAC mode, Output: SW5-MII PHY mode.
RQ: Output SW5-RMII 50MHz clock, this clock is used when opposite doesn’t provide RMII reference clock or the system doesn’t provide an external 50MHz clock for the RMII interface.</td></tr>
<tr><td>79</td><td>SMRXDV/SMCRSDV</td><td>IPD/O</td><td></td><td>MQ/FMQ: SMRXDV is for Switch MAC5 MII receive data valid.
RQ: SMCRSDV is for MAC5 RMII Carrier Sense/Receive Data Valid Output.</td></tr>
<tr><td>80</td><td>SMRXD3</td><td>IPD/O</td><td></td><td>MQ/FMQ: Port 5 Switch MII receive bit 3.
RQ: no connection for RMII
Strap option:
PD (default) = Disable Switch SW5-MII full-duplex flow control
PU = Enable Switch SW5-MII full-duplex flow control.</td></tr>
<tr><td>81</td><td>SMRXD2</td><td>IPD/O</td><td></td><td>MQ/FMQ: Port 5 Switch MII receive bit 2.
RQ: no connection for RMII
Strap option:
PD (default) = Switch SW5-MII in full-duplex mode;
PU = Switch SW5-MII in half-duplex mode.</td></tr>
<tr><td>82</td><td>SMRXD1</td><td>IPD/O</td><td></td><td>Port 5 Switch MII/RMII receive bit 1.
Strap option:
PD (default) = Port 5 Switch SW5-MII in 100Mbps mode.
PU = Switch SW5-MII in 10Mbps mode.</td></tr>
<tr><td>83</td><td>SMRXD0</td><td>IPD/O</td><td></td><td>Port 5 Switch MII/RMII receive bit 0.
Strap option:
LED mode
PD (default) = mode 0; PU = mode 1. See “Register 11.”
Mode 0, link at:
100/Full LEDx[2,1,0] = 0, 0, 0
100/Half LEDx[2,1,0] = 0, 1, 0
10/Full LEDx[2,1,0] = 0, 0, 1
10/Half LEDx[2,1,0] = 0, 1, 1
Mode 1, link at:
100/Full LEDx[2,1,0] = 0, 1, 0
100/Half LEDx[2,1,0] = 0, 1, 1
10/Full LEDx[2,1,0] = 1, 0, 0
10/Half LEDx[2,1,0] = 1, 0, 1
<table>
<tr><td></td><td>Mode 0</td><td>Mode 1</td></tr>
<tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/Act</td></tr>
<tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/Act</td></tr>
<tr><td>LEDX_0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
</td></tr>
<tr><td>84</td><td>SCOL</td><td>IPD/O</td><td></td><td>MQ/FMQ: Port 5 Switch MII collision detect,
Input: SW5-MII MAC modes, Output: SW5-MII PHY modes.
RQ: no connection for RMII</td></tr>
<tr><td>85</td><td>SCRS</td><td>IPD/O</td><td></td><td>MQ/FMQ: Port 5 Switch MII modes carrier sense,
Input: SW5-MII MAC modes, Output: SW5-MII PHY modes.
RQ: no connection for RMII</td></tr>
</table>

Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Port</th><th colspan="3">Pin Function(2)</th></tr>
<tr><td rowspan="10">86</td><td rowspan="10">SCONF1</td><td rowspan="10">IPD</td><td rowspan="10"></td><td colspan="3">Pins 91, 86, and 87 are dual MII/RMII configuration pins for the Port 5 MAC5 MII/RMII and PHY[5] MII/RMII. SW5-MII supports both MAC mode and PHY modes. P5-MII supports PHY mode only. See pins configuration below.</td></tr>
<tr><td>Pin# (91, 86, 87)</td><td>Port 5 Switch MAC5 SW5-MII/RMII</td><td>Port5 PHY5 P5- MII/RMII</td></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable (default)</td><td>Disable (default)</td></tr>
<tr><td>101</td><td>PHY Mode MII or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>110</td><td>MAC Mode MII or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>P5-MII/RMII</td></tr>
<tr><td>87</td><td>SCONF0</td><td>IPD</td><td></td><td colspan="3">Dual MII/RMII configuration pin. See pin 86 descriptions.</td></tr>
<tr><td>88</td><td>GNDD</td><td>GND</td><td></td><td colspan="3">Digital ground.</td></tr>
<tr><td>89</td><td>VDDC</td><td>P</td><td></td><td colspan="3">1.2V digital core V_{DD}.</td></tr>
<tr><td>90</td><td>LED5-2</td><td>IPU/O</td><td>5</td><td colspan="3">LED indicator 2.
Strap option:
Aging setup. See “Aging” section.
PU (default) = aging enable
PD = aging disable.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>IPU/O</td><td>5</td><td colspan="3">LED indicator 1.
Strap option:
PU (default): enable PHY[5] MII I/F.
PD: tristate all PHY[5] MII output. See “Pin 86 SCONF1.”</td></tr>
<tr><td>92</td><td>LED5-0</td><td>IPU/O</td><td>5</td><td colspan="3">LED indicator 0.
Strap option for port 4 only.
PU (default) = Enable auto-negotiation.
PD = Disable auto-negatiation. Strap to register76 bit[7].</td></tr>
<tr><td>93</td><td>LED4-2</td><td>IPU/O</td><td>4</td><td colspan="3">LED indicator 2.</td></tr>
<tr><td>94</td><td>LED4-1</td><td>IPU/O</td><td>4</td><td colspan="3">LED indicator 1.</td></tr>
<tr><td>95</td><td>LED4-0</td><td>IPU/O</td><td>4</td><td colspan="3">LED indicator 0.
Strap option:
PU (default) = Normal mode.
PD = Energy Detection mode (EDPD mode)
Strap to register 14 bits[4:3]</td></tr>
<tr><td>96</td><td>LED3-2</td><td>IPU/O</td><td>3</td><td colspan="3">LED indicator 2.</td></tr>
<tr><td>97</td><td>LED3-1</td><td>IPU/O</td><td>3</td><td colspan="3">LED indicator 1.</td></tr>
<tr><td>98</td><td>LED3-0</td><td>IPU/O</td><td>3</td><td colspan="3">LED indicator 0.
Strap option:
PU (default) = Select I/O drive strength (8mA);
PD = Select I/O drive strength (12mA).
Strap to register132 bit[7-6].</td></tr>
<tr><td>99</td><td>GNDD</td><td>GND</td><td></td><td colspan="3">Digital ground.</td></tr>
</table>

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
100	VDDIO	P		3.3V, 2.5V or 1.8V digital V_{DD} for digital I/O circuitry.
101	LED2-2	IPU/O	2	LED indicator 2. Strap option for RQ only: PU (default) = Select the device as clock mode in SW5- RMII, 25MHz crystal/oscillator to X1/X2 pins of the device and pins of SMRXC and PMRXC output 50MHz clock. PD = Select the device as normal mode in SW5-RMII. Switch MAC5 used only. The input clock from X1/X2 pins is not used, the device's clock source comes from SMTXC/SMREFCLK pin which the 50MHz reference clock comes from external 50MHz clock source, PMRXC can output 50MHz clock for P5-RMII interface in the normal mode.
102	LED2-1	IPU/O	2	LED indicator 1. Strap option: for Port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negatiation. Strap to register60 bit[7].
103	LED2-0	IPU/O	2	LED indicator 0.
104	LED1-2	IPU/O	1	LED indicator 2.
105	LED1-1	IPU/O	1	LED indicator 1. Strap option: for port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to register60 bit[4].
106	LED1-0	IPU/O	1	LED indicator 0. Strap option for port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to register60 bit[5].
107	MDC	IPU	All	Switch or PHY[5] MII management (MIIM registers) data clock. Or SMI interface clock
108	MDIO	IPU/O	All	Switch or PHY[5] MII management (MIIM registers) data I/O. Or SMI interface data I/O. Features internal pull down to define pin state when not driven. Note: Need an external pull-up when driven.
109	SPIQ	IPU/O	All	SPI serial data output in SPI slave mode. Note: Need an external pull-up when driven.
110	SPIC/SCL	IPU/O	All	(1) Input clock up to 25MHz in SPI slave mode, (2) output clock at 61kHz in I^2C master mode. See "Pin 113." Note: Need an external pull-up when driven.
111	SSPID/SDA	IPU/O	All	(1) Serial data input in SPI slave mode; (2) serial data input/output in I^2C master mode. See "Pin 113." Note: Need an external pull-up when driven.
112	SPIS_N	IPU	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KSZ8895MQ/RQ/FMQ is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer. (2) not used in I^2C master mode.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
113	PS1	IPD		Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MQ/RQ/FMQ will start itself with the PS[1.0] = 00 default register values.
				Pin Configuration: Serial Bus Configuration
				PS[1.0] = 00: I^2C Master Mode for EEPROM
				PS[1.0] = 01: SMI Interface Mode
				PS[1.0] = 10: SPI Slave Mode for CPU Interface
				PS[1.0] = 11: Factory Test Mode (BIST)
114	PS0	IPD		Serial bus configuration pin. See “Pin 113.”
115	RST_N	IPU		Reset the KSZ8895MQ/RQ/FMQ device. Active low.
116	GNDD	GND		Digital ground.
117	VDDC	P		1.2V digital core V_{DD}.
118	TESTEN	IPD		NC for normal operation. Factory test pin.
119	SCANEN	IPD		NC for normal operation. Factory test pin.
120	NC	NC		No connect.
121	X1	I		25MHz crystal clock connection/or 3.3V Oscillator input. Crystal/Oscillator should be ±50ppm tolerance.
122	X2	O		25MHz crystal clock connection.
123	NC	NC		No connect.
124	NC	NC		No connect.
125	LDO_O	P		When pin126 is pull-up, the Internal 1.2V LDO controller is enabled and creates a 1.2V output when using an external FET. When pin126 is pull-down, the pin 125 is tristated. Note: Use a 200Ω (approximately) resistor between the source and drain pins on the FET if 3.3V power rail exhibits a slow ramp (>5ms) when using this internal 1.2V LDO controller. You can also use an external 1.2V LDO when 3.3V power ramp time is slow.
126	IN_PWR_SEL	I		Pull-up to enable LDO_O of pin 125. Pull-down to disable LDO_0. Note: A 4.3K pull-up and a 1K pull-down resistor divider is recommended if using the internal 1.2V LDO controller plus an external MOSFET for 1.2V power.
127	GNDA	GND		Analog ground.
128	TEST2	NC		NC for normal operation. Factory test pin.

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   IPU = Input w/internal pull-up.
   IPD = Input w/internal pull-down.
   IPD/O = Input w/internal pull-down during reset, output pin otherwise.
   IPU/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   OTRI = Output tristated.

Pin for Strap-In Options

The KSZ8895MQ/RQ/FMQ can function as a managed switch or an unmanaged switch. If no EEPROM or micro-controller exists, then the KSZ8895MQ/RQ/FMQ will operate from its default setting. The strap-in option pins can be configured by external pull-up/down resistors and take effect after power down reset or warm reset. The functions are described in the following table.

Pin #	Pin Name	PU/PD[1]	Description[1]
1	MDI-XDIS	IPD	Disable auto MDI/MDI-X. Strap option: PD = (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
62	PMRXD3	IPD/O	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
63	PMRXD2	IPD/O	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
64	PMRXD1	IPD/O	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
65	PMRXD0	IPD/O	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
66	PMRXER	IPD/O	PHY[5] MII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.
67	PCRS	IPD/O	PHY[5] MII carrier sense Strap option for Port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails. Refer to register 76.
68	PCOL	IPD/O	PHY[5] MII collision detect Strap option for Port 4 only. PD (default) = no force flow control. PU = force flow control. Refer to register 66.
80	SMRXD3	IPD/O	Switch MII receive bit 3. Strap option: PD (default) = disable switch SW5-MII full-duplex flow control; PU = enable switch SW5-MII full-duplex flow control.
81	SMRXD2	IPD/O	Switch MII receive bit 2. Strap option: PD (default) = switch SW5-MII in full-duplex mode; PU = switch SW5-MII in half-duplex mode.
82	SMRXD1	IPD/O	Switch MII receive bit 1. Strap option: PD (default) = switch SW5-MII in 100Mbps mode. PU = switch MII in 10Mbps mode.

Pin for Strap-In Options (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>PU/PD(1)</th><th>Description(1)</th></tr>
<tr><td rowspan="5">83</td><td rowspan="5">SMRXD0</td><td rowspan="5">IPD/O</td><td colspan="3">Switch MII receive bit 0.
Strap option: LED mode PD (default) = mode 0; PU = mode 1. See “Register 11.”</td></tr>
<tr><td></td><td>Mode 0</td><td>Mode 1</td></tr>
<tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/Act</td></tr>
<tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/Act</td></tr>
<tr><td>LEDX_0</td><td>Speed</td><td>Fulld</td></tr>
<tr><td rowspan="10">86</td><td rowspan="10">SCONF1</td><td rowspan="10">IPD</td><td colspan="3">Pin 91,86,87 are dual MII/RMII configuration pins for the Port 5 MAC 5 MII/RMII and PHY[5] MII/RMII. SW5-MII supports both MAC mode and PHY modes. P5-MII supports PHY mode only. See pins configuration below.</td></tr>
<tr><td>Pins [91, 86, 87]</td><td>Port 5 MAC 5 Switch SW5-MII</td><td>Port 5 PHY [5] MII/RMII P5-MII/RMII</td></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII or RMII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII or RMII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable</td><td>Disable</td></tr>
<tr><td>101</td><td>PHY Mode MII or RMII</td><td>P5- MII/RMII</td></tr>
<tr><td>110</td><td>MAC Mode MII or RMII</td><td>P5- MII/RMII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>P5- MII/RMII</td></tr>
<tr><td>87</td><td>SCONF0</td><td>IPD</td><td colspan="3">Dual MII/RMII configuration pin. See pin 86 description.</td></tr>
<tr><td>90</td><td>LED5-2</td><td>IPU/O</td><td colspan="3">LED5 indicator 2.
Strap option: Aging setup. See “Aging” section
PU (default) = aging enable;
PD = aging disable.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>IPU/O</td><td colspan="3">LED5 indicator 1.
Strap option:
PU (default): enable PHY[5] MII I/F.
PD: tristate all PHY[5] MII output. See “Pin 86 SCONF1.”</td></tr>
<tr><td>92</td><td>LED5-0</td><td>IPU/O</td><td colspan="3">LED5 indicator 0.
Strap option for Port 4 only.
PU (default) = Enable auto-negotiation.
PD = Disable auto-negatiation. Strap to register76 bit[7].</td></tr>
<tr><td>95</td><td>LED4-0</td><td>IPU/O</td><td colspan="3">LED indicator 0.
Strap option:
PU (default) = Normal mode.
PD = Energy Detection mode (EDPD mode).
Strap to register 14 bits[4:3].</td></tr>
<tr><td>98</td><td>LED3-0</td><td>IPU/O</td><td colspan="3">LED3 indicator 0.
Strap option:
PU (default) = Select I/O current drive strength (8mA);
PD = Select I/O current drive strength (12mA).
Strap to register132 bit[7:6].</td></tr>
</table>

Pin for Strap-In Options (Continued)

Pin #	Pin Name	PU/PD[1]	Description[1]	
101	LED2-2	IPU/O	LED2 indicator 2. Strap option for KSZ8895RQ only: PU (default) = Select the device as clock mode in RQ SW5- RMII, 25MHz crystal to X1/X2 pins of the device and REFCLK output 50MHz clock. PD = Select the device as normal mode in SW5-RMII. Switch MAC5 used only. The input clock is useless from X1/X2 pin, the device's clock comes from SMTXC/SMREFCLK pin, 50MHz reference clock from external 50MHz clock source.	
102	LED2-1	IPU/O	LED2 indicator 1. Strap option for Port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negatiation. Strap to register60 bit[7].	
105	LED1-1	IPU/O	LED1 indicator 1. Strap option for Port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to register50 bit[4].	
106	LED1-0	IPU/O	LED1 indicator 0. Strap option for Port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to register60 bit[5].	
113	PS1	IPD	Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MQ/RQ/FMQ will start itself with the PS[1:0] = 00 default register values .	
			Pin Configuration	**Serial Bus Configuration**
			PS[1:0] = 00	I^2C Master Mode for EEPROM
			PS[1:0] = 01	SMI Interface Mode
			PS[1:0] = 10	SPI Slave Mode for CPU Interface
			PS[1:0] = 11	Factory Test Mode (BIST)
114	PS0	IPD	Serial bus configuration pin. See "Pin 113."	
128	TEST2	NC	NC for normal operation. Factory test pin.	

Note:

1. NC = No connect.
   IPD = Input w/internal pull-down.
   IPD/O = Input w/internal pull-down during reset, output pin otherwise.
   IPU/O = Input w/internal pull-up during reset, output pin otherwise.