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KSZ8895MLU

Integrated 5-Port 10/100 Managed Switch

Revision 1.2

General Description

The KSZ8895MLU is a highly-integrated Layer 2-managed 5-port switch with an optimized design and plentiful features, qualified to meet AEC-Q100 standard for automotive applications. It is designed for cost-sensitive 10/100Mbps 5-port switch systems with on-chip termination, lowest power consumption and internal core power controller. These features will save more system cost. It has 1.4Gbps high-performance memory bandwidth, shared memory based switch fabric with full non-blocking configuration. It also provides an extensive feature set such as power management, programmable rate limit and priority ratio, tag/port-based VLAN, packets filtering, quality-of-service (QoS) four-queue prioritization, management interface, and MIB counters. Port 5 is a MAC 5 MII interface with PHY mode as default at switch side. The SW5-MII interface can be connected to a processor with a MAC MII interface.

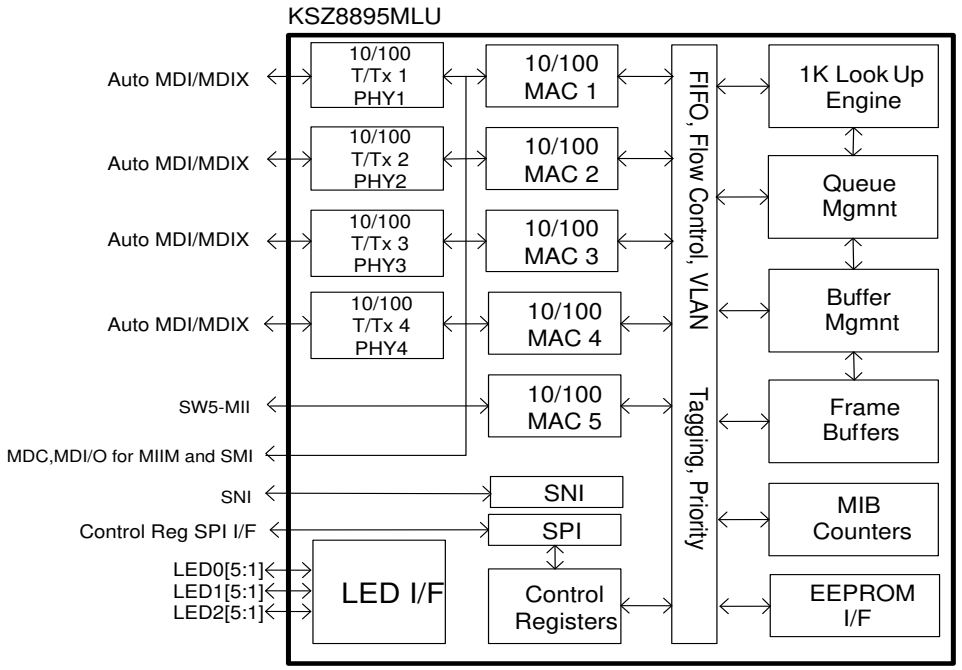
The KSZ8895MLU consists of 10/100 PHYs with patented and enhanced mixed-signal technology, media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory. The KSZ8895MLU contains five MACs and four integrated PHYs. All PHYs support 10/100Base-T/TX.

All registers of MACs and PHYs units can be managed by the SPI interface or the SMI interface. MIIM registers of the PHYs can be accessed through the MDC/MDIO interface. EEPROM can set all control registers for the unmanaged mode.

The KSZ8895MLU provides multiple CPU control/data interfaces to effectively address both current and emerging fast Ethernet applications.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Functional Diagram



Features

Advanced Switch Features

- IEEE 802.1q VLAN support for up to 128 VLAN groups (full-range 4096 of VLAN IDs).
- Static MAC table supports up to 32 entries.
- VLAN ID tag/untag options, per port basis.
- IEEE 802.1p/q tag insertion or removal on a per port basis based on ingress port (egress).
- Programmable rate limiting at the ingress and egress on a per port basis.
- Jitter-free per packet based rate-limiting support.
- Broadcast storm protection with percentage control (global and per port basis).
- IEEE 802.1d rapid spanning tree protocol RSTP support.
- Tail tag mode (1byte added before FCS) support at Port 5 to inform the processor which ingress port receives the packet.
- 1.4Gbps high-performance memory bandwidth and shared memory-based switch fabric with fully non-blocking configuration.
- MII with MAC 5 on Port 5, SW5-MII for MAC 5 MII interface.
- Enable/Disable option for huge frame size up to 2000 bytes per frame.
- IGMP v1/v2 snooping (Ipv4) support for multicast packet filtering.
- IPv4/IPv6 QoS support.
- Support unknown unicast/multicast address and unknown VID packet filtering.
- Self-address filtering.

Comprehensive Configuration Register Access

- Serial management interface (MDC/MDIO) to all PHYs registers and SMI interface (MDC/MDIO) to all registers.
- High-speed SPI (up to 25MHz) and I^2C master Interface to all internal registers.
- I/0 pins strapping and EEPROM to program selective registers in unmanaged switch mode.
- Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…).

QoS/CoS Packet Prioritization Support

- Per port, 802.1p and DiffServ-based.
- 1/2/4-queue QoS prioritization selection.
- Programmable weighted fair queuing for ratio control.
- Re-mapping of 802.1p priority field per port basis.

Integrated 5-Port 10/100 Ethernet Switch

- New generation switch with five MACs and five PHYs fully compliant with IEEE 802.3u standard.
- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K MAC address lookup table and a store-and-forward architecture.
- New generation switch with five MACs and five PHYs fully compliant with IEEE 802.3u standard.
- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K MAC address lookup table and a store-and-forward architecture.
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table).
- Full duplex IEEE 802.3x flow control (PAUSE) with force mode option.
- Half-duplex back pressure flow control.
- HP Auto MDI/MDI-X and IEEE Auto crossover support.
- Port 5 MAC5 SW5-MII interface supports PHY mode and MAC mode.
- 7-wire serial network interface (SNI) support for legacy MAC.
- Per port LED Indicators for link, activity, and 10/100 speed.
- Register port status support for link, activity, full/half duplex and 10/100 speed.
- On-chip terminations and internal biasing technology for cost down and lowest power consumption.

Switch Monitoring Features

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII.
- MIB counters for fully-compliant statistics gathering 34 MIB counters per port.
- Loop-back support for MAC, PHY, and remote diagnostic of failure.
- Interrupt for the link change on any ports.

Low Power Dissipation

- Full-chip hardware power-down.
- Full-chip software power-down/per port software power down.
- Energy-detect mode support <100mW full-chip power consumption when all ports have no activity.
- Very-low, full-chip power consumption (<0.5W), without extra power consumption on transformers.
- Dynamic clock-tree shutdown feature.
- Voltages: Single 3.3V supply with 3.3V VDDIO and Internal 1.2V LDO controller enabled or external 1.2V LDO solution:
  - Analog VDDAT 3.3V only
  - VDDIO support 3.3V, 2.5V, and 1.8V
  - Low 1.2V core power
- 0.13um CMOS technology
- Industrial Temperature Range: –40°C to +85°C.
- Available in 128-pin LQFP, lead-free package.

Applications

- In-vehicle diagnostics (OBD)
- High-speed software download
- Gateway switch
- Head unit
- Rear seat entertainment

Ordering Information

Part Number	Temperature Range	Package	Lead Finish/Grade
KSZ8895MLU (Automotive Grade)	–40°C to +85°C	128-Pin LQFP	Pb-Free/Automotive
KSZ8895MLU-EVAL Board	Evaluation Board for KSZ8895MLU		

Revision History

Revision	Date	Summary of Changes
1.0	03/16/11	Initial
1.1	09/27/11	Update some descriptions, updates for descriptions of SMI mode and IGMP mode, update register default values, pins type and some parameters.
1.2	04/28/14	Updates timing data for MII PHY mode. Update descriptions for VLAN table and I2C master mode. Update the equation in the broadcast storm protection section. Update the operation rating to ±5% and TTL min/max I/O voltage in different VDDIO. Change I/O from TTL to CMOS. Update SPI description from 127 to 255 for all registers. Update the table of tail tag rules. Update description for Register 1 bits [7:4]. Update table 8 from bit [57:55] to bit [58:56]. Update the port register control 2 bit [6] description bits [20:16] change to bits [11:7]. Add evaluation Board in the ordering information table. Remove port 5 in the pin configuration and pin description. Update notes description for pin 125 and pin 126 in the pins descriptions. Update operating rating and correct typos.

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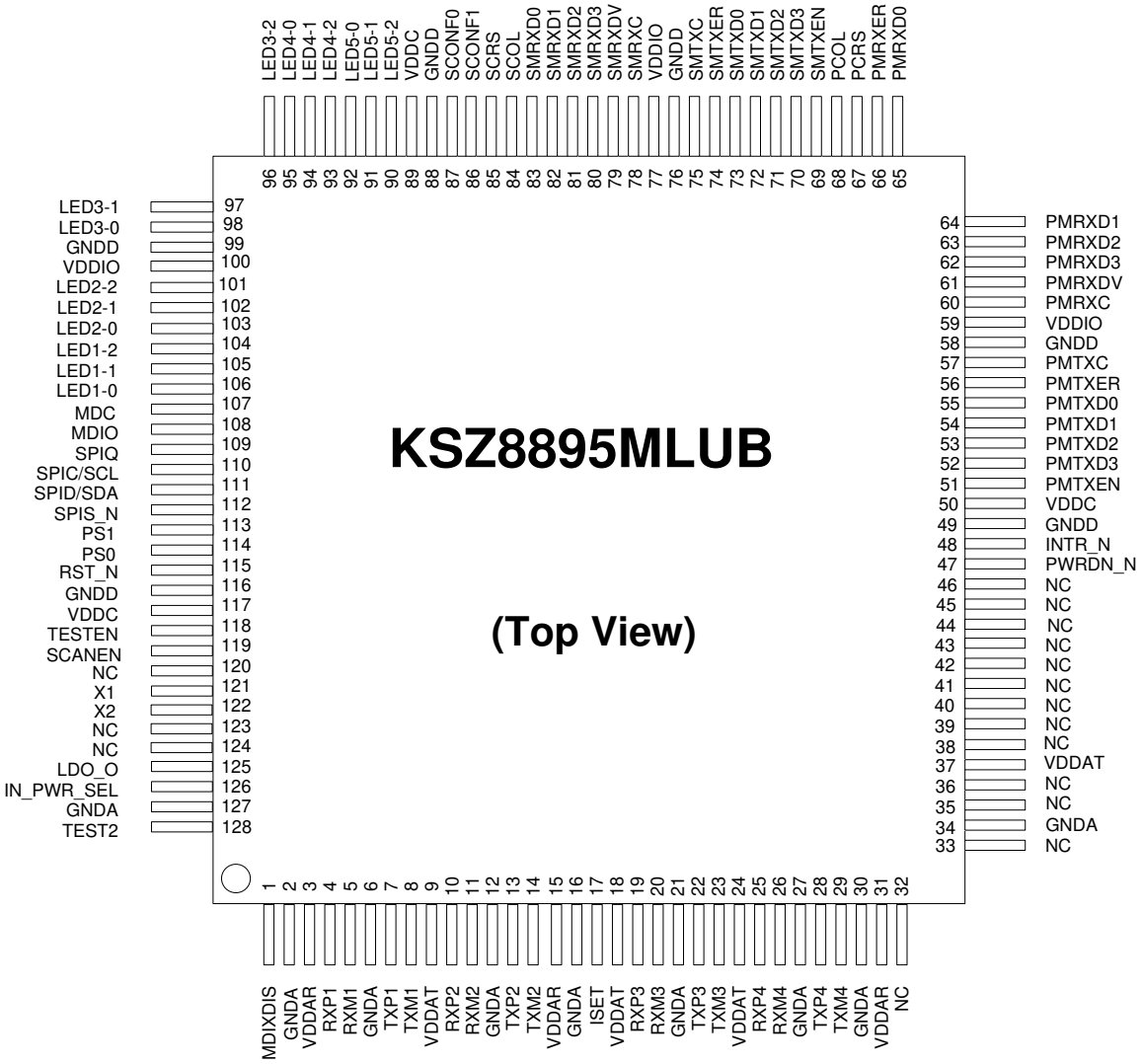
Pin Configuration



128-Pin LQFP

Pin Description

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
1	MDI-XDIS	Ipd	1 – 5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GNDA	GND		Analog ground.
3	VDDAR	P		1.2V analog V_{DD}.
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal – (differential).
6	GNDA	GND		Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal – (differential).
9	VDDAT	P		3.3V analog V_{DD}.
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal – (differential).
12	GNDA	GND		Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
15	VDDAR	P		1.2V analog V_{DD}.
16	GNDA	GND		Analog ground.
17	ISET			Set physical transmit output current. Pull-down with a 12.4kΩ1% resistor.
18	VDDAT	P		3.3V analog V_{DD}.
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal - (differential).
21	GNDA	GND		Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
24	VDDAT	P		3.3V analog V_{DD}.
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal - (differential).
27	GNDA	GND		Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
30	GNDA	GND		Analog ground.
31	VDDAR	P		1.2V analog V_{DD}.
32	NC	NC		No connect.
33	NC	NC		No connect.
34	GNDA	GND		Analog ground.
35	NC	NC		No connect.
36	NC	NC		No connect.
37	VDDAT	P		3.3V analog V_{DD}.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
38	NC	NC		No connect.
39	NC	NC		No connect.
40	NC	NC		No connect.
41	NC	NC		No connect.
42	NC	NC		No connect.
43	NC	NC		No connect.
44	NC	NC		No connect.
45	NC	NC		No connect.
46	NC	NC		No connect.
47	PWRDN_N	Ipu		Full-chip power down. Active low.
48	INTR_N	Opu		Interrupt. This pin is open-drain output pin.
49	GNDD	GND		Digital ground.
50	VDDC	P		1.2V digital core V_{DD}.
51	PMTXEN	Ipd	5	Reserved for MLU. No connect.
52	PMTXD3	Ipd	5	Reserved for MLU. No connect.
53	PMTXD2	Ipd	5	Reserved for MLU. No connect.
54	PMTXD1	Ipd	5	Reserved for MLU. No connect.
55	PMTXD0	Ipd	5	Reserved for MLU. No connect.
56	PMTXER	Ipd	5	Reserved for MLU. No connect.
57	PMTXC	I/O	5	Reserved for MLU. No connect.
58	GNDD	GND		Digital ground.
59	VDDIO	P		3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry.
60	PMRXC	I/O	5	Reserved for MLU. No connect.
61	PMRXDV	Ipd/O	5	Reserved for MLU. No connect.
62	PMRXD3	Ipd/O	5	Reserved for MLU. Strap option: PD (default) = enable flow control. PU = disable flow control.
63	PMRXD2	Ipd/O	5	Reserved for MLU. Strap option: PD (default) = disable back pressure. PU = enable back pressure.
64	PMRXD1	Ipd/O	5	Reserved for MLU. Strap option: PD (default) = drop excessive collision packets. PU = does not drop excessive collision packets.
65	PMRXD0	Ipd/O	5	Reserved for MLU. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode. PU = enable for performance enhancement.
66	PMRXER	Ipd/O	5	Reserved for MLU. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
67	PCRS	Ipd/O	5	Reserved for MLU. Strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
68	PCOL	Ipd/O	5	Reserved for MLU. Strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.
69	SMTXEN	Ipd		Port 5 Switch MII transmit enable.
70	SMTXD3	Ipd		Port 5 Switch MII transmit bit 3.
71	SMTXD2	Ipd		Port 5 Switch MII transmit bit 2.
72	SMTXD1	Ipd		Port 5 Switch MII transmit bit 1.
73	SMTXD0	Ipd		Port 5 Switch MII transmit bit 0.
74	SMTXER	Ipd		Port 5 Switch MII transmit error.
75	SMTXC	I/O		Port 5 Switch MII transmit clock: Input: SW5-MII MAC mode. Output: SW5-MII PHY modes.
76	GNDD	GND		Digital ground.
77	VDDIO	P		3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry.
78	SMRXC	I/O		Port 5 Switch MII receive clock: Input: SW5-MII MAC mode. Output: SW5-MII PHY mode.
79	SMRXDV	Ipd/O		Switch MII receive data valid.
80	SMRXD3	Ipd/O		Port 5 Switch MII receive bit 3. Strap option: PD (default) = Disable Switch SW5-MII full-duplex flow control PU = Enable Switch SW5-MII full-duplex flow control.
81	SMRXD2	Ipd/O		Port 5 Switch MII receive bit 2. Strap option: PD (default) = Switch SW5-MII in full-duplex mode; PU = Switch SW5-MII in half-duplex mode.
82	SMRXD1	Ipd/O		Port 5 Switch MII receive bit 1. Strap option: PD (default) =Port 5 Switch SW5-MII in 100Mbps mode; SW5-TMII in 200Mbps mode. PU = Switch SW5-MII in 10Mbps mode.
83	SMRXD0	Ipd/O		Port 5 Switch MII receive bit 0. Strap option: LED mode PD (default) = mode 0; PU = mode 1. See “Register 11.” Mode 0, link at 100/Full LEDx[2,1,0]=0,0,0 100/Half LEDx[2,1,0]=0,1,0 10/Full LEDx[2,1,0]=0,0,1 10/Half LEDx[2,1,0]=0,1,1 Mode 1, link at 100/Full LEDx[2,1,0]=0,1,0 100/Half LEDx[2,1,0]=0,1,1 10/Full LEDx[2,1,0]=1,0,0 10/Half LEDx[2,1,0]=1,0,1

	Mode 0	Mode 1
LEDX_2	Lnk/Act	100Lnk/Act
LEDX_1	Fulld/Col	10Lnk/Act
LEDX_0	Speed	Full duplex

84	SCOL	Ipd/O		Port 5 Switch MII collision detect: Input: SW5-MII MAC modes. Output: SW5-MII PHY modes.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]	
85	SCRS	Ipd/O		Port 5 Switch MII modes carrier sense: Input: SW5-MII MAC modes. Output: SW5-MII PHY modes.	
86	SCONF1	Ipd		Pin 91,86,87 are dual MII configuration pins for the Port5 MAC5 MII. SW5-MII supports both MAC mode and PHY modes.	
				Pin#: (91, 86, 87)	**Port5 Switch MAC5 SW5- MII**
				000	Disable, Otri
				001	PHY Mode MII
				010	MAC Mode MII
				011	PHY Mode SNI
				100	Disable (Default)
				101	PHY Mode MII
				110	MAC Mode MII
				111	PHY Mode SNI
87	SCONF0	Ipd		Dual MII configuration pin. See pin 86 descriptions.	
88	GNDD	GND		Digital ground.	
89	VDDC	P		1.2V digital core V_{DD}.	
90	LED5-2	Ipu/O	5	Reserved for MLU Strap option: aging setup. See “Aging” section. PU (default) = Aging enable PD = Aging disable.	
91	LED5-1	Ipu/O	5	Reserved for MLU Strap option: PU (default): enable PHY[5] MII I/F. PD: tristate and disable all PHY[5] MII output. (Design should pull this pin down as default for MLU.	
92	LED5-0	Ipu/O	5	Reserved for MLU Strap option for port 4 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to register76 bit[7].	
93	LED4-2	Ipu/O	4	LED indicator 2.	
94	LED4-1	Ipu/O	4	LED indicator 1.	
95	LED4-0	Ipu/O	4	LED indicator 0. Strap option: PU (default) = Normal mode. PD = Energy Detection mode (EDPD mode). Strap to register 14 bits[4:3]	
96	LED3-2	Ipu/O	3	LED indicator 2.	
97	LED3-1	Ipu/O	3	LED indicator 1.	
98	LED3-0	Ipu/O	3	LED indicator 0. Strap option: PU (default) = Select I/O drive strength (8mA); PD = Select I/O drive strength (12mA). Strap to register132 bit[7-6].	
99	GNDD	GND		Digital ground.	
100	VDDIO	P		3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry.	
101	LED2-2	Ipu/O	2	LED indicator 2.	

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
102	LED2-1	Ipu/O	2	LED indicator 1. Strap option: for port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to register60 bit[7].
103	LED2-0	Ipu/O	2	LED indicator 0.
104	LED1-2	Ipu/O	1	LED indicator 2.
105	LED1-1	Ipu/O	1	LED indicator 1. Strap option: for port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to register60 bit[4].
106	LED1-0	Ipu/O	1	LED indicator 0. Strap option for port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to register60 bit[5].
107	MDC	Ipu	All	Switch MII management data clock. Or SMI interface clock.
108	MDIO	Ipu/O	All	Switch MII management data I/O. Or SMI interface data I/O. Features internal pull down to define pin state when not driven. Need an external pull-up when driven.
109	SPIQ	Ipu/O	All	SPI serial data output in SPI slave mode.
110	SPIC/SCL	Ipu/O	All	SPI slave mode: clock input (1) Input clock up to 25MHz in SPI slave mode, (2) output clock at 61kHz in I^2C master mode. See “Pin 113.”
111	SSPID/SDA	Ipu/O	All	SPI slave mode: serial data input. (1) Serial data input in SPI slave mode; (2) Serial data input/output in I^2C master mode. See “Pin 113.”
112	SPIS_N	Ipu	All	SPI slave mode: chip select (active low). (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KSZ8895MLU is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer. (2) not used in I^2C master mode.
113	PS1	Ipd		Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MLU will start itself with the PS[1.0] = 00 default register values.
				Pin Configuration / **Serial Bus Configuration**
				PS[1.0]=00 / I^2C Master Mode for EEPROM
				PS[1.0]=01 / SMI Interface Mode
				PS[1.0]=10 / SPI Slave Mode for CPU Interface
				PS[1.0]=11 / Factory Test Mode (BIST)
114	PS0	Ipd		Serial bus configuration pin. See “Pin 113.”
115	RST_N	Ipu		Reset the KSZ8895MLU device. Active low.
116	GNDD	GND		Digital ground.
117	VDDC	P		1.2V digital core V_{DD}.
118	TESTEN	Ipd		NC for normal operation. Factory test pin.
119	SCANEN	Ipd		NC for normal operation. Factory test pin.
120	NC	NC		No connect.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
121	X1	I		25MHz crystal clock connection/or 3.3V Oscillator input. Crystal/Oscillator should be ±50ppm tolerance.
122	X2	O		25MHz crystal clock connection.
123	NC	NC		No connect.
124	NC	NC		No connect.
125	LDO_O	P		LDO_O pin connect to Gate pin of MOSFET if using the internal 1.2V LDO controller. LDO_O pin will be floating if using an external 1.2V LDO. Note: When pin126 voltage is greater than the internal 1.2V LDO controller enable threshold (0.58V), the Internal 1.2V LDO controller is enabled and creates a 1.2V output when using an external MOSFET. When pin126 is pull-down, the internal 1.2V LDO controller is disabled and pin 125 tri-stated.
126	IN_PWR_SEL	I		Pull-up or a Resistor divider: Enable internal 1.2V LDO controller. Pull-down: Disable internal 1.2V LDO controller. Note: A 4.3K pull-up and a 1K pull-down resistors divider network is recommended if using the internal 1.2V LDO controller and an external MOSFET for 1.2V power. A 100Ω (approximately) resistor between the source and drain pins on the MOSFET is highly recommended as well. You can also use an external 1.2V LDO for 1.2V power supply.
127	GNDA	GND		Analog ground.
128	TEST2	NC		NC for normal operation. Factory test pin.

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   OTRI = Output tristated.

Pin for Strap-In Options

The KSZ8895MLU can function as a managed switch or unmanaged switch. If no EEPROM or microcontroller exists, the KSZ8895MLU will operate from its default setting. The strap-in option pins can be configures by external pull-up/down resistors and take the effect after power-down reset or warm reset, the functions are described in the following tables.

Pin Number	Pin Name	PU/PD[1]	Description[2]
1	MDI-XDIS	Ipd	Disable auto MDI/MDI-X. PD = (default) = normal operation PU = disable auto MDI/MDI-X on all ports.
62	PMRXD3	Ipd/O	Strap option: PD (default) = enable flow control; PU = disable flow control.
63	PMRXD2	Ipd/O	Strap option: PD (default) = disable back pressure; PU = enable back pressure.
64	PMRXD1	Ipd/O	Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
65	PMRXD0	Ipd/O	Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
66	PMRXER	Ipd/O	Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.
67	PCRS	Ipd/O	Strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails. Refer to register 76.
68	PCOL	Ipd/O	Strap option for port 4 only. PD (default) = no force flow control. PU = force flow control. Refer to register 66.
80	SMRXD3	Ipd/O	Switch MII receive bit 3. Strap option: PD (default) = disable switch SW5-MII full-duplex flow control; PU = enable switch SW5-MII full-duplex flow control.
81	SMRXD2	Ipd/O	Switch MII receive bit 2. Strap option: PD (default) = switch SW5-MII in full-duplex mode; PU = switch SW5-MII in half-duplex mode.
82	SMRXD1	Ipd/O	Switch MII receive bit 1. Strap option: PD (default) = switch SW5-MII in 100Mbps mode and SW5-TMII in 200Mbps PU = switch MII in 10Mbps mode.
83	SMRXD0	Ipd/O	Switch MII receive bit 0. Strap option: LED mode PD (default) = mode 0; PU = mode 1. See “Register 11.”

	Mode 0	Mode 1
LEDX_2	Lnk/Act	100Lnk/Act
LEDX_1	Fulld/Col	10Lnk/Act
LEDX_0	Speed	Fulld

Pin for Strap-In Options (Continued)

Pin Number	Pin Name	PU/PD[1]	Description[2]	
86	SCONF1	Ipd	Pins 91, 86, 87 are dual MII configuration pins for the Port5 MAC5 MII. SW5-MII supports both MAC mode and PHY modes.	
			Pin#: (91, 86, 87)	**Port5 Switch MAC5 SW5- MII**
			000	Disable, Otri
			001	PHY Mode MII
			010	MAC Mode MII
			011	PHY Mode SNI
			100	Disable
			101	PHY Mode MII
			110	MAC Mode MII
			111	PHY Mode SNI
87	SCONF0	Ipd	Dual MII configuration pin. See pin 86 descriptions.	
90	LED5-2	Ipu/O	Strap option: Aging setup. See “Aging” section PU (default) = aging enable; PD = aging disable.	
91	LED5-1	Ipu/O	Strap option: PU (default): enable PHY[5] MII I/F. PD: tristate all PHY[5] MII output. See “Pin 86 SCONF1.”	
92	LED5-0	Ipu/O	Strap option for port 4 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to register76 bit[7]	
95	LED4-0	Ipu/O	LED indicator 0. Strap option: PU (default) = Normal mode. PD = Energy Detection mode (EDPD mode). Strap to register 14 bits[4:3]	
98	LED3-0	Ipu/O	LED3 indicator 0. Strap option: PU (default) = Select I/O current drive strength (8mA); PD = Select I/O current drive strength (12mA). Strap to register132 bit[7:6].	
102	LED2-1	Ipu/O	LED2 indicator 1. Strap option for port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to register60 bit[7]	
105	LED1-1	Ipu/O	LED1 indicator 1. Strap option for port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to register50 bit[4]	

Pin for Strap-In Options (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>PU/PD(1)</th><th colspan="2">Description(2)</th></tr>
<tr><td>106</td><td>LED1-0</td><td>Ipu/O</td><td colspan="2">LED1 indicator 0.
Strap option for port 3 only.
PU (default) = force half-duplex if auto-negotiation is disabled or fails.
PD = force full-duplex if auto negotiation is disabled or fails.
Strap to register60 bit[5].</td></tr>
<tr><td rowspan="6">113</td><td rowspan="6">PS1</td><td rowspan="6">Ipd</td><td colspan="2">Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MLU will start itself with the PS[1:0] =00 default register values.</td></tr>
<tr><td>Pin Configuration</td><td>Serial Bus Configuration</td></tr>
<tr><td>PS[1:0]=00</td><td>I^2C Master Mode for EEPROM</td></tr>
<tr><td>PS[1:0]=01</td><td>SMI Interface Mode</td></tr>
<tr><td>PS[1:0]=10</td><td>SPI Slave Mode for CPU Interface</td></tr>
<tr><td>PS[1:0]=11</td><td>Factory Test Mode (BIST)</td></tr>
<tr><td>114</td><td>PS0</td><td>Ipd</td><td colspan="2">Serial bus configuration pin. See “Pin 113.”</td></tr>
</table>

Notes:

1. Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.

Introduction

The KSZ8895MLU contains four 10/100 physical layer transceivers and five media access control (MAC) units with an integrated Layer 2 managed switch. The device runs in two modes. The first mode is as a 4-port integrated switch. The second is as a 4-port switch with the fifth MAC. In this mode, access to the fifth MAC is provided through a media independent interface (MII).

The KSZ8895MLU has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the KSZ8895MLU via the SPI bus, or via the MDC/MDIO interface with SMI mode. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KSZ8895MLU supports IEEE 802.3 10BASE-T, 100BASE-TX on all ports with Auto MDI/MDIX. The KSZ8895MLU can be used as fully-managed 4-port standalone switch or hook up to microprocessor by its SW-MII interface for an application solution.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

There are a number of major enhancements from the KS8995MA to the KSZ8895MLU. These include: more host interface options, four queues prioritization, tag as well as port based VLAN, rapid spanning tree support, IGMP snooping support, port mirroring support and more flexible rate limiting and filtering functionality.

Physical Layer Transceiver

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 12.4kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KSZ8895MLU generates 125MHz, 83MHz, 41MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator.

Scrambler/De-Scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

10BASE-T Transmit

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.