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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





KSZ8895MLU

Integrated 5-Port 10/100 Managed Switch

Revision 1.2

General Description

The KSZ8895MLU is a highly-integrated Layer 2-managed 5-port switch with an optimized design and plentiful features, qualified to meet AEC-Q100 standard for automotive applications. It is designed for cost-sensitive 10/100Mbps 5-port switch systems with on-chip termination, lowest power consumption and internal core power controller. These features will save more system cost. It has 1.4Gbps high-performance memory bandwidth, shared memory based switch fabric with full non-blocking configuration. It also provides an extensive feature set such as power management, programmable rate limit and priority ratio, tag/port-based VLAN, packets filtering, quality-of-service (QoS) four-queue prioritization, management interface, and MIB counters. Port 5 is a MAC 5 MII interface with PHY mode as default at switch side. The SW5-MII interface can be connected to a processor with a MAC MII interface.

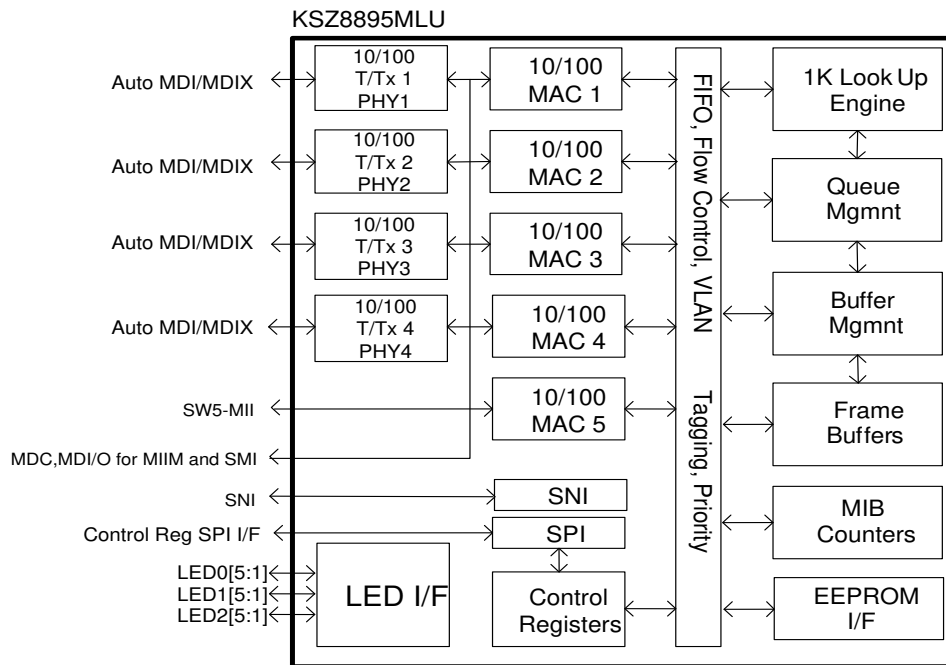
The KSZ8895MLU consists of 10/100 PHYs with patented and enhanced mixed-signal technology, media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory. The KSZ8895MLU contains five MACs and four integrated PHYs. All PHYs support 10/100Base-T/TX.

All registers of MACs and PHYs units can be managed by the SPI interface or the SMI interface. MIIM registers of the PHYs can be accessed through the MDC/MDIO interface. EEPROM can set all control registers for the unmanaged mode.

The KSZ8895MLU provides multiple CPU control/data interfaces to effectively address both current and emerging fast Ethernet applications.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Functional Diagram



Features

Advanced Switch Features

- IEEE 802.1q VLAN support for up to 128 VLAN groups (full-range 4096 of VLAN IDs).
- Static MAC table supports up to 32 entries.
- VLAN ID tag/untag options, per port basis.
- IEEE 802.1p/q tag insertion or removal on a per port basis based on ingress port (egress).
- Programmable rate limiting at the ingress and egress on a per port basis.
- Jitter-free per packet based rate-limiting support.
- Broadcast storm protection with percentage control (global and per port basis).
- IEEE 802.1d rapid spanning tree protocol RSTP support.
- Tail tag mode (1byte added before FCS) support at Port 5 to inform the processor which ingress port receives the packet.
- 1.4Gbps high-performance memory bandwidth and shared memory-based switch fabric with fully non-blocking configuration.
- MII with MAC 5 on Port 5, SW5-MII for MAC 5 MII interface.
- Enable/Disable option for huge frame size up to 2000 bytes per frame.
- IGMP v1/v2 snooping (Ipv4) support for multicast packet filtering.
- IPv4/IPv6 QoS support.
- Support unknown unicast/multicast address and unknown VID packet filtering.
- Self-address filtering.

Comprehensive Configuration Register Access

- Serial management interface (MDC/MDIO) to all PHYs registers and SMI interface (MDC/MDIO) to all registers.
- High-speed SPI (up to 25MHz) and I²C master Interface to all internal registers.
- I/O pins strapping and EEPROM to program selective registers in unmanaged switch mode.
- Control registers configurable on the fly (port-priority, 802.1p/d/q, AN...).

QoS/CoS Packet Prioritization Support

- Per port, 802.1p and DiffServ-based.
- 1/2/4-queue QoS prioritization selection.
- Programmable weighted fair queuing for ratio control.
- Re-mapping of 802.1p priority field per port basis.

Integrated 5-Port 10/100 Ethernet Switch

- New generation switch with five MACs and five PHYs fully compliant with IEEE 802.3u standard.
- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K MAC address lookup table and a store-and-forward architecture.
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- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K MAC address lookup table and a store-and-forward architecture.
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table).
- Full duplex IEEE 802.3x flow control (PAUSE) with force mode option.
- Half-duplex back pressure flow control.
- HP Auto MDI/MDI-X and IEEE Auto crossover support.
- Port 5 MAC5 SW5-MII interface supports PHY mode and MAC mode.
- 7-wire serial network interface (SNI) support for legacy MAC.
- Per port LED Indicators for link, activity, and 10/100 speed.
- Register port status support for link, activity, full/half duplex and 10/100 speed.
- On-chip terminations and internal biasing technology for cost down and lowest power consumption.

Switch Monitoring Features

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII.
- MIB counters for fully-compliant statistics gathering 34 MIB counters per port.
- Loop-back support for MAC, PHY, and remote diagnostic of failure.
- Interrupt for the link change on any ports.

Low Power Dissipation

- Full-chip hardware power-down.
- Full-chip software power-down/per port software power down.
- Energy-detect mode support <100mW full-chip power consumption when all ports have no activity.
- Very-low, full-chip power consumption (<0.5W), without extra power consumption on transformers.
- Dynamic clock-tree shutdown feature.
- Voltages: Single 3.3V supply with 3.3V VDDIO and Internal 1.2V LDO controller enabled or external 1.2V LDO solution:
 - Analog VDDAT 3.3V only
 - VDDIO support 3.3V, 2.5V, and 1.8V
 - Low 1.2V core power
- 0.13um CMOS technology
- Industrial Temperature Range: -40°C to +85°C.
- Available in 128-pin LQFP, lead-free package.

Applications

- In-vehicle diagnostics (OBD)
- High-speed software download
- Gateway switch
- Head unit
- Rear seat entertainment

Ordering Information

Part Number	Temperature Range	Package	Lead Finish/Grade
KSZ8895MLU (Automotive Grade)	-40°C to +85°C	128-Pin LQFP	Pb-Free/Automotive
KSZ8895MLU-EVAL Board	Evaluation Board for KSZ8895MLU		

Revision History

Revision	Date	Summary of Changes
1.0	03/16/11	Initial
1.1	09/27/11	Update some descriptions, updates for descriptions of SMI mode and IGMP mode, update register default values, pins type and some parameters.
1.2	04/28/14	<p>Updates timing data for MII PHY mode.</p> <p>Update descriptions for VLAN table and I2C master mode.</p> <p>Update the equation in the broadcast storm protection section.</p> <p>Update the operation rating to $\pm 5\%$ and TTL min/max I/O voltage in different VDDIO. Change I/O from TTL to CMOS.</p> <p>Update SPI description from 127 to 255 for all registers.</p> <p>Update the table of tail tag rules.</p> <p>Update description for Register 1 bits [7:4].</p> <p>Update table 8 from bit [57:55] to bit [58:56].</p> <p>Update the port register control 2 bit [6] description bits [20:16] change to bits [11:7].</p> <p>Add evaluation Board in the ordering information table.</p> <p>Remove port 5 in the pin configuration and pin description.</p> <p>Update notes description for pin 125 and pin 126 in the pins descriptions.</p> <p>Update operating rating and correct typos.</p>

Contents

Features	2
Advanced Switch Features	2
Comprehensive Configuration Register Access	2
QoS/CoS Packet Prioritization Support	2
Integrated 5-Port 10/100 Ethernet Switch	2
Switch Monitoring Features	2
Low Power Dissipation	2
Ordering Information	3
Revision History	3
List of Figures	13
List of Tables	14
Pin Configuration	15
Pin Description	16
Pin for Strap-In Options	22
Introduction	25
Physical Layer Transceiver	25
100BASE-TX Transmit	25
10BASE-T Transmit.....	25
10BASE-T Receive	26
MDI/MDI-X Auto Crossover	26
Auto-Negotiation	27
Power Management	29
Normal Operation Mode	29
Energy Detect Mode	29
Soft Power-Down Mode.....	30
Power-Saving Mode.....	30
Port-Based Power-Down Mode	30
Switch Core.....	30
Address Look-Up	30
Learning	30
Migration	30
Aging	30
Forwarding	31
Switching Engine	31
Media Access Controller (MAC) Operation	31
MII Interface Operation	34

Port 5 MAC 5 SW5-MII Interface	34
SNI Interface Operation	35
Advanced Functionality	37
QoS Priority Support	37
Port-Based Priority	37
802.1p-Based Priority	37
Spanning Tree Support	38
Rapid Spanning Tree Support	39
Tail Tagging Mode	39
IGMP Support	40
Port Mirroring Support	41
VLAN Support	41
Rate Limiting Support	42
Ingress Rate Limit	42
Egress Rate Limit	42
Transmit Queue Ratio Programming	43
Filtering for Self-Address, Unknown Unicast/Multicast Address and Unknown VID Packet/IP Multicast	43
Configuration Interfaces	44
I ² C Master Serial Bus Configuration	44
SPI Slave Serial Bus Configuration	44
MII Management Interface (MIIM)	47
Serial Management Interface (SMI)	47
Register Description	49
Global Registers	51
Register 0 (0x00): Chip ID0	51
Register 1 (0x01): Chip ID1 / Start Switch	51
Register 2 (0x02): Global Control 0	51
Register 2 (0x02): Global Control 0	52
Register 3 (0x03): Global Control 1	52
Register 3 (0x03): Global Control 1	53
Register 4 (0x04): Global Control 2	54
Register 4 (0x04): Global Control 2	55
Register 5 (0x05): Global Control 3	55
Register 6 (0x06): Global Control 4	56
Register 7 (0x07): Global Control 5	57
Register 8 (0x08): Global Control 6	57

Register 9 (0x09): Global Control 7	57
Register 10 (0x0A): Global Control 8.....	57
Register 11 (0x0B): Global Control 9.....	57
Register 11 (0x0B): Global Control 9.....	58
<i>Register 12 (0x0C): Global Control 10</i>	<i>59</i>
Register 13 (0x0D): Global Control 11	59
Register 14 (0x0E): Power-Down Management Control 1	60
Register 14 (0x0E): Power-Down Management Control 1	60
Register 15 (0x0F): Power-Down Management Control 2	60
Port Registers.....	61
Register 16 (0x10): Port 1 Control 0.....	61
Register 32 (0x20): Port 2 Control 0.....	61
Register 48 (0x30): Port 3 Control 0.....	61
Register 64 (0x40): Port 4 Control 0.....	61
Register 80 (0x50): Port 5 Control 0.....	61
Register 16 (0x10): Port 1 Control 0.....	62
Register 32 (0x20): Port 2 Control 0.....	62
Register 48 (0x30): Port 3 Control 0.....	62
Register 64 (0x40): Port 4 Control 0.....	62
Register 80 (0x50): Port 5 Control 0.....	62
Register 17 (0x11): Port 1 Control 1	62
Register 33 (0x21): Port 2 Control 1	62
Register 49 (0x31): Port 3 Control 1	62
Register 65 (0x41): Port 4 Control 1	62
Register 81 (0x51): Port 4 Control 1	62
Register 18 (0x12): Port 1 Control 2.....	63
Register 34 (0x22): Port 2 Control 2.....	63
Register 50 (0x32): Port 3 Control 2.....	63
Register 66 (0x42): Port 4 Control 2.....	63
Register 82 (0x52): Port 5 Control 2.....	63
Register 18 (0x12): Port 1 Control 2.....	64
Register 34 (0x22): Port 2 Control 2.....	64
Register 50 (0x32): Port 3 Control 2.....	64
Register 66 (0x42): Port 4 Control 2.....	64
Register 82 (0x52): Port 5 Control 2.....	64
Register 19 (0x13): Port 1 Control 3.....	65

Register 35 (0x23): Port 2 Control 3.....	65
Register 51 (0x33): Port 3 Control 3.....	65
Register 67 (0x43): Port 4 Control 3.....	65
Register 83 (0x53): Port 5 Control 3.....	65
Register 20 (0x14): Port 1 Control 4.....	65
Register 36 (0x24): Port 2 Control 4.....	65
Register 52 (0x34): Port 3 Control 4.....	65
Register 68 (0x44): Port 4 Control 4.....	65
Register 84 (0x54): Port 5 Control 4.....	65
Register 87 (0x57): Reserved Control Register	65
Register 25 (0x19): Port 1 Status 0	66
Register 41 (0x29): Port 2 Status 0	66
Register 57 (0x39): Port 3 Status 0	66
Register 73 (0x49): Port 4 Status 0	66
Register 89 (0x59): Reserved.....	66
Register 26 (0x1A): Reserved	66
Register 42 (0x2A): Reserved	66
Register 58 (0x3A): Reserved	66
Register 74 (0x4A): Reserved	66
Register 90 (0x5A): Reserved	66
Register 27 (0x1B): Reserved	66
Register 43 (0x2B): Reserved	66
Register 59 (0x3B): Reserved	66
Register 75 (0x4B): Reserved	66
Register 91 (0x5B): Reserved	66
Register 28 (0x1C): Port 1 Control 5	67
Register 44 (0x2C): Port 2 Control 5	67
Register 60 (0x3C): Port 3 Control 5	67
Register 76 (0x4C): Port 4 Control 5	67
Register 92 (0x5C): Reserved	67
Register 28 (0x1C): Port 1 Control 5	68
Register 44 (0x2C): Port 2 Control 5	68
Register 60 (0x3C): Port 3 Control 5	68
Register 76 (0x4C): Port 4 Control 5	68
Register 92 (0x5C): Reserved	68
Register 29 (0x1D): Port 1 Control 6	68

Register 45 (0x2D): Port 2 Control 6	68
Register 61 (0x3D): Port 3 Control 6	68
Register 77 (0x4D): Port 4 Control 6	68
Register 93 (0x5D): Reserved	68
Register 29 (0x1D): Port 1 Control 6	69
Register 45 (0x2D): Port 2 Control 6	69
Register 61 (0x3D): Port 3 Control 6	69
Register 77 (0x4D): Port 4 Control 6	69
Register 93 (0x5D): Reserved	69
Register 30 (0x1E): Port 1 Status 1	69
Register 46 (0x2E): Port 2 Status 1	69
Register 62 (0x3E): Port 3 Status 1	69
Register 78 (0x4E): Port 4 Status 1	69
Register 94 (0x5E): Reserved	69
Register 31 (0x1F): Port 1 Control 7 and Status 2	70
Register 47 (0x2F): Port 2 Control 7 and Status 2	70
Register 63 (0x3F): Port 3 Control 7 and Status 2	70
Register 79 (0x4F): Port 4 Control 7 and Status 2	70
Register 95 (0x5F): Reserved	70
Advanced Control Registers.....	71
Register 104 (0x68): MAC Address Register 0	71
Register 105 (0x69): MAC Address Register 1	71
Register 106 (0x6A): MAC Address Register 2	71
Register 107 (0x6B): MAC Address Register 3	71
Register 108 (0x6C): MAC Address Register 4	71
Register 109 (0x6D): MAC Address Register 5	71
Register 110 (0x6E): Indirect Access Control 0	72
Register 111 (0x6F): Indirect Access Control 1	72
Register 112 (0x70): Indirect Data Register 8	72
Register 113 (0x71): Indirect Data Register 7	72
Register 114 (0x72): Indirect Data Register 6	72
Register 115 (0x73): Indirect Data Register 5	72
Register 116 (0x74): Indirect Data Register 4	72
Register 117 (0x75): Indirect Data Register 3	73
Register 118 (0x76): Indirect Data Register 2	73
Register 119 (0x77): Indirect Data Register 1	73

Register 120 (0x78): Indirect Data Register 0	73
Register 124 (0x7C): Interrupt Status Register	73
Register 125 (0x7D): Interrupt Mask Register	74
Register 128 (0x80): Global Control 12	74
Register 129 (0x81): Global Control 13	74
Register 130 (0x82): Global Control 14	75
Register 131 (0x83): Global Control 15	75
Register 132 (0x84): Global Control 16	76
Register 133(0x85): Global Control 17	76
Register 134 (0x86): Global Control 18	77
Register 135 (0x87): Global Control 19	77
Register 144 (0x90): TOS Priority Control Register 0	78
Register 145 (0x91): TOS Priority Control Register 1	78
Register 146 (0x92): TOS Priority Control Register 2	78
Register 147 (0x93): TOS Priority Control Register 3	78
<i>Register 148 (0x94): TOS Priority Control Register 4</i>	<i>79</i>
Register 149 (0x95): TOS Priority Control Register 5	79
Register 150 (0x96): TOS Priority Control Register 6	79
Register 151 (0x97): TOS Priority Control Register 7	79
Register 152 (0x98): TOS Priority Control Register 8	79
Register 153 (0x99): TOS Priority Control Register 9	80
Register 154 (0x9A): TOS Priority Control Register 10	80
Register 155 (0x9B): TOS Priority Control Register 11	80
Register 156 (0x9C): TOS Priority Control Register 12	80
Register 157 (0x9D): TOS Priority Control Register 13	80
Register 158 (0x9E): TOS Priority Control Register 14	81
Register 159 (0x9F): TOS Priority Control Register 15	81
Register 176 (0xB0): Port 1 Control 8.....	81
Register 192 (0xC0): Port 2 Control 8	81
Register 208 (0xD0): Port 3 Control 8	81
Register 224 (0xE0): Port 4 Control 8.....	81
Register 240 (0xF0): Port 5 Control 8.....	81
Register 176 (0xB0): Port 1 Control 8.....	82
Register 192 (0xC0): Port 2 Control 8	82
Register 208 (0xD0): Port 3 Control 8	82
Register 224 (0xE0): Port 4 Control 8.....	82
Register 240 (0xF0): Port 5 Control 8.....	82

Register 177 (0xB1): Port 1 Control 9.....	82
Register 193 (0xC1): Port 2 Control 9	82
Register 209 (0xD1): Port 3 Control 9	82
Register 225 (0xE1): Port 4 Control 9.....	82
Register 241 (0xF1): Port 5 Control 9.....	82
Register 178 (0xB2): Port 1 Control 10	83
Register 194 (0xC2): Port 2 Control 10	83
Register 210 (0xD2): Port 3 Control 10	83
Register 226 (0xE2): Port 4 Control 10	83
Register 242 (0xF2): Port 5 Control 10.....	83
Register 179 (0xB3): Port 1 Control 11	83
Register 195 (0xC3): Port 2 Control 11	83
Register 211 (0xD3): Port 3 Control 11	83
Register 227 (0xE3): Port 4 Control 11	83
Register 243 (0xF3): Port 5 Control 11.....	83
Register 180 (0xB4): Port 1 Control 12	83
Register 196 (0xC4): Port 2 Control 12	83
Register 212 (0xD4): Port 3 Control 12	83
Register 228 (0xE4): Port 4 Control 12	83
Register 244 (0xF4): Port 5 Control 12.....	83
Register 181 (0xB5): Port 1 Control 13	84
Register 197 (0xC5): Port 2 Control 13	84
Register 213 (0xD5): Port 3 Control 13	84
Register 229 (0xE5): Port 4 Control 13	84
Register 245 (0xF5): Port 5 Control 13.....	84
Register 182 (0xB6): Port 1 Rate Limit Control	84
Register 198 (0xC6): Port 2 Rate Limit Control	84
Register 214 (0xD6): Port 3 Rate Limit Control	84
Register 230 (0xE6): Port 4 Rate Limit Control	84
Register 246 (0xF6): Port 5 Rate Limit Control	84
Register 183 (0xB7): Port 1 Priority 0 Ingress Limit Control 1	85
Register 199 (0xC7): Port 2 Priority 0 Ingress Limit Control 1.....	85
Register 215 (0xD7): Port 3 Priority 0 Ingress Limit Control 1.....	85
Register 231 (0xE7): Port 4 Priority 0 Ingress Limit Control 1.....	85
Register 247 (0xF7): Port 5 Priority 0 Ingress Limit Control 1	85
Register 184 (0xB8): Port 1 Priority 1 Ingress Limit Control 2.....	85
Register 200 (0xC8): Port 2 Priority 1 Ingress Limit Control 2.....	85

Register 216 (0xD8): Port 3 Priority 1 Ingress Limit Control 2.....	85
Register 232 (0xE8): Port 4 Priority 1 Ingress Limit Control 2.....	85
Register 248 (0xF8): Port 5 Priority 1 Ingress Limit Control 2.....	85
Register 185 (0xB9): Port 1 Priority 2 Ingress Limit Control 3.....	85
Register 201 (0xC9): Port 2 Priority 2 Ingress Limit Control 3.....	85
Register 217 (0xD9): Port 3 Priority 2 Ingress Limit Control 3.....	85
Register 233 (0xE9): Port 4 Priority 2 Ingress Limit Control 3.....	85
Register 249 (0xF9): Port 5 Priority 2 Ingress Limit Control 3.....	85
Register 186 (0xBA): Port 1 Priority 3 Ingress Limit Control 4.....	86
Register 202 (0xCA): Port 2 Priority 3 Ingress Limit Control 4.....	86
Register 218 (0xDA): Port 3 Priority 3 Ingress Limit Control 4.....	86
Register 234 (0xEA): Port 4 Priority 3 Ingress Limit Control 4.....	86
Register 250 (0xFA): Port 5 Priority 3 Ingress Limit Control 4.....	86
Register 187 (0xBB): Port 1 Queue 0 Egress Limit Control 1.....	86
Register 203 (0xCB): Port 2 Queue 0 Egress Limit Control 1.....	86
Register 219 (0xDB): Port 3 Queue 0 Egress Limit Control 1.....	86
Register 235 (0xEB): Port 4 Queue 0 Egress Limit Control 1.....	86
Register 251 (0xFB): Port 5 Queue 0 Egress Limit Control 1.....	86
Register 188 (0xBC): Port 1 Queue 1 Egress Limit Control 2.....	86
Register 204 (0xCC): Port 2 Queue 1 Egress Limit Control 2.....	86
Register 220 (0xDC): Port 3 Queue 1 Egress Limit Control 2.....	86
Register 236 (0xEC): Port 4 Queue 1 Egress Limit Control 2.....	86
Register 252 (0xFC): Port 5 Queue 1 Egress Limit Control 2.....	86
Register 189 (0xBD): Port 1 Queue 2 Egress Limit Control 3.....	87
Register 205 (0xCD): Port 2 Queue 2 Egress Limit Control 3.....	87
Register 221 (0xDD): Port 3 Queue 2 Egress Limit Control 3.....	87
Register 237 (0xED): Port 4 Queue 2 Egress Limit Control 3.....	87
Register 253 (0xFD): Port 5 Queue 2 Egress Limit Control 3.....	87
Register 190 (0xBE): Port 1 Queue 3 Egress Limit Control 4.....	87
Register 206 (0xCE): Port 2 Queue 3 Egress Limit Control 4.....	87
Register 222 (0xDE): Port 3 Queue 3 Egress Limit Control 4.....	87
Register 238 (0xEE): Port 4 Queue 3 Egress Limit Control 4.....	87
Register 254 (0xFE): Port 5 Queue 3 Egress Limit Control 4.....	87
Register 191(0xBF): Testing Register.....	89
Register 207(0xCF): Reserved Control Register.....	89
Register 223(0xDF): Test Register 2.....	89
Register 239(0xEF): Test Register 3.....	89

Register 255(0xFF): Testing Register4.....	89
Static MAC Address Table	90
VLAN Table	92
Dynamic MAC Address Table	94
Management Information Base (MIB) Counters.....	96
Port 1 MIB Counter Indirect Memory Offsets.....	96
Format of “Per port” MIB Counter	97
MIIM Registers.....	100
Register 0h: MII Control.....	100
Register 1h: MII Status	101
Register 2h: PHYID HIGH	101
Register 3h: PHYID LOW	101
Register 4h: Advertisement Ability.....	102
Register 5h: Link Partner Ability	102
Register 1dh: Reserved	103
Register 1fh: PHY Special Control/Status	103
Absolute Maximum Ratings⁽¹⁾	104
Operating Ratings⁽²⁾	104
Electrical Characteristics^(4, 5)	104
Timing Diagrams	106
EEPROM Timing.....	106
SNI Timing	107
SPI Timing	110
Auto-Negotiation Timing	112
Reset Timing.....	113
Reset Circuit Diagram.....	114
Isolation Transformer Selection	115
Reference Crystal Selection.....	115
Package Information	116

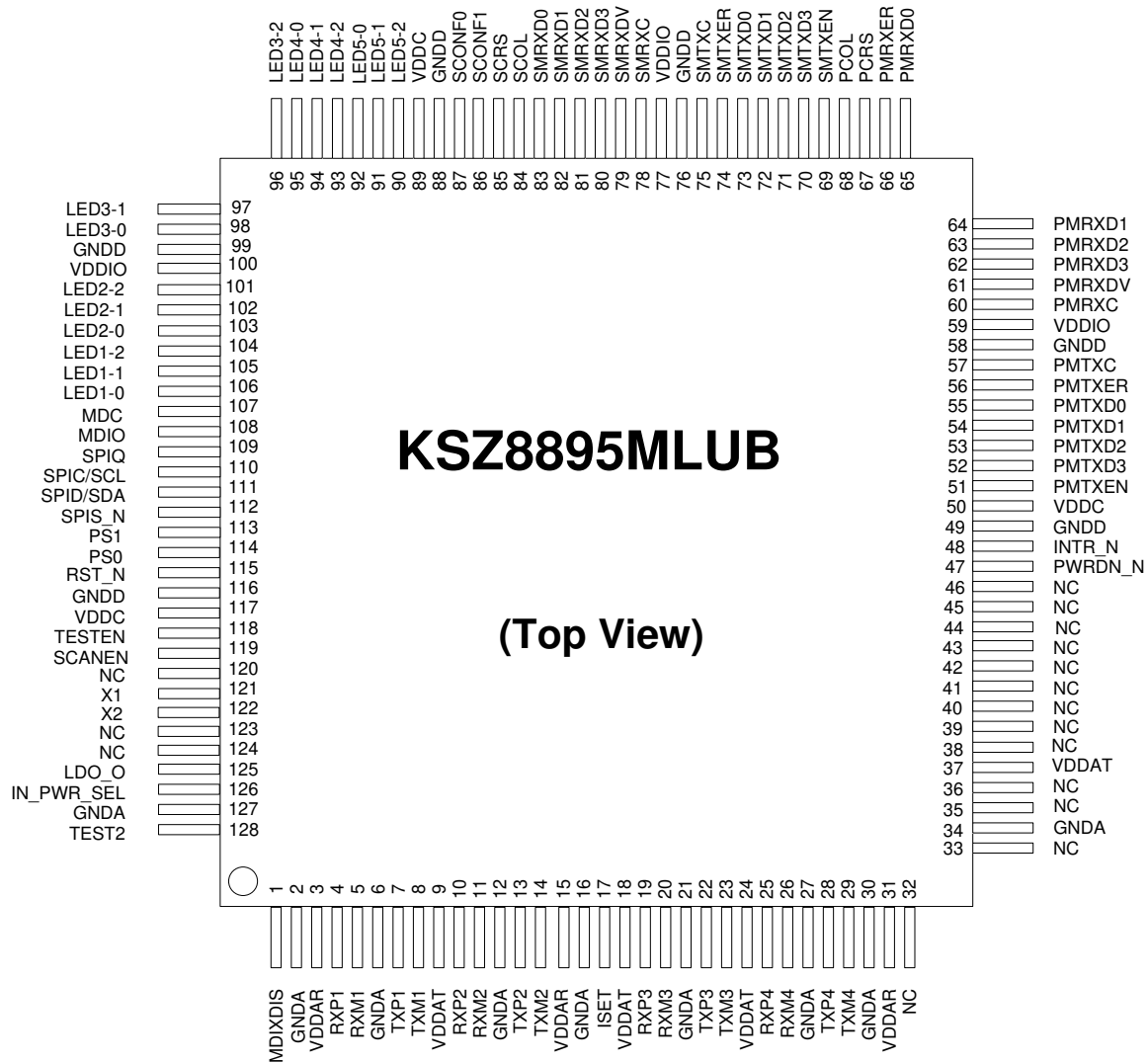
List of Figures

Figure 1. Typical Straight Cable Connection	26
Figure 2. Typical Crossover Cable Connection	27
Figure 3. Auto-Negotiation	28
Figure 4. Destination Address Lookup Flow Chart (Stage 1)	32
Figure 5. Destination Address Resolution Flow Chart (Stage 2)	33
Figure 6. 802.1p Priority Field Format	37
Figure 7. Tail Tag Frame Format	39
Figure 8. KSZ8895MLU EEPROM Configuration Timing Diagram.....	44
Figure 9. SPI Write Data Cycle	45
Figure 10. SPI Read Data Cycle	45
Figure 11. SPI Multiple Write	46
Figure 12. SPI Multiple Read	46
Figure 13. EEPROM Interface Input Receive Timing Diagram.....	106
Figure 14. EEPROM Interface Output Transmit Timing Diagram	106
Figure 15. SNI Input Timing	107
Figure 16. SNI Output Timing	107
Figure 17. MAC Mode MII Timing – Data Received from MII	108
Figure 18. MAC Mode MII Timing – Data Transmitted from MII	108
Figure 19. PHY Mode MII Timing – Data Received from MII.....	109
Figure 20. PHY Mode MII Timing – Data Transmitted from MII.....	109
Figure 21. SPI Input Timing	110
Figure 22. SPI Output Timing.....	111
Figure 23. Auto-Negotiation Timing	112
Figure 24. Reset Timing	113
Figure 25. Recommended Reset Circuit	114
Figure 26. Recommended Circuit for Interfacing with CPU/FPGA Reset.....	114

List of Tables

Table 1. MDI/MDI-X Pin Definitions	26
Table 2. Internal Function Block Status	29
Table 3. Switch MAC 5 MII Signals.....	35
Table 4. SNI Signals	36
Table 5. Tail Tag Rules	40
Table 6. FID+DA Look-Up in the VLAN Mode	41
Table 7. FID+SA Look-Up in the VLAN Mode	42
Table 8. SPI Connections	45
Table 9. MII Management Interface Frame Format	47
Table 10. Serial Management Interface (SMI) Frame Format	47
Table 11. Data Rate Selection in 100BT.....	88
Table 12. Data Rate Selection in 10BT.....	88
Table 13. Format of Static MAC Table for Read (32 Entries)	90
Table 14. Format of Static MAC Table for Writes (32 Entries)	91
Table 15. Format of Static VLAN Table (Support Max 4096 VLAN ID Entries and 128 Active VLANs).....	92
Table 16. VLAN ID and Indirect Registers	93
Table 17. Format of Dynamic MAC Address Table (1K Entries)	94
Table 18. All Port Dropped Packet MIB Counters.....	97
Table 19. Format of All Dropped Packet MIB Counters.....	98
Table 20. EEPROM Timing Parameters	106
Table 21. SNI Timing Parameters.....	107
Table 22. MAC Mode MII Timing Parameters.....	108
Table 23. PHY Mode MII Timing Parameters	109
Table 24. SPI Input Timing Parameters	110
Table 25. SPI Output Timing Parameters	111
Table 26. Auto-Negotiation Timing Parameters.....	112
Table 27. Reset Timing Parameters	113
Table 28. Transformer Selection Criteria	115
Table 29. Qualified Magnetic Vendors	115
Table 30. Typical Reference Crystal Characteristics	115

Pin Configuration



128-Pin LQFP

Pin Description

Pin Number	Pin Name	Type ⁽¹⁾	Port	Pin Function ⁽²⁾
1	MDI-XDIS	lpd	1 – 5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GNDA	GND		Analog ground.
3	VDDAR	P		1.2V analog V _{DD} .
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal – (differential).
6	GNDA	GND		Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal – (differential).
9	VDDAT	P		3.3V analog V _{DD} .
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal – (differential).
12	GNDA	GND		Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
15	VDDAR	P		1.2V analog V _{DD} .
16	GNDA	GND		Analog ground.
17	ISET			Set physical transmit output current. Pull-down with a 12.4kΩ1% resistor.
18	VDDAT	P		3.3V analog V _{DD} .
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal - (differential).
21	GNDA	GND		Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
24	VDDAT	P		3.3V analog V _{DD} .
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal - (differential).
27	GNDA	GND		Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
30	GNDA	GND		Analog ground.
31	VDDAR	P		1.2V analog V _{DD} .
32	NC	NC		No connect.
33	NC	NC		No connect.
34	GNDA	GND		Analog ground.
35	NC	NC		No connect.
36	NC	NC		No connect.
37	VDDAT	P		3.3V analog V _{DD} .

Pin Description (Continued)

Pin Number	Pin Name	Type ⁽¹⁾	Port	Pin Function ⁽²⁾
38	NC	NC		No connect.
39	NC	NC		No connect.
40	NC	NC		No connect.
41	NC	NC		No connect.
42	NC	NC		No connect.
43	NC	NC		No connect.
44	NC	NC		No connect.
45	NC	NC		No connect.
46	NC	NC		No connect.
47	PWRDN_N	lpu		Full-chip power down. Active low.
48	INTR_N	Opu		Interrupt. This pin is open-drain output pin.
49	GNDD	GND		Digital ground.
50	VDDC	P		1.2V digital core V _{DD} .
51	PMTXEN	lpd	5	Reserved for MLU. No connect.
52	PMTXD3	lpd	5	Reserved for MLU. No connect.
53	PMTXD2	lpd	5	Reserved for MLU. No connect.
54	PMTXD1	lpd	5	Reserved for MLU. No connect.
55	PMTXD0	lpd	5	Reserved for MLU. No connect.
56	PMTXER	lpd	5	Reserved for MLU. No connect.
57	PMTXC	I/O	5	Reserved for MLU. No connect.
58	GNDD	GND		Digital ground.
59	VDDIO	P		3.3V, 2.5V, or 1.8V digital V _{DD} for digital I/O circuitry.
60	PMRXC	I/O	5	Reserved for MLU. No connect.
61	PMRXDV	lpd/O	5	Reserved for MLU. No connect.
62	PMRXD3	lpd/O	5	Reserved for MLU. Strap option: PD (default) = enable flow control. PU = disable flow control.
63	PMRXD2	lpd/O	5	Reserved for MLU. Strap option: PD (default) = disable back pressure. PU = enable back pressure.
64	PMRXD1	lpd/O	5	Reserved for MLU. Strap option: PD (default) = drop excessive collision packets. PU = does not drop excessive collision packets.
65	PMRXD0	lpd/O	5	Reserved for MLU. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode. PU = enable for performance enhancement.
66	PMRXER	lpd/O	5	Reserved for MLU. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.

Pin Description (Continued)

Pin Number	Pin Name	Type ⁽¹⁾	Port	Pin Function ⁽²⁾		
67	PCRS	lpd/O	5	Reserved for MLU. Strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.		
68	PCOL	lpd/O	5	Reserved for MLU. Strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.		
69	SMTXEN	lpd		Port 5 Switch MII transmit enable.		
70	SMTXD3	lpd		Port 5 Switch MII transmit bit 3.		
71	SMTXD2	lpd		Port 5 Switch MII transmit bit 2.		
72	SMTXD1	lpd		Port 5 Switch MII transmit bit 1.		
73	SMTXD0	lpd		Port 5 Switch MII transmit bit 0.		
74	SMTXER	lpd		Port 5 Switch MII transmit error.		
75	SMTXC	I/O		Port 5 Switch MII transmit clock: Input: SW5-MII MAC mode. Output: SW5-MII PHY modes.		
76	GNDD	GND		Digital ground.		
77	VDDIO	P		3.3V, 2.5V, or 1.8V digital V _{DD} for digital I/O circuitry.		
78	SMRXC	I/O		Port 5 Switch MII receive clock: Input: SW5-MII MAC mode. Output: SW5-MII PHY mode.		
79	SMRXDV	lpd/O		Switch MII receive data valid.		
80	SMRXD3	lpd/O		Port 5 Switch MII receive bit 3. Strap option: PD (default) = Disable Switch SW5-MII full-duplex flow control PU = Enable Switch SW5-MII full-duplex flow control.		
81	SMRXD2	lpd/O		Port 5 Switch MII receive bit 2. Strap option: PD (default) = Switch SW5-MII in full-duplex mode; PU = Switch SW5-MII in half-duplex mode.		
82	SMRXD1	lpd/O		Port 5 Switch MII receive bit 1. Strap option: PD (default) =Port 5 Switch SW5-MII in 100Mbps mode; SW5-TMII in 200Mbps mode. PU = Switch SW5-MII in 10Mbps mode.		
83	SMRXD0	lpd/O		Port 5 Switch MII receive bit 0. Strap option: LED mode PD (default) = mode 0; PU = mode 1. See "Register 11." Mode 0, link at 100/Full LEDx[2,1,0]=0,0,0 100/Half LEDx[2,1,0]=0,1,0 10/Full LEDx[2,1,0]=0,0,1 10/Half LEDx[2,1,0]=0,1,1 Mode 1, link at 100/Full LEDx[2,1,0]=0,1,0 100/Half LEDx[2,1,0]=0,1,1 10/Full LEDx[2,1,0]=1,0,0 10/Half LEDx[2,1,0]=1,0,1		
					Mode 0	Mode 1
				LEDX_2	Lnk/Act	100Lnk/Act
				LEDX_1	FullD/Col	10Lnk/Act
	LEDX_0	Speed	Full duplex			
84	SCOL	lpd/O		Port 5 Switch MII collision detect: Input: SW5-MII MAC modes. Output: SW5-MII PHY modes.		

Pin Description (Continued)

Pin Number	Pin Name	Type ⁽¹⁾	Port	Pin Function ⁽²⁾
85	SCRS	lpd/O		Port 5 Switch MII modes carrier sense: Input: SW5-MII MAC modes. Output: SW5-MII PHY modes.
86	SCONF1	lpd		Pin 91,86,87 are dual MII configuration pins for the Port5 MAC5 MII. SW5-MII supports both MAC mode and PHY modes.
				Pin#: (91, 86, 87)
				Port5 Switch MAC5 SW5- MII
				000 Disable, Otri
				001 PHY Mode MII
				010 MAC Mode MII
				011 PHY Mode SNI
				100 Disable (Default)
				101 PHY Mode MII
				110 MAC Mode MII
				111 PHY Mode SNI
87	SCONF0	lpd		Dual MII configuration pin. See pin 86 descriptions.
88	GNDD	GND		Digital ground.
89	VDDC	P		1.2V digital core V _{DD} .
90	LED5-2	lpu/O	5	Reserved for MLU Strap option: aging setup. See "Aging" section. PU (default) = Aging enable PD = Aging disable.
91	LED5-1	lpu/O	5	Reserved for MLU Strap option: PU (default): enable PHY[5] MII I/F. PD: tristate and disable all PHY[5] MII output. (Design should pull this pin down as default for MLU.
92	LED5-0	lpu/O	5	Reserved for MLU Strap option for port 4 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to register76 bit[7].
93	LED4-2	lpu/O	4	LED indicator 2.
94	LED4-1	lpu/O	4	LED indicator 1.
95	LED4-0	lpu/O	4	LED indicator 0. Strap option: PU (default) = Normal mode. PD = Energy Detection mode (EDPD mode). Strap to register 14 bits[4:3]
96	LED3-2	lpu/O	3	LED indicator 2.
97	LED3-1	lpu/O	3	LED indicator 1.
98	LED3-0	lpu/O	3	LED indicator 0. Strap option: PU (default) = Select I/O drive strength (8mA); PD = Select I/O drive strength (12mA). Strap to register132 bit[7-6].
99	GNDD	GND		Digital ground.
100	VDDIO	P		3.3V, 2.5V, or 1.8V digital V _{DD} for digital I/O circuitry.
101	LED2-2	lpu/O	2	LED indicator 2.

Pin Description (Continued)

Pin Number	Pin Name	Type ⁽¹⁾	Port	Pin Function ⁽²⁾	
102	LED2-1	lpu/O	2	LED indicator 1. Strap option: for port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to register60 bit[7].	
103	LED2-0	lpu/O	2	LED indicator 0.	
104	LED1-2	lpu/O	1	LED indicator 2.	
105	LED1-1	lpu/O	1	LED indicator 1. Strap option: for port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to register60 bit[4].	
106	LED1-0	lpu/O	1	LED indicator 0. Strap option for port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to register60 bit[5].	
107	MDC	lpu	All	Switch MII management data clock. Or SMI interface clock.	
108	MDIO	lpu/O	All	Switch MII management data I/O. Or SMI interface data I/O. Features internal pull down to define pin state when not driven. Need an external pull-up when driven.	
109	SPIQ	lpu/O	All	SPI serial data output in SPI slave mode.	
110	SPIC/SCL	lpu/O	All	SPI slave mode: clock input (1) Input clock up to 25MHz in SPI slave mode, (2) output clock at 61kHz in I ² C master mode. See "Pin 113."	
111	SSPID/SDA	lpu/O	All	SPI slave mode: serial data input. (1) Serial data input in SPI slave mode; (2) Serial data input/output in I ² C master mode. See "Pin 113."	
112	SPIS_N	lpu	All	SPI slave mode: chip select (active low). (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KSZ8895MLU is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer. (2) not used in I ² C master mode.	
113	PS1	lpd		Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MLU will start itself with the PS[1.0] = 00 default register values.	
				Pin Configuration	Serial Bus Configuration
				PS[1.0]=00	I ² C Master Mode for EEPROM
				PS[1.0]=01	SMI Interface Mode
				PS[1.0]=10	SPI Slave Mode for CPU Interface
				PS[1.0]=11	Factory Test Mode (BIST)
114	PS0	lpd		Serial bus configuration pin. See "Pin 113."	
115	RST_N	lpu		Reset the KSZ8895MLU device. Active low.	
116	GNDD	GND		Digital ground.	
117	VDDC	P		1.2V digital core V _{DD} .	
118	TESTEN	lpd		NC for normal operation. Factory test pin.	
119	SCANEN	lpd		NC for normal operation. Factory test pin.	
120	NC	NC		No connect.	

Pin Description (Continued)

Pin Number	Pin Name	Type ⁽¹⁾	Port	Pin Function ⁽²⁾
121	X1	I		25MHz crystal clock connection/or 3.3V Oscillator input. Crystal/Oscillator should be ± 50 ppm tolerance.
122	X2	O		25MHz crystal clock connection.
123	NC	NC		No connect.
124	NC	NC		No connect.
125	LDO_O	P		LDO_O pin connect to Gate pin of MOSFET if using the internal 1.2V LDO controller. LDO_O pin will be floating if using an external 1.2V LDO. Note: When pin126 voltage is greater than the internal 1.2V LDO controller enable threshold (0.58V), the Internal 1.2V LDO controller is enabled and creates a 1.2V output when using an external MOSFET. When pin126 is pull-down, the internal 1.2V LDO controller is disabled and pin 125 tri-stated.
126	IN_PWR_SEL	I		Pull-up or a Resistor divider: Enable internal 1.2V LDO controller. Pull-down: Disable internal 1.2V LDO controller. Note: A 4.3K pull-up and a 1K pull-down resistors divider network is recommended if using the internal 1.2V LDO controller and an external MOSFET for 1.2V power. A 100 Ω (approximately) resistor between the source and drain pins on the MOSFET is highly recommended as well. You can also use an external 1.2V LDO for 1.2V power supply.
127	GNDA	GND		Analog ground.
128	TEST2	NC		NC for normal operation. Factory test pin.

Notes:

- P = Power supply.
 - I = Input.
 - O = Output.
 - I/O = Bidirectional.
 - GND = Ground.
 - Ipu = Input w/internal pull-up.
 - Ipd = Input w/internal pull-down.
 - Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
 - Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
 - NC = No connect.
- PU = Strap pin pull-up.
 - PD = Strap pull-down.
 - OTRI = Output tristated.

Pin for Strap-In Options

The KSZ8895MLU can function as a managed switch or unmanaged switch. If no EEPROM or microcontroller exists, the KSZ8895MLU will operate from its default setting. The strap-in option pins can be configured by external pull-up/down resistors and take the effect after power-down reset or warm reset, the functions are described in the following tables.

Pin Number	Pin Name	PU/PD ⁽¹⁾	Description ⁽²⁾		
1	MDI-XDIS	lpd	Disable auto MDI/MDI-X. PD = (default) = normal operation PU = disable auto MDI/MDI-X on all ports.		
62	PMRXD3	lpd/O	Strap option: PD (default) = enable flow control; PU = disable flow control.		
63	PMRXD2	lpd/O	Strap option: PD (default) = disable back pressure; PU = enable back pressure.		
64	PMRXD1	lpd/O	Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.		
65	PMRXD0	lpd/O	Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.		
66	PMRXER	lpd/O	Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.		
67	PCRS	lpd/O	Strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails. Refer to register 76.		
68	PCOL	lpd/O	Strap option for port 4 only. PD (default) = no force flow control. PU = force flow control. Refer to register 66.		
80	SMRXD3	lpd/O	Switch MII receive bit 3. Strap option: PD (default) = disable switch SW5-MII full-duplex flow control; PU = enable switch SW5-MII full-duplex flow control.		
81	SMRXD2	lpd/O	Switch MII receive bit 2. Strap option: PD (default) = switch SW5-MII in full-duplex mode; PU = switch SW5-MII in half-duplex mode.		
82	SMRXD1	lpd/O	Switch MII receive bit 1. Strap option: PD (default) = switch SW5-MII in 100Mbps mode and SW5-TMII in 200Mbps PU = switch MII in 10Mbps mode.		
83	SMRXD0	lpd/O	Switch MII receive bit 0. Strap option: LED mode PD (default) = mode 0; PU = mode 1. See "Register 11."		
				Mode 0	Mode 1
			LEDX_2	Lnk/Act	100Lnk/Act
			LEDX_1	FullD/Col	10Lnk/Act
	LEDX_0	Speed	FullD		

Pin for Strap-In Options (Continued)

Pin Number	Pin Name	PU/PD ⁽¹⁾	Description ⁽²⁾																		
86	SCONF1	lpd	Pins 91, 86, 87 are dual MII configuration pins for the Port5 MAC5 MII. SW5-MII supports both MAC mode and PHY modes.																		
			<table border="1"> <thead> <tr> <th>Pin#: (91, 86, 87)</th> <th>Port5 Switch MAC5 SW5- MII</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Disable, Otri</td> </tr> <tr> <td>001</td> <td>PHY Mode MII</td> </tr> <tr> <td>010</td> <td>MAC Mode MII</td> </tr> <tr> <td>011</td> <td>PHY Mode SNI</td> </tr> <tr> <td>100</td> <td>Disable</td> </tr> <tr> <td>101</td> <td>PHY Mode MII</td> </tr> <tr> <td>110</td> <td>MAC Mode MII</td> </tr> <tr> <td>111</td> <td>PHY Mode SNI</td> </tr> </tbody> </table>	Pin#: (91, 86, 87)	Port5 Switch MAC5 SW5- MII	000	Disable, Otri	001	PHY Mode MII	010	MAC Mode MII	011	PHY Mode SNI	100	Disable	101	PHY Mode MII	110	MAC Mode MII	111	PHY Mode SNI
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101	PHY Mode MII																				
110	MAC Mode MII																				
111	PHY Mode SNI																				
87	SCONF0	lpd	Dual MII configuration pin. See pin 86 descriptions.																		
90	LED5-2	lpu/O	Strap option: Aging setup. See "Aging" section PU (default) = aging enable; PD = aging disable.																		
91	LED5-1	lpu/O	Strap option: PU (default): enable PHY[5] MII I/F. PD: tristate all PHY[5] MII output. See "Pin 86 SCONF1."																		
92	LED5-0	lpu/O	Strap option for port 4 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to register76 bit[7]																		
95	LED4-0	lpu/O	LED indicator 0. Strap option: PU (default) = Normal mode. PD = Energy Detection mode (EDPD mode). Strap to register 14 bits[4:3]																		
98	LED3-0	lpu/O	LED3 indicator 0. Strap option: PU (default) = Select I/O current drive strength (8mA); PD = Select I/O current drive strength (12mA). Strap to register132 bit[7:6].																		
102	LED2-1	lpu/O	LED2 indicator 1. Strap option for port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to register60 bit[7]																		
105	LED1-1	lpu/O	LED1 indicator 1. Strap option for port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to register50 bit[4]																		

Pin for Strap-In Options (Continued)

Pin Number	Pin Name	PU/PD ⁽¹⁾	Description ⁽²⁾	
106	LED1-0	lpu/O	LED1 indicator 0. Strap option for port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to register60 bit[5].	
113	PS1	lpd	Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MLU will start itself with the PS[1:0] =00 default register values.	
			Pin Configuration	Serial Bus Configuration
			PS[1:0]=00	I ² C Master Mode for EEPROM
			PS[1:0]=01	SMI Interface Mode
			PS[1:0]=10	SPI Slave Mode for CPU Interface
			PS[1:0]=11	Factory Test Mode (BIST)
114	PS0	lpd	Serial bus configuration pin. See "Pin 113."	

Notes:

- lpu = Input w/internal pull-up.
 - lpd = Input w/internal pull-down.
 - lpd/O = Input w/internal pull-down during reset, output pin otherwise.
 - lpu/O = Input w/internal pull-up during reset, output pin otherwise.
- PU = Strap pin pull-up.
 - PD = Strap pull-down.

Introduction

The KSZ8895MLU contains four 10/100 physical layer transceivers and five media access control (MAC) units with an integrated Layer 2 managed switch. The device runs in two modes. The first mode is as a 4-port integrated switch. The second is as a 4-port switch with the fifth MAC. In this mode, access to the fifth MAC is provided through a media independent interface (MII).

The KSZ8895MLU has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the KSZ8895MLU via the SPI bus, or via the MDC/MDIO interface with SMI mode. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KSZ8895MLU supports IEEE 802.3 10BASE-T, 100BASE-TX on all ports with Auto MDI/MDIX. The KSZ8895MLU can be used as fully-managed 4-port standalone switch or hook up to microprocessor by its SW-MII interface for an application solution.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

There are a number of major enhancements from the KS8995MA to the KSZ8895MLU. These include: more host interface options, four queues prioritization, tag as well as port based VLAN, rapid spanning tree support, IGMP snooping support, port mirroring support and more flexible rate limiting and filtering functionality.

Physical Layer Transceiver

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 12.4k Ω resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KSZ8895MLU generates 125MHz, 83MHz, 41MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator.

Scrambler/De-Scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

10BASE-T Transmit

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.