Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

KSZ8895MQX/RQX/FQX/MLX

Integrated 5-Port 10/100 Managed Ethernet Switch with MII/RMII Interface

Features

Advanced Switch Features

- IEEE 802.1q VLAN Support for up to 128 Active VLAN Groups (Full-Range 4096 of VLAN IDs)
- Static MAC Table Supports up to 32 Entries
- VLAN ID Tag/Untagged Options, Per Port Basis
- IEEE 802.1p/q Tag Insertion or Removal on a Per Port Basis Based on Ingress Port (Egress)
- Programmable Rate Limiting at the Ingress and Egress on a Per Port Basis
- Jitter-Free Per Packet Based Rate Limiting Support
- Broadcast Storm Protection with Percentage Control (Global and Per Port Basis)
- IEEE 802.1d Rapid Spanning Tree Protocol RSTP Support
- Tail Tag Mode (1 Byte Added Before FCS) Support at Port 5 to Inform the Processor Which Ingress Port Receives the Packet
- 1.4 Gbps High-Performance Memory Bandwidth and Shared Memory Based Switch Fabric with Fully Non-Blocking Configuration
- Dual MII with MAC 5 and PHY 5 on Port 5, SW5-MII/RMII for MAC 5 and P5-MII/RMII for PHY 5
- Enable/Disable Option for Huge Frame Size up to 2000 Bytes Per Frame
- IGMP v1/v2 Snooping (IPv4) Support for Multicast Packet Filtering
- IPv4/IPv6 QoS Support
- Support Unknown Unicast/Multicast Address and Unknown VID Packet Filtering
- Self-Address Filtering

Comprehensive Configuration Register Access

- Serial Management Interface (MDC/MDIO) to All PHYs Registers and SMI Interface (MDC/MDIO) to All Registers
- High-Speed SPI (up to 25 MHz) and I^2C Master Interface to all Internal Registers
- I/O Pins Strapping and EEPROM to Program Selective Registers in Unmanaged Switch Mode
- Control Registers Configurable on the Fly (Port-Priority, 802.1p/d/q, AN…)

QoS/CoS Packet Prioritization Support

- Per Port, 802.1p and DiffServ-Based
- 1/2/4-Queue QoS Prioritization Selection
- Programmable Weighted Fair Queuing for Ratio Control
- Re-Mapping of 802.1p Priority Field Per Port Basis

Integrated 5-Port 10/100 Ethernet Switch

- New Generation Switch with Five MACs and Five PHYs that are Fully Compliant with the IEEE 802.3u Standard
- PHYs Designed with Patented Enhanced Mixed-Signal Technology
- Non-Blocking Switch Fabric Ensures Fast Packet Delivery by Utilizing a 1K MAC Address Lookup Table and a Store-and-Forward Architecture
- On-Chip 64Kbyte Memory for Frame Buffering (Not Shared with 1K Unicast Address Table)
- Full-Duplex IEEE 802.3x Flow Control (PAUSE) with Force Mode Option
- Half-Duplex Back Pressure Flow Control
- HP Auto MDI/MDI-X and IEEE Auto Crossover Support
- SW-MII Interface Supports Both MAC Mode and PHY Mode
- 7-Wire Serial Network Interface (SNI) Support for Legacy MAC
- Per Port LED Indicators for Link, Activity, and 10/100 Speed
- Register Port Status Support for Link, Activity, Full-/Half-Duplex and 10/100 Speed
- LinkMD® Cable Diagnostic Capabilities
- On-Chip Terminations and Internal Biasing Technology for Cost Down and Lowest Power Consumption

Switch Monitoring Features

- Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port or MII
- MIB Counters for Fully Compliant Statistics Gathering; 34 MIB Counters Per Port
- Loopback Support for MAC, PHY, and Remote Diagnostic of Failure
- Interrupt for the Link Change on Any Ports

Low-Power Dissipation

- Full-Chip Hardware Power-Down
- Full-Chip Software Power-Down and Per Port Software Power-Down
- Energy-Detect Mode Support <100 mW Full-Chip Power Consumption When All Ports Have No

Activity

- Very-Low Full-Chip Power Consumption (<0.5W) in Standalone 5-Port, without Extra Power Consumption on Transformers
- Dynamic Clock Tree Shutdown Feature
- Voltages: Single 3.3V Supply with 3.3V V_{DDIO} and Internal 1.2V LDO Controller Enabled, or External 1.2V LDO Solution
  - Analog V_{DDAT} 3.3V Only
  - V_{DDIO} Support 3.3V, 2.5V, and 1.8V
  - Low 1.2V Core Power
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 128-pin PQFP and 128-pin LQFP, Lead-Free Packages

Target Applications

- Typical
- VoIP Phone
- Set-Top/Game Box
- Industrial Control
- IPTV POF
- SOHO Residential Gateway
- Broadband Gateway/Firewall/VPN
- Integrated DSL/Cable Modem
- Wireless LAN Access Point + Gateway
- Standalone 10/100 5-Port Switch

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ8895MQX/RQX/FQX/MLX is a highly-integrated, Layer 2 managed, five-port switch with numerous features designed to reduce system cost. Intended for cost-sensitive 10/100Mbps five-port switch systems with low power consumption, on-chip termination, and internal core power controllers, it supports high-performance memory bandwidth and shared memory-based switch fabric with non-blocking configuration. Its extensive feature set includes power management, programmable rate limit and priority ratio, tag/port-based VLAN, packets filtering, four-queue QoS prioritization, management interfaces, and MIB counters. The KSZ8895 family provides multiple CPU data interfaces to effectively address both current and emerging fast Ethernet applications when Port 5 is configured to separate MAC5 with SW5-MII/RMII and PHY5 with P5-MII/RMII interfaces.

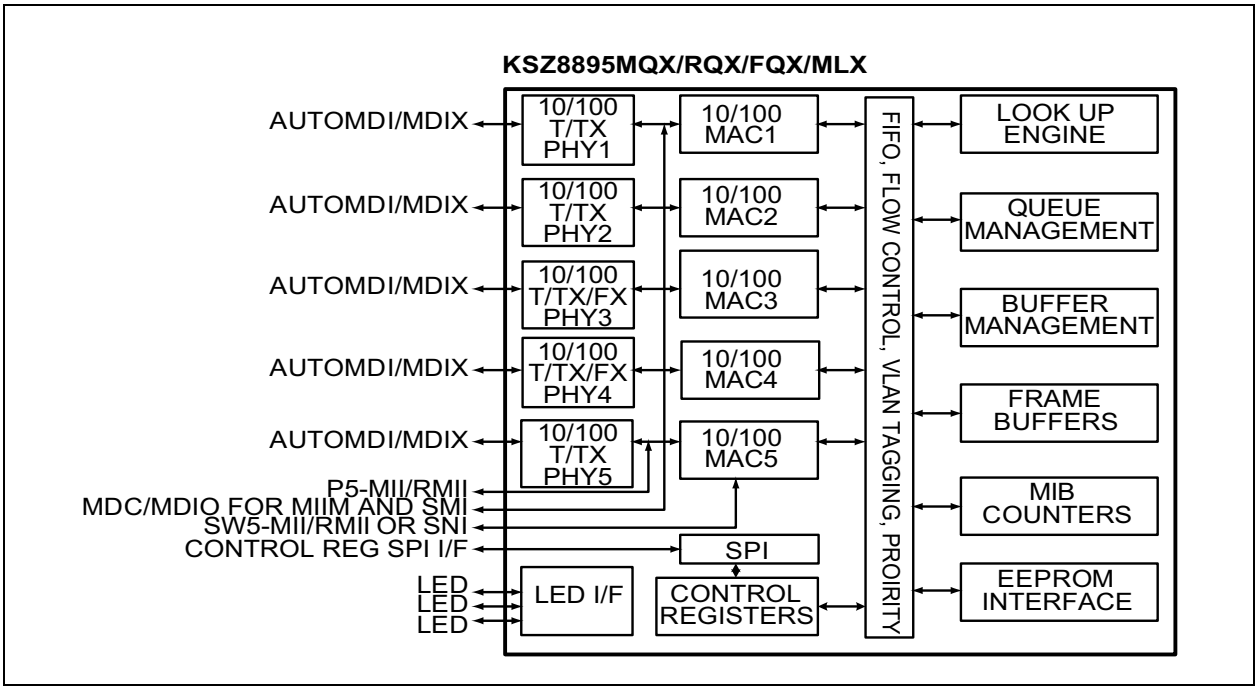
The KSZ8895 family offers three configurations, providing the flexibility to meet different requirements:

- KSZ8895MQX/MLX: Five 10/100Base-T/TX transceivers, One SW5-MII, and One P5-MII interface
- KSZ8895RQX: Five 10/100Base-T/TX transceivers, One SW5-RMII, and One P5-RMII interface
- KSZ8895FQX: Four 10/100Base-T/TX transceivers on Ports 1, 2, 3, and 5 (port 3 can be set to fiber mode). One 100Base-FX transceiver on Port 4. One SW5-MII and One P5-MII interface

All registers of MACs and PHYs units can be managed by the SPI or the SMI interface. MIIM registers can be accessed through the MDC/MDIO interface. EEPROM can set all control registers for the unmanaged mode.

KSZ8895MQX/RQX/FQX are available in the 128-pin PQFP package. KSZ8895MLX is available as a 128-pin LQFP package.

FIGURE 1-1: FUNCTIONAL DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 128-PQFP PIN ASSIGNMENT (TOP VIEW)

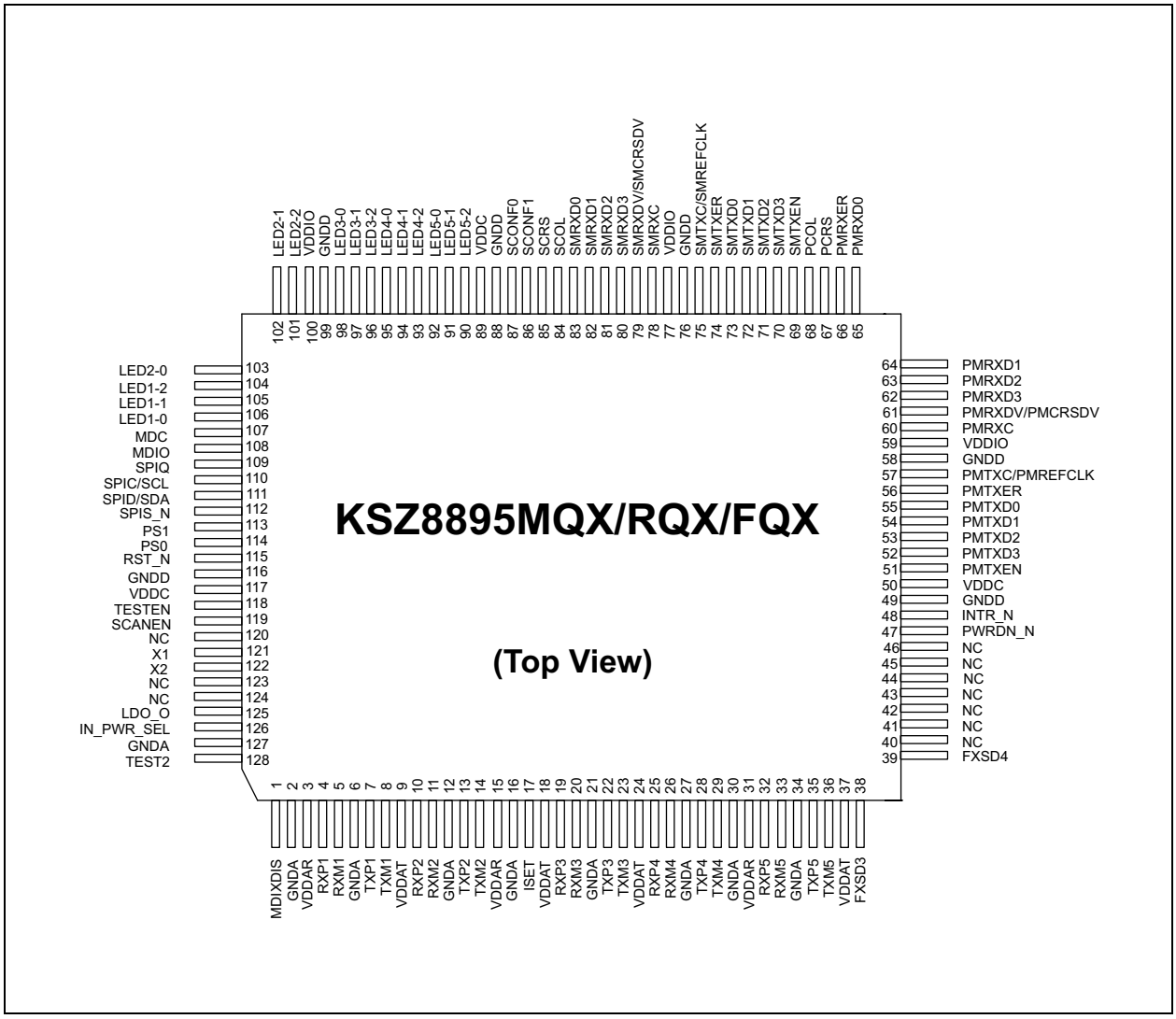


FIGURE 2-2: 128-LQFP PIN ASSIGNMENT (TOP VIEW)

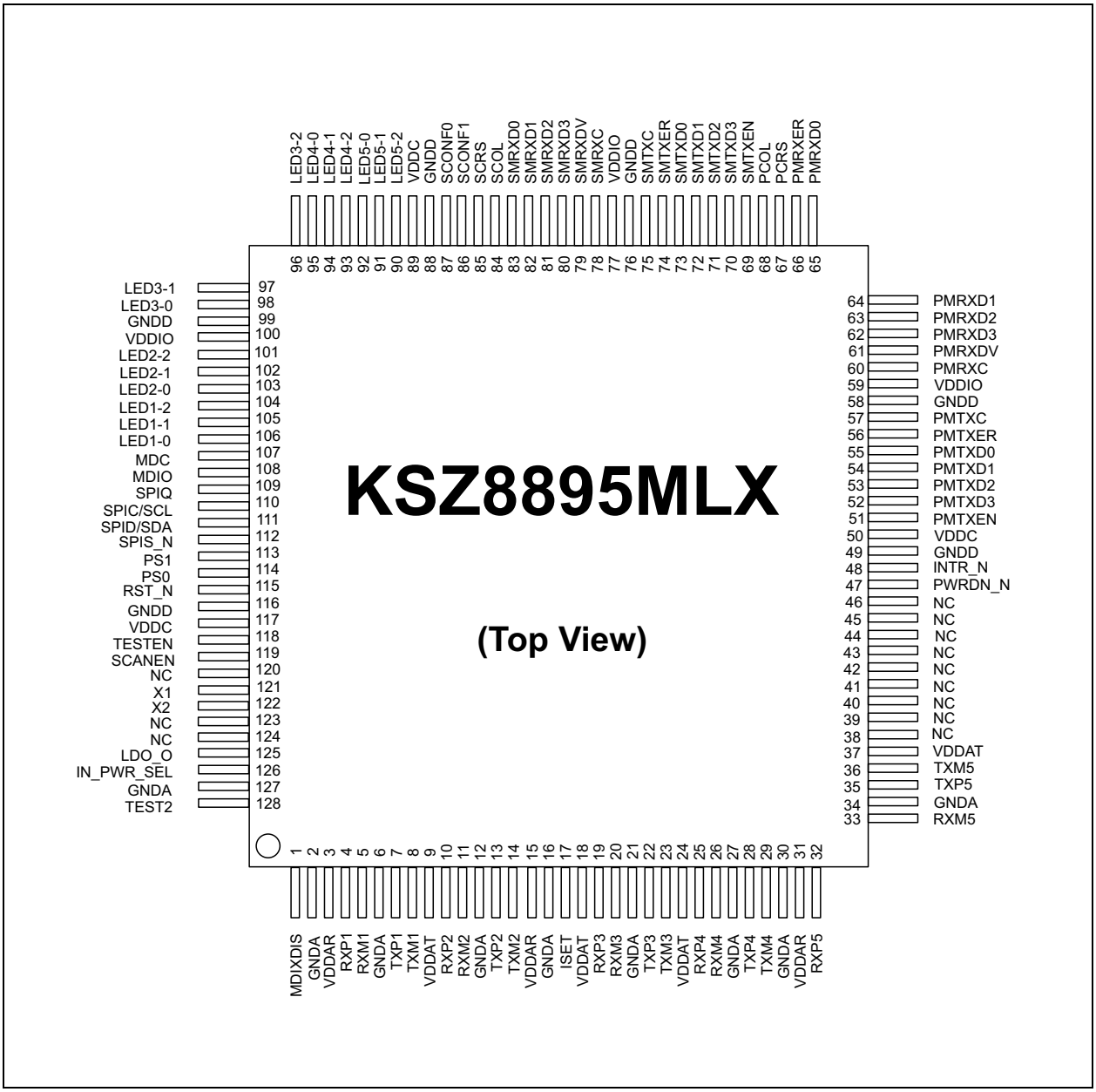


TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
1	MDI-XDIS	IPD	1 - 5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GNDA	GND	—	Analog ground.

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
3	VDDAR	P	—	1.2V analog V_{DD}.
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal - (differential).
6	GNDA	GND	—	Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal - (differential).
9	VDDAT	P	—	3.3V analog V_{DD}.
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal - (differential).
12	GNDA	GND	—	Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal - (differential).
15	VDDAR	P	—	1.2V analog V_{DD}.
16	GNDA	GND	—	Analog ground.
17	ISET	—	—	Set physical transmit output current. Pull-down with a 12.4 kΩ 1% resistor.
18	VDDAT	P	—	3.3V analog V_{DD}.
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal - (differential).
21	GNDA	GND	—	Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal - (differential).
24	VDDAT	P	—	3.3V analog V_{DD}.
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal - (differential).
27	GNDA	GND	—	Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal - (differential).
30	GNDA	GND	—	Analog ground.
31	VDDAR	P	—	1.2V analog V_{DD}.
32	RXP5	I	5	Physical receive signal + (differential).

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
33	RXM5	I	5	Physical receive signal - (differential).
34	GNDA	GND	—	Analog ground.
35	TXP5	O	5	Physical transmit signal + (differential).
36	TXM5	O	5	Physical transmit signal - (differential).
37	VDDAT	P	—	3.3V analog V_{DD}.
38	NC/FXSD3	IPD	3	FQX: This pin can be floating when port 3 is used as copper port (default). Port 3 can be set to fiber mode by Register 239 bit [7], this pin is used for fiber signal detect pin on Port 3 in Fiber mode. MQX/RQX/MLX: no connection.
39	FXSD4	IPD	4	FQX: Fiber signal detect pin for Port 4. MQX/RQX/MLX: no connection.
40	NC	NC	—	No connection. Leave NC pin floating.
41	NC	NC	—	No connection. Leave NC pin floating.
42	NC	NC	—	No connection. Leave NC pin floating.
43	NC	NC	—	No connection. Leave NC pin floating.
44	NC	NC	—	No connection. Leave NC pin floating.
45	NC	NC	—	No connection. Leave NC pin floating.
46	NC	NC	—	No connection. Leave NC pin floating.
47	PWRDN_N	IPU	—	Full-chip power down. Active low.
48	INTR_N	OPU	—	Interrupt. This pin is Open-Drain output pin.
49	GNDD	GND	—	Digital ground.
50	VDDC	P	—	1.2V digital core V_{DD}.
51	PMTXEN	IPD	5	PHY [5] MII/RMII transmit enable.
52	PMTXD3	IPD	5	MQX/FQX/MLX: PHY [5] MII transmit bit 3. RQX: no connection for RMII.
53	PMTXD2	IPD	5	MQX/FQX/MLX: PHY [5] MII transmit bit 2. RQX: no connection for RMII.
54	PMTXD1	IPD	5	PHY [5] MII/RMII transmit bit 1.
55	PMTXD0	IPD	5	PHY [5] MII/RMII transmit bit 0.
56	PMTXER	IPD	5	MQX/FQX/MLX: PHY [5] MII transmit error. RQX: no connection for RMII.
57	PMTXC/ PMREFCLK	I/O	5	MQX/FQX/MLX: Output PHY [5] MII transmit clock RQX: Input PHY [5] RMII reference clock, 50 MHz ±50 ppm, the 50 MHz clock comes from PMRXC Pin 60.
58	GNDD	GND	—	Digital ground.

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
59	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry.
60	PMRXC	I/O	5	MQX/FQX/MLX: Output PHY [5] MII receive clock. RQX: Output PHY [5] RMII reference clock, this clock is used when opposite doesn't provide RMII 50 MHz clock or the system doesn't provide an external 50 MHz clock for the P5-RMII interface.
61	PMRXDV/ PMCRSDV	IPD/O	5	MQX/FQX/MLX: PMRXDV is for PHY [5] MII receive data valid. RQX: PMCRSDV is for PHY [5] RMII Carrier Sense/Receive Data Valid Output.
62	PMRXD3	IPD/O	5	MQX/FQX/MLX: PHY [5] MII receive bit 3. RQX: no connection for RMII. Strap option: PD (default) = enable flow control. PU = disable flow control.
63	PMRXD2	IPD/O	5	MQX/FQX/MLX: PHY [5] MII receive bit 2. RQX: no connection for RMII. Strap option: PD (default) = disable back pressure. PU = enable back pressure.
64	PMRXD1	IPD/O	5	MQX/FQX/MLX: PHY [5] MII receive bit 1. RQX: PHY [5] RMII receive bit 1. Strap option: PD (default) = drop excessive collision packets. PU = does not drop excessive collision packets.
65	PMRXD0	IPD/O	5	MQX/FQX/MLX: PHY [5] MII receive bit 0. RQX: PHY [5] RMII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode. PU = enable for performance enhancement.
66	PMRXER	IPD/O	5	MQX/FQX/MLX:PHY [5] MII receive error RQX: PHY [5] RMII receive error Strap option: PD (default) = packet size 1518/1522 bytes. PU = 1536 bytes.
67	PCRS	IPD/O	5	MQX/FQX/MLX: PHY [5] MII carrier sense. RQX: no connection for RMII. Strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
68	PCOL	IPD/O	5	MQX/FQX/MLX: PHY [5] MII collision detect. RQX: no connection. Strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
69	SMTXEN	IPD	—	Port 5 Switch MII/RMII transmit enable.
70	SMTXD3	IPD	—	MQX/FQX/MLX: Port 5 Switch MII transmit bit 3. RQX: no connection for RMII.
71	SMTXD2	IPD	—	MQX/FQX/MLX: Port 5 Switch MII transmit bit 2. RQX: no connection for RMII.
72	SMTXD1	IPD	—	Port 5 Switch MII/RMII transmit bit 1.
73	SMTXD0	IPD	—	Port 5 Switch MII/RMII transmit bit 0.
74	SMTXER	IPD	—	MQX/FQX/MLX: Port 5 Switch MII transmit error RQX: Port 5 Switch RMII transmit error
75	SMTXC/ SMREFCLK	I/O	—	MQX/FQX/MLX: Port 5 Switch MII transmit clock, Input: SW5-MII MAC mode, Output: SW5-MII PHY modes. RQX: Input SW5-RMII 50MHz ±50 ppm reference clock. The 50 MHz clock comes from SMRXC Pin 78 when the device is the clock mode which the device's clock comes from 25 MHz crystal/ oscillator from Pins X1/X2. Or the 50 MHz clock comes from external 50 MHz clock source when the device is the normal mode which the device's clock source comes from SMTXC pin not from X1/X2 pins.
76	GNDD	GND	—	Digital ground.
77	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry.
78	SMRXC	I/O	—	MQX/FQX/MLX: Port 5 Switch MII receive clock, Input: SW5-MII MAC mode, Output: SW5-MII PHY mode. RQX: Output SW5-RMII 50 MHz clock, this clock is used when opposite doesn't provide RMII reference clock or the system doesn't provide an external 50 MHz clock for the RMII interface.
79	SMRXDV/ SMCRSDV	IPD/O	—	MQX/FQX/MLX: SMRXDV is for Switch MAC5 MII receive data valid. RQX: SMCRSDV is for MAC5 RMII Carrier Sense/Receive Data Valid Output.
80	SMRXD3	IPD/O	—	MQX/FQX/MLX: Port 5 Switch MII receive bit 3. RQX: no connection for RMII Strap option: PD (default) = Disable Switch SW5-MII/RMII full-duplex flow control PU = Enable Switch SW5-MII/RMII full-duplex flow control.
81	SMRXD2	IPD/O	—	MQX/FQX/MLX: Port 5 Switch MII receive bit 2. RQX: no connection for RMII Strap option: PD (default) = Switch SW5-MII/RMII in full-duplex mode; PU = Switch SW5-MII/RMII in half-duplex mode.
82	SMRXD1	IPD/O	—	MQX/FQX/MLX: Port 5 Switch MII receive bit 1. RQX: Port 5 Switch RMII receive bit 1. Strap option: PD (default) = Port 5 Switch SW5-MII/RMII in 100 Mbps mode. PU = Switch SW5-MII/RMII in 10 Mbps mode.

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type, Note 2-1</th><th>Port</th><th colspan="3">Pin Function, Note 2-2</th></tr>
<tr><td rowspan="5">83</td><td rowspan="5">SMRXD0</td><td rowspan="5">IPD/O</td><td rowspan="5">—</td><td colspan="3">MQX/FQX/MLX: Port 5 Switch MII receive bit 0.
RQX: Port 5 Switch RMII receive bit 0
Strap option:
LED mode
PD (default) = mode 0; PU = mode 1. See “Register 11.”
Mode 0, link at:
100/Full LEDx[2,1,0] = 0, 0, 0
100/Half LEDx[2,1,0] = 0, 1, 0
10/Full LEDx[2,1,0] = 0, 0, 1
10/Half LEDx[2,1,0] = 0, 1, 1
Mode 1, link at:
100/Full LEDx[2,1,0] = 0, 1, 0
100/Half LEDx[2,1,0] = 0, 1, 1
10/Full LEDx[2,1,0] = 1, 0, 0
10/Half LEDx[2,1,0] = 1, 0, 1</td></tr>
<tr><td>—</td><td>Mode 0</td><td>Mode 1</td></tr>
<tr><td>LEDx_2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>LEDx_1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>LEDx_0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td>84</td><td>SCOL</td><td>IPD/O</td><td>—</td><td colspan="3">MQX/FQX/MLX: Port switch MII collision detect,
Input: SW5-MII MAC modes, Output: SW5-MII PHY modes
RQX: no connection for RMII</td></tr>
<tr><td>85</td><td>SCRS</td><td>IPD/O</td><td>—</td><td colspan="3">MQX/FQX/MLX: Port switch MII collision detect,
Input: SW5-MII MAC modes, Output: SW5-MII PHY modes
RQX: no connection for RMII</td></tr>
</table>

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type, Note 2-1</th><th>Port</th><th colspan="3">Pin Function, Note 2-2</th></tr>
<tr><td rowspan="10">86</td><td rowspan="10">SCONF1</td><td rowspan="10">IPD</td><td rowspan="10">—</td><td colspan="3">Pins 91, 86, and 87 are dual MII/RMII configuration pins for the Port 5 MAC5 MII/RMII and PHY [5] MII/RMII. SW5-MII supports both MAC mode and PHY modes. P5-MII supports PHY mode only. See pins configuration below:</td></tr>
<tr><td>Pin# (91, 86, 87)</td><td>Port 5 Switch MAC5 SW5- MII/ RMII</td><td>Port5 PHY5 P5- MII/RMII</td></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable (default)</td><td>Disable (default)</td></tr>
<tr><td>101</td><td>PHY Mode MII or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>110</td><td>MAC Mode MII or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>P5-MII/RMII</td></tr>
<tr><td>87</td><td>SCONF0</td><td>IPD</td><td>—</td><td colspan="3">Dual MII/RMII configuration pin. See Pin 86 descriptions.</td></tr>
<tr><td>88</td><td>GNDD</td><td>GND</td><td>—</td><td colspan="3">Digital ground.</td></tr>
<tr><td>89</td><td>VDDC</td><td>P</td><td>—</td><td colspan="3">1.2V digital core V_{DD}.</td></tr>
<tr><td>90</td><td>LED5-2</td><td>IPU/O</td><td>5</td><td colspan="3">LED indicator 2.
Strap option:
Aging setup. See “Aging” section.
PU (default) = aging enable
PD = aging disable.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>IPU/O</td><td>5</td><td colspan="3">LED indicator 1.
Strap option:
PU (default): enable PHY [5] MII I/F.
PD: tri-state all PHY [5] MII output. See “Pin 86 SCONF1.”</td></tr>
<tr><td>92</td><td>LED5-0</td><td>IPU/O</td><td>5</td><td colspan="3">LED indicator 0.
Strap option for port 4 only.
PU (default) = Enable auto-negotiation.
PD = Disable auto-negotiation. Strap to Register76 bit [7].</td></tr>
<tr><td>93</td><td>LED4-2</td><td>IPU/O</td><td>4</td><td colspan="3">LED indicator 2</td></tr>
<tr><td>94</td><td>LED4-1</td><td>IPU/O</td><td>4</td><td colspan="3">LED indicator 1</td></tr>
</table>

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
95	LED4-0	IPU/O	4	LED indicator 0. Strap option: PU (default) = Normal mode. PD = Energy Detection mode (EDPD mode) Strap to Register 14 bits [4:3]
96	LED3-2	IPU/O	3	LED indicator 2.
97	LED3-1	IPU/O	3	LED indicator 1.
98	LED3-0	IPU/O	3	LED indicator 0. Strap option: PU (default) = Select I/O drive strength (8 mA); PD = Select I/O drive strength (12 mA). Strap to Register132 bit [7-6].
99	GNDD	GND	—	Digital ground.
100	VDDIO	P	—	3.3V, 2.5V, or 1.8V digital V_{DD} for digital I/O circuitry.
101	LED2-2	IPU/O	2	LED indicator 2. Strap option for RQX only: PU (default) = Select the device as clock mode in SW5- RMII, 25MHz crystal/oscillator to X1/X2 pins of the device and pins of SMRXC and PMRXC output 50 MHz clock. PD = Select the device as normal mode in SW5-RMII. Switch MAC5 used only. The input clock from X1/X2 pins is not used, the device's clock source comes from SMTXC/SMREFCLK pin which the 50 MHz reference clock comes from external 50 MHz clock source, PMRXC can output 50 MHz clock for P5-RMII interface in the normal mode.
102	LED2-1	IPU/O	2	LED indicator 1. Strap option: for Port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to Register60 bit [7].
103	LED2-0	IPU/O	2	LED indicator 0.
104	LED1-2	IPU/O	1	LED indicator 2.
105	LED1-1	IPU/O	1	LED indicator 1. Strap option: for port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to Register60 bit [4].
106	LED1-0	IPU/O	1	LED indicator 0. Strap option for port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to Register60 bit [5].
107	MDC	IPU	All	PHYs MII management (MIIM registers) data clock. Or SMI interface clock

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
108	MDIO	IPU/O	All	PHYs MII management (MIIM registers) data I/O. Or SMI interface data I/O Note: Need an external pull-up when driven.
109	SPIQ	IPU/O	All	SPI serial data output in SPI slave mode. Note: Need an external pull-up when driven.
110	SPIC/SCL	IPU/O	All	(1) Input clock up to 25 MHz in SPI slave mode, (2) Output clock at 61 kHz in I^2C master mode. See “Pin 113.” Note: Need an external pull-up when driven.
111	SSPID/SDA	IPU/O	All	(1) Serial data input in SPI slave mode; (2) Serial data input/output in I^2C master mode. See “Pin 113.” Note: Need an external pull-up when driven.
112	SPIS_N	IPU	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KSZ8895MQX/RQX/FQX/MLX is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer. (2) not used in I^2C master mode.
113	PS1	IPD	—	Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MQX/RQX/FQX/MLX will start itself with the PS [1:0] = 00 default register values.

Pin Configuration	Serial Bus Configuration
PS[1:0] = 00	I^2C Master Mode for EEPROM
PS[1:0] = 01	SMI Interface Mode
PS[1:0] = 10	SPI Slave Mode for CPU Interface
PS[1:0] = 11	Factory Test Mode (BIST)

114	PS0	IPD	—	Serial bus configuration pin. See “Pin 113.”
115	RST_N	IPU	—	Reset the KSZ8895MQX/RQX/FQX/MLX device. Active low.
116	GNDD	GND	—	Digital ground.
117	VDDC	P	—	1.2V digital core V_{DD}.
118	TESTEN	IPD	—	NC for normal operation. Factory test pin.
119	SCANEN	IPD	—	NC for normal operation. Factory test pin.
120	NC	NC	—	No connection. Leave NC pin floating.
121	X1	I	—	25 MHz crystal clock connection/or 3.3V Oscillator input. Crystal/Oscillator should be ±50 ppm tolerance.
122	X2	O	—	25 MHz crystal clock connection.

TABLE 2-1: SIGNALS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

Pin Number	Pin Name	Type, Note 2-1	Port	Pin Function, Note 2-2
123	NC	NC	—	No connection. Leave NC pin floating.
124	NC	NC	—	No connection. Leave NC pin floating.
125	LDO_O	P	—	LDO_O pin connect to gate pin of MOSFET if using the internal 1.2V LDO controller. LDO_O pin will be floating if using an external 1.2V LDO. Note: When Pin126 voltage is greater than the internal 1.2V LDO controller enable threshold (1V), the internal 1.2V LDO controller is enabled and creates a 1.2V output when using an external MOSFET. When Pin126 is pull-down, the internal 1.2V LDO controller is disabled and Pin 125 tri-stated.
126	IN_PWR_SEL	I	—	A resistor divider: Enable internal 1.2V LDO controller. Pull-down: Disable internal 1.2V LDO controller by a pull-down resistor when using an external 1.2V LDO for 1.2V power supply. Note: A 4 kΩ pull-up and a 2 kΩ pull-down resistors divider network is recommended if using the internal 1.2V LDO controller and an external MOSFET for 1.2V power. A 100Ω (approximately) resistor between the source and drain pins on the MOSFET is highly recommended as well.
127	GNDA	GND	—	Analog ground.
128	TEST2	NC	—	NC for normal operation. Factory test pin.

Note 2-1 P = Power supply.
I = Input.
O = Output.
I/O = Bidirectional.
GND = Ground.
IPU = Input with internal pull-up.
IPD = Input with internal pull-down.
IPD/O = Input with internal pull-down during reset, output pin otherwise.
OTRI = Output tri-stated.

Note 2-2 NC = Do not connect to PCB.
PU = Strap pin pull-up.
PD = Strap pull-down.

The KSZ8895MQX/RQX/FQX/MLX can function as a managed switch or an unmanaged switch. If no EEPROM or micro-controller exists, then the KSZ8895MQX/RQX/FQX/MLX will operate from its default setting. The strap-in option pins can be configured by external pull-up/down resistors and take effect after power down reset or warm reset. The functions are described in the table below.

TABLE 2-2: STRAP-IN OPTIONS - KSZ8895MQX/RQX/FQX/MLX

Pin Number	Pin Name	Type, Note 2-3	Description, Note 2-4
1	MDI-XDIS	IPD	Disable auto MDI/MDI-X. Strap option: PD = (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
62	PMRXD3	IPD/O	PHY [5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
63	PMRXD2	IPD/O	PHY [5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
64	PMRXD1	IPD/O	PHY [5] MII/RMII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
65	PMRXD0	IPD/O	PHY [5] MII/RMII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
66	PMRXER	IPD/O	PHY [5] MII/RMII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.
67	PCRS	IPD/O	PHY [5] MII carrier sense Strap option for Port 4 only PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails. Refer to Register 76.
68	PCOL	IPD/O	PHY [5] MII collision detect Strap option for Port 4 only. PD (default) = no force flow control. PU = force flow control. Refer to Register 66.
80	SMRXD3	IPD/O	Switch MII receive bit 3. Strap option: PD (default) = disable switch SW5-MII/RMII full-duplex flow control; PU = enable switch SW5-MII/RMII full-duplex flow control.
81	SMRXD2	IPD/O	Switch MII receive bit 2. Strap option: PD (default) = switch SW5-MII/RMII in full-duplex mode; PU = switch SW5-MII/RMII in half-duplex mode.
82	SMRXD1	IPD/O	Switch MII/RMII receive bit 1 Strap option: PD (default) = switch SW5-MII/RMII in 100 Mbps mode. PU = switch MII/RMII in 10 Mbps mode.

TABLE 2-2: STRAP-IN OPTIONS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type,
Note 2-3</th><th colspan="3">Description, Note 2-4</th></tr>
<tr><td rowspan="5">83</td><td rowspan="5">SMRXD0</td><td rowspan="5">IPD/O</td><td colspan="3">Switch MII/RMII receive bit 0.
Strap option: LED mode PD (default) = mode 0; PU = mode 1. See “Register 11.”</td></tr>
<tr><td>—</td><td>Mode 0</td><td>Mode 1</td></tr>
<tr><td>LEDx_2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>LEDx_1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>LEDx_0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td rowspan="10">86</td><td rowspan="10">SCONF1</td><td rowspan="10">IPD</td><td colspan="3">Pin 91,86,87 are dual MII/RMII configuration pins for the Port 5 MAC 5 MII/RMII and PHY [5] MII/RMII. SW5-MII supports both MAC mode and PHY modes. P5-MII supports PHY mode only. See pins configuration below.</td></tr>
<tr><td>Pins
[91, 86, 87]</td><td>Port 5 Switch MAC5
SW5- MII/RMII</td><td>Port 5 PHY5 P5-MII/RMII</td></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable (default)</td><td>Disable (default)</td></tr>
<tr><td>101</td><td>PHY Mode MII, or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>110</td><td>MAC Mode MII, or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>P5-MII/RMII</td></tr>
<tr><td>87</td><td>SCONF0</td><td>IPD</td><td colspan="3">Dual MII/RMII configuration pin. See Pin 86 description.</td></tr>
<tr><td>90</td><td>LED5-2</td><td>IPU/O</td><td colspan="3">LED5 indicator 2.
Strap option: Aging setup. See “Aging” section
PU (default) = aging enable;
PD = aging disable.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>IPU/O</td><td colspan="3">LED5 indicator 1.
Strap option:
PU (default): enable PHY [5] MII I/F.
PD: Tri-state all PHY [5] MII output. See “Pin 86 SCONF1.”</td></tr>
<tr><td>92</td><td>LED5-0</td><td>IPU/O</td><td colspan="3">LED5 indicator 0.
Strap option for Port 4 only.
PU (default) = Enable auto-negotiation.
PD = Disable auto-negotiation. Strap to Register76 bit [7].</td></tr>
<tr><td>95</td><td>LED4-0</td><td>IPU/O</td><td colspan="3">LED indicator 0.
Strap option:
PU (default) = Normal mode.
PD = Energy Detection mode (EDPD mode).
Strap to Register 14 bits [4:3].</td></tr>
<tr><td>98</td><td>LED3-0</td><td>IPU/O</td><td colspan="3">LED3 indicator 0.
Strap option:
PU (default) = Select I/O current drive strength (8 mA);
PD = Select I/O current drive strength (12 mA).
Strap to Register132 bit [7:6].</td></tr>
</table>

TABLE 2-2: STRAP-IN OPTIONS - KSZ8895MQX/RQX/FQX/MLX (CONTINUED)

Pin Number	Pin Name	Type, Note 2-3	Description, Note 2-4
101	LED2-2	IPU/O	LED2 indicator 2. Strap option for KSZ8895RQX only: PU (default) = Select the device as clock mode in RQX SW5- RMII, 25 MHz crystal to X1/X2 pins of the device and REFCLK output 50 MHz clock. PD = Select the device as normal mode in SW5-RMII. Switch MAC5 used only. The input clock is useless from X1/X2 pin, the device's clock comes from SMTXC/SMREFCLK pin, 50 MHz reference clock from external 50 MHz clock source.
102	LED2-1	IPU/O	LED2 indicator 1. Strap option for Port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to Register60 bit [7].
105	LED2-0	IPU/O	LED1 indicator 1. Strap option for Port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to Register50 bit [4].
106	LED1-0	IPU/O	LED1 indicator 0. Strap option for Port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to Register60 bit [5].
113	PS1	IPD	Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MQX/RQX/FQX/MLX will start itself with the PS[1:0] = 00 default register values. **Pin Configuration** / **Serial Bus Configuration** PS[1:0] = 00 / I^2C Master Mode for EEPROM PS[1:0] = 01 / SMI Interface Mode PS[1:0] = 10 / SPI Slave Mode for CPU Interface PS[1:0] = 11 / Factory Test Mode (BIST)
114	PS0	IPD	Serial bus configuration pin. See "Pin 113."
128	TEST2	NC	NC for normal operation. Factory test pin.

Note 2-3 NC = No connect.
IPD = Input with internal pull-down.
IPU/O = Input with internal pull-up during reset; output pin otherwise.
IPD/O = Input with internal pull-down during reset; output pin otherwise.

Note 2-4 NC = Do not connect to PCB.
PU = Strap pin pull-up.
PD = Strap pin pull-down.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8895MQX/RQX/FQX/MLX contains five 10/100 physical layer transceivers and five media access control (MAC) units with an integrated Layer 2 managed switch. The device runs in three modes. The first mode is as a five-port integrated switch. The second is as a five-port switch with the fifth port decoupled from the physical port. In this mode, access to the fifth MAC is provided through a media independent interface (MII/RMII). This is useful for implementing an integrated broadband router. The third mode uses the dual MII/RMII feature to recover the use of the fifth PHY. This allows the additional broadband gateway configuration, where the fifth PHY may be accessed through the P5-MII/RMII port.

The KSZ8895MQX/RQX/FQX/MLX has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the KSZ8895MQX/RQX/FQX/MLX via the SPI bus, or the MDC/MDIO interface. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KSZ8895MQX/RQX/FQX/MLX supports IEEE 802.3 10BASE-T, 100BASE-TX on all copper ports with Auto MDI/MDIX. The KSZ8895FQX supports 100BASE-FX on port 4, and port 3 is configurable either copper as default or fiber. The KSZ8895MQX/RQX/FQX/MLX can be used as a fully managed five-port switch or hooked up to a microprocessor by its SW-MII/RMII interfaces for any application solutions.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry and DSP technology that make the design more efficient and allows for reduced power consumption and strong electrical noise immunity.

Major enhancements from the KS8995MQ/RQ/FMQ to the KSZ8895MQX/RQX/FQX include more saving power, there is no a limitation for the center taps of the transformer in KSZ8895MQX/RQX/FQX, KSZ8895MQ/RQ/FMQ request the center taps of RX an TX of the transformer not to be tied together for saving power, except using 0.11 µm process and add Microchip LinkMD feature in KSZ8895MQX/RQX/FQX switches. The KSZ8895MQX/RQX/FQX are complete compatible with KSZ8895MQ/RQ/FMQ.

3.1 Physical Layer Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 12.4 kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, descrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for intersymbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.1.3 PLL CLOCK SYNTHESIZER

The KSZ8895MQX/RQX/FQX/MLX generates 125 MHz, 83 MHz, 41 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator.

3.1.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then descramble the incoming data stream with the same sequence at the transmitter.

3.1.5 100BASE-FX OPERATION

100BASE-FX operation is very similar to 100BASE-TX operation except that the scrambler/descrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode, the auto-negotiation feature is bypassed since there is no standard that supports fiber auto-negotiation.

3.1.6 100BASE-FX SIGNAL DETECTION

The physical port runs in 100BASE-FX fiber mode for the Port 3 and Port 4 of the KSZ8895FQX. This signal is internally referenced to 1.2V. The fiber module interface should be set by a voltage divider such that FXSDx ‘H’ is above this 1.2V reference, indicating signal detect, and FXSDx ‘L’ is below the 1.2V reference to indicate no signal. There is no auto-negotiation for 100BASE-FX mode, the ports must be forced to either full or half-duplex for the fiber ports. Note that strap-in options support Port 3 and Port 4 to disable auto-negotiation, force 100Base-FX speed, force duplex mode, and force flow control for KSZ8895FQX with unmanaged mode.

3.1.7 100BASE-FX FAR END FAULT

Far end fault occurs when the signal detection is logically false from the receive fiber module. When this occurs, the transmission side signals the other end of the link by sending 84 1s followed by a zero in the idle period between frames. The far end fault may be disabled through register settings.

3.1.8 10BASE-T TRANSMIT

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

3.1.9 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8864CNX/RMNUB decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.1.10 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8895MQX/RQX/FQX/MLX supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8895MQX/RQX/FQX/MLX device. This feature is extremely useful when end users are unaware of cable types and saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers or MIIM PHY registers. The IEEE 802.3u standard MDI and MDI-X definitions are:

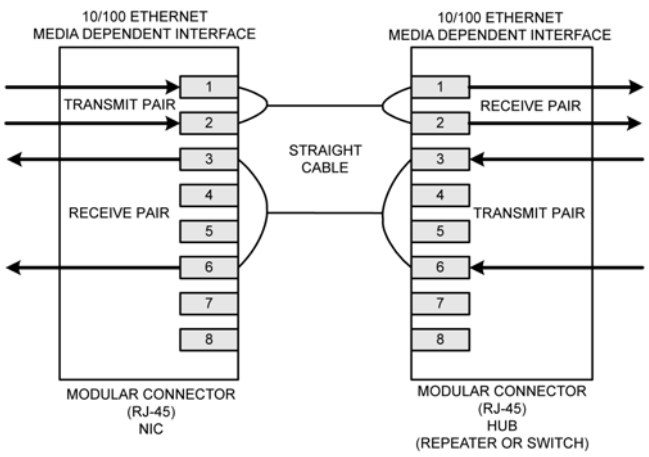
TABLE 3-1: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.1.10.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

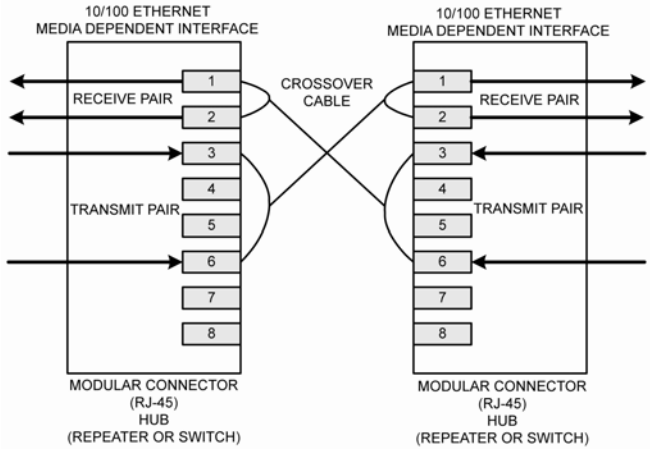
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.1.10.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



3.1.11 AUTO-NEGOTIATION

The KSZ8895MQX/RQX/FQX/MLX conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation. Auto-negotiation is supported for the copper ports only.

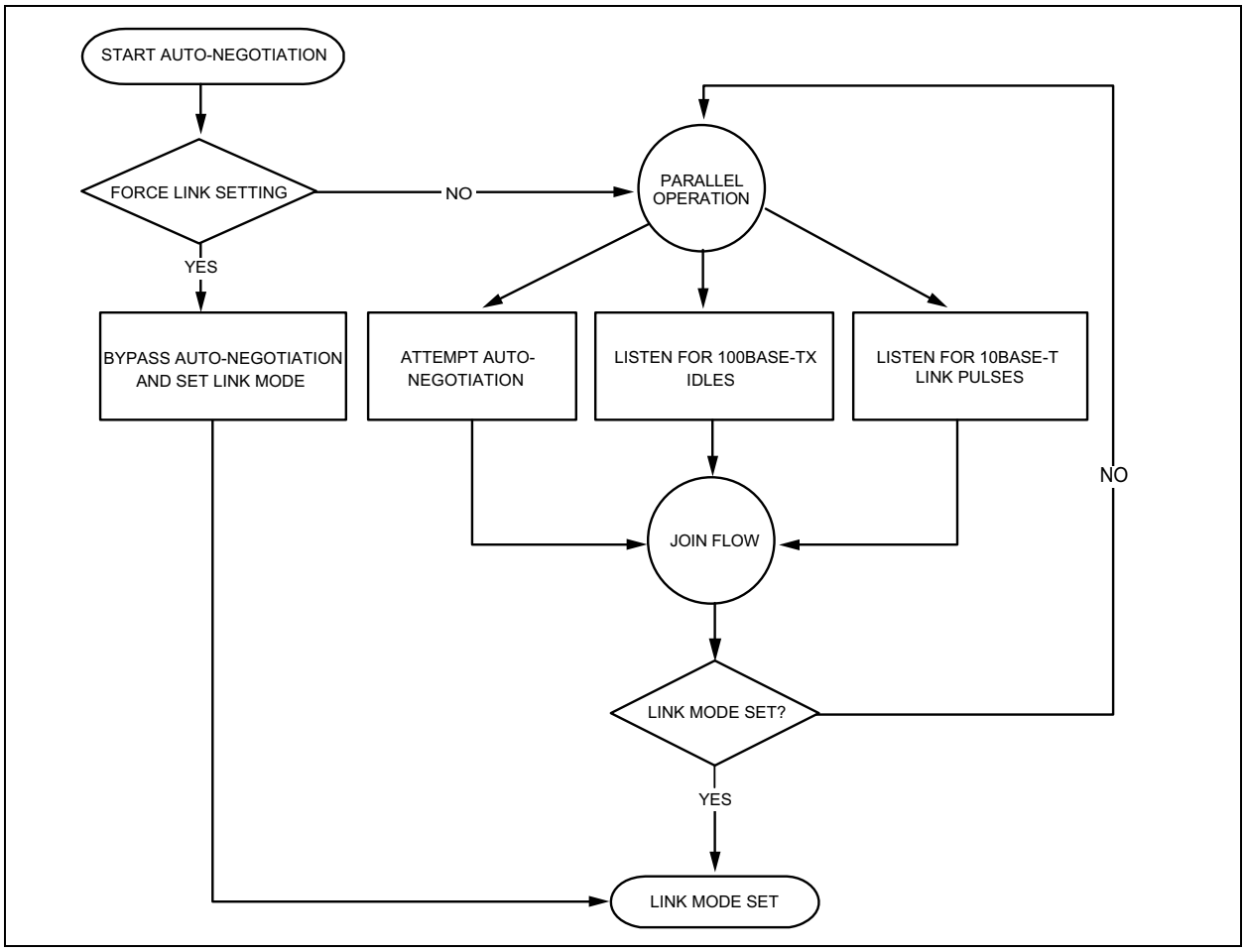
The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex

- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ8895MQX/RQX/FQX/MLX link partner is forced to bypass auto-negotiation, the KSZ8895MQX/RQX/FQX/MLX sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8895MQX/RQX/FQX/MLX to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. The auto-negotiation link up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION FLOW CHART



3.1.12 LINKMD® CABLE DIAGNOSTICS

The LinkMD® feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with maximum distance of 200m and accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format.

Note: Cable diagnostics are only valid for copper connections and do not support fiber optic operation.

3.1.12.1 Access

LinkMD® is initiated by accessing the PHY special control/status Registers {26, 42, 58, 74, 90} and the LinkMD result Registers {27, 43, 59, 75, 91} for ports 1, 2, 3, 4 and 5 respectively; and in conjunction with the Registers Port Control 12 and 13 for ports 1, 2, 3, 4 and 5 respectively to disable Auto-Negotiation and Auto MDI/MDI-X.

Alternatively, the MIIM PHY Registers 0 and 1d can be used for LinkMD® access also.

3.1.12.2 Usage

The following is a sample procedure for using LinkMD with Registers {26, 27, 28, 29} on port 1.

1. Disable Auto-Negotiation by writing a '1' to Register 28 (0x1c), bit [7].
2. Disable auto MDI/MDI-X by writing a '1' to Register 29 (0x1d), bit [2] to enable manual control over the differential pair used to transmit the LinkMD® pulse.
3. A software sequence set up to the internal registers for LinkMD only, see an example below.
4. Start cable diagnostic test by writing a '1' to Register 26 (0x1a), bit [4]. This enable bit is self-clearing.
5. Wait (poll) for Register 26 (0x1a), bit [4] to return a '0', and indicating cable diagnostic test is completed.
6. Read cable diagnostic test results in Register 26 (0x1a), bits [6:5]. The results are as follows:

   00 = normal condition (valid test)

   01 = open condition detected in cable (valid test)

   10 = short condition detected in cable (valid test)

   11 = cable diagnostic test failed (invalid test)

The '11' case, invalid test, occurs when the KSZ8895 is unable to shut down the link partner. In this instance, the test is not run, because it would be impossible for the KSZ8895 to determine if the detected signal is a reflection of the signal generated or a signal from another source.

7. Get distance to fault by concatenating Register 26 (0x1a), bit [0] and Register 27 (0x1b), bits [7:0]; and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

   D (distance to cable fault) = 0.4 x {(Register 26, bit [0]),(Register 27, bits [7:0])}

D (distance to cable fault) is expressed in meters.

Concatenated value of Registers 26 bit [0] and 27 bit [7:0] should be converted to decimal before decrease 26 and multiplying by 0.4.

The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

For port 2, 3, 4, 5 and for the MIIM PHY registers, LinkMD® usage is similar.

3.1.12.3 A LinkMD Example

The following is a sample procedure for using LinkMD on port 1.

```
//Set Force 100/Full and Force MDI-X mode
//W is WRITE the register. R is READ register
W 1c ff
W 1d 04
//Set Internal Registers Temporary Adjustment for LinkMD
W 47 b0
W 27 00
W 37 04 (03-port 1, 04-port 2, 05-port 3, 06-port 4, 07-port 5)
W 47 80 (bit7-port 1, bit6-port 2, bit5-port 3, bit4-port 4, bit3-port 5)
W 27 00
W 37 00
//Enable LinkMD Testing with Fault Cable for port 1
W 1a 10
R 1a
R 1b
//Result analysis based on the values of the Register 0x1a and 0x1b for port 1:
//The Register 0x1a bits [6-5] are for the open or the short detection.
//The Register 0x1a bit [0] + the Register 0x1b bits [7-0] = Vct_Fault [8-0]
//The distance to fault is about 0.4 x {Vct_Fault [8-0]}
```

Note: After testing ends, set all registers above to their default values. The default values are ‘00’ for the Register (0x37) and the Register (0x47)

3.1.13 ON-CHIP TERMINATION RESISTORS

The KSZ8895MQX/RQX/FQX/MLX reduces the board cost and simplifies the board layout by using on-chip termination resistors for all ports and RX/TX differential pairs without the external termination resistors. The combination of the on-chip termination and internal biasing will save power consumption as compared to using external biasing and termination resistors, and the transformer will not consume power any more. The center tap of the transformer does not need to be tied to the analog power and does not tie the center taps together between RX and TX pairs for its application.

3.1.14 INTERNAL 1.2V LDO CONTROLLER

The KSZ8895MQX/RQX/FQX/MLX reduces board cost and simplifies board layout by integrating an internal 1.2V LDO controller to drive a low cost MOSFET to supply the 1.2V core power voltage for a single 3.3V power supply solution.

The internal 1.2V LDO controller can be disabled by Pin 126 IN_PWR_SEL pull-down in order to use an external 1.2V LDO.

3.2 Power

The KSZ8895 device has two options for the power circuit in the design. one is a single 3.3V supply with 3.3V I/O power by using internal 1.2V LDO controller and one MOSFET for 1.2V analog and digital power. Another one is using external 1.2V LDO and provide 1.2V power for 1.2V analog and digital power. Table 3-2 illustrates the various voltage options and requirements of the device.

TABLE 3-2: VOLTAGES AND POWER PINS

Power Signal Name	Device Pins	Requirement
VDDAT	9, 18, 24, 37	3.3V analog power to the transceiver of the device.
VDDIO	59, 77, 100	Choice of 1.8V or 2.5V or 3.3V for the I/O circuits. These input power pins power the I/O circuitry of the device.
VDDAR	3, 15, 31	Filtered 1.2V analog voltage. This is where filtered 1.2V is fed back into the device to power the analog block.
VDDC	50, 89, 117	Filtered 1.2V digital voltage. This pin feeds 1.2V to digital circuits within the analog block.
GNDA	2, 6, 12, 16, 21, 27, 30, 34, 127	Analog Ground.
GNDD	49, 58, 76, 88, 99, 116	Digital Ground.

3.2.1 USING INTERNAL 1.2V LDO CONTROLLER

The preferred method of using the internal 1.2V LDO controller with an external MOSFET is illustrated in the figure below. The number of capacitors, ferrite beads (FB), values of capacitors, and exact placement of components will depend on the specific design. The 1.2V rail from the drain pin of the MOSFET to VDDAR Pin 3 is the 1.2V LDO feedback path. This connection should be as short as possible and there should be no series components on this feedback path. When the voltage of Pin 126 is just over 1V, along with the 3.3V power-up, the internal 1.2V LDO controller is enabled. The 1.2V LDO regulator (internal 1.2V LDO controller plus an external MOSFET) requests about 3.0V voltage at the ‘S’ pin of MOSFET when the internal 1.2V LDO controller is just enabled, the resistor divider will meet this requirement.