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KS8993F/KS8993FL

Single Chip Fast Ethernet Media Converter with TS-1000 OAM

Revision 1.3

General Description

The Micrel KS8993F is the industry's first single chip Fast Ethernet Media Converter with built-in OAM functions. The KS8993F integrates three MACs, two PHYs, OAM, frame buffer and high performance switch into a single chip. It is ideal for use in 100BASE-FX to 10BASE-T or 100BASE-TX conversion in the FTTx market.

The KS8993F provides remote loop back and OAM (Operation, Administration and Maintenance) to manage subscriber access network from carrier center side to terminal side.

The KS8993F supports advanced features such as rate limiting, force flow control and link transparency.

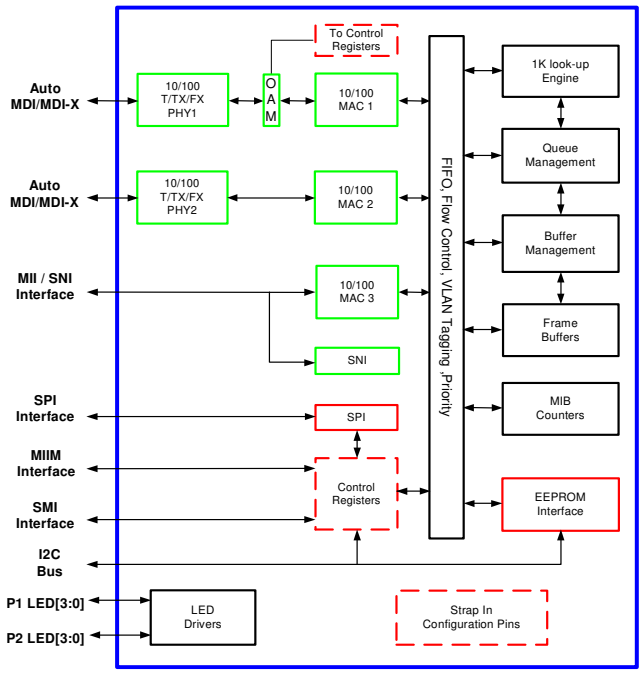
The KS8993F with built-in Layer 2 switch capability will filter packets and forward them to valid destination. It will discard any unwanted frames and frames with invalid destination.

The KS8993FL is the single supply version with all the identical rich features of the KS8993F.

Features

- First single-chip 10BASE-T/100BASE-TX to 100BASE-FX media converter with TS-1000 OAM
- Integrated 3-Port 10/100 Ethernet Switch with 3 MACs and 2 PHYs
- Unique User Defined Register (UDR) feature brings OAM to low cost/complexity nodes
- Automatic MDI/MDI-X crossover with disable and enable option
- Non-blocking switch fabric assures fast packet delivery by utilizing an 1K MAC Address lookup table and a store-and-forward architecture
- Comprehensive LED indicator support for link, activity, full/half duplex and 10/100 speed
- Full complement of MII/SNI, SPI, MIIM, SMI and I2C interfaces
- Low Power Dissipation:< 800mW (includes PHY transmit drivers)

Block Diagram



KS8993F / KS8993FL

Features (continued)

- **OAM Features:**
- Supports OAM sub-layer which conforms to TS-1000 specification from TTC (Telecommunication Technology Committee)
- Sends and receives OAM frames to Center or Terminal side
- Loop back mode to support loop back packet from Center side to Terminal side
- Far-end fault detection with disable and enable
- Link Transparency to indicate the link down from link partner
- **Comprehensive Configuration Register access:**
- Serial Management Interface (SMI) to all internal registers
- MII Management (MIIM) Interface to PHY registers
- SPI and I2C Interface to all internal registers
- I/0 Pins Strapping and EEPROM to program selective registers in unmanaged switch mode
- Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…)
- **QoS / CoS packets prioritization support**
- per-port, 802.1p and DiffServ based
- Re-mapping of 802.1p priority field per-port basis
- **Advanced Switch Features**
- IEEE 802.1q VLAN support for up to 16 groups (full-range of VLAN ID)
- VLAN ID tag/untag options, per-port basis
- IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
- Programmable Rate Limiting from 0 to 100 Mbps at the ingress & egress port, rate options for high & low priority, per port basis
- Broadcast storm protection with % control (global & per-port basis)
- Double Tagging support
- **Switch Management Features:**
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
- MIB (Management Information Base) counters for fully compliant statistics gathering, 34 MIB counters per port
- Full-chip hardware power-down (register configuration not saved)
- Per-port based software power-save on PHY (idle link detection, register configuration preserved)
- 0.18um CMOS technology
- Voltages:
  - Core 1.8V
  - I/O and Transceiver 3.3V
- **Available in 128-pin PQFP**

Ordering Information

Part Number		Temperature Range	Package
Pb-Free	**Standard**		
KSZ8993F	KS8993F	0^{o}– 70^{o} C	128-PQFP
KSZ8993FL	KS8993FL	0^{o}– 70^{o} C	128-PQFP

Revision History

Revision	Date	Summary of Changes
P0	1/14/03	Preliminary Information
P1	2/11/03	Added separate Link and activity on port 1 and port 2's LED (pin #20, pin #23, pin #25). Added disable auto MDI/MDIX (pin #28) Added select of MDI and MDIX (pin #29)
P2	4/1/03	Updated register information
P3	12/4/03	Started overhaul of datasheet. Updated strap option definition for pin #85. Renamed supply voltages and ground references to match schematics. Corrected Remote Loop back path. Updated MC registers descriptions. Changed 3.3V voltage pins to (3.3V or 2.5V).
P4	3/11/04	Completed overhaul of datasheet. Revised datasheet format. Updated KS8993F block diagram. Updated Feature Highlights. Updated MC registers descriptions. Updated Electrical Characteristics (Vih, Vil, Voh, Vol).
P5	3/23/04	Updated MC loop back description in pin #19 and register 11 bits[3:2], and path in loop back diagram. Updated flow diagram for Destination Address resolution flowchart, stage2. Changed S10 status bit from RO to R/W in register 81 bit[2]. Added KS8993FL to General Description (page 1) and Functional Description Overview (section 2.1). Updated pin description for pin 22 to the following: VDDC : For KS8993F, this is an input power pin for the 1.8V digital core VDD. VOUT_1V8 : For KS8993FL, this is an 1.8V output power pin to supply the KS8993FL's input power pins: VDDAP (pin 63), VDDC (pins 91, 123) and VDDA (pins 38, 43, 57). Improved/clarified pin description.
1.0	8/26/04	Updated PPM spec for 25 MHz crystal/oscillator. Improved/clarified pin description for P1LCRCD (pin 18), P2MDIX (pin 29) and MDIO (pin 95). Corrected aging time. Removed loop back support from MIIM and Port Control Registers, so that there is no confusion with MC loop back which is used exclusively in KS8993F application. Updated HWPOVR description in section 2.2.5. Corrected default definition for FEF in section 2.3.6, and MIIM and Port Control Registers. Added register note to indicate port sniffing is not supported if the unicast packets can cross VLAN boundary bit is set. Improved/clarified switch/PHY registers descriptions for Force MDIX and CRC drop. Improved/clarified MC registers descriptions for Remote Command (registers 74, 75, 76), My Status (registers 80, 81) and LNK Partner Status (registers 88, 89). Added register note to set Register 85: My Model Info (1) to values of 0x22, 0x26, 0x2A and 0x2E if the Remote Command feature is used. Updated MIB counters descriptions to indicate counter overflow must be tracked by application.
1.1	4/7/05	Corrected VDDIO, VDDATX, VDDARX supply pins to 3.3V only. Updated reset timing requirement. Corrected 10BASE-T Transmitter Jitters Added.
1.2	5/22/06	Removed Industrial Temperature line from Features and Ordering info.
1.3	6/25/09	Add the parts KSZ8993F, KSZ8993FL on the order information

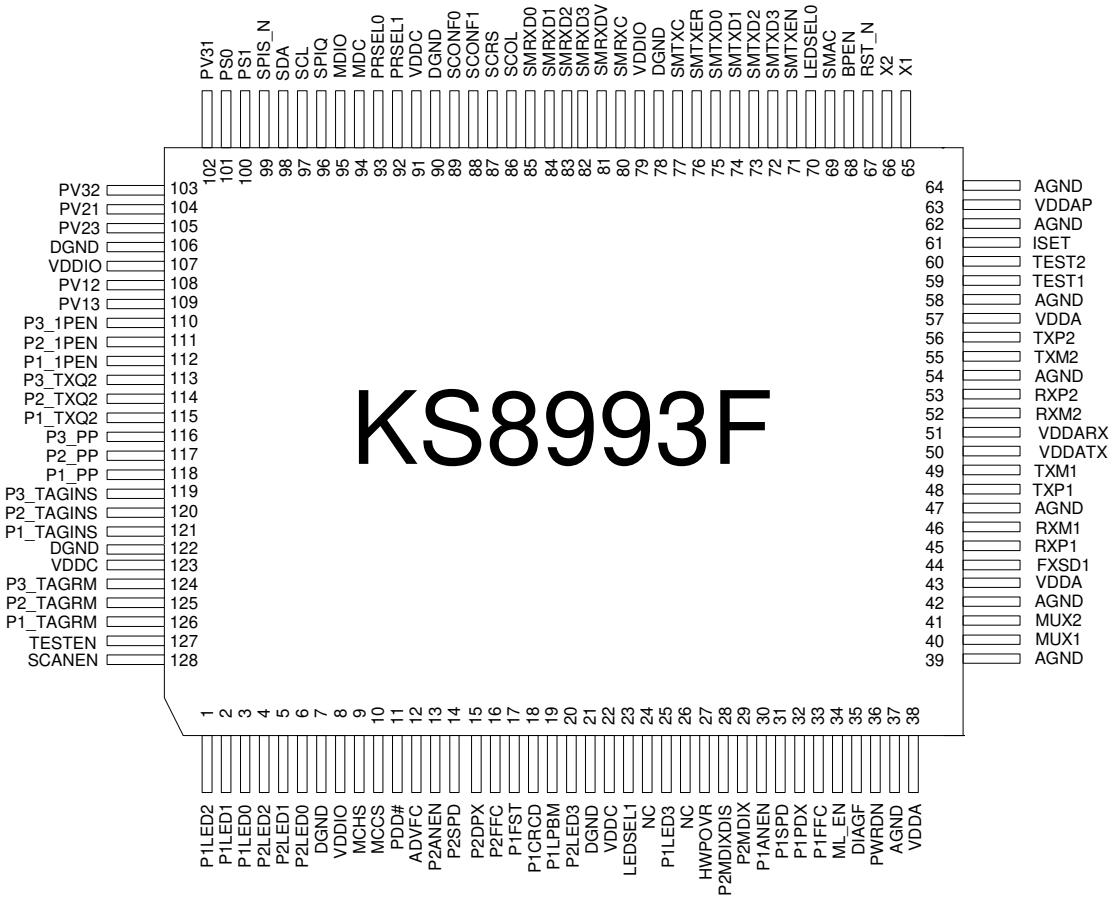
Table Of Contents

List of Tables

List of Figures

1 Signal Description

1.1 KS8993F Pin Diagram



1.2 Pin Description and I/O Assignment

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>P1LED2</td><td>I(pu)/O</td><td rowspan="3">Port 1 LED indicators, defined as below:

<table><tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr><tr><th></th><th>[0,0]</th><th>[0,1]</th></tr><tr><td>P1LED3</td><td>------</td><td>------</td></tr><tr><td>P1LED2</td><td>LINK/ACT</td><td>100LINK/ACT</td></tr><tr><td>P1LED1</td><td>FULLD/COL</td><td>10LINK/ACT</td></tr><tr><td>P1LED0</td><td>SPEED</td><td>FULL_DPX</td></tr></table>
<table><tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr><tr><th></th><th>[1,0]</th><th>[1,1]</th></tr><tr><td>P1LED3</td><td>ACT</td><td>------</td></tr><tr><td>P1LED2</td><td>LINK</td><td>------</td></tr><tr><td>P1LED1</td><td>FULL_DPX/COL</td><td>------</td></tr><tr><td>P1LED0</td><td>SPEED</td><td>------</td></tr></table>
<u>Notes:</u>
LEDSEL0 is external strap-in pin #70.
LEDSEL1 is external strap-in pin #23.
P1LED3 is pin #25.
During reset, P1LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>2</td><td>P1LED1</td><td>I(pu)/O</td></tr>
<tr><td>3</td><td>P1LED0</td><td>I(pu)/O</td></tr>
<tr><td>4</td><td>P2LED2</td><td>I(pu)/O</td><td rowspan="3">Port 2 LED indicators, defined as below:

<table><tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr><tr><th></th><th>[0,0]</th><th>[0,1]</th></tr><tr><td>P2LED3</td><td>------</td><td>------</td></tr><tr><td>P2LED2</td><td>LINK/ACT</td><td>100LINK/ACT</td></tr><tr><td>P2LED1</td><td>FULLD/COL</td><td>10LINK/ACT</td></tr><tr><td>P2LED0</td><td>SPEED</td><td>FULL_DPX</td></tr></table>
<table><tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr><tr><th></th><th>[1,0]</th><th>[1,1]</th></tr><tr><td>P2LED3</td><td>ACT</td><td>------</td></tr><tr><td>P2LED2</td><td>LINK</td><td>------</td></tr><tr><td>P2LED1</td><td>FULL_DPX/COL</td><td>------</td></tr><tr><td>P2LED0</td><td>SPEED</td><td>------</td></tr></table>
<u>Notes:</u>
LEDSEL0 is external strap-in pin #70.
LEDSEL1 is external strap-in pin #23.
P2LED3 is pin #20.
During reset, P2LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>5</td><td>P2LED1</td><td>I(pu)/O</td></tr>
<tr><td>6</td><td>P2LED0</td><td>I(pu)/O</td></tr>
<tr><td>7</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>8</td><td>VDDIO</td><td>Pwr</td><td>3.3V digital VDD</td></tr>
</table>

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>9</td><td>MCHS</td><td>Ipd</td><td rowspan="2">KS8993F operating modes, defined as below:

<table><tr><th>(MCHS, MCCS)</th><th>Description</th></tr><tr><td>(0, 0)</td><td>Normal 3 port switch mode (3 MAC + 2 PHY)
MC mode is disabled.
Port 1 is either Fiber or UTP.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr><tr><td>(0, 1)</td><td>Center MC mode (3 MAC + 2 PHY)
MC mode is enabled.
Port 1 is Fiber and has Center MC enabled.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr><tr><td>(1, 0)</td><td>Terminal MC mode (2 MAC + 2 PHY)
MC mode is enabled.
Port 1 is Fiber and has Terminal MC enabled.
Port 2 is UTP.
Port 3 (MII) is disabled.</td></tr><tr><td>(1, 1)</td><td>Terminal MC mode (3 MAC + 2 PHY)
MC mode is enabled.
Port 1 is Fiber and has Terminal MC enabled.
Port 2 is UTP.
Port 3 (MII) is enabled.</td></tr></table></td></tr>
<tr><td>10</td><td>MCCS</td><td>Ipd</td></tr>
<tr><td>11</td><td>PDD#</td><td>Ipu</td><td>Power Down Detect
1 = normal operation
0 = power down detected

In Terminal MC mode (pin MCHS is ‘1’), a high to low transition to this pin will cause port 1 (fiber) to generate and send out an “Indicate Terminal MC Condition” OAM frame with the S0 status bit set to ‘1’.</td></tr>
<tr><td>12</td><td>ADVFC</td><td>Ipu</td><td>1= advertise the switch’s flow control capability via auto negotiation.
0 = will not advertise the switch’s flow control capability via auto negotiation.</td></tr>
<tr><td>13</td><td>P2ANEN</td><td>Ipu</td><td>1 = enable auto negotiation on port 2.
0 = disable auto negotiation on port 2.</td></tr>
<tr><td>14</td><td>P2SPD</td><td>Ipd</td><td>1 = Force port 2 to 100BT if P2ANEN = 0.
0 = Force port 2 to 10BT if P2ANEN = 0.</td></tr>
<tr><td>15</td><td>P2DPX</td><td>Ipd</td><td>1 = port 2 default to full duplex mode if P2ANEN = 1 and auto negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0.
0 = port 2 default to half duplex mode if P2ANEN = 1 and auto negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0.</td></tr>
<tr><td>16</td><td>P2FFC</td><td>Ipd</td><td>1 = always enable (force) port 2 flow control feature.
0 = port 2 flow control feature enable is determined by auto negotiation result.</td></tr>
<tr><td>17</td><td>P1FST</td><td>Opu</td><td>1 = normal function
0 = MC in loop back mode, or MC abnormal conditions happen</td></tr>
<tr><td>18</td><td>P1LCRCD</td><td>Ipd</td><td>In MC loop back mode,

1 = Drop OAM frames and Ethernet frames with the following errors –</td></tr>
</table>

Pin #	Pin Name	Type	Description
			CRC, undersize, oversize. Loop back Ethernet frames with only good CRC and valid length. 0 = Drop OAM frames only. Loop back all Ethernet frames including those with errors.
19	P1LPBM	Ipd	0 = perform MC loop back at MAC of port 2 1 = reserve. Do not use.
20	P2LED3	Opd	Port 2 LED Indicator Note: Internal pull down is weak; it will not turn ON the LED. *See description in pin# (4).*
21	DGND	Gnd	Digital ground
22	**VDDC / VOUT_1V8**	**Pwr**	**VDDC : For KS8993F, this is an input power pin for the 1.8V digital core VDD.** **VOUT_1V8 : For KS8993FL, this is an 1.8V output power pin to supply the KS8993FL's input power pins: VDDAP (pin 63), VDDC (pins 91, 123) and VDDA (pins 38, 43, 57).**
23	LEDSEL1	I_{pd}	LED display mode select *See description in pin# (1,4).*
24	NC	O_{pd}	Reserved
25	P1LED3	O_{pd}	Port 1 LED Indicator Note: An external 1K pull down is needed on this pin if it is connected to a LED. *See description in pin# (1).*
26	NC	O_{pd}	Reserved
27	HWPOVR	Ipd	Hardware Pin Overwrite 0 = Disable. All strap-in pins configurations are overwritten by the EEPROM configuration data. 1 = Enable. All strap-in pins configurations are overwritten by the EEPROM configuration data, except for P2ANEN (pin 13), P2SPD (pin 14), P2DPX (pin 15) and ML_EN (pin 34).
28	P2MDIXDIS	Ipd	Port 2 auto MDI/MDI-X 0 = enable (default) 1 = disable
29	P2MDIX	Ipd	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled 0 = MDI-X (default), {transmit on TXP2/TXM2 pins} 1 = MDI, {transmit on RXP2/RXM2 pins}
30	P1ANEN	Ipu	1 = enable auto negotiation on port 1 0 = disable auto negotiation on port 1
31	P1SPD	Ipd	1 = Force port 1 to 100BT if P1ANEN = 0. 0 = Force port 1 to 10BT if P1ANEN = 0.
32	P1DPX	Ipd	1 = port 1 default to full duplex mode if P1ANEN = 1 and auto negotiation fails. Force port 1 in full duplex mode if P1ANEN = 0. 0 = port 1 default to half duplex mode if P1ANEN = 1 and auto negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0.
33	P1FFC	Ipd	1 = always enable (force) port 1 flow control feature 0 = port 1 flow control feature enable is determined by auto negotiation result.
34	ML_EN	Ipd	1 = enable missing link

Pin #	Pin Name	Type	Description
			0 = disable missing link
35	DIAGF	Ipd	1 = diagnostic fail 0 = diagnostic normal
36	PWRDN	I	Chip power down input (active low)
37	AGND	Gnd	Analog ground
38	VDDA	Pwr	1.8V analog VDD
39	AGND	Gnd	Analog ground
40	MUX1	I	Factory test pin – float for normal operation
41	MUX2	I	Factory test pin – float for normal operation
42	AGND	Gnd	Analog ground
43	VDDA	Pwr	1.8V analog VDD
44	FXSD1	I	Fiber signal detect / factory test pin
45	RXP1	I/O	Physical receive or transmit signal (+ differential)
46	RXM1	I/O	Physical receive or transmit signal (- differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Physical transmit or receive signal (+ differential)
49	TXM1	I/O	Physical transmit or receive signal (- differential)
50	VDDATX	Pwr	3.3V analog VDD
51	VDDARX	Pwr	3.3V analog VDD
52	RXM2	I/O	Physical receive or transmit signal (– differential)
53	RXP2	I/O	Physical receive or transmit signal (+ differential)
54	AGND	Gnd	Analog ground
55	TXM2	I/O	Physical transmit or receive signal (– differential)
56	TXP2	I/O	Physical transmit or receive signal (+ differential)
57	VDDA	Pwr	1.8V analog VDD
58	AGND	Gnd	Analog ground
59	TEST1	I	Factory test pin – float for normal operation
60	TEST2	I	Factory test pin – float for normal operation
61	ISET	O	Set physical transmit output current. Pull down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	Pwr	1.8V analog VDD for PLL
64	AGND	Gnd	Analog ground
65	X1	I	25 MHz crystal/oscillator clock connections Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. **Note:** Clock is +/- 50ppm for both crystal and oscillator.
66	X2	O	
67	RST_N	Ipu	Hardware reset pin (active low)
68	BPEN	Ipd	Half Duplex Backpressure 1 = enable 0 = disable
69	SMAC	Ipd	Special Mac Mode In this mode, the switch will do faster backoffs than normal. 1 = enable 0 = disable
70	LEDSEL0	Ipd	LED display mode select *See description in pin# (1,4).*
71	SMTXEN	Ipd	Switch MII transmit enable
72	SMTXD3	Ipd	Switch MII transmit data bit 3

Pin #	Pin Name	Type	Description
73	SMTXD2	Ipd	Switch MII transmit data bit 2
74	SMTXD1	Ipd	Switch MII transmit data bit 1
75	SMTXD0	Ipd	Switch MII transmit data bit 0
76	SMTXER	Ipd	Switch MII transmit error
77	SMTXC	Ipd/O	Switch MII transmit clock Output in PHY MII mode Input in MAC MII mode
78	DGND	Gnd	Digital ground
79	VDDIO	Pwr	3.3V digital VDD
80	SMRXC	Ipd/O	Switch MII receive clock Output in PHY MII mode Input in MAC MII mode
81	SMRXDV	O	Switch MII receive data valid
82	SMRXD3	Ipd/O	Switch MII receive data bit 3 Strap option: Switch MII full duplex flow control PD (default) = disable PU = enable
83	SMRXD2	Ipd / O	Switch MII receive bit 2 Strap option: Switch MII is in PD (default) = full duplex mode PU = half duplex mode
84	SMRXD1	Ipd/O	Switch MII receive bit 1 Strap option: Switch MII is in PD (default) = 100Mbps mode PU = 10Mbps mode
85	SMRXD0	Ipd/O	Switch MII receive bit 0 Strap option: Switch will accept packet size up to PD (default) = 1536 bytes (inclusive); PU = 1522 bytes (tagged), 1518 bytes (untagged)
86	SCOL	Ipd/O	Switch MII collision detect
87	SCRS	Ipd/O	Switch MII carrier sense
88	SCONF1	Ipd	Switch MII interface configuration
89	SCONF0	Ipd	(SCONF1, SCONF0) — Description (0,0) — disable, output tri-stated (0,1) — PHY mode MII (1,0) — MAC mode MII (1,1) — PHY mode SNI
90	DGND	Gnd	Digital ground
91	VDDC	Pwr	1.8V digital VDD
92	PRSEL1	Ipd	**Priority Select** Select queue servicing if using split queues. Use the table

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>93</td><td>PRSEL0</td><td>Ipd</td><td>below to select the desired servicing. Note that this selection affects all split transmit queue ports in the same way.

<table><tr><th>(PRSEL,PRSEL0)</th><th>Description</th></tr><tr><td>(0,0)</td><td>Transmit all high priority before low priority</td></tr><tr><td>(0,1)</td><td>Transmit high priority and low priority at 10:1 ratio.</td></tr><tr><td>(1,0)</td><td>Transmit high priority and low priority at 5:1 ratio.</td></tr><tr><td>(1,1)</td><td>Transmit high priority and low priority at 2:1 ratio.</td></tr></table></td></tr>
<tr><td>94</td><td>MDC</td><td>Ipu</td><td>MII Management interface: clock input</td></tr>
<tr><td>95</td><td>MDIO</td><td>Ipu/O</td><td>MII Management interface: data input/output

Note: An external 4.7K pull up is needed on this pin when it is in use.</td></tr>
<tr><td>96</td><td>SPIQ</td><td>Opu</td><td>SPI slave mode: serial data output

See description in pin# (100, 101)</td></tr>
<tr><td>97</td><td>SCL</td><td>Ipu/O</td><td>SPI slave mode / I2C slave mode: clock input
I2C master mode: clock output

See description in pin# (100, 101)</td></tr>
<tr><td>98</td><td>SDA</td><td>Ipu/O</td><td>SPI slave mode: serial data input
I2C master/slave mode: serial data input/output

See description in pin# (100, 101)</td></tr>
<tr><td>99</td><td>SPIS_N</td><td>Ipu</td><td>SPI slave mode: chip select (active low)

When SPIS_N is high, the KS8993F is deselected and SPIQ is held in high impedance state.

A high-to-low transition is used to initiate SPI data transfer.

See description in pin# (100, 101)</td></tr>
<tr><td>100</td><td>PS1</td><td>Ipd</td><td>Serial bus configuration pins to select mode of access to KS8993F internal</td></tr>
</table>

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>101</td><td>PS0</td><td>Ipd</td><td>registers.

[PS1, PS0] = [0, 0] --- I2C master (EEPROM) mode
(If EEPROM is not detected, the power up default values of the KS8993F internal registers will be used)
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used. (tri-stated)</td></tr>
<tr><td>SCL</td><td>O</td><td>I2C clock</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I2C data I/O</td></tr>
<tr><td>SPIS_N</td><td>Ipu</td><td>Not used.</td></tr>
</table>
[PS1, PS0] = [0, 1] --- I2C slave mode
The external I2C master will drive the SCL clock.
The KS8993F device addresses are:
1011_1111 <read>
1011_1110 <write>
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used. (tri-stated)</td></tr>
<tr><td>SCL</td><td>I</td><td>I2C clock</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I2C data I/O</td></tr>
<tr><td>SPIS_N</td><td>Ipu</td><td>Not used.</td></tr>
</table>
[PS1, PS0] = [1, 0] --- SPI slave mode
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>SPI Data Out</td></tr>
<tr><td>SCL</td><td>I</td><td>SPI clock</td></tr>
<tr><td>SDA</td><td>I</td><td>SPI Data In</td></tr>
<tr><td>SPIS_N</td><td>Ipu</td><td>SPI chip select</td></tr>
</table>
[PS1, PS0] = [1, 1] --- SMI mode
In this mode, the KS8993F provides access to all its internal 8 bit registers thru its MDC and MDIO pins.

<u>Note</u>
When (PS1, PS0) ≠ (1,1), the KS8993F provides access to its 16 bit MIIM registers thru its MDC and MDIO pins.</td></tr>
<tr><td>102</td><td>PV31</td><td>Ipu</td><td rowspan="2">Port 3 port based VLAN mask bits. Use to select which ports may transmit packets received on port 3.

PV31 = 1, port 1 may transmit packets received on port 3.
PV31 = 0, port 1 will not transmit any packets received on port 3.

PV32 = 1, port 2 may transmit packets received on port 3.
PV32 = 0, port 2 will not transmit any packets received on port 3.</td></tr>
<tr><td>103</td><td>PV32</td><td>Ipu</td></tr>
<tr><td>104</td><td>PV21</td><td>Ipu</td><td rowspan="2">Port 2 port based VLAN mask bits. Use to select which ports may transmit packets received on port 2.

PV21 = 1, port 1 may transmit packets received on port 2.
PV21 = 0, port 1 will not transmit any packets received on port 2.

PV23 = 1, port 3 may transmit packets received on port 2.
PV23 = 0, port 3 will not transmit any packets received on port 2.</td></tr>
<tr><td>105</td><td>PV23</td><td>Ipu</td></tr>
<tr><td>106</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
</table>

Pin #	Pin Name	Type	Description
107	VDDIO	Pwr	3.3V digital VDD
108	PV12	Ipu	**Port 1 port based VLAN mask bits**. Use to select which ports may transmit packets received on port 1. PV12 = 1, port 2 may transmit packets received on port 1. PV12 = 0, port 2 will not transmit any packets received on port 1. PV13 = 1, port 3 may transmit packets received on port 1. PV13 = 0, port 3 will not transmit any packets received on port 1.
109	PV13	Ipu	
110	P3_1PEN	Ipd	**Enable 802.1p priority classification on port 3 ingress** 1 = enable 0 = disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P3_PP pin.
111	P2_1PEN	Ipd	**Enable 802.1p priority classification on port 2 ingress** 1 = enable 0 = disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P2_PP pin.
112	P1_1PEN	Ipd	**Enable 802.1p priority classification on port 1 ingress** 1 = enable 0 = disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P1_PP pin.
113	P3_TXQ2	Ipd	**Select transmit queue split on port 3** 1 = split 0 = no split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 3 is set by P3_TXQ2.
114	P2_TXQ2	Ipd	**Select transmit queue split on port 2** 1 = split 0 = no split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 2 is set by P2_TXQ2.
115	P1_TXQ2	Ipd	**Select transmit queue split on port 1** 1 = split 0 = no split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 1 is set by P1_TXQ2.
116	P3_PP	Ipd	**Select port-based priority on port 3 ingress**

Pin #	Pin Name	Type	Description
			1 = high 0 = low <default> 802.1p and Diffserv, if applicable, will take precedence.
117	P2_PP	Ipd	**Select port-based priority on port 2 ingress** 1 = high 0 = low <default> 802.1p and Diffserv, if applicable, will take precedence.
118	P1_PP	Ipd	**Select port-based priority on port 1 ingress** 1 = high 0 = low <default> 802.1p and Diffserv, if applicable, will take precedence.
119	P3_TAGINS	Ipd	**Enable tag insertion on port 3 egress** 1 = enable 0 = disable All packets transmitted from port 3 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.
120	P2_TAGINS	Ipd	**Enable tag insertion on port 2 egress** 1 = enable 0 = disable All packets transmitted from port 2 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.
121	P1_TAGINS	Ipd	**Enable tag insertion on port 1 egress** 1 = enable 0 = disable All packets transmitted from port 1 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.
122	DGND	Gnd	Digital ground
123	VDDC	Pwr	1.8V digital VDD
124	P3_TAGRM	Ipd	**Enable tag removal on port 3 egress** 1 = enable 0 = disable All packets transmitted from port 3 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
125	P2_TAGRM	Ipd	**Enable tag removal on port 2 egress** 1 = enable 0 = disable All packets transmitted from port 2 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
126	P1_TAGRM	Ipd	**Enable tag removal on port 1 egress**

Pin #	Pin Name	Type	Description
			1 = enable 0 = disable All packets transmitted from port 1 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
127	TESTEN	Ipd	Scan Test Enable For normal operation, pull down this pin to ground
128	SCANEN	Ipd	Scan Test Scan Mux Enable For normal operation, pull down this pin to ground

Note:
Pwr = power supply;
Gnd = ground;
I = input;
O = output;
I/O = bi-directional
Ipu = input w/ internal pull up;
Ipd = input w/ internal pull down;
Ipu/O = input w/ internal pull up during reset, output pin otherwise;
Ipd/O = input w/ internal pull down during reset, output pin otherwise;
PD = strap pull down;
PU = strap pull up;
Otri = output tri-stated;
Opu = Output with internal pull-up;
Opd = Output with internal pull-down

2 Functional Description

2.1 Overview

The KS8993F is a single-chip Fast Ethernet media converter. It contains two 10/100 physical layer transceivers, three MAC (Media Access Control) units, layer-2 managed switch, and frame buffer. On the media side, the KS8993F supports IEEE 802.3 10BASE-T, 100BASE-TX on ports 1 and 2, and 100BASE-FX on port 1.

The KS8993F implements the unique OAM sub-layer, which resides between RS and PCS layer in the IEEE 802.3 standard. The KS8993F sends and receives an OAM frame that has a fixed length of 96 bits. This special frame is used for the transmission of OAM information between center MC and terminal MC.

The KS8993F has the flexibility to reside in an unmanaged or managed design. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time. In a managed design, a host processor has complete control of the KS8993F via the SMI, MIIM, SPI or I^2C interface.

The KS8993F supports advanced Quality Of Service, port mirroring, rate limiting, broadcast storm protection, and management via SNMP.

The KS8993FL is the single supply version with all the identical rich features of the KS8993F. In the KS8993FL version, pin number 22 provides 1.8V output power to the KS8993FL's VDDC, VDDA and VDDAP power pins. Refer to the pin description of pin number 22 in section 1.2, Pin Description and I/0 Assignment, for more details.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry that makes the design more efficient, and allows for lowest power consumption and smaller chip die size.

2.2 Media Converter Function

The KS8993F is the industry's first single-chip Fast Ethernet media converter that conforms to the TS-1000 spec. The TS-1000 spec. has been standardized by the TELECOMMUNICATION TECHNOLOGY COMMITTEE (TTC) of Japan in May 2002 and can be purchased from TTC. Some key TS-1000 features include:

- Private point-to-point communication between two TS-1000 compliant devices
- 96 bits (12 bytes) frames for the transmission of OAM information between center MC and terminal MC
- Transmission of MC status between center MC and terminal MC
- Automatic generation of OAM frame to inform MC link partner of local MC's status change
- Transmission of vendor code and model number information between center MC and terminal MC for device identification
- Inquisition of terminal MC status by center MC
- Remote loop back for diagnostic by center MC

2.2.1 OAM (Operations, Administration, and Management) Frame Format

Bit	Command		Description
F0-F7	Preamble		1010 1010
C0	Conservation Delimiter		0
C1	Direction Delimiter		0: Upstream (from terminal MC to center MC) 1: Downstream (from center MC to terminal MC)
C2-C3	Configuration Delimiter		10: request 11:reponse 01: indication 00:reserved
C4-C7	Version		0000
C8-C15	Control signal		1000 0000: Start loop back test 0000 0000: Stop loop back test 0100 0000: Notify status
S0	Status	Power	0: normal operation 1: power down
S1		Optical	0: normal 1:abnormal
S2		UTP link	0: link up 1: link down
S3		MC	0: normal 1:brake
S4		Way for information	0: use conservation frame 1: use FEFI
S5		Loop mode	0: normal operation 1: in loop mode
S6		Terminal MC Link option	0: Center side MC have to set always “0” 1: Terminal side MC have to set always “1”
S7		Terminal MC Link Speed1	This bit must be set “0”
S8		Terminal MC Link Speed2	0: 10Mbps 1: 100Mbps These bits have to be set “0”, if S2 is “1” (Center side MC have to set always “0”)
S9		Terminal MC Link Duplex	0: Half Duplex 1: Full Duplex This bit have to be set “0”, if S2 is “1” (Center side MC have to set always “0”)
S10		Terminal MC Auto-Negotiation capability	0: Not Support Auto-Negotiation 1: Support Auto-Negotiation (Center side MC have to set always “0”)
S11		Multiple link partner	0: one link partner on UTP side 1: multiple link partner on UTP side
S12 – S15		Reserve	All bits must be set “0”
M0-M23	Vendor code		
M24-M47	Model number		
E0-E7	FCS		Create FCS at this sub-layer (C0-M47)

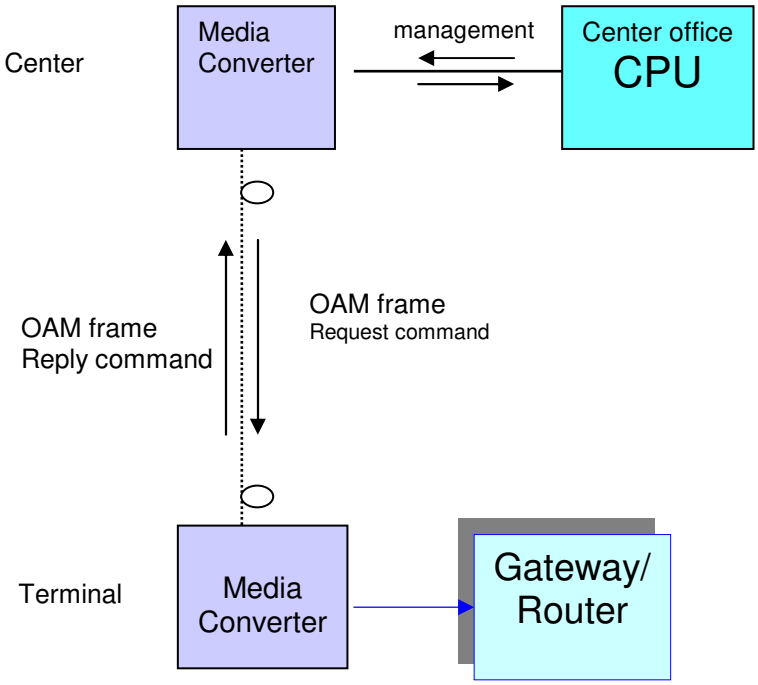
2.2.2 MC (Media Converter) Mode

MC (Media Converter) mode is selected and configured using hardware pins: MCCS and MCHS.

Terminal MC mode without port 3 support is enabled when MCCS=0 and MCHS=1. In this mode, port 1 is 100BASE-FX, port 2 is 10BASE-TX or 100BASE-TX and port 3 is disabled. Terminal MC function is enabled, and the OAM sub-layer responds to the center MC with OAM frames, such as condition inform reply, loop mode start reply, and loop mode stop reply.

Terminal MC mode with port 3 support is enabled when MCCS=1 and MCHS=1. In this mode, port 1 is 100BASE-FX, port 2 is 10BASE-T or 100BASE-TX and port 3 supports MII or SNI interface. Terminal MC function is enabled, and the OAM sub-layer responds to the center MC with OAM frames, such as condition inform reply, loop mode start reply, and loop mode stop reply.

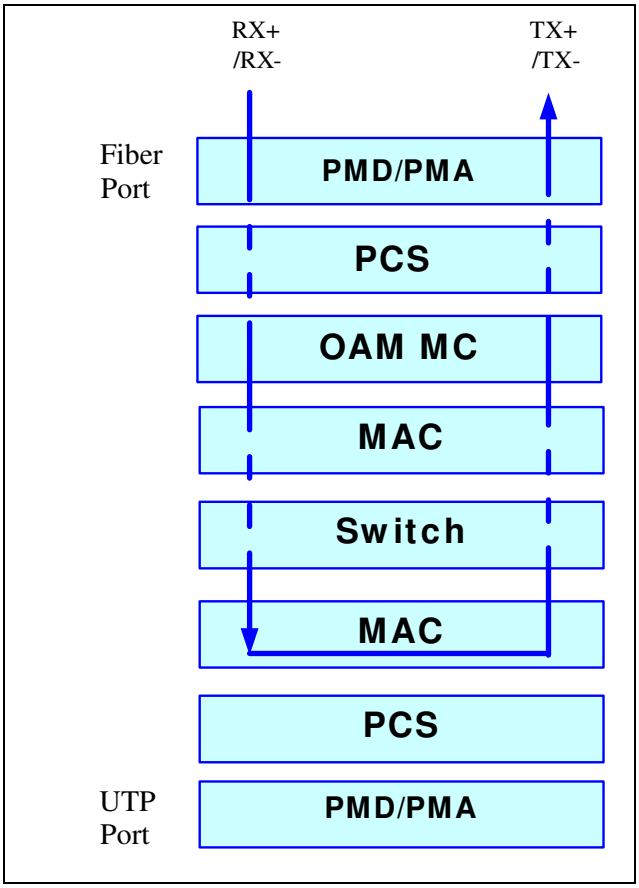
Center MC mode with port 3 support is enabled when MCCS=1 and MCHS=0. In this mode, port 1 is 100BASE-FX, port 2 is 10BASE-T or 100BASE-TX and port 3 supports MII or SNI interface. Center MC function is enabled, and the OAM sub-layer generates and sends OAM frames, such as condition inform request, loop mode start request and loop mode stop request to the terminal MC.



2.2.3 MC Loop Back Function

MC loop back operation is initiated and enabled by the center MC. The terminal MC provides the loop back path to return the loop back packet back to the center MC. In terminal MC mode, the KS8993F provides the following loop back path:

- Receive loop back packet from center MC at RXP1/RXM1 input pins of port 1 (fiber).
- Turn around loop back packet at MAC of port 2 (copper).
- Transmit loop back packet back to center MC from TXP1/TXM1 output pins of port 1 (fiber).



2.2.4 Registers for Media Converter Functions

The KS8993F provides 32 dedicated registers (0x40 to 0x5F) for MC communication between center MC and terminal MC. Some MC register functions include:

- PHY address & configuration
- Loop back counters for CRC error, timeout, good packet
- Remote commands
- Counters for valid MC packet transmitted and received
- MC - status, vendor code, and model number
- Link Partner - status, vendor code, and model number

2.2.5 Unique I/O Feature Definition

Pin	Signal Name	Type	Description
#27	HWPOVR	Input	Hardware pin strapping to override the EEPROM value after reset When HWPOVR = 0, the reset sequence for KS8993F are: • Reads HW pin strapping configuration after reset. • Reads EEPROM configuration for all registers. When HWPOVR = 1, the reset sequence for KS8993F are: • Reads HW pin strapping configuration after reset. • Reads EEPROM configuration for all registers, except for port 2 (auto negotiation, speed, duplex) and Missing Link. When HWPOVR = 1 during normal switch operation: 1. Port 2 (auto negotiation, speed, duplex) can be updated via pins P2ANEN, P2SPD and P2DPX, respectively. These three pins are polled by the KS8993F.

2.2.6 Port 1 LED Indicator Definition

	LEDSEL1 = 0		LEDSEL1 = 1	
	LEDSEL0=0	LEDSEL0=1	LEDSEL0=0	LEDSEL0=1
P1LED3	Tri-state, Pull-Down	Tri-state, Pull-Down	Activity	---
P1LED2	Link/Activity	100BASE-TX Link/Activity	Link	---
P1LED1	Full Duplex/ Collision	10BASE-T Link/Activity	Full Duplex/ Collision	---
P1LED0	Speed	Full Duplex	Speed	---

2.2.7 Port 2 LED Indicator Definition

	LEDSEL1 = 0		LEDSEL1 = 1	
	LEDSEL0=0	LEDSEL0=1	LEDSEL0=0	LEDSEL0=1
P2LED3	Tri-state, Pull-Down	Tri-state, Pull-Down	Activity	---
P2LED2	Link/Activity	100BASE-TX Link/Activity	Link	---
P2LED1	Full Duplex/ Collision	10BASE-T Link/Activity	Full Duplex/ Collision	---
P2LED0	Speed	Full Duplex	Speed	---

2.3 Physical Transceiver

2.3.1 100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ to NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel to serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01 KΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

2.3.2 100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, de-scrambling, 4B/5B decoding and serial to parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then it tunes itself for optimization. This is an ongoing process and can self adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

2.3.3 PLL Clock Synthesizer

The KS8993F generates 125 MHz, 31.25 MHz, 25 MHz and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator.

2.3.4 Scrambler/De-scrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

2.3.5 100BASE-FX Operation and Signal Detection

100BASE-FX operation is very similar to 100BASE-TX operation with the differences being that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode, the auto negotiation feature is bypassed since there is no standard that supports fiber auto negotiation, and the auto MDI/MDI-X feature is also disabled.