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KSZ8993M/ML

Integrated 3-Port 10/100 Managed Switch with PHYs

Rev 1.06

General Description

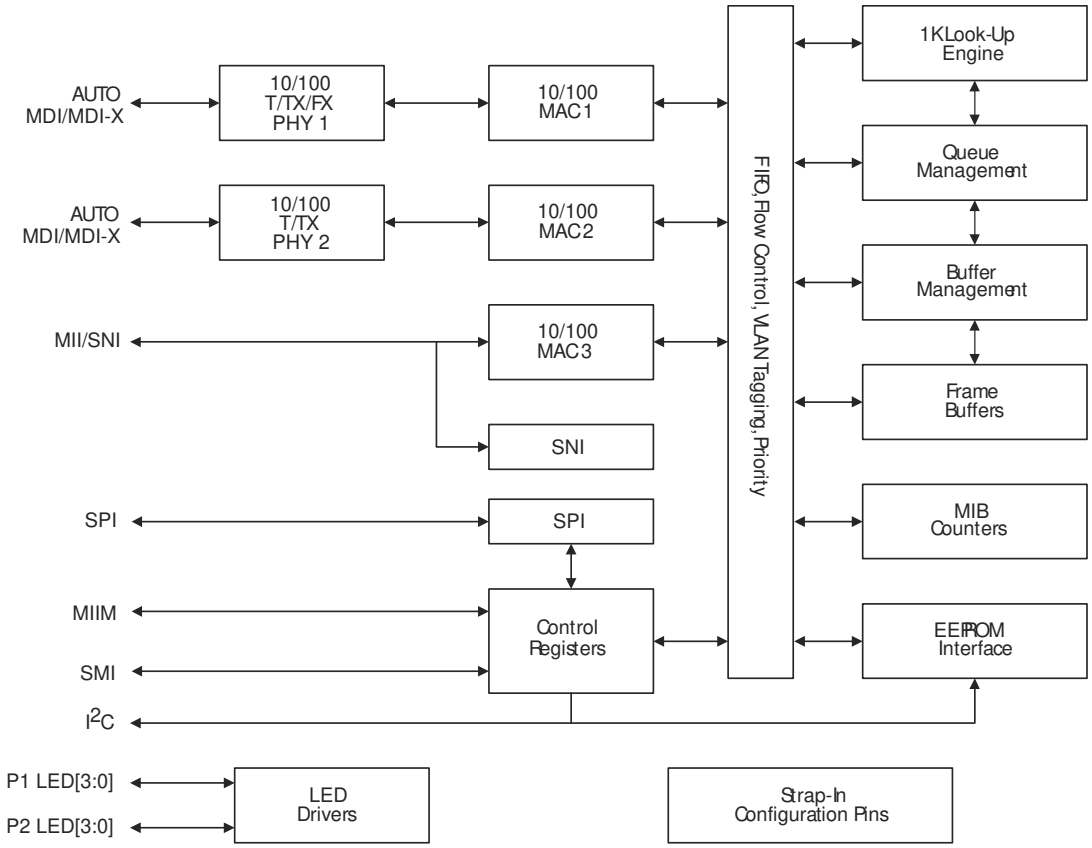
The KSZ8993M, a highly integrated Layer 2 managed switch, is designed for low port count, cost-sensitive 10/100 Mbps switch systems. It offers an extensive feature set that includes tag/port-based VLAN, quality of service (QoS) priority, management, management information base (MIB) counters, MII/SNI, and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KSZ8993M contains two 10/100 transceivers with patented mixed-signal low-power technology, three media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

Both PHY units support 10BASE-T and 100BASE-TX. In addition, one of the PHY unit supports 100BASE-FX.

The KSZ8993ML is the single supply version with all the identical rich features of the KSZ8993M.

Functional Diagram



Features

- **Proven Integrated 3-Port 10/100 Ethernet Switch**
  – 2nd generation switch with three MACs and two PHYs fully compliant to IEEE 802.3u standard
  – Non-blocking switch fabric assures fast packet delivery by utilizing a 1K MAC address lookup table and a store-and-forward architecture
  – Full duplex IEEE 802.3x flow control (pause) with force mode option
  – Half-duplex back pressure flow control
  – Automatic MDI/MDI-X crossover with disable and enable option
  – 100BASE-FX support on port 1
  – MII interface supports both MAC mode and PHY mode
  – 7-wire serial network interface (SNI) support for legacy MAC
  – Comprehensive LED Indicator support for link, activity, full/half duplex and 10/100 speed
- **Comprehensive Configuration Register Access**
  – Serial management interface (SMI) to all internal registers
  – MII management (MIIM) interface to PHY registers
  – SPI and I^2C Interface to all internal registers
  – I/0 Pins strapping and EEPROM to program selective registers in unmanaged switch mode
  – Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…)
- **QoS/CoS Packet Prioritization Support**
  – Per port, 802.1p and DiffServ-based
  – Re-mapping of 802.1p priority field per port basis
- **Advanced Switch Features**
  – IEEE 802.1q VLAN support for up to 16 groups (full-range of VLAN ID)
  – VLAN ID tag/untag options, per port basis
  – IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
  – Programmable rate limiting from 0Mbps to 100Mbps at the ingress and egress port, rate options for high and low priority per port basis
  – Broadcast storm protection with % control (global and per port basis)
  – IEEE 802.1d spanning tree protocol support
  – Upstream special tagging mode to inform the processor which ingress port receives the packet
  – IGMP v1/v2 snooping support for multicast packet filtering
  – Double-tagging support

- **Switch Management Features**
  – Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
  – MIB counters for fully compliant statistics gathering, 34 MIB counters per port
  – Loopback modes for remote diagnostic of failure
- **Low Power Dissipation**: <0.8 Watts (includes PHY transmit drivers)
  – Full-chip hardware power-down (register configuration not saved)
  – Per port based software power-save on PHY (idle link detection, register configuration preserved)
  – 0.18um CMOS technology
  – Voltages: Core 1.8V
  I/O and Transceiver 3.3V
  Use K8993ML for 3.3V only operation
- Available in128-Pin PQFP

Applications

- **Universal Solutions**
  – Broadband gateway / Firewall / VPN
  – Integrated DSL or cable modem multi-port router
  – Wireless LAN access point + gateway
  – Residential and enterprise VoIP gateway/phone
  – Set-top/game box
  – Home networking expansion
  – Standalone 10/100 switch
  – FTTx customer premises equipment
  – Fiber broadband gateway
- **Upgradeable Solutions**[1]
  – Unmanaged switch with future option to migrate to a managed solution
  – Single PHY alternative with future expansion option for two ports
- **Industrial Solutions**
  – Applications requiring port redundancy and port monitoring
  – Sensor devices in redundant ring topology

Note:
1. The cost and time of PCB re-spin.

Ordering Information

Part Number		Temperature Range	Package
Pb-Free	**Standard**		
KSZ8993M	KS8993M	0°C to 70°C	128-Pin PQFP, Lead-free
KSZ8993ML	KS8993ML	0°C to 70°C	128-Pin PQFP, Lead-free
KSZ8993MI	KS8993MI	–40°C to +85°C	128-Pin PQFP, Lead-free
KSZ8993MLI	KS8993MLI	–40°C to +85°C	128-Pin PQFP, Lead-free

Revision History

Revision	Date	Summary of Changes
1.00	5/14/03	Created.
1.01	5/28/03	Added KS8993MI availability in Q4 2003.
1.02	12/8/03	Changed V_{DDIO}, V_{DDATX} and V_{DDARX} supply voltages from 3.3V to (3.3V or 2.5V). Changed [PS1,PS0] = [1,1] setting from Reserved to SMI mode. Changed Special Tagging Mode to Upstream Special Tagging Mode (Switch port 3 to processor support only). Updated recommended magnetic manufacturer list. Added 25MHz crystal/oscillator clock's ppm spec. in Pin Description. Updated I^2C Slave Serial Bus Configuration section. Updated KSZ8993MI availability to from Q1 2004.
1.03	9/22/04	Added KS8993ML to General Description (page 1) and to the Functional Description. Updated Part Ordering Information table. Updated pin description for pin 22 to the following: V_{DDC}: For KS8993M, this is an input power pin for the 1.8V digital core V_{DD}. V_{OUT}_1V8: For KS8993ML, this is an 1.8V output power pin to supply the KS8993ML's input power pins: V_{DDAP} (pin 63), V_{DDC} (pins 91, 123), and V_{DDA} (pins 38, 43, 57). Updated pin description for P1LED3 (pin 25) to indicate that an external 1K pull-down is needed if a LED is connected. Updated pin description for MDIO (pin 95) to indicate that an external 4.7K pull-up is needed if this pin is in used. Changed the aging period from 300 +/–75 seconds to about 200 seconds. Updated Electrical Characteristics (V_{IH}, V_{IL}, V_{OH}, V_{OL}). Transferred to new format.
1.04	4/12/05	Removed references to 2.5V operation Added reset circuit recommendation
1.05	2/14/05	Updated to add Pb-Free spwcifications
1.06	2/13/07	Add the P/N KSZ8993I into the Ordering information table
1.06a	10/28/08	Add the P/N KSZ8993MLI into the Ordering information table Modify the current consumption table from board to device.

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Pin Description and I/O Assignment

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<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>1</td><td>P1LED2</td><td>Ipu/O</td><td rowspan="3">Port 1 LED indicators
<table><tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr><tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr><tr><td>P1LED3</td><td>—</td><td>—</td></tr><tr><td>P1LED2</td><td>Link/Act</td><td>100Link/Act</td></tr><tr><td>P1LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr><tr><td>P1LED0</td><td>Speed</td><td>Full duplex</td></tr></table><table><tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr><tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr><tr><td>P1LED3</td><td>Act</td><td>—</td></tr><tr><td>P1LED2</td><td>Link</td><td>—</td></tr><tr><td>P1LED1</td><td>Full duplex/Col</td><td>—</td></tr><tr><td>P1LED0</td><td>Speed</td><td>—</td></tr></table>Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P1LED3 is pin 25.
During reset, P1LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>2</td><td>P1LED1</td><td>Ipu/O</td></tr>
<tr><td>3</td><td>P1LED0</td><td>Ipu/O</td></tr>
<tr><td>4</td><td>P2LED2</td><td>Ipu/O</td><td rowspan="3">Port 2 LED indicators
<table><tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr><tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr><tr><td>P2LED3</td><td>—</td><td>—</td></tr><tr><td>P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr><tr><td>P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr><tr><td>P2LED0</td><td>Speed</td><td>Full duplex</td></tr></table><table><tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr><tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr><tr><td>P2LED3</td><td>Act</td><td>—</td></tr><tr><td>P2LED2</td><td>Link</td><td>—</td></tr><tr><td>P2LED1</td><td>Full duplex/Col</td><td>—</td></tr><tr><td>P2LED0</td><td>Speed</td><td>—</td></tr></table>Notes:
LEDSEL0 is external strap-in pin 70.
LEDSEL1 is external strap-in pin 23.
P2LED3 is pin 20.
During reset, P2LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>5</td><td>P2LED1</td><td>Ipu/O</td></tr>
<tr><td>6</td><td>P2LED0</td><td>Ipu/O</td></tr>
<tr><td>7</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
</table>

Note:

1. Ipu/O = Input with internal pull-up during reset, output pin otherwise.
   Gnd = Ground.

Pin Number	Pin Name	Type (1)	Description
8	VDDIO	P	3.3V digital V_{DD}
9	NC	Ipd	No connect
10	NC	Ipd	No connect
11	NC	Ipu	No connect
12	ADVFC	Ipu	1 = advertise the switch's flow control capability via auto negotiation. 0 = will not advertise the switch's flow control capability via auto negotiation.
13	P2ANEN	Ipu	1 = enable auto negotiation on port 2 0 = disable auto negotiation on port 2
14	P2SPD	Ipd	1 = force port 2 to 100BT if P2ANEN = 0 0 = force port 2 to 10BT if P2ANEN = 0
15	P2DPX	Ipd	1 = port 2 default to full duplex mode if P2ANEN = 1 and auto negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0. 0 = port 2 default to half duplex mode if P2ANEN = 1 and auto negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0.
16	P2FFC	Ipd	1 = always enable (force) port 2 flow control feature 0 = port 2 flow control feature enable is determined by auto negotiation result.
17	NC	Opu	No connect
18	NC	Ipd	No connect
19	NC	Ipd	No connect
20	P2LED3	Opd	Port 2 LED indicator Note: Internal pull-down is weak; it will not turn ON the LED. See description in pin 4.
21	DGND	Gnd	Digital ground
22	VDDC/VOUT_1V8	P	V_{DDC}: For KSZ8993M, this is an input power pin for the 1.8V digital core V_{DD}. V_{OUT_1V8}: For KSZ8993ML, this is a 1.8V output power pin to supply the KSZ8993ML's input power pins: V_{DDAP} (pin 63), V_{DDC} (pins 91 and 123), and V_{DDA} (pins 38, 43, and 57).
23	LEDSEL1	Ipd	LED display mode select See description in pins 1 and 4.
24	NC	O	No connect
25	P1LED3	Opd	Port 1 LED indicator Note: An external 1K pull-down is needed on this pin if it is connected to a LED. The 1K resistor will not turn ON the LED. See description in pin 1.

Note:

1. P = Power supply.
   Gnd = Ground.
   O = Output.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Opu = Output with internal pull-up. Opd = Output internal pull-down.

Pin Number	Pin Name	Type [1]	Description
26	NC	O	No connect
27	HWPOVR	Ipd	Hardware pin overwrite 0 = Disable. All strap-in pins configurations are overwritten by the EEPROM configuration data 1 = Enable. All strap-in pins configurations are overwritten by the EEPROM configuration data, except for register 0x2C bits [7:5], (port 2: auto-negotiation enable, force speed, force duplex).
28	P2MDIXDIS	Ipd	Port 2 Auto MDI/MDI-X PD (default) = enable PU = disable
29	P2MDIX	Ipd	Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled. PD (default) = MDI-X (transmit on TXP2 / TXM2 pins) PU = MDI, (transmit on RXP2 / RXM2 pins)
30	P1ANEN	Ipu	1 = enable auto negotiation on port 1 0 = disable auto negotiation on port 1
31	P1SPD	Ipd	1 = force port 1 to 100BT if P1ANEN = 0 0 = force port 1 to 10BT if P1ANEN = 0
32	P1DPX	Ipd	1 = port 1 default to full duplex mode if P1ANEN = 1 and auto negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0. 0 = port 1 default to half duplex mode if P1ANEN = 1 and auto negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0.
33	P1FFC	Ipd	1 = always enable (force) port 1 flow control feature 0 = port 1 flow control feature enable is determined by auto negotiation result.
34	NC	Ipd	No connect
35	NC	Ipd	No connect
36	PWRDN	Ipu	Chip power-down input (active low)
37	AGND	Gnd	Analog ground
38	VDDA	P	1.8V analog V_{DD}
39	AGND	Gnd	Analog ground
40	MUX1	I	Factory test pin - float for normal operation
41	MUX2	I	Factory test pin - float for normal operation
42	AGND	Gnd	Analog ground
43	VDDA	P	1.8V analog V_{DD}
44	FXSD1	I	Fiber signal detect/factory test pin

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.

Pin Number	Pin Name	Type (1)	Description
45	RXP1	I/O	Physical receive or transmit signal (+ differential)
46	RXM1	I/O	Physical receive or transmit signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Physical transmit or receive signal (+ differential)
49	TXM1	I/O	Physical transmit or receive signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Physical receive or transmit signal (– differential)
53	RXP2	I/O	Physical receive or transmit signal (+ differential)
54	AGND	Gnd	Analog ground.
55	TXM2	I/O	Physical transmit or receive signal (– differential)
56	TXP2	I/O	Physical transmit or receive signal (+ differential)
57	VDDA	P	1.8 analog V_{DD}
58	AGND	Gnd	Analog ground
59	TEST1	I	Factory test pin - float for normal operation
60	TEST2	Ipu	Factory test pin - float or pull-up for normal operation
61	ISET	O	Set physical transmit output current. Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	P	1.8V analog V_{DD} for PLL
64	AGND	Gnd	Analog ground.
65	X1	I	25MHz crystal/oscillator clock connections Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is +/- 50ppm for both crystal and oscillator.
66	X2	O	
67	RST_N	Ipu	Hardware reset pin (active low)
68	BPEN	Ipd	Half-duplex backpressure 1 = enable 0 = disable
69	SMAC	Ipd	Special Mac-mode In this mode, the switch will do faster back-offs than normal. 1 = enable 0 = disable

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.

Pin Number	Pin Name	Type (1)	Description
70	LEDSEL0	Ipd	LED display mode select See description in pins 1 and 4.
71	SMTXEN	Ipd	Switch MII transmit enable
72	SMTXD3	Ipd	Switch MII transmit data bit 3
73	SMTXD2	Ipd	Switch MII transmit data bit 2
74	SMTXD1	Ipd	Switch MII transmit data bit 1
75	SMTXD0	Ipd	Switch MII transmit data bit 0
76	SMTXER	Ipd	Switch MII transmit error
77	SMTXC	Ipd/O	Switch MII transmit clock Output in PHY MII mode Input in MAC MII mode
78	DGND	Gnd	Digital ground
79	VDDIO	P	3.3V digital V_{DD}
80	SMRXC	Ipd/O	Switch MII receive clock. Output in PHY MII mode Input in MAC MII mode
81	SMRXDV	O	Switch MII receive data valid
82	SMRXD3	Ipd/O	Switch MII receive data bit 3 Strap option: switch MII full-duplex flow control PD (default) = disable PU = enable
83	SMRXD2	Ipd/O	Switch MII receive bit 2 Strap option: switch MII is in PD (default) = full-duplex mode PU = half-duplex mode
84	SMRXD1	Ipd/O	Switch MII receive bit 1 Strap option: Switch MII is in PD (default) = 100Mbps mode PU = 10Mbps mode
85	SMRXD0	Ipd/O	Switch MII receive bit 0 Strap option: switch will accept packet size up to PD (default) = 1536 bytes (inclusive) PU = 1522 bytes (tagged), 1518 bytes (untagged)
86	SCOL	Ipd/O	Switch MII collision detect
87	SCRS	Ipd/O	Switch MII carrier sense

Note:

1. P = Power supply.
   Gnd = Ground.
   O = Output.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>88</td><td>SCONF1</td><td>Ipd</td><td rowspan="2">Switch MII interface configuration
<table><tr><th>(SCONF1, SCONF0)</th><th>Description</th></tr><tr><td>(0,0)</td><td>disable, outputs tri-stated</td></tr><tr><td>(0,1)</td><td>PHY mode MII</td></tr><tr><td>(1,0)</td><td>MAC mode MII</td></tr><tr><td>(1,1)</td><td>PHY mode SNI</td></tr></table></td></tr>
<tr><td>89</td><td>SCONF0</td><td>Ipd</td></tr>
<tr><td>90</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>91</td><td>VDDC</td><td>P</td><td>1.8V digital VDD</td></tr>
<tr><td>92</td><td>PRSEL1</td><td>Ipd</td><td rowspan="2">Priority select. Select queue servicing if using split queues. Use the table below to select the desired servicing. Note that this selection effects all split transmit queue ports in the same way.
<table><tr><th>(PRSEL1, PRSEL0)</th><th>Description</th></tr><tr><td>(0,0)</td><td>Transmit all high priority before low priority</td></tr><tr><td>(0,1)</td><td>Transmit high priority and low priority at 10:1 ratio.</td></tr><tr><td>(1,0)</td><td>Transmit high priority and low priority at 5:1 ratio.</td></tr><tr><td>(1,1)</td><td>Transmit high priority and low priority at 2:1 ratio.</td></tr></table></td></tr>
<tr><td>93</td><td>PRSEL0</td><td>Ipd</td></tr>
<tr><td>94</td><td>MDC</td><td>Ipu</td><td>MII management interface: clock input</td></tr>
<tr><td>95</td><td>MDIO</td><td>Ipu/O</td><td>MII management interface: data input/output
Note: an external 4.7K pull-up is needed on this pin when it is in use.</td></tr>
<tr><td>96</td><td>SPIQ</td><td>Opu</td><td>SPI slave mode: serial data output
See description in pins 100 and 101.</td></tr>
<tr><td>97</td><td>SCL</td><td>Ipu/O</td><td>SPI slave mode / I^2C slave mode: clock input
I^2C master mode: clock output
See description in pins 100 and 101.</td></tr>
<tr><td>98</td><td>SDA</td><td>Ipu/O</td><td>SPI slave mode: serial data input
I^2C master/slave mode: serial data input/output
See description in pins 100 and 101.</td></tr>
<tr><td>99</td><td>SPIS_N</td><td>Ipu</td><td>SPI slave mode: chip select (active low)
When SPIS_N is high, the KSZ8993M is deselected and SPIQ is held in high impedance state.
A high-to-low transition is used to initiate SPI data transfer.
See description in pins 100 and 101.</td></tr>
</table>

Note:

1. P = Power supply.
   Gnd = Ground.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   Opu = Output w/ internal pull-up.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>100</td><td>PS1</td><td>Ipd</td><td rowspan="2">Serial bus configuration pins to select mode of access to KSZ8993M internal registers.

[PS1, PS0] = [0, 0] — I²C master (EEPROM) mode
(If EEPROM is not detected, the power-up default values of the KSZ8993M internal registers will be used.)
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>O</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>Ipu</td><td>Not used</td></tr></table>
[PS1, PS0] = [0, 1] — I²C slave mode
The external I²C master will drive the SCL clock.
The KSZ8993M device addresses are:
1011_1111 <read>
1011_1110 <write>
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>I</td><td>I²C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I²C data I/O</td></tr><tr><td>SPIS_N</td><td>Ipu</td><td>Not used</td></tr></table>
[PS1, PS0] = [1, 0] — SPI slave mode
<table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr><tr><td>SCL</td><td>I</td><td>SPI clock</td></tr><tr><td>SDA</td><td>I</td><td>SPI data In</td></tr><tr><td>SPIS_N</td><td>Ipu</td><td>SPI chip select</td></tr></table>
[PS1, PS0] = [1, 1] – SMI-mode
In this mode, the KSZ8993M provides access to all its internal 8 bit registers through its MDC and MDIO pins.

Note:
When (PS1, PS0) ≠ (1,1), the KSZ8993M provides access to its 16 bit MIIM registers through its MDC and MDIO pins.</td></tr>
<tr><td>101</td><td>PS0</td><td>Ipd</td></tr>
<tr><td>102</td><td>PV31</td><td>Ipu</td><td rowspan="2">Port 3 port-based VLAN mask bits – Use to select which ports may transmit packets received on port 3.
PV31 = 1, port 1 may transmit packets received on port 3
PV31 = 0, port 1 will not transmit any packets received on port 3
PV32 = 1, port 2 may transmit packets received on port 3
PV32 = 0, port 2 will not transmit any packets received on port 3</td></tr>
<tr><td>103</td><td>PV32</td><td>Ipu</td></tr>
</table>

Note:

1. I = Input. Ipu = Input w/ internal pull-up. I/O = Bi-directional.
   O= Output. Ipd = Input w/ internal pull-down.

Pin Number	Pin Name	Type (1)	Description
104	PV21	Ipu	**Port 2 port-based VLAN mask bits** – Use to select which ports may transmit packets received on port 2. PV21 = 1, port 1 may transmit packets received on port 2 PV21 = 0, port 1 will not transmit any packets received on port 2 PV23 = 1, port 3 may transmit packets received on port 2 PV23 = 0, port 3 will not transmit any packets received on port 2
105	PV23	Ipu	
106	DGND	Gnd	Digital ground
107	VDDIO	P	3.3V digital V_{DD}
108	PV12	Ipu	**Port 1 port-based VLAN mask bits** – Use to select which ports may transmit packets received on port 1. PV12 = 1, port 2 may transmit packets received on port 1 PV12 = 0, port 2 will not transmit any packets received on port 1 PV13 = 1, port 3 may transmit packets received on port 1 PV13 = 0, port 3 will not transmit any packets received on port 1
109	PV13	Ipu	
110	P3_1PEN	Ipd	**Enable 802.1p priority classification on port 3 ingress** 1 = enable 0 = disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P3_PP pin.
111	P2_1PEN	Ipd	**Enable 802.1p priority classification on port 2 ingress** 1 = enable 0 = disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P2_PP pin.
112	P1_1PEN	Ipd	**Enable 802.1p priority classification on port 1 ingress** 1 = enable 0 = disable Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P1_PP pin.
113	P3_TXQ2	Ipd	**Select transmit queue split on port 3** 1 = split 0 = no split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 3 is set by P3_TXQ2.

Note:

1. P = Power supply.
   Gnd = Ground.
   Ipu = Input w/ internal pull-up. Ipd = Input w/ internal pull-down.

Pin Number	Pin Name	Type [1]	Description
114	P2_TXQ2	Ipd	**Select transmit queue split on port 2** 1 = split 0 = no split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 2 is set by P2_TXQ2.
115	P1_TXQ2	Ipd	**Select transmit queue split on port 1** 1 = split 0 = no split The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 1 is set by P1_TXQ2.
116	P3_PP	Ipd	**Select port-based priority on port 3 ingress** 1 = high 0 = low <default> 802.1p and DiffServ, if applicable, takes precedence.
117	P2_PP	Ipd	**Select port-based priority on port 2 ingress** 1 = high 0 = low <default> 802.1p and DiffServ, if applicable, takes precedence.
118	P1_PP	Ipd	**Select port-based priority on port 1 ingress** 1 = high 0 = low <default> 802.1p and DiffServ, if applicable, takes precedence.
119	P3_TAGINS	Ipd	**Enable tag insertion on port 3 egress** 1 = enable 0 = disable All packets transmitted from port 3 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.
120	P2_TAGINS	Ipd	**Enable tag insertion on port 2 egress** 1 = enable 0 = disable All packets transmitted from port 2 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.

Note:

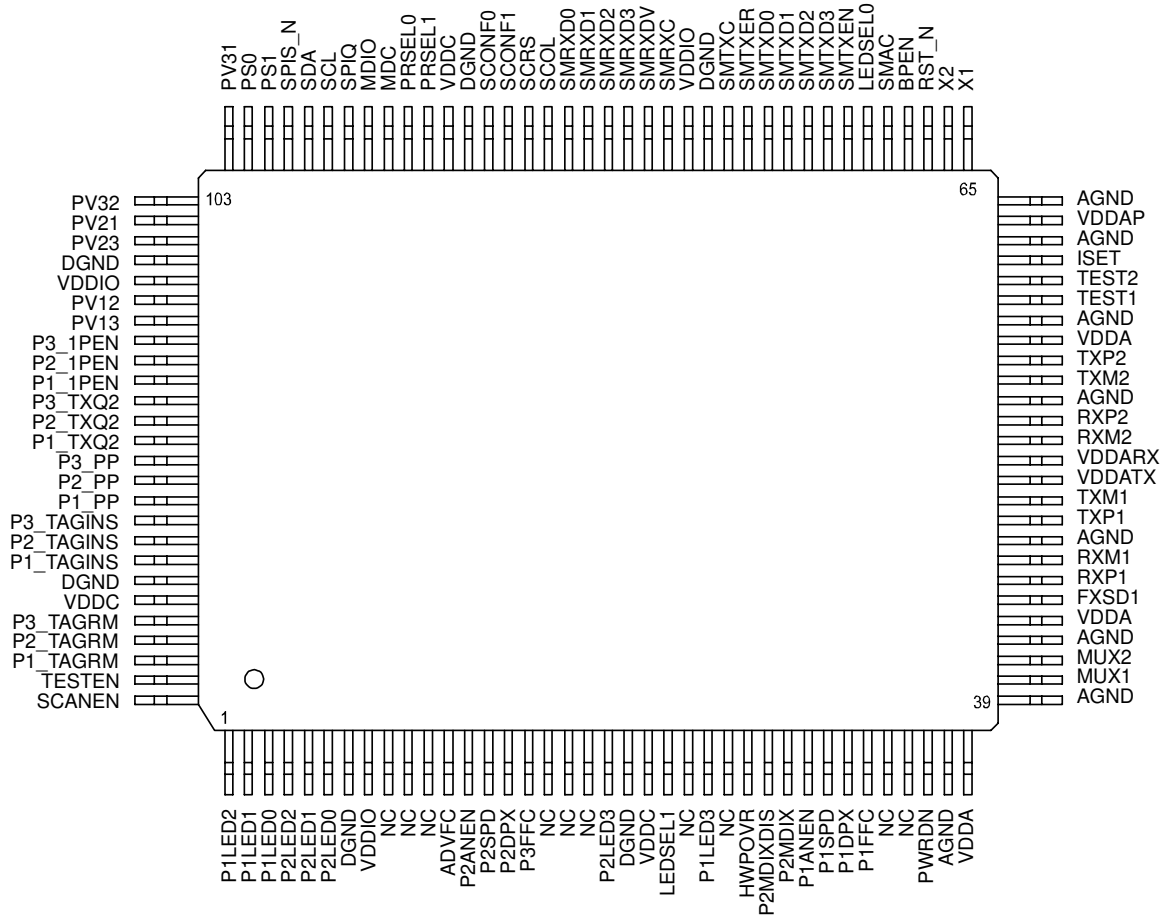
1. Ipd = Input w/ internal pull-down.

Pin Number	Pin Name	Type (1)	Description
121	P1_TAGINS	Ipd	**Enable tag insertion on port 1 egress** 1 = enable 0 = disable All packets transmitted from port 1 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag.
122	DGND	Gnd	Digital ground
123	VDDC	P	1.8V digital V_{DD}
124	P3_TAGRM	Ipd	**Enable tag removal on port 3 egress** 1 = enable 0 = disable All packets transmitted from port 3 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
125	P2_TAGRM	Ipd	**Enable tag removal on port 2 egress** 1 = enable 0 = disable All packets transmitted from port 2 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
126	P1_TAGRM	Ipd	**Enable tag removal on port 1 egress** 1 = enable 0 = disable All packets transmitted from port 1 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact.
127	TESTEN	Ipd	Scan Test Enable For normal operation, pull-down this pin to ground.
128	SCANEN	Ipd	Scan Test Scan Mux Enable For normal operation, pull-down this pin to ground.

Note:

1. P = Power supply.
   Gnd = Ground.
   Ipd = Input w/ internal pull-down.

Pin Configuration



128-Pin PQFP (Top View)

Functional Description

The KSZ8993M contains two 10/100 physical layer transceivers and three MAC units with an integrated Layer 2 managed switch.

The KSZ8993M has the flexibility to reside in either a managed or unmanaged design. In a managed design, the host processor has complete control of the KSZ8993M via the SMI interface, MIIM interface, SPI bus, or I^2C bus. An unmanaged design is achieved through I/O strapping and/or EEPROM programming at system reset time.

On the media side, the KSZ8993M supports IEEE 802.3 10BASE-T and 100BASE-TX on both PHY ports, and 100BASE-FX on PHY port 1. The KSZ8993M can be used as a media converter.

The KSZ8993ML is the single supply version with all the identical rich features of the KSZ8993M. In the KSZ8993ML version, pin number 22 provides 1.8V output power to the KSZ8993ML's V_{DDC}, V_{DDA}, and V_{DDAP} power pins. Refer to the Pin Description table for information about pin 22 (Pin Description and I/0 Assignment).

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

Functional Overview: Physical Layer Transceiver

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ to NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01 KΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, de-scrambling, 4B/5B decoding and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then it tunes itself for optimization. This is an ongoing process and can self adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KSZ8993M generates 125MHz, 31.25MHz, 25MHz, and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator.

Scrambler/De-scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

100BASE-FX Operation

100BASE-FX operation is very similar to 100BASE-TX operation with the differences being that the scrambler / de-scrambler and MLT3 encoder / decoder are bypassed on transmission and reception. In 100BASE-FX mode, the auto negotiation feature is bypassed since there is no standard that supports fiber auto negotiation. The auto-MDI/MDI-X feature is also disabled.

100BASE-FX Signal Detection

In fiber operation, the KSZ8993M's FXSD1 (fiber signal detect) input pin is usually connected to the fiber transceiver's SD (signal detect) output pin. 100BASE-FX mode is activated when the FXSD1 input pin is greater than 1V. When FXSD1 is between 1V and 1.8V, no fiber signal is detected and a far end fault (FEF) is generated. When FXSD1 is over 2.2V, the fiber signal is detected.

Alternatively, the designer may choose not to implement the FEF feature. In this case, the FXSD1 input pin is tied high to force 100BASE-FX mode.

100BASE-FX signal detection is summarized in the following table:

Part Number	Mode
Less than 0.2V	TX mode
Greater than 1V, but less than 1.8V	FX mode No signal detected. Far-end fault generated
Greater than 2.2V I	FX mode Signal detected

Table 1. FX and TX Mode Selection

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver's SD output voltage swing to match the KSZ8993M's FXSD1 input voltage threshold.

100BASE-FX Far End Fault

An FEF occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8993M detects a FEF when its FXSD1 input is between 1.0V and 1.8V. When an FEF occurs, the transmission side signals the other end of the link by sending 84 1's followed by a zero in the idle period between frames.

Upon receiving an FEF, the LINK will go down (even when a fiber signal is detected) to indicate a fault condition. The transmitting side is not affected when an FEF is received, and will continue to send out its normal transmit pattern from the MAC. By default, FEF is enabled. The FEF feature can be disabled through register setting.

10BASE-T Transmit

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8993M decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

Power Management

The KSZ8993M features a per-port power down mode. To save power, the user can power down ports that are not in use by setting the port control registers, or MII control registers. In addition, there is a full chip power down mode. When activated, the entire chip will be shut down.

MDI /MDI-X Auto Crossover

The KSZ8993M supports MDI/ DI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the KSZ8993M device. This feature can be extremely useful when end users are unaware of cable types and can also save on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

Based on the IEEE 802.3 standard, the MDI and MDI-X definitions are as follows:

MDI		MDI-X	
RJ45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 2. MDI/MDI-X Pin Definitions

Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. The following diagram depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

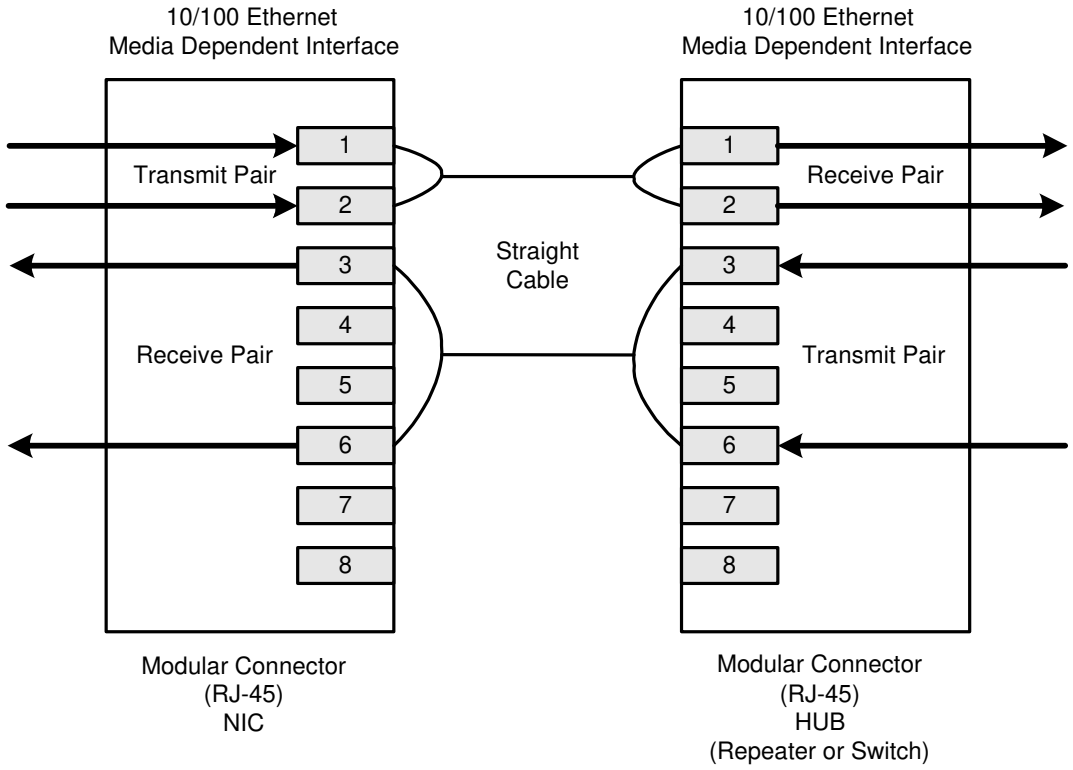


Figure 1. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

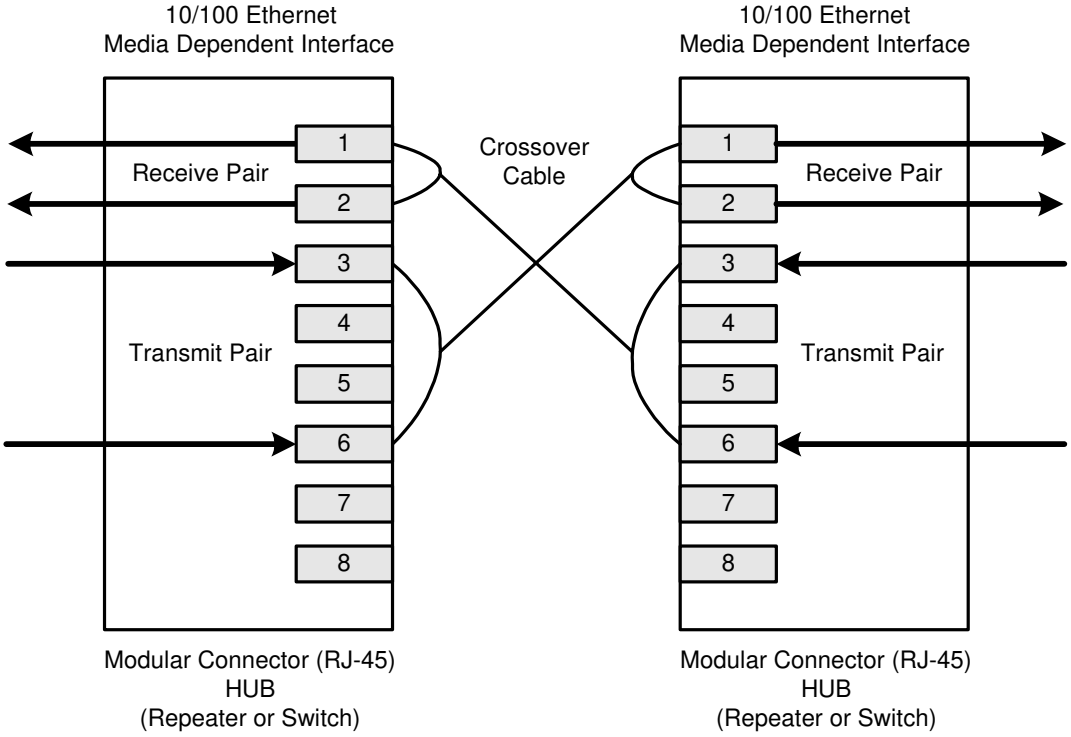


Figure 2. Typical Crossover Cable Connection

Auto Negotiation

The KSZ8993M conforms to the auto negotiation protocol as described by the 802.3 committee. Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8993M is forced to bypass auto negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link setup is shown in the following flow diagram.