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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

KS8995MA/FQ

Integrated 5-Port 10/100 Managed Switch

Rev. 3.0

General Description

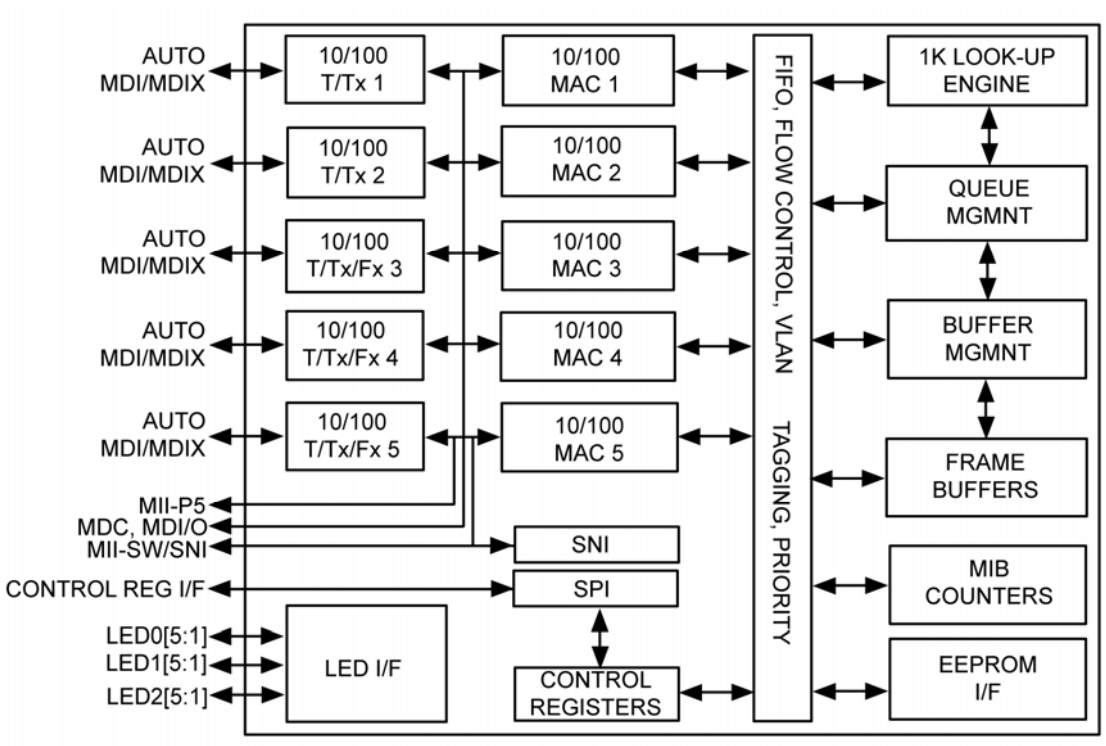
The KS8995MA/FQ is a highly-integrated Layer 2 managed switch with optimized bill of materials (BOM) cost for low port count, cost-sensitive 10/100Mbps switch systems with both copper and optic fiber media. It also provides an extensive feature set such as tag/port-based VLAN, quality of service (QoS) priority, management, MIB counters, dual MII interfaces and CPU control/data interfaces to effectively address both current and emerging fast Ethernet applications.

The KS8995MA/FQ contains five 10/100 transceivers with patented mixed-signal low-power technology, five media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

All PHY units support 10BASE-T and 100BASE-TX. In addition, two of the PHY units support 100BASE-FX on ports 4 and 5 for KSZ8995MA, two of the PHY units support 100BASE-FX on ports 3 and 4 for KSZ8995FQ.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Diagram



Features

- Integrated switch with five MACs and five fast Ethernet transceivers fully-compliant to IEEE 802.3u standard
- Shared memory based switch fabric with fully non-blocking configuration
- 1.4Gbps high-performance memory bandwidth
- 10BASE-T, 100BASE-TX, and 100BASE-FX modes
- Dual MII configuration: MII-Switch (MAC or PHY mode MII) and MII-P5 (PHY mode MII).
- IEEE 802.1q tag-based VLAN (16 VLANs, full-range VID) for DMZ port, WAN/LAN separation or inter-VLAN switch links
- VLAN ID tag/untag options, per-port basis
- Programmable rate limiting 0Mbps to 100Mbps, ingress and egress port, rate options for high and low priority, per-port basis in 32Kbps increments
- Flow control or drop packet rate limiting (ingress port)
- Integrated MIB counters for fully-compliant statistics gathering, 34 MIB counters per port
- Enable/Disable option for huge frame size up to 1916 bytes per frame
- IGMP v1/v2 snooping for multicast packet filtering
- Special tagging mode to send CPU info on ingress packet's port value
- SPI slave (complete) and MDIO (MII PHY only) serial management interface for control of register configuration
- MAC-id based security lock option
- Control registers configurable on-the-fly (port-priority, 802.1p/d/q, AN...)
- CPU read access to MAC forwarding table entries
- 802.1d spanning tree protocol
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
- Broadcast storm protection with % control – global and per-port basis
- Optimization for fiber-to-copper media conversion
- Full-chip hardware power-down support (register configuration not saved)
- Per-port based software power-save on PHY (idle link detection, register configuration preserved)
- QoS/CoS packets prioritization supports:
  - Per port, 802.1p and DiffServ based
- 802.1p/q tag insertion or removal on a per-port basis (egress)
- MDC and MDI/O interface support to access the MII PHY control registers (not all control registers)
- MII local loopback support
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table)
- Wire-speed reception and transmission
- Integrated look-up engine with dedicated 1K MAC addresses
- Full duplex IEEE 802.3x and half-duplex back pressure flow control
- Comprehensive LED support
- 7-wire SNI support for legacy MAC interface
- Automatic MDI/MDI-X crossover for plug-and-play
- Disable automatic MDI/MDI-X option
- Low power:
  - Core: 1.8V
  - Digital I/O: 3.3V
  - Analog I/O: 3.3V
- 0.18µm CMOS technology
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: –40°C to +85°C
- Available in 128-pin PQFP package

Applications

- Broadband gateway/firewall/VPN
- Integrated DSL or cable modem multi-port router
- Wireless LAN access point plus gateway
- Home networking expansion
- Standalone 10/100 switch
- Hotel/campus/MxU gateway
- Enterprise VoIP gateway/phone
- FTTx customer premise equipment
- Managed media converter

Ordering Information

Part Number		Temperature Range	Package
Standard	**Pb (lead)-Free**		
KS8995MA	KSZ8995MA	0°C to +70°C	128-Pin PQFP
KS8995FQ	KSZ8995FQ	0°C to +70°C	128-Pin PQFP
KS8995MAI	KSZ8995MAI	–40°C to +85°C	128-Pin PQFP
KS8995FQI	KSZ8995FQI	–40°C to +85°C	128-Pin PQFP

Revision History

Revision	Date	Summary of Changes
2.0	10/10/03	Created.
2.1	10/30/03	Editorial changes on electrical characteristics.
2.2	04/01/04	Editorial changes on the TTL input and output electrical characteristics.
2.3	01/19/05	Insert recommended reset circuit, pg. 70. Editorial, Pg. 36.
2.4	04/13/05	Changed VDDIO to 3.3V. Changed Jitter to 16 ns Max.
2.5	02/06/06	Added Pb-Free option for Industrial version.
2.6	07/12/06	Add a note for VLAN table write, improve the timing diagram for MII interface, update pin description for PCRS, PCOL, etc. And update the description of the register bits for the loopback, etc.
2.7	06/01/07	Add the package thermal information in the operating rating and the transformer power consumption information in the electrical characteristics note.
2.8	03/20/08	Add KSZ8995FQ information and pin description.
2.9	09/15/08	Add KSZ8995FQ block diagram and descriptions for revision ID and LED mode.
3.0	10/26/11	Update some descriptions for VDDAT voltage, MDI/MDIX bits of the registers. Update the equation of the broadcast storm protection, correct typo.
	12/09/11	Update the description of MDI/MDIX in the MIIM register 0. Correct the typo error for MDI/MDIX bits of the registers.
	01/27/12	Update the description for the VDDAT analog voltage.
	11/08/12	Correct typo error for the commercial temperature and Thermal Resistance θ_{JC}.
	12/12/12	Correct typo and add notes for pins 109, 111.

Contents

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System Level Applications

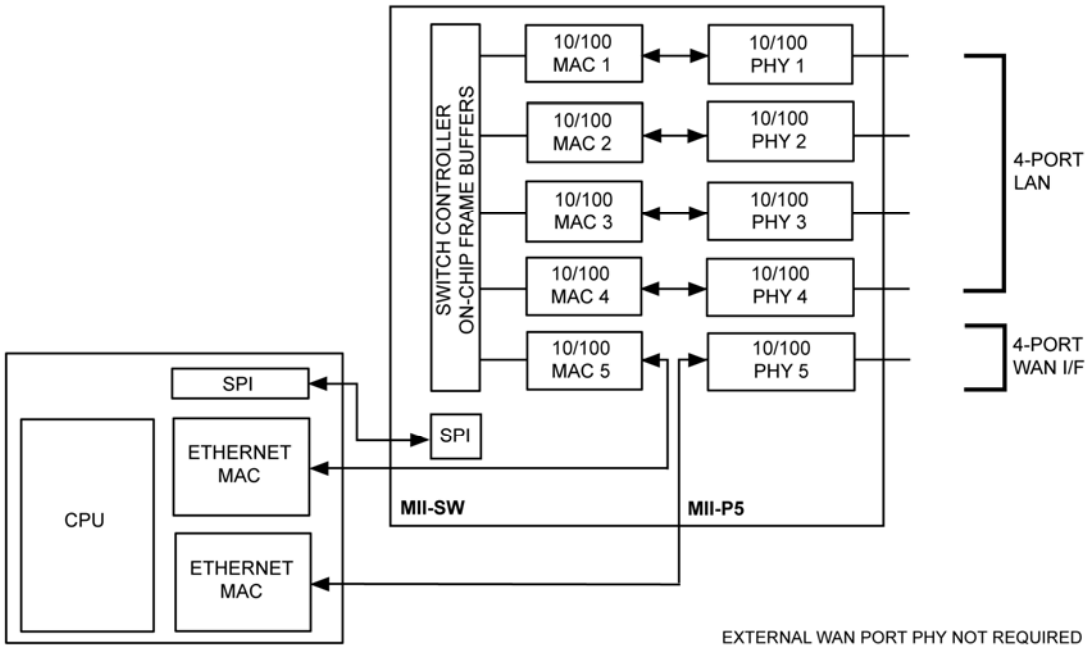


Figure 1. Broadband Gateway

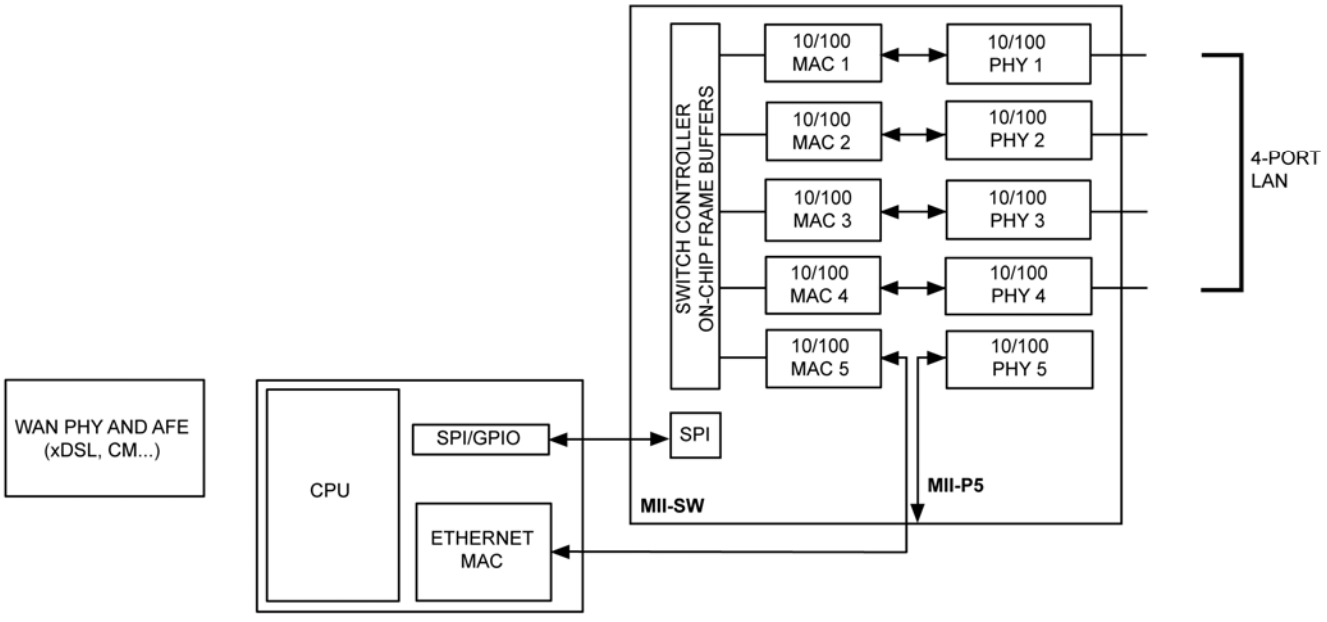


Figure 2. Integrated Broadband Router

System Level Applications (Continued)

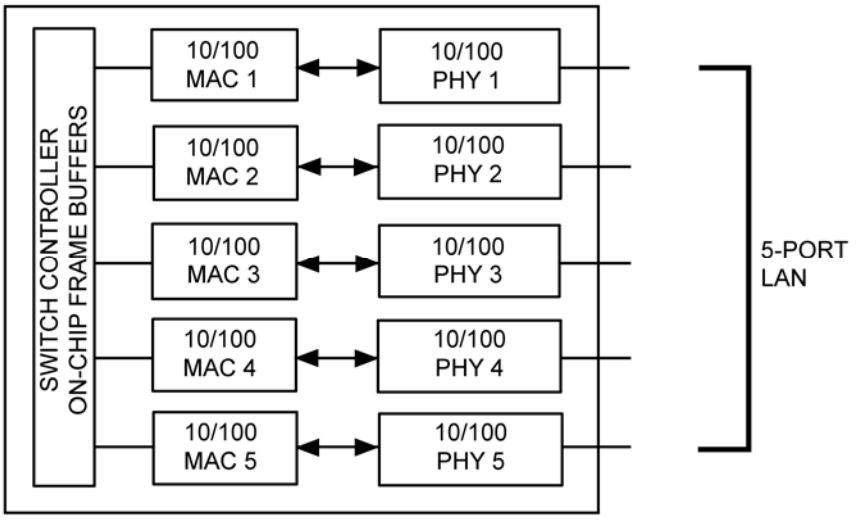


Figure 3. Standalone Switch

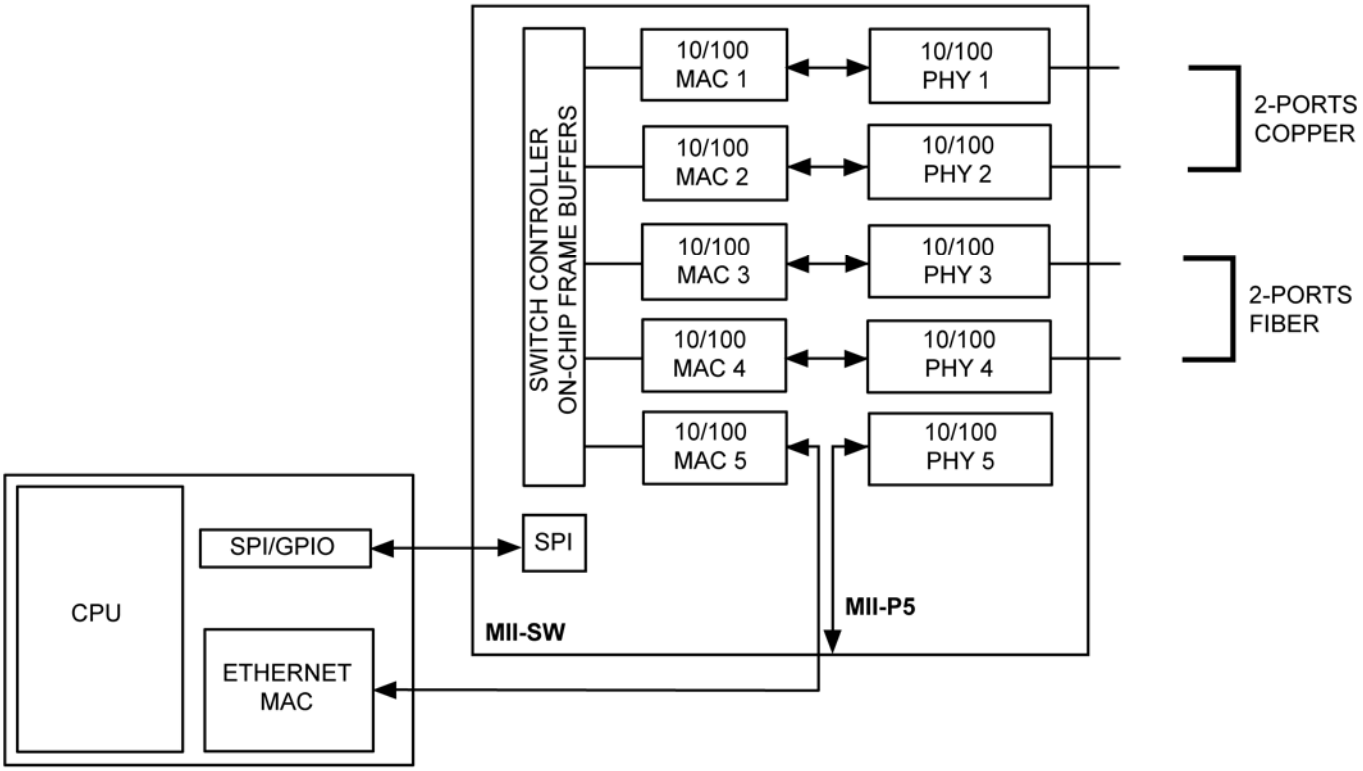
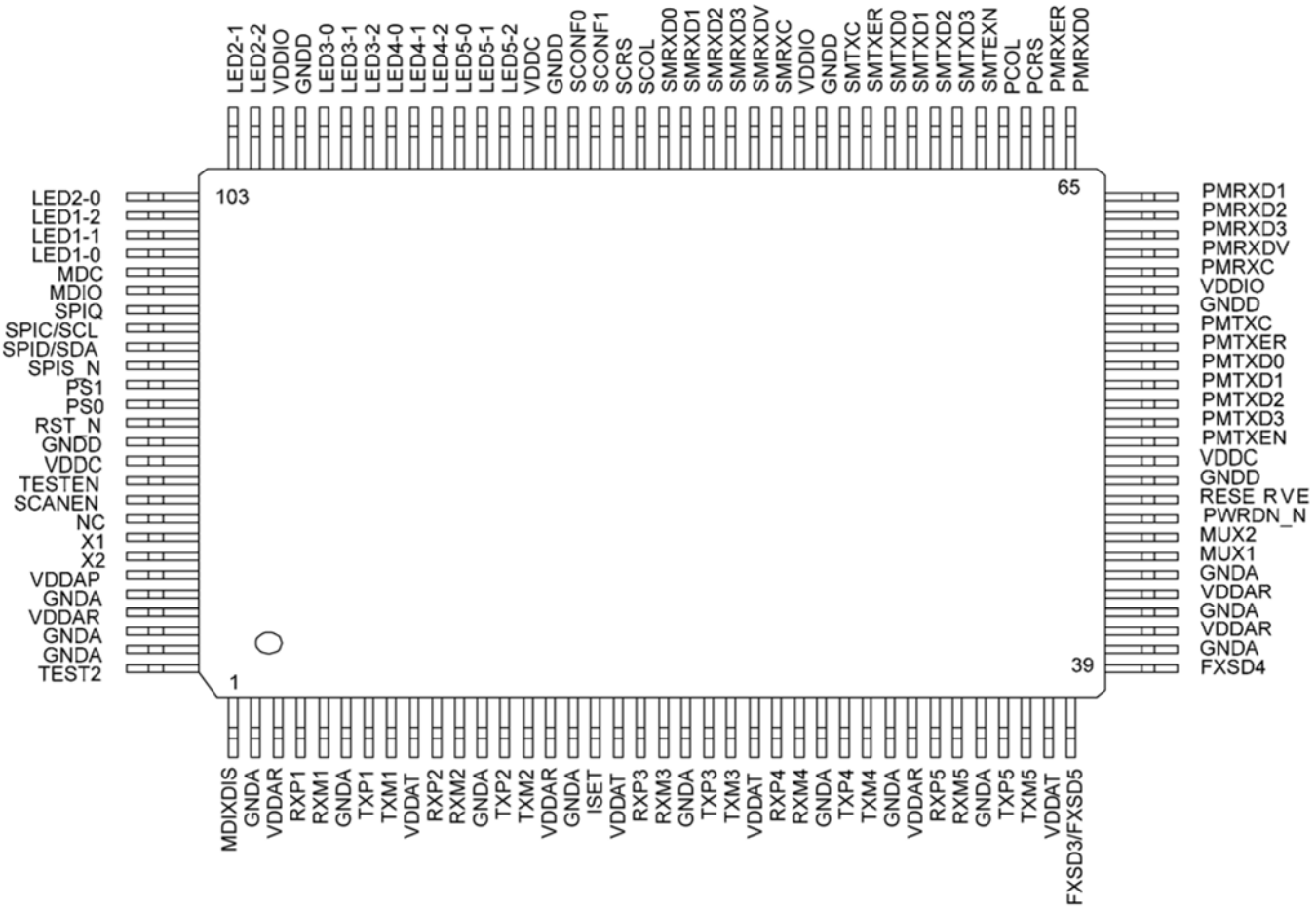


Figure 4. Using KS8995FQ for Dual Media Converter or Fiber Daisy Chain Connection

Pin Configuration



128-Pin PQFP

Pin Description – By Number

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
1	MDI-XDIS	Ipd	1 – 5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GNDA	GND		Analog ground.
3	VDDAR	P		1.8V analog V_{DD}.
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal – (differential).
6	GNDA	GND		Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal – (differential).
9	VDDAT	P		3.3V analog V_{DD}. (2.5V or 3.3V is for B3 and previous chip revision). 3.3V is recommended for new design.
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal – (differential).
12	GNDA	GND		Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
15	VDDAR	P		1.8V analog V_{DD}.
16	GNDA	GND		Analog ground.
17	ISET			Set physical transmit output current. Pull-down with a 3.01kΩ1% resistor.
18	VDDAT	P		3.3V analog V_{DD}. (2.5V or 3.3V is for B3 and previous chip revision). 3.3V is recommended for new design.
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal - (differential).
21	GNDA	GND		Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
24	VDDAT	P		3.3V analog V_{DD}. (2.5V or 3.3V is for B3 and previous chip revision). 3.3V is recommended for new design.
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal - (differential).
27	GNDA	GND		Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
30	GNDA	GND		Analog ground.

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.

Pin Description – By Numbers (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function
31	VDDAR	P		1.8V analog V_{DD}.
32	RXP5	I	5	Physical receive signal + (differential).
33	RXM5	I	5	Physical receive signal – (differential).
34	GNDA	GND		Analog ground.
35	TXP5	O	5	Physical transmit signal + (differential).
36	TXM5	O	5	Physical transmit signal – (differential).
37	VDDAT	P		3.3V analog V_{DD}. (2.5V or 3.3V is for B3 and previous chip revision). 3.3V is recommended for new design.
38	FXSD5/FXSD3	Ipd	5/3	Fiber signal detect pin. FXSD5 is for port 5 of the KS8995MA. FXSD3 is for port 3 of the KS8995FQ
39	FXSD4	Ipd	4	Fiber signal detect pin for port 4.
40	GNDA	GND		Analog ground.
41	VDDAR	P		1.8V analog V_{DD}.
42	GNDA	GND		Analog ground.
43	VDDAR	P		1.8V analog V_{DD}.
44	GNDA	GND		Analog ground.
45	MUX1	NC		Factory test pins. MUX1 and MUX2 should be left unconnected for normal operation.
46	MUX2	NC		**Mode** / **MUX1** / **MUX2** Normal Operation / NC / NC
47	PWRDN_N	Ipu		Full-chip power down. Active low.
48	RESERVE	NC		Reserved pin. No connect.
49	GNDD	GND		Digital ground.
50	VDDC	P		1.8V digital core V_{DD}.
51	PMTXEN	Ipd	5	PHY[5] MII transmit enable.
52	PMTXD3	Ipd	5	PHY[5] MII transmit bit 3.
53	PMTXD2	Ipd	5	PHY[5] MII transmit bit 2.
54	PMTXD1	Ipd	5	PHY[5] MII transmit bit 1.
55	PMTXD0	Ipd	5	PHY[5] MII transmit bit 0.
56	PMTXER	Ipd	5	PHY[5] MII transmit error.
57	PMTXC	O	5	PHY[5] MII transmit clock. PHY mode MII.
58	GNDD	GND		Digital ground.
59	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
60	PMRXC	O	5	PHY[5] MII receive clock. PHY mode MII.

Note:

1. P = Power supply.
   I = Input.
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   I/O = Bidirectional.
   GND = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Description – By Numbers (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
61	PMRXDV	Ipd/O	5	PHY[5] MII receive data valid.
62	PMRXD3	Ipd/O	5	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
63	PMRXD2	Ipd/O	5	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
64	PMRXD1	Ipd/O	5	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
65	PMRXD0	Ipd/O	5	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
66	PMRXER	Ipd/O	5	PHY[5] MII receive error. Strap option: PD (default) = packet size 1518/1522 bytes; PU = 1536 bytes.
67	PCRS	Ipd/O	5	PHY[5] MII carrier sense/strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
68	PCOL	Ipd/O	5	PHY[5] MII collision detect/ strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66
69	SMTXEN	Ipd		Switch MII transmit enable.
70	SMTXD3	Ipd		Switch MII transmit bit 3.
71	SMTXD2	Ipd		Switch MII transmit bit 2.
72	SMTXD1	Ipd		Switch MII transmit bit 1.
73	SMTXD0	Ipd		Switch MII transmit bit 0.
74	SMTXER	Ipd		Switch MII transmit error.
75	SMTXC	I/O		Switch MII transmit clock. Input in MAC mode, output in PHY mode MII.
76	GNDD	GND		Digital ground.
77	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
78	SMRXC	I/O		Switch MII receive clock. Input in MAC mode, output in PHY mode MII.
79	SMRXDV	Ipd/O		Switch MII receive data valid.
80	SMRXD3	Ipd/O		Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control.
81	SMRXD2	Ipd/O		Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full-duplex mode; PU = Switch MII in half-duplex mode.

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.

Pin Description – By Numbers (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
82	SMRXD1	Ipd/O		Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode.
83	SMRXD0	Ipd/O		Switch MII receive bit 0; Strap option: LED mode; PD (default) = mode 0; PU = mode 1. See "Register 11". Mode 0, link at: 100/Full LEDx[2,1,0]=0,0,0 100/Half LEDx[2,1,0]=0,1,0 10/Full LEDx[2,1,0]=0,0,1 10/Half LEDx[2,1,0]=0,1,1 Mode 1, link at 100/Full LEDx[2,1,0]=0,1,0 100/Half LEDx[2,1,0]=0,1,1 10/Full LEDx[2,1,0]=1,0,0 10/Half LEDx[2,1,0]=1,0,1
				Mode 0 / **Mode 1**
				LEDX_2: Lnk/Act / 100Lnk/Act
				LEDX_1: Fulld/Col / 10Lnk/Act
				LEDX_0: Speed / Full duplex
84	SCOL	Ipd/O		Switch MII collision detect.
85	SCRS	Ipd/O		Switch mode carrier sense.
86	SCONF1	Ipd		Dual MII configuration pin. For the Switch MII, KSZ8995MA supports both MAC mode and PHY mode, KSZ8995FQ supports PHY mode only.
				Pin# (91, 86, 87): / **Switch MII** / **PHY [5] MII**
				000: Disable, Otri / Disable, Otri
				001: PHY Mode MII / Disable, Otri
				010: MAC Mode MII / Disable, Otri
				011: PHY Mode SNI / Disable, Otri
				100: Disable / Disable
				101: PHY Mode MII / PHY Mode MII
				110: MAC Mode MII / PHY Mode MII
				111: PHY Mode SNI / PHY Mode MII
87	SCONF0	Ipd		Dual MII configuration pin.
88	GNDD	GND		Digital ground.
89	VDDC	P		1.8V digital core V_{DD}.
90	LED5-2	Ipu/O	5	LED indicator 2. Strap option: aging setup. See "Aging" section. PU (default) = aging enable; PD = aging disable.
91	LED5-1	Ipu/O	5	LED indicator 1. Strap option: PU (default): enable PHY[5] MII I/F. PD: tristate all PHY[5] MII output. See "Pin 86 SCONF1."

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   Otri = Output tristated.
   Fulld = Full duplex

Pin Description – By Numbers (Continued)

Pin Number	Pin Name	Type(1)	Port	Pin Function
92	LED5-0	Ipu/O	5	LED indicator 0.
93	LED4-2	Ipu/O	4	LED indicator 2.
94	LED4-1	Ipu/O	4	LED indicator 1.
95	LED4-0	Ipu/O	4	LED indicator 0.
96	LED3-2	Ipu/O	3	LED indicator 2.
97	LED3-1	Ipu/O	3	LED indicator 1.
98	LED3-0	Ipu/O	3	LED indicator 0.
99	GNDD	GND		Digital ground.
100	VDDIO	P		3.3V digital V_{DD} for digital I/O.
101	LED2-2	Ipu/O	2	LED indicator 2.
102	LED2-1	Ipu/O	2	LED indicator 1.
103	LED2-0	Ipu/O	2	LED indicator 0.
104	LED1-2	Ipu/O	1	LED indicator 2.
105	LED1-1	Ipu/O	1	LED indicator 1.
106	LED1-0	Ipu/O	1	LED indicator 0.
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock.
108	MDIO	I/O	All	Switch or PHY[5] MII management data I/O. Features internal pull down to define pin state when not driven.
109	SPIQ	Otri	All	SPI serial data output in SPI slave mode. Note: an external pull-up is needed on this pin when it is in use.
110	SPIC/SCL	I/O	All	(1) Input clock up to 5MHz in SPI slave mode; (2) output clock at 61kHz in I^2C master mode. See “Pin 113.”
111	SSPID/SDA	I/O	All	(1) Serial data input in SPI slave mode; (2) serial data input/output in I^2C master mode. See “Pin 113.” Note: an external pull-up is needed on this pin when it is in use.
112	SPIS_N	Ipu	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KS8995MA/FQ is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer; (2) not used in I^2C master mode.
113	PS1	Ipd		Serial bus configuration pin. For this case, if the EEPROM is not present, the KS8995MA/FQ will start itself with the PS[1.0] = 00 default register values.
				Pin Configuration / **Serial Bus Configuration**
				PS[1.0]=00 / I^2C Master Mode for EEPROM
				PS[1.0]=01 / Reserved
				PS[1.0]=10 / SPI Slave Mode for CPU Interface
				PS[1.0]=11 / Factory Test Mode (BIST)

Note:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Description – By Numbers (Continued)

Pin Number	Pin Name	Type(1)	Port	Pin Function
114	PS0	Ipd		Serial bus configuration pin. See “Pin 113.”
115	RST_N	Ipu		Reset the KS8995MA/FQ. Active low.
116	GNDD	GND		Digital ground.
117	VDDC	P		1.8V digital core V_{DD}.
118	TESTEN	Ipd		NC for normal operation. Factory test pin.
119	SCANEN	Ipd		NC for normal operation. Factory test pin.
120	NC	NC		No connect.
121	X1	I		25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±50ppm.
122	X2	O		25MHz crystal clock connection.
123	VDDAP	P		1.8V analog V_{DD} for PLL.
124	GNDA	GND		Analog ground.
125	VDDAR	P		1.8V analog V_{DD}.
126	GNDA	GND		Analog ground.
127	GNDA	GND		Analog ground.
128	TEST2	NC		NC for normal operation. Factory test pin.

Note:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   Ipu = Input w/internal pull-up
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Description – By Name

Pin Number	Pin Name	Type[1]	Port	Pin Function
39	FXSD4	I	4	Fiber signal detect/Factory test pin.
38	FXSD3/FXSD5	I	3/5	Fiber signal detect/Factory test pin for FQ port 3 or MA port 5
124	GNDA	GND		Analog ground.
42	GNDA	GND		Analog ground.
44	GNDA	GND		Analog ground.
2	GNDA	GND		Analog ground.
16	GNDA	GND		Analog ground.
30	GNDA	GND		Analog ground.
6	GNDA	GND		Analog ground.
12	GNDA	GND		Analog ground.
21	GNDA	GND		Analog ground.
27	GNDA	GND		Analog ground.
34	GNDA	GND		Analog ground.
40	GNDA	GND		Analog ground.
120	NC	NC		No connect.
127	GNDA	GND		Analog ground.
126	GNDA	GND		Analog ground.
49	GNDD	GND		Digital ground.
88	GNDD	GND		Digital ground.
116	GNDD	GND		Digital ground.
58	GNDD	GND		Digital ground.
76	GNDD	GND		Digital ground.
99	GNDD	GND		Digital ground.
17	ISET			Set physical transmit output current. Pull-down with a 3.01kΩ1% resistor.
106	LED1-0	Ipu/O	1	LED indicator 0.
105	LED1-1	Ipu/O	1	LED indicator 1.
104	LED1-2	Ipu/O	1	LED indicator 2.
103	LED2-0	Ipu/O	2	LED indicator 0.
102	LED2-1	Ipu/O	2	LED indicator 1.
101	LED2-2	Ipu/O	2	LED indicator 2.
98	LED3-0	Ipu/O	3	LED indicator 0.

Note:

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   GND = Ground.
   Ipu = Input w/internal pull-up.
   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Description – By Name (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
97	LED3-1	Ipu/O	3	LED indicator 1.
96	LED3-2	Ipu/O	3	LED indicator 2.
95	LED4-0	Ipu/O	4	LED indicator 0.
94	LED4-1	Ipu/O	4	LED indicator 1.
93	LED4-2	Ipu/O	4	LED indicator 2.
92	LED5-0	Ipu/O	5	LED indicator 0.
91	LED5-1	Ipu/O	5	LED indicator 1. Strap option: PU (default) = enable PHY MII I/F PD: tristate all PHY MII output. See “Pin 86 SCONF1.”
90	LED5-2	Ipu/O	5	LED indicator 2. Strap option: aging setup. See “Aging” section. (default) = aging enable; PD = aging disable.
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock.
108	MDIO	I/O	All	Switch or PHY[5] MII management data I/O.
1	MDI-XDIS	Ipd	1-5	Disable auto MDI/MDI-X.
45	MUX1	NC		Factory test pins. MUX1 and MUX2 should be left unconnected for normal operation.
46	MUX2	NC		
				Mode / **MUX1** / **MUX2**
				Normal Operation / NC / NC
68	PCOL	Ipd/O	5	PHY[5] MII collision detect/force flow control. See “Register 18.” For port 4 only. PD (default) = no force flow control. PU = force flow control.
67	PCRS	Ipd/O	5	PHY[5] MII carrier sense/force duplex mode. See “Register 28.” For port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails.
60	PMRXC	O	5	PHY[5] MII receive clock. PHY mode MII.
65	PMRXD0	Ipd/O	5	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
64	PMRXD1	Ipd/O	5	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
63	PMRXD2	Ipd/O	5	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
62	PMRXD3	Ipd/O	5	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
61	PMRXDV	Ipd/O	5	PHY[5] MII receive data valid.

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   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.

Pin Description – By Name

Pin Number	Pin Name	Type[1]	Port	Pin Function	
57	PMTXC	O	5	PHY[5] MII transmit clock. PHY mode MII.	
55	PMTXD0	Ipd	5	PHY[5] MII transmit bit 0.	
54	PMTXD1	Ipd	5	PHY[5] MII transmit bit 1.	
53	PMTXD2	Ipd	5	PHY[5] MII transmit bit 2.	
52	PMTXD3	Ipd	5	PHY[5] MII transmit bit 3.	
51	PMTXEN	Ipd	5	PHY[5] MII transmit enable.	
56	PMTXER	Ipd	5	PHY[5] MII transmit error.	
114	PS0	Ipd		Serial bus configuration pin. See “Pin 113.”	
113	PS1	Ipd		Serial bus configuration pin. If EEPROM is not present, the KS8995MA/FQ will start itself with chip default (00)...	
				Pin Configuration	**Serial Bus Configuration**
				PS[1:0]=00	I^2C Master Mode for EEPROM
				PS[1:0]=01	Reserved
				PS[1:0]=10	SPI Slave Mode for CPU Interface
				PS[1:0]=11	Factory Test Mode (BIST)
47	PWRDN_N	Ipu		Full-chip power down. Active low.	
48	RESERVE	NC		Reserved pin. No connect.	
115	RST_N	Ipu		Reset the KS8995MA/FQ. Active low.	
5	RXM1	I	1	Physical receive signal – (differential).	
11	RXM2	I	2	Physical receive signal – (differential).	
20	RXM3	I	3	Physical receive signal – (differential).	
26	RXM4	I	4	Physical receive signal – (differential).	
33	RXM5	I	5	Physical receive signal – (differential).	
4	RXP1	I	1	Physical receive signal + (differential).	
10	RXP2	I	2	Physical receive signal + (differential).	
19	RXP3	I	3	Physical receive signal + (differential).	
25	RXP4	I	4	Physical receive signal + (differential).	
32	RXP5	I	5	Physical receive signal + (differential).	
119	SCANEN	Ipd		NC for normal operation. Factory test pin.	
84	SCOL	Ipd/O		Switch MII collision detect.	
87	SCONF0	Ipd		Dual MII configuration pin.	

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   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   NC = No connect.

Pin Description – By Name

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]		
86	SCONF1	Ipd		Dual MII configuration pin. For the Switch MII, KSZ8995MA supports both MAC mode and PHY mode, KSZ8995FQ supports PHY mode only.		
				Pin# (91, 86, 87):	**Switch MII**	**PHY [5] MII**
				000	Disable, Otri	Disable, Otri
				001	PHY Mode MII	Disable, Otri
				010	MAC Mode MII	Disable, Otri
				011	PHY Mode SNI	Disable, Otri
				100	Disable	Disable
				101	PHY Mode MII	PHY Mode MII
				110	MAC Mode MII	PHY Mode MII
				111	PHY Mode SNI	PHY Mode MII
85	SCRS	Ipd/O		Switch mode carrier sense.		
78	SMRXC	I/O		Switch MII receive clock. Input in MAC mode, output in PHY mode MII.		
83	SMRXD0	Ipd/O		Switch MII receive bit 0; Strap option: LED mode PD (default) = mode 0; PU = mode 1. See “Register 11.”		
					Mode 0	**Mode 1**
				LEDX_2	Lnk/Act	100Lnk/Act
				LEDX_1	Fulld/Col	10Lnk/Act
				LEDX_0	Speed	Full duplex
82	SMRXD1	Ipd/O		Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode.		
81	SMRXD2	Ipd/O		Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full-duplex mode; PU = Switch MII in half-duplex mode.		
80	SMRXD3	Ipd/O		Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control.		
79	SMRXDV	Ipd/O		Switch MII receive data valid.		
75	SMTXC	I/O		Switch MII transmit clock. Input in MAC mode, output in PHY mode MII.		
73	SMTXD0	Ipd		Switch MII transmit bit 0.		
72	SMTXD1	Ipd		Switch MII transmit bit 1.		
71	SMTXD2	Ipd		Switch MII transmit bit 2.		
70	SMTXD3	Ipd		Switch MII transmit bit 3.		
69	SMTXEN	Ipd		Switch MII transmit enable.		
74	SMTXER	Ipd		Switch MII transmit error.		

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   I/O = Bidirectional.
   GND = Ground.
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   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   Otri = Output tristated.
   NC = No connect.
2. PU = Strap pin pull-up.
   PD = Strap pull-down.
   Fulld = Full duplex

Pin Description – By Name

Pin Number	Pin Name	Type(1)	Port	Pin Function
110	SPIC/SCL	I/O	All	(1) Input clock up to 5MHz in SPI slave mode; (2) output clock at 61kHz in I^2C master mode. See “Pin 113.”
111	SSPID/SDA	I/O	All	(1) Serial data input in SPI slave mode; (2) serial data input/output in I^2C master mode. See “Pin 113.” Note: an external pull-up is needed on this pin when it is in use.
109	SPIQ	Otri	All	SPI serial data output in SPI slave mode. Note: an external pull-up is needed on this pin when it is in use.
112	SPIS_N	Ipu	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KS8995MA/FQ is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer; (2) not used in I^2C master mode.
128	TEST2	NC		NC for normal operation. Factory test pin.
118	TESTEN	Ipd		NC for normal operation. Factory test pin.
8	TXM1	O	1	Physical transmit signal – (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
36	TXM5	O	5	Physical transmit signal – (differential).
7	TXP1	O	1	Physical transmit signal + (differential).
13	TXP2	O	2	Physical transmit signal + (differential).
22	TXP3	O	3	Physical transmit signal + (differential).
28	TXP4	O	4	Physical transmit signal + (differential).
35	TXP5	O	5	Physical transmit signal + (differential).
123	VDDAP	P		1.8V analog V_{DD} for PLL.
41	VDDAR	P		1.8V analog V_{DD}.
43	VDDAR	P		1.8V analog V_{DD}.
3	VDDAR	P		1.8V analog V_{DD}.
15	VDDAR	P		1.8V analog V_{DD}.
31	VDDAR	P		1.8V analog V_{DD}.
125	VDDAR	P		1.8V analog V_{DD}.
18	VDDAT	P		3.3V analog V_{DD}.
9	VDDAT	P		3.3V analog V_{DD}.
24	VDDAT	P		3.3V analog V_{DD}.
37	VDDAT	P		3.3V analog V_{DD}.
50	VDDC	P		1.8V digital core V_{DD}.

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   Ipd = Input w/internal pull-down.
   Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
   Otri = Output tristated.
   NC = No connect.

Pin Description – By Name

Pin Number	Pin Name	Type[1]	Port	Pin Function
89	VDDC	P		1.8V digital core V_{DD}.
117	VDDC	P		1.8V digital core V_{DD}.
59	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
77	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
100	VDDIO	P		3.3V digital V_{DD} for digital I/O circuitry.
121	X1	I		25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±50ppm.
122	X2	O		25MHz crystal clock connection.

Note:
1. P = Power supply.
I = Input.
O = Output.