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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# KS8995M

## Integrated 5-Port 10/100 Managed Switch

**Rev 1.13**

## General Description

The KS8995M is a highly integrated Layer-2 managed switch with optimized BOM (Bill of Materials) cost for low port count, cost-sensitive 10/100Mbps switch systems. It also provides an extensive feature set such as tag/port-based VLAN, QoS (Quality of Service) priority, management, MIB counters, dual MII interfaces and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KS8995M contains five 10/100 transceivers with patented mixed-signal low-power technology, five MAC (Media Access Control) units, a high-speed non-blocking switch fabric, a dedicated address look-up engine, and an on-chip frame buffer memory.

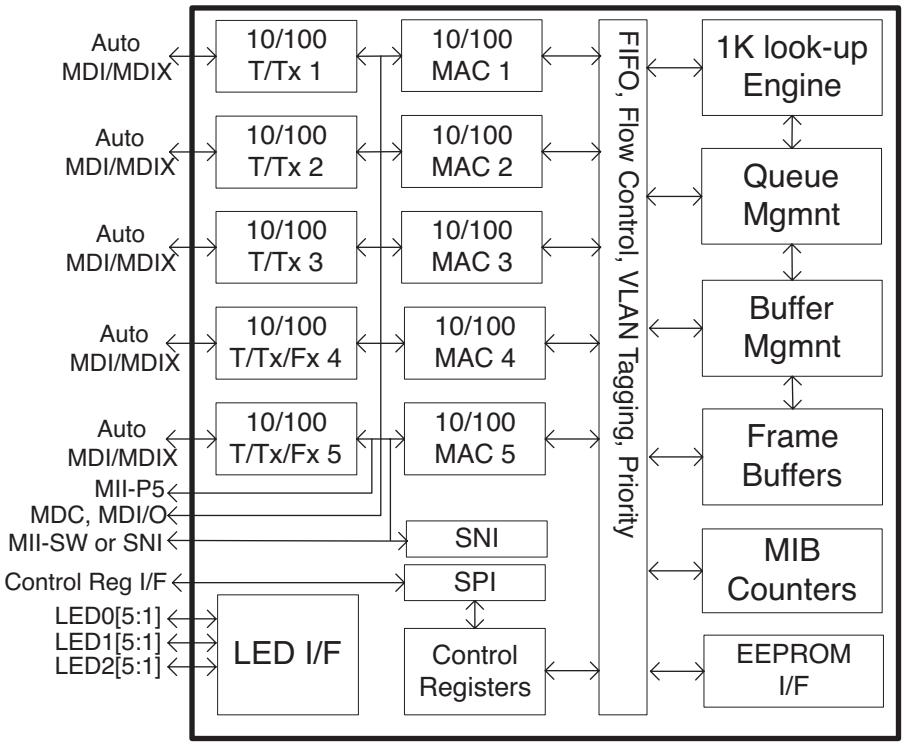
All PHY units support 10BaseT and 100BaseTX. In addition, two of the PHY units support 100BaseFX (Ports 4 and 5).

All support documentation can be found on Micrel's web site at: www.micrel.com.

## Features

- Integrated switch with five MACs and five Fast Ethernet transceivers fully compliant to IEEE 802.3u standard
- Shared memory based switch fabric with fully non-blocking configuration
- 1.4Gbps high-performance memory bandwidth
- 10BaseT, 100BaseTX and 100BaseFX modes (FX in Ports 4 and 5)
- Dual MII configuration: MII-Switch (MAC or PHY mode MII) and MII-P5 (PHY mode MII)
- IEEE 802.1q tag-based VLAN (16 VLANs, full-range VID) for DMZ port, WAN/LAN separation or inter-VLAN switch links
- VLAN ID tag/untag options, per-port basis
- Programmable rate limiting 0Mbps to 100Mbps, ingress and egress port, rate options for high and low priority, per-port-basis
- Flow control or drop packet rate limiting (ingress port)
- Integrated MIB counters for fully compliant statistics gathering, 34 MIB counters per port

## Functional Diagram




**KS8995M**

## Features (continued)

- Enable/Disable option for huge frame size up to 1916 bytes per frame
- IGMP v1/v2 snooping for multicast packet filtering
- Special tagging mode to send CPU info on ingress packet's port value
- SPI slave (complete) and MDIO (MII PHY only) serial management interface for control of register configuration
- MAC-id based security lock option
- Control registers configurable on-the-fly (port-priority, 802.1p/d/q, AN...)
- CPU read access to MAC forwarding table entries
- 802.1d Spanning Tree Protocol
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
- Broadcast storm protection with percent control – global and per-port basis
- Optimization for fiber-to-copper media conversion
- Full-chip hardware power-down support (register configuration not saved)
- Per-port based software power-save on PHY (idle link detection, register configuration preserved)
- QoS/CoS packets prioritization supports: per port, 802.1p and DiffServ based
- 802.1p/q tag insertion or removal on a per port basis (egress)
- MDC and MDI/O interface support to access the MII PHY control registers (not all control registers)
- MII local loopback support
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table)
- Wire-speed reception and transmission
- Integrated look-up engine with dedicated 1K MAC addresses
- Full duplex IEEE 802.3x and half-duplex back pressure flow control
- Comprehensive LED support
- 7-wire SNI support for legacy MAC interface
- Automatic MDI/MDI-X crossover for plug-and-play
- Disable Automatic MDI/MDI-X option
- Low power:
  Core: 1.8V
  I/O: 2.5V or 3.3V
- 0.18μm CMOS technology
- Commercial temperature range: 0°C to +70°C
- Industrial temperature range: –40°C to +85°C
- Available in 128-pin PQFP package

## Applications

- Broadband gateway/firewall/VPN
- Integrated DSL or cable modem multi-port router
- Wireless LAN access point plus gateway
- Home networking expansion
- Standalone 10/100 switch
- Hotel/campus/MxU gateway
- Enterprise VoIP gateway/phone
- FTTx customer premise equipment
- Managed media converter

## Ordering Information

| Part Number | Temperature Range | Package |
|---|---|---|
| KS8995M | 0°C to +70°C | 128-Pin PQFP |
| KSZ8995M | 0°C to +70°C | 128-Pin PQFP Lead Free |
| KS8995MI | –40°C to +85°C | 128-Pin PQFP |

## Revision History

| Revision | Date | Summary of Changes |
|---|---|---|
| 1.00 | 11/05/01 | Created |
| 1.01 | 11/09/01 | Pinout Mux1/2, DVCC-IO 2.5/3.3V, feature list, register spec 11-09 |
| 1.02 | 12/03/01 | Editorial changes, added new register and MIB descriptions. Added paragraph describing TOS registers. Imported functional descriptions. Formatting. |
| 1.03 | 12/12/01 | Incorporate changes per engineering feedback as well as updating functional descriptions and adding new timing information. |
| 1.04 | 12/13/01 | Changed Rev. and For. Modes to PHY and MAC modes respectively. Added MIIM clarification in “MII Management Interface” section. Reformatted section sequence. Added hex register addresses. Added advertisement ability descriptions. |
| 1.05 | 12/18/01 | Inserted switch forwarding flow charts. |
| 1.06 | 12/20/01 | Added new KS8995M block diagram, editorial changes, register descriptions changes and cross-references from functional descriptions to register and strap in options. |
| 1.07 | 1/22/01 | Changed FXSD pins to inputs, added new descriptions to “Configuration Interfaces” section. Edited pin descriptions. |
| 1.08 | 3/1/02 | Editorial changes in “Dynamic MAC Address table and “MIB Counters.” Updated figure 2 flowchart. Updated table 2 for MAC mode connections. Separate static MAC bit assignments for read and write. Edited read and write examples to MAC tables and MIB counters. Changed Table 3 KS8995M signals to “S” suffix. Changed aging description in Register 2, bit 0. Changed “Port Registers” section and listed all port register addresses. Changed port control 11 description for bits [7:5]. Changed MIB counter descriptions. |
| 1.09 | 5/17/02 | Changed MII setting in “Pin Descriptions.” Changed pu/pd descriptions for SMRXD2. “Register 18,” changed pu/pd description for forced flow control. “Illegal Frames. ” Edited large packet sizes back in. “Elecrical Characteristics,” Added in typical supply current numbers for 100 BaseTX and 10 BaseTX operation. “Register 18,” Added in note for illegal half-duplex, force flow control. “Pin Description,” Added extra X1 clock input description. “Elecrical Characteristics,” Updated to chip only current numbers. Added SPI Timing. Feature Highlights. |
| 1.10 | 7/29/02 | “Pin Description,” changed SMRXC and SMTXC to I/O. Input in MAC mode, output in PHY mode MII. “Elecrical Characteristics,” modified current consumption to chip only numbers. “Half-Duplex Back Pressure,” added description for no dropped packets in half-duplex mode. Added recommended operating conditions. Added Idle mode current consumption in “Elecrical Characteristics,” added “Selection of Isolation Transformers,” Added 3.01kΩ resistor instructions for ISET “Pin Description” section. Changed Polarity of transmit pairs in “Pin Description.” Changed description for Register 2, bit 1, in “Register Description” section. Added “Reset Timing” section. |
| 1.11 | 12/17/02 | “Register 3” changed 802.1x to 802.3x. “Register 6,” changed default column to disable flow control for pull-down, and enable flow control for pull-up. “Register 29” and “Register 0” indicate loop back is at the PHY. Added description to register 4 bit 2 to indicate that STPID packets from CPU to normal ports are not allowed as 1522 byte tag packets. Fixed dynamic MAC address example errors in “Dynamic MAC Address Table.” Changed definition of forced MDI, MDIX in section “Register 29,” “Register 30” and “Register 0.” Added “Part Ordering Information.” Added Ambient operating temperature for KS8995MI |
| 1.12 | 3/10/03 | Changed pin 120 description to NC. Changed SPIQ pin description to Otri. Changed logo. Changed contact information. |
| 1.13 | 7/5/06 | Add a note for VLAN table write, improve the timing diagram of MAC mode and PHY mode for MII interface, change VDDIO support 3.3V only, update pin description for PCRS, PCOL, and so on. |

# Table of Contents

**System Level Applications** ..... 7
**Pin Description (by Number)** ..... 9
**Pin Description (by Name)** ..... 15
**Pin Configuration** ..... 21
**Introduction** ..... 22
**Functional Overview: Physical Layer Transceiver** ..... 22
100BaseTX Transmit ..... 22
100BaseTX Receive ..... 22
PLL Clock Synthesizer ..... 22
Scrambler/De-scrambler (100BaseTX only) ..... 22
100BaseFX Operation ..... 22
100BaseFX Signal Detection ..... 22
100BaseFX Far End Fault ..... 23
10BaseT Transmit ..... 23
10BaseT Receive ..... 23
Power Management ..... 23
MDI/MDI-X Auto Crossover ..... 23
Auto-Negotiation ..... 23
**Functional Overview: Switch Core** ..... 24
Address Look-Up ..... 24
Learning ..... 24
Migration ..... 24
Aging ..... 24
Forwarding ..... 24
Switching Engine ..... 24
MAC Operation ..... 24
Inter-Packet Gap (IPG) ..... 24
Backoff Algorithm ..... 24
Late Collision ..... 26
Illegal Frames ..... 26
Flow Control ..... 26
Half-Duplex Back Pressure ..... 26
Broadcast Storm Protection ..... 26
MII Interface Operation ..... 26
SNI Interface Operation ..... 28
**Advanced Functionality** ..... 28
Spanning Tree Support ..... 28
Special Tagging Mode ..... 29
IGMP Support ..... 30
Port Mirroring Support ..... 31
VLAN Support ..... 31
Rate Limit Support ..... 32
Configuration Interface ..... 33
I2C Master Serial Bus Configuration ..... 35
SPI Slave Serial Bus Configuration ..... 35
MII Management Interface (MIIM) ..... 38

**Register Description** ..... 39
Global Registers ..... 39
Register 0 (0x00): Chip ID0 ..... 39
Register 1 (0x01): Chip ID1/Start Switch ..... 39
Register 2 (0x02): Global Control 0 ..... 40
Register 3 (0x03): Global Control 1 ..... 40
Register 4 (0x04): Global Control 2 ..... 41
Register 5 (0x05): Global Control 3 ..... 42
Register 6 (0x06): Global Control 4 ..... 42
Register 7 (0x07): Global Control 5 ..... 43
Register 8 (0x08): Global Control 6 ..... 43
Register 9 (0x09): Global Control 7 ..... 43
Register 10 (0x0A): Global Control 8 ..... 43
Register 11 (0x0B): Global Control 9 ..... 43
Port Registers ..... 44
Register 16 (0x10): Port 1 Control 0 ..... 44
Register 17 (0x11): Port 1 Control 1 ..... 44
Register 18 (0x12): Port 1 Control 2 ..... 45
Register 19 (0x13): Port 1 Control 3 ..... 46
Register 20 (0x14): Port 1 Control 4 ..... 46
Register 21 (0x15): Port 1 Control 5 ..... 46
Register 22 (0x16): Port 1 Control 6 ..... 46
Register 23 (0x17): Port 1 Control 7 ..... 46
Register 24 (0x18): Port 1 Control 8 ..... 47
Register 25 (0x19): Port 1 Control 9 ..... 47
Register 26 (0x1A): Port 1 Control 10 ..... 47
Register 27 (0x1B): Port 1 Control 11 ..... 47
Register 28 (0x1C): Port 1 Control 12 ..... 48
Register 29 (0x1D): Port 1 Control 13 ..... 49
Register 30 (0x1E): Port 1 Status 0 ..... 49
Register 31 (0x1F): Port 1 Status 1 ..... 50
Advanced Control Registers ..... 50
Register 96 (0x60): TOS Priority Control Register 0 ..... 50
Register 97 (0x61): TOS Priority Control Register 1 ..... 50
Register 98 (0x62): TOS Priority Control Register 2 ..... 50
Register 99 (0x63): TOS Priority Control Register 3 ..... 50
Register 100 (0x64): TOS Priority Control Register 4 ..... 50
Register 101 (0x65): TOS Priority Control Register 5 ..... 50
Register 102 (0x66): TOS Priority Control Register 6 ..... 50
Register 103 (0x67): TOS Priority Control Register 7 ..... 50
Register 104 (0x68): MAC Address Register 0 ..... 50
Register 105 (0x69): MAC Address Register 1 ..... 50
Register 106 (0x6A): MAC Address Register 2 ..... 50
Register 107 (0x6B): MAC Address Register 3 ..... 50
Register 108 (0x6C): MAC Address Register 4 ..... 50
Register 109 (0X6D): MAC Address Register 5 ..... 50
Register 110 (0x6E): Indirect Access Control 0 ..... 51
Register 111 (0x6F): Indirect Access Control 1 ..... 51

Register 112 (0x70): Indirect Data Register 8 ..... 51
Register 113 (0x71): Indirect Data Register 7 ..... 51
Register 114 (0x72): Indirect Data Register 6 ..... 51
Register 115 (0x73): Indirect Data Register 5 ..... 51
Register 116 (0x74): Indirect Data Register 4 ..... 51
Register 117 (0x75): Indirect Data Register 3 ..... 51
Register 118 (0x76): Indirect Data Register 2 ..... 51
Register 119 (0x77): Indirect Data Register 1 ..... 51
Register 120 (0x78): Indirect Data Register 0 ..... 51
Register 121 (0x79): Digital Testing Status 0 ..... 51
Register 122 (0x7A): Digital Testing Status 1 ..... 51
Register 123 (0x7B): Digital Testing Control 0 ..... 51
Register 124 (0x7C): Digital Testing Control 1 ..... 51
Register 125 (0x7D): Analog Testing Control 0 ..... 51
Register 126 (0x7E): Analog Testing Control 1 ..... 52
Register 127 (0x7F): Analog Testing Status ..... 52
**Static MAC Address** ..... 53
**VLAN Address** ..... 55
**Dynamic MAC Address** ..... 56
**MIB Counters** ..... 57
**MIIM Registers** ..... 60
Register 0: MII Control ..... 60
Register 1: MII Status ..... 61
Register 2: PHYID HIGH ..... 61
Register 3: PHYID LOW ..... 61
Register 4: Advertisement Ability ..... 61
Register 5: Link Partner Ability ..... 62
**Absolute Maximum Ratings** ..... 63
**Operating Ratings** ..... 63
**Electrical Characteristics** ..... 63
**Timing Diagrams** ..... 65
**Selection of Isolation Transformers** ..... 72
**Qualified Magnetic Lists** ..... 72
**Package Information** ..... 73

## System Level Applications

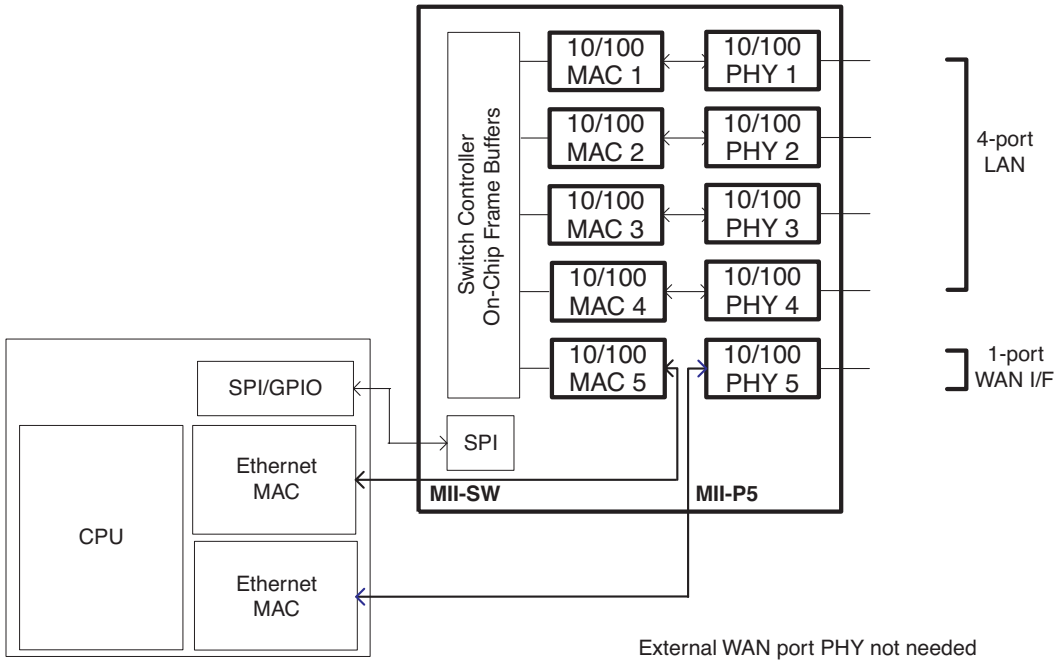



**Figure 1. Broadband Gateway**

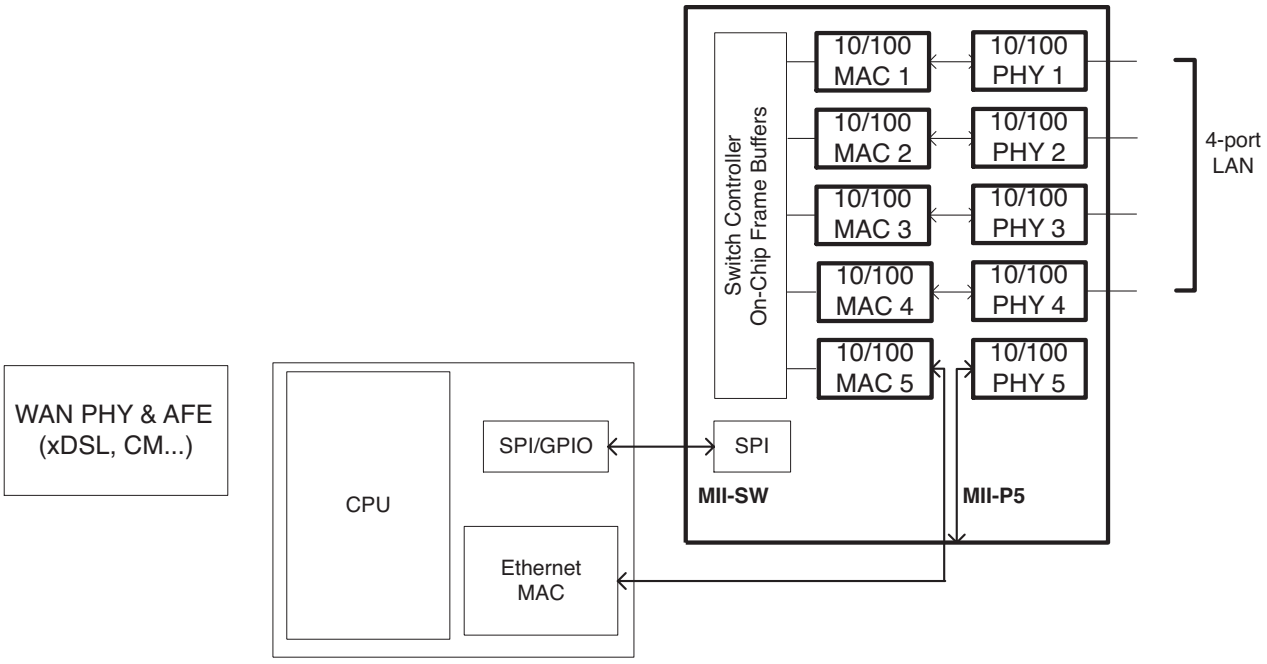



**Figure 2. Integrated Broadband Router**

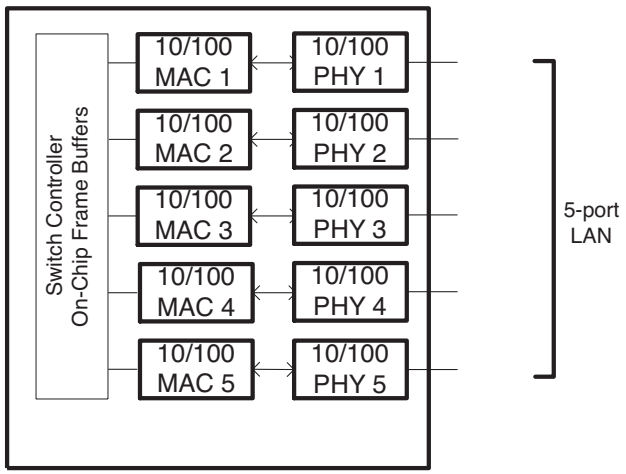



**Figure 3. Standalone Switch**

## Pin Description (by Number)

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 1 | TEST1 | NC | | NC for normal operation. Factory test pin. |
| 2 | GNDA | Gnd | | Analog ground |
| 3 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 4 | RXP1 | I | 1 | Physical receive signal + (differential) |
| 5 | RXM1 | I | 1 | Physical receive signal - (differential) |
| 6 | GNDA | Gnd | | Analog ground |
| 7 | TXM1 | O | 1 | Physical transmit signal - (differential) |
| 8 | TXP1 | O | 1 | Physical transmit signal + (differential) |
| 9 | VDDAT | P | | 2.5V analog $V_{DD}$ |
| 10 | RXP2 | I | 2 | Physical receive signal + (differential) |
| 11 | RXM2 | I | 2 | Physical receive signal - (differential) |
| 12 | GNDA | Gnd | | Analog ground |
| 13 | TXM2 | O | 2 | Physical transmit signal - (differential) |
| 14 | TXP2 | O | 2 | Physical transmit signal + (differential) |
| 15 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 16 | GNDA | Gnd | | Analog ground |
| 17 | ISET | | | Set physical transmit output current. Pull-down with a 3.01kΩ 1% resistor. |
| 18 | VDDAT | P | | 2.5V analog $V_{DD}$ |
| 19 | RXP3 | I | 3 | Physical receive signal + (differential) |
| 20 | RXM3 | I | 3 | Physical receive signal - (differential) |
| 21 | GNDA | Gnd | | Analog ground |
| 22 | TXM3 | O | 3 | Physical transmit signal - (differential) |
| 23 | TXP3 | O | 3 | Physical transmit signal + (differential) |
| 24 | VDDAT | P | | 2.5V analog $V_{DD}$ |
| 25 | RXP4 | I | 4 | Physical receive signal + (differential) |
| 26 | RXM4 | I | 4 | Physical receive signal - (differential) |
| 27 | GNDA | Gnd | | Analog ground |
| 28 | TXM4 | O | 4 | Physical transmit signal - (differential) |
| 29 | TXP4 | O | 4 | Physical transmit signal + (differential) |
| 30 | GNDA | Gnd | | Analog ground |
| 31 | VDDAR | P | | 1.8V analog $V_{DD}$ |

**Note:**

1. P = Power supply
   I = Input
   O = Output
   I/O = Bi-directional
   Gnd = Ground
   Ipu = Input w/ internal pull-up
   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 32 | RXP5 | I | 5 | Physical receive signal + (differential) |
| 33 | RXM5 | I | 5 | Physical receive signal - (differential) |
| 34 | GNDA | Gnd | | Analog ground |
| 35 | TXM5 | O | 5 | Physical transmit signal - (differential) |
| 36 | TXP5 | O | 5 | Physical transmit signal + (differential) |
| 37 | VDDAT | P | | 2.5V analog $V_{DD}$ |
| 38 | FXSD5 | I | 5 | Fiber signal detect/factory test pin, pull-down for TX mode |
| 39 | FXSD4 | I | 4 | Fiber signal detect/factory test pin, pull-down for TX mode |
| 40 | GNDA | Gnd | | Analog ground |
| 41 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 42 | GNDA | Gnd | | Analog ground |
| 43 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 44 | GNDA | Gnd | | Analog ground |
| 45 | MUX1 | NC | | MUX1 and MUX2 should be left unconnected for normal operation. They are factory test pins. |
| 46 | MUX2 | NC | | |

| Mode | Mux1 | Mux2 |
|---|---|---|
| Normal Operation | NC | NC |
| Remote Analog Loopback Mode for Testing only | 0 | 1 |
| Reserved | 1 | 0 |
| Power Save Mode for Testing only | 1 | 1 |

| | | | | |
|---|---|---|---|---|
| 47 | PWRDN_N | Ipu | | Full-chip power down. Active low. |
| 48 | RESERVE | NC | | Reserved pin. No connect. |
| 49 | GNDD | Gnd | | Digital ground |
| 50 | VDDC | P | | 1.8V digital core $V_{DD}$ |
| 51 | PMTXEN | Ipd | 5 | PHY[5] MII transmit enable |
| 52 | PMTXD3 | Ipd | 5 | PHY[5] MII transmit bit 3 |
| 53 | PMTXD2 | Ipd | 5 | PHY[5] MII transmit bit 2 |
| 54 | PMTXD1 | Ipd | 5 | PHY[5] MII transmit bit 1 |
| 55 | PMTXD0 | Ipd | 5 | PHY[5] MII transmit bit 0 |
| 56 | PMTXER | Ipd | 5 | PHY[5] MII transmit error |
| 57 | PMTXC | O | 5 | PHY[5] MII transmit clock. PHY mode MII. |
| 58 | GNDD | Gnd | | Digital ground |

**Note:**

1. P = Power supply
   I = Input
   O = Output
   I/O = Bi-directional
   Gnd = Ground
   Ipu = Input w/ internal pull-up
   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 59 | VDDIO | P | | 3.3V digital $V_{DD}$ for digital I/O circuitry |
| 60 | PMRXC | O | 5 | PHY[5] MII receive clock. PHY mode MII |
| 61 | PMRXDV | Ipd/O | 5 | PHY[5] MII receive data valid |
| 62 | PMRXD3 | Ipd/O | 5 | PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control. |
| 63 | PMRXD2 | Ipd/O | 5 | PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure. |
| 64 | PMRXD1 | Ipd/O | 5 | PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets. |
| 65 | PMRXD0 | Ipd/O | 5 | PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement. |
| 66 | PMRXER | Ipd/O | 5 | PHY[5] MII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes. |
| 67 | PCRS | Ipd/O | 5 | PHY[5] MII carrier sense. Strap option for port 4 only. See *"Register 76."* PD (default) = Force half-duplex if auto-negotiation is disabled or fails. PU = Force full-duplex if auto-negotiation is disabled or fails. |
| 68 | PCOL | Ipd/O | 5 | PHY[5] MII collision detect. Strap option for port 4 only. See *"Register 66."* PD (default) = No force flow control. PU = Force flow control. |
| 69 | SMTXEN | Ipd | | Switch MII transmit enable |
| 70 | SMTXD3 | Ipd | | Switch MII transmit bit 3 |
| 71 | SMTXD2 | Ipd | | Switch MII transmit bit 2 |
| 72 | SMTXD1 | Ipd | | Switch MII transmit bit 1 |
| 73 | SMTXD0 | Ipd | | Switch MII transmit bit 0 |
| 74 | SMTXER | Ipd | | Switch MII transmit error |
| 75 | SMTXC | I/O | | Switch MII transmit clock. Input in MAC mode, output in PHY mode MII. |
| 76 | GNDD | Gnd | | Digital ground |
| 77 | VDDIO | P | | 3.3V digital $V_{DD}$ for digital I/O circuitry |
| 78 | SMRXC | I/O | | Switch MII receive clock. Input in MAC mode, output in PHY mode MII. |
| 79 | SMRXDV | Ipd/O | | Switch MII receive data valid |
| 80 | SMRXD3 | Ipd/O | | Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control. |
| 81 | SMRXD2 | Ipd/O | | Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full-duplex mode; PU = Switch MII in half-duplex mode. |

**Note:**

1. P = Power supply
   I = Input
   O = Output
   I/O = Bi-directional
   Gnd = Ground
   Ipu = Input w/ internal pull-up
   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 82 | SMRXD1 | Ipd/O | | Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode. |
| 83 | SMRXD0 | Ipd/O | | Switch MII receive bit 0; Strap option: LED Mode<br>PD (default) = Mode 0; PU = Mode 1. See *"Register 11."* |

| | **Mode 0** | **Mode 1** |
|---|---|---|
| LEDX_2 | Lnk/Act | 100Lnk/Act |
| LEDX_1 | Fulld/Col | 10Lnk/Act |
| LEDX_0 | Speed | Fulld |

| | | | | |
|---|---|---|---|---|
| 84 | SCOL | Ipd/O | | Switch MII collision detect |
| 85 | SCRS | Ipd/O | | Switch MII carrier sense |
| 86 | SCONF1 | Ipd | | Dual MII configuration pin |

| **Pin# (91, 86, 87):** | **Switch MII** | **PHY [5] MII** |
|---|---|---|
| 000 | Disable, Otri | Disable, Otri |
| 001 | PHY Mode MII | Disable, Otri |
| 010 | MAC Mode MII | Disable, Otri |
| 011 | PHY Mode SNI | Disable, Otri |
| 100 | Disable | Disable |
| 101 | PHY Mode MII | PHY Mode MII |
| 110 | MAC Mode MII | PHY Mode MII |
| 111 | PHY Mode SNI | PHY Mode MII |

| | | | | |
|---|---|---|---|---|
| 87 | SCONF0 | Ipd | | Dual MII configuration pin |
| 88 | GNDD | Gnd | | Digital ground |
| 89 | VDDC | P | | 1.8V digital core $V_{DD}$ |
| 90 | LED5-2 | Ipu/O | 5 | LED indicator 2. Strap option: Aging setup. See *"Aging"* section<br>PU (default) = Aging Enable; PD = Aging disable. |
| 91 | LED5-1 | Ipu/O | 5 | LED indicator 1. Strap option: PU (default): enable PHY [5] MII I/F<br>PD: tristate all PHY [5] MII output. See *"pin# 86 SCONF1."* |
| 92 | LED5-0 | Ipu/O | 5 | LED indicator 0 |
| 93 | LED4-2 | Ipu/O | 4 | LED indicator 2 |
| 94 | LED4-1 | Ipu/O | 4 | LED indicator 1 |
| 95 | LED4-0 | Ipu/O | 4 | LED indicator 0 |
| 96 | LED3-2 | Ipu/O | 3 | LED indicator 2 |
| 97 | LED3-1 | Ipu/O | 3 | LED indicator 1 |

**Note:**

1. P = Power supply
   I = Input
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   I/O = Bi-directional
   Gnd = Ground
   Ipu = Input w/ internal pull-up
   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 98 | LED3-0 | Ipu/O | 3 | LED indicator 0 |
| 99 | GNDD | Gnd | | Digital ground |
| 100 | VDDIO | P | | 3.3V digital $V_{DD}$ for digital I/O |
| 101 | LED2-2 | Ipu/O | 2 | LED indicator 2 |
| 102 | LED2-1 | Ipu/O | 2 | LED indicator 1 |
| 103 | LED2-0 | Ipu/O | 2 | LED indicator 0 |
| 104 | LED1-2 | Ipu/O | 1 | LED indicator 2 |
| 105 | LED1-1 | Ipu/O | 1 | LED indicator 1 |
| 106 | LED1-0 | Ipu/O | 1 | LED indicator 0 |
| 107 | MDC | Ipu | All | Switch or PHY[5] MII management data clock |
| 108 | MDIO | I/O | All | Switch or PHY[5] MII management data I/O.<br>Features internal pull down to define pin state when not driven. |
| 109 | SPIQ | Otri | All | (1) SPI serial data output in SPI slave mode; (2) Not used in I2C master mode. See *"pin# 113."* |
| 110 | SPIC/SCL | I/O | All | (1) Input clock up to 5MHz in SPI slave mode; (2) Output clock at 81KHz in I2C master mode. See *"pin# 113."* |
| 111 | SPID/SDA | I/O | All | (1) Serial data input in SPI slave mode; (2) Serial data input/output in I2C master mode See *"pin# 113."* |
| 112 | SPIS_N | Ipu | All | Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KS8995M is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer; (2) Not used in I2C master mode. |
| 113 | PS1 | Ipd | | Serial bus configuration pin<br>If EEPROM is not present, the KS8995M will start itself with chip default (00)... |
| | | | | **Pin Config.** / **Serial Bus Configuration** |
| | | | | PS[1:0]=00 / I2C Master Mode for EEPROM |
| | | | | PS[1:0]=01 / Reserved |
| | | | | PS[1:0]=10 / SPI Slave Mode for CPU Interface |
| | | | | PS[1:0]=11 / Factory Test Mode (BIST) |
| 114 | PS0 | Ipd | | Serial bus configuration pin. See *"pin# 113."* |
| 115 | RST_N | Ipu | | Reset the KS8995M. Active low. |
| 116 | GNDD | Gnd | | Digital ground |
| 117 | VDDC | P | | 1.8V digital core $V_{DD}$ |
| 118 | TESTEN | Ipd | | NC for normal operation. Factory test pin. |

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   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 119 | SCANEN | Ipd | | NC for normal operation. Factory test pin. |
| 120 | NC | NC | | No Connect |
| 121 | X1 | I | | 25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±100ppm. |
| 122 | X2 | O | | 25MHz crystal clock connection |
| 123 | VDDAP | P | | 1.8V analog $V_{DD}$ for PLL |
| 124 | GNDA | Gnd | | Analog ground |
| 125 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 126 | GNDA | Gnd | | Analog ground |
| 127 | GNDA | Gnd | | Analog ground |
| 128 | TEST2 | NC | | NC for normal operation. Factory test pin. |

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   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

## Pin Description (by Name)

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 39 | FXSD4 | I | 4 | Fiber signal detect/factory test pin. Pull-down for TX mode. |
| 38 | FXSD5 | I | 5 | Fiber signal detect/factory test pin. Pull-down for TX mode |
| 124 | GNDA | Gnd | | Analog ground |
| 42 | GNDA | Gnd | | Analog ground |
| 44 | GNDA | Gnd | | Analog ground |
| 2 | GNDA | Gnd | | Analog ground |
| 16 | GNDA | Gnd | | Analog ground |
| 30 | GNDA | Gnd | | Analog ground |
| 6 | GNDA | Gnd | | Analog ground |
| 12 | GNDA | Gnd | | Analog ground |
| 21 | GNDA | Gnd | | Analog ground |
| 27 | GNDA | Gnd | | Analog ground |
| 34 | GNDA | Gnd | | Analog ground |
| 40 | GNDA | Gnd | | Analog ground |
| 120 | NC | NC | | No connect |
| 127 | GNDA | Gnd | | Analog ground |
| 126 | GNDA | Gnd | | Analog ground |
| 49 | GNDD | Gnd | | Digital ground |
| 88 | GNDD | Gnd | | Digital ground |
| 116 | GNDD | Gnd | | Digital ground |
| 58 | GNDD | Gnd | | Digital ground |
| 76 | GNDD | Gnd | | Digital ground |
| 99 | GNDD | Gnd | | Digital ground |
| 17 | ISET | | | Set physical transmit output current. Pull-down with a 3.01kΩ 1% resistor. |
| 106 | LED1-0 | Ipu/O | 1 | LED indicator 0 |
| 105 | LED1-1 | Ipu/O | 1 | LED indicator 1 |
| 104 | LED1-2 | Ipu/O | 1 | LED indicator 2 |
| 103 | LED2-0 | Ipu/O | 2 | LED indicator 0 |
| 102 | LED2-1 | Ipu/O | 2 | LED indicator 1 |
| 101 | LED2-2 | Ipu/O | 2 | LED indicator 2 |
| 98 | LED3-0 | Ipu/O | 3 | LED indicator 0 |

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   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 97 | LED3-1 | Ipu/O | 3 | LED indicator 1 |
| 96 | LED3-2 | Ipu/O | 3 | LED indicator 2 |
| 95 | LED4-0 | Ipu/O | 4 | LED indicator 0 |
| 94 | LED4-1 | Ipu/O | 4 | LED indicator 1 |
| 93 | LED4-2 | Ipu/O | 4 | LED indicator 2 |
| 92 | LED5-0 | Ipu/O | 5 | LED indicator 0 |
| 91 | LED5-1 | Ipu/O | 5 | LED indicator 1. Strap option: PU (default): enable PHY MII I/F. PD: tristate all PHY MII output. See *"pin# 86 SCONF1."* |
| 90 | LED5-2 | Ipu/O | 5 | LED indicator 2. Strap option: Aging setup. See *"Aging"* section. (default) = Aging Enable; PD = Aging disable |
| 107 | MDC | Ipu | All | Switch or PHY[5] MII management data clock. |
| 108 | MDIO | I/O | All | Switch or PHY[5] MII management data I/O. |
| 1 | TEST1 | NC | | NC for normal operation. Factory test pin. |
| 45 | MUX1 | NC | | MUX1 and MUX2 should be left unconnected for normal operation. They are factory test pins. |
| 46 | MUX2 | NC | | |

| Mode | MUX1 | MUX2 |
|---|---|---|
| Normal Operation | NC | NC |
| Remote Analog Loopback Mode for Testing only | 0 | 1 |
| Reserved | 1 | 0 |
| Power Save Mode for Testing only | 1 | 1 |

| | | | | |
|---|---|---|---|---|
| 68 | PCOL | Ipd/O | 5 | PHY[5] MII collision detect. Strap option for port 4 only. See *"Register 18."* PD (default) = No force flow control. PU = Force flow control. |
| 67 | PCRS | Ipd/O | 5 | PHY[5] MII carrier sense. Strap option for port 4 only. See *"Register 28."* PD (default) = Force half-duplex if auto-negotiation is disabled or fails. PU = Force full-duplex if auto-negotiation is disabled or fails. |
| 60 | PMRXC | O | 5 | PHY[5] MII receive clock. PHY mode MII. |
| 65 | PMRXD0 | Ipd/O | 5 | PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement. |
| 64 | PMRXD1 | Ipd/O | 5 | PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets. |
| 63 | PMRXD2 | Ipd/O | 5 | PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure. |
| 62 | PMRXD3 | Ipd/O | 5 | PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control. |

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   Ipu = Input w/ internal pull-up
   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 61 | PMRXDV | Ipd/O | 5 | PHY[5] MII receive data valid. |
| 66 | PMRXER | Ipd/O | 5 | PHY[5] MII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes. |
| 57 | PMTXC | O | 5 | PHY[5] MII transmit clock. PHY mode MII |
| 55 | PMTXD0 | Ipd | 5 | PHY[5] MII transmit bit 0 |
| 54 | PMTXD1 | Ipd | 5 | PHY[5] MII transmit bit 1 |
| 53 | PMTXD2 | Ipd | 5 | PHY[5] MII transmit bit 2 |
| 52 | PMTXD3 | Ipd | 5 | PHY[5] MII transmit bit 3 |
| 51 | PMTXEN | Ipd | 5 | PHY[5] MII transmit enable |
| 56 | PMTXER | Ipd | 5 | PHY[5] MII transmit error |
| 114 | PS0 | Ipd | | Serial bus configuration pin. See *"pin# 113."* |
| 113 | PS1 | Ipd | | Serial bus configuration pin<br>If EEPROM is not present, the KS8995M will start itself with chip default (00)... |
| | | | | **Pin Config.** / **Serial Bus Configuration** |
| | | | | PS[1:0]=00 / I2C Master Mode for EEPROM |
| | | | | PS[1:0]=01 / Reserved |
| | | | | PS[1:0]=10 / SPI Slave Mode for CPU Interface |
| | | | | PS[1:0]=11 / Factory Test Mode (BIST) |
| 47 | PWRDN_N | Ipu | | Full-chip power down. Active low. |
| 48 | RESERVE | NC | | Reserved pin. No connect. |
| 115 | RST_N | Ipu | | Reset the KS8995M. Active low. |
| 5 | RXM1 | I | 1 | Physical receive signal - (differential) |
| 11 | RXM2 | I | 2 | Physical receive signal - (differential) |
| 20 | RXM3 | I | 3 | Physical receive signal - (differential) |
| 26 | RXM4 | I | 4 | Physical receive signal - (differential) |
| 33 | RXM5 | I | 5 | Physical receive signal - (differential) |
| 4 | RXP1 | I | 1 | Physical receive signal + (differential) |
| 10 | RXP2 | I | 2 | Physical receive signal + (differential) |
| 19 | RXP3 | I | 3 | Physical receive signal + (differential) |
| 25 | RXP4 | I | 4 | Physical receive signal + (differential) |
| 32 | RXP5 | I | 5 | Physical receive signal + (differential) |
| 119 | SCANEN | Ipd | | NC for normal operation. Factory test pin. |
| 84 | SCOL | Ipd/O | | Switch MII collision detect. |

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   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 87 | SCONF0 | Ipd | | Dual MII configuration pin |
| 86 | SCONF1 | Ipd | | Dual MII configuration pin |

| Pin# (91, 86, 87): | Switch MII | PHY [5] MII |
|---|---|---|
| 000 | Disable, Otri | Disable, Otri |
| 001 | PHY Mode MII | Disable, Otri |
| 010 | MAC Mode MII | Disable, Otri |
| 011 | PHY Mode SNI | Disable, Otri |
| 100 | Disable | Disable |
| 101 | PHY Mode MII | PHY Mode MII |
| 110 | MAC Mode MII | PHY Mode MII |
| 111 | PHY Mode SNI | PHY Mode MII |

| | | | | |
|---|---|---|---|---|
| 85 | SCRS | Ipd/O | | Switch MII carrier sense |
| 78 | SMRXC | I/O | | Switch MII receive clock. Input in MAC mode, output in PHY mode MII. |
| 83 | SMRXD0 | Ipd/O | | Switch MII receive bit 0; Strap option: LED Mode<br>PD (default) = Mode 0; PU = Mode 1. See *"Register 11."* |

| | Mode 0 | Mode 1 |
|---|---|---|
| LEDX_2 | Lnk/Act | 100Lnk/Act |
| LEDX_1 | Fulld/Col | 10Lnk/Act |
| LEDX_0 | Speed | Fulld |

| | | | | |
|---|---|---|---|---|
| 82 | SMRXD1 | Ipd/O | | Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode. |
| 81 | SMRXD2 | Ipd/O | | Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full-duplex mode; PU = Switch MII in half-duplex mode. |
| 80 | SMRXD3 | Ipd/O | | Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control. |
| 79 | SMRXDV | Ipd/O | | Switch MII receive data valid |
| 75 | SMTXC | I/O | | Switch MII transmit clock. Input in MAC mode, output in PHY mode MII. |
| 73 | SMTXD0 | Ipd | | Switch MII transmit bit 0 |
| 72 | SMTXD1 | Ipd | | Switch MII transmit bit 1 |
| 71 | SMTXD2 | Ipd | | Switch MII transmit bit 2 |
| 70 | SMTXD3 | Ipd | | Switch MII transmit bit 3 |
| 69 | SMTXEN | Ipd | | Switch MII transmit enable |
| 74 | SMTXER | Ipd | | Switch MII transmit error |

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   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 110 | SPIC/SCL | I/O | All | (1) Input clock up to 5MHz in SPI slave mode; (2) Output clock at 81KHz in I2C master mode. See *"pin# 113."* |
| 111 | SPID/SDA | I/O | All | (1) Serial data input in SPI slave mode; (2) Serial data input/output in I2C master mode. See *"pin# 113."* |
| 109 | SPIQ | Otri | All | (1) SPI serial data output in SPI slave mode; (2) Not used in I2C master mode. See *"pin# 113."* |
| 112 | SPIS_N | Ipu | All | Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KS8995M is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer; (2) Not used in I2C master mode. |
| 128 | TEST2 | NC | | No connect for normal operation. Factory test pin. |
| 118 | TESTEN | Ipd | | No Connect for normal operation. Factory test pin. |
| 8 | TXP1 | O | 1 | Physical transmit signal + (differential) |
| 14 | TXP2 | O | 2 | Physical transmit signal + (differential) |
| 23 | TXP3 | O | 3 | Physical transmit signal + (differential) |
| 29 | TXP4 | O | 4 | Physical transmit signal + (differential) |
| 36 | TXP5 | O | 5 | Physical transmit signal + (differential) |
| 7 | TXM1 | O | 1 | Physical transmit signal - (differential) |
| 13 | TXM2 | O | 2 | Physical transmit signal - (differential) |
| 22 | TXM3 | O | 3 | Physical transmit signal - (differential) |
| 28 | TXM4 | O | 4 | Physical transmit signal - (differential) |
| 35 | TXM5 | O | 5 | Physical transmit signal - (differential) |
| 123 | VDDAP | P | | 1.8V analog $V_{DD}$ for PLL |
| 41 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 43 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 3 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 15 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 31 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 125 | VDDAR | P | | 1.8V analog $V_{DD}$ |
| 18 | VDDAT | P | | 2.5V analog $V_{DD}$ |
| 9 | VDDAT | P | | 2.5V analog $V_{DD}$ |
| 24 | VDDAT | P | | 2.5V analog $V_{DD}$ |
| 37 | VDDAT | P | | 2.5V analog $V_{DD}$ |
| 50 | VDDC | P | | 1.8V digital core $V_{DD}$ |

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   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

| Pin Number | Pin Name | Type(1) | Port | Pin Function |
|---|---|---|---|---|
| 89 | VDDC | P | | 1.8V digital core $V_{DD}$ |
| 117 | VDDC | P | | 1.8V digital core $V_{DD}$ |
| 59 | VDDIO | P | | 3.3V digital $V_{DD}$ for digital I/O circuitry |
| 77 | VDDIO | P | | 3.3V digital $V_{DD}$ for digital I/O circuitry |
| 100 | VDDIO | P | | 3.3V digital $V_{DD}$ for digital I/O circuitry |
| 121 | X1 | I | | 25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±100ppm. |
| 122 | X2 | O | | 25MHz crystal clock connection. |

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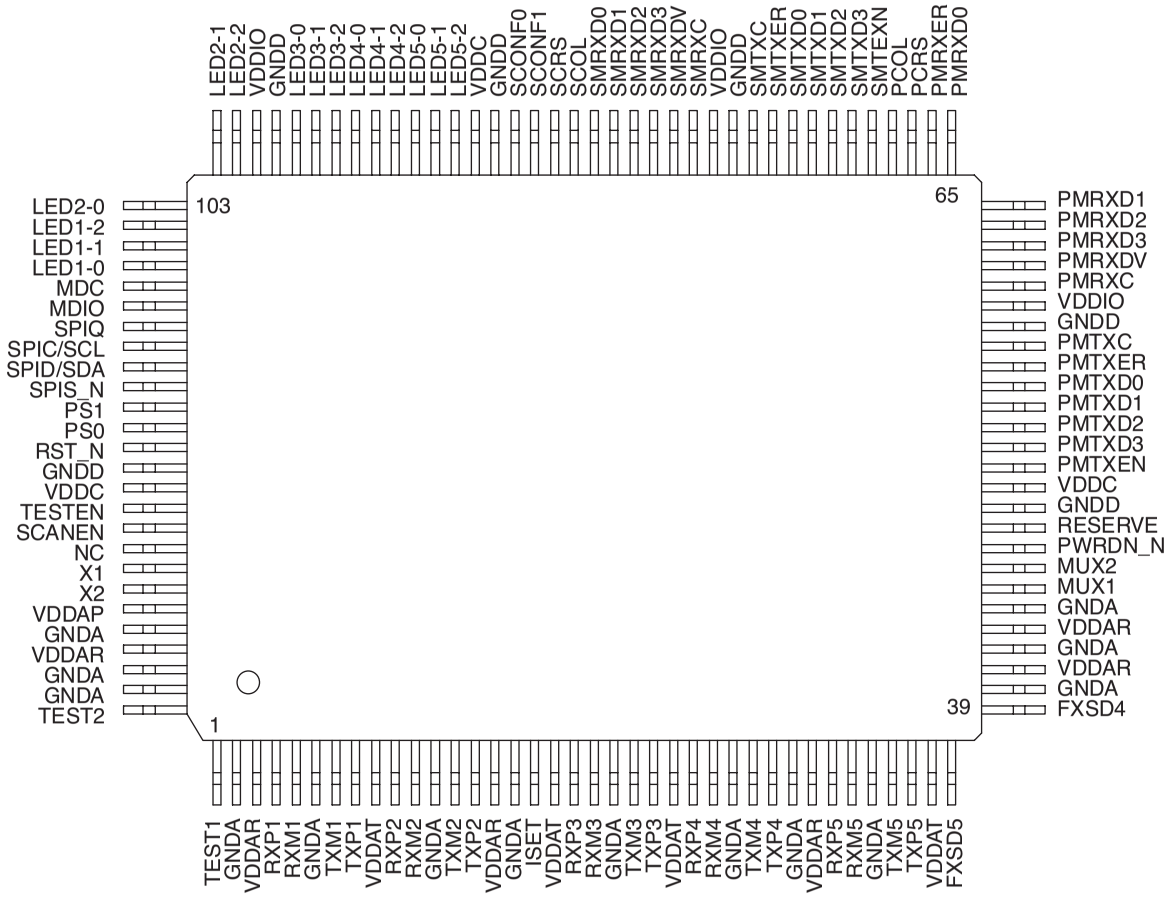
   Ipd = Input w/ internal pull-down
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise
   PU = Strap pin pull-up
   PD = Strap pin pull-down
   Otri = Output tristated
   NC = No Connect

## Pin Configuration




**128-Pin PQFP (PQ)**

# Introduction

The KS8995M contains five 10/100 physical layer transceivers and five MAC (Media Access Control) units with an integrated layer 2 managed switch. The device runs in three modes. The first mode is as a five-port integrated switch. The second is as a five-port switch with the fifth port decoupled from the physical port. In this mode access to the fifth MAC is provided through an MII (Media Independent Interface). This is useful for implementing an integrated broadband router. The third mode uses the dual MII feature to recover the use of the fifth PHY. This allows the additional broadband gateway configuration, where the fifth PHY may be accessed through the MII-P5 port.

The KS8995M has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the KS8995M via the SPI bus, or partial control via the MDC/MDIO interface. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KS8995M supports IEEE 802.3 10BaseT, 100BaseTX on all ports, and 100BaseFX on ports 4 and 5. The KS8995M can be used as two separate media converters.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

The major enhancements from the KS8995E to the KS8995M are support for host processor management, a dual MII interface, tag as well as port based VLAN, spanning tree protocol support, IGMP snooping support, port mirroring support and rate limiting functionality.

# Functional Overview: Physical Layer Transceiver

## 100BaseTX Transmit

The 100BaseTX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10BaseT output is also incorporated into the 100BaseTX transmitter.

## 100BaseTX Receive

The 100BaseTX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, it then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

## PLL Clock Synthesizer

The KS8995M generates 125MHz, 42MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator.

## Scrambler/De-scrambler (100BaseTX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

## 100BaseFX Operation

100BaseFX operation is very similar to 100BaseTX operation except that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode the auto-negotiation feature is bypassed since there is no standard that supports fiber auto-negotiation.

## 100BaseFX Signal Detection

The physical port runs in 100BaseFX mode if FXSDx >0.6V for ports 4 and 5 only. This signal is internally referenced to 1.25V. The fiber module interface should be set by a voltage divider such that FXSDx 'H' is above this 1.25V reference, indicating signal

detect, and FXSDx 'L' is below the 1.25V reference to indicate no signal. When FXSDx is below 0.6V then 100BaseFX mode is disabled. Since there is no auto-negotiation for 100BaseFX mode, ports 4 and 5 must be forced to either full or half-duplex. Note that strap in options exist to set duplex mode for port 4, but not for port 5.

## 100BaseFX Far End Fault

Far end fault occurs when the signal detection is logically false from the receive fiber module. When this occurs, the transmission side signals the other end of the link by sending 84 1s followed by a zero in the idle period between frames. The far end fault may be disabled through register settings.

## 10BaseT Transmit

The output 10BaseT driver is incorporated into the 100BaseT driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

## 10BaseT Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8995M decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

## Power Management

The KS8995M features a per port power down mode. To save power the user can power down ports that are not in use by setting port control registers or MII control registers. In addition, it also supports full chip power down mode. When activated, the entire chip will be shut down.

## MDI/MDI-X Auto Crossover

The KS8995M supports MDI/MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the Micrel device. This can be highly useful when end users are unaware of cable types and can also save on an additional uplink configuration connection. The auto crossover feature may be disabled through the port control registers.

## Auto-Negotiation

The KS8995M conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows UTP (Unshielded Twisted Pair) link partners to select the best common mode of operation. In auto-negotiation the link partners advertise capabilities across the link to each other. If auto-negotiation is not supported or the link partner to the KS8995M is forced to bypass auto-negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The flow for the link set up is depicted in Figure 4.

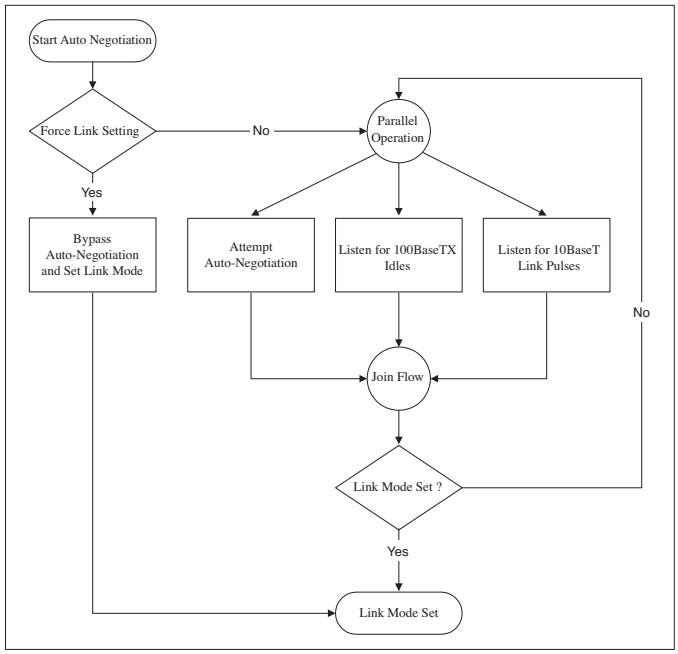



**Figure 4. Auto-Negotiation**

# Functional Overview: Switch Core

## Address Look-Up

The internal look-up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KS8995M is guaranteed to learn 1K addresses and distinguishes itself from hash-based look-up tables which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

## Learning

The internal look-up engine will update its table with a new entry if the following conditions are met:

- The received packet's SA (Source Address) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will insert the qualified SA into the table, along with the port number, time stamp. If the table is full, the last entry of the table will be deleted first to make room for the new entry.

## Migration

The internal look-up engine also monitors whether a station is moved. If it happens, it will update the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

## Aging

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 + 75 seconds. This feature can be enabled or disabled through Register 3 or by external pull-up or pull-down resistors on LED[5][2]. See *"Register 3"* section.

## Forwarding

The KS8995M will forward packets using an algorithm that is depicted in the following flowcharts. Figure 5 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with "port to forward 1" (PTF1). PTF1 is then further modified by the spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with "port to forward 2" (PTF2) as shown in Figure 6. This is where the packet will be sent.

## The KS8995M will not forward the following packets:

- Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
- 802.3x pause frames. The KS8995M will intercept these packets and perform the appropriate actions.
- "Local" packets. Based on DA (Destination Address) look-up. If the destination port from the look-up table matches the port where the packet was from, the packet is defined as "local."

## Switching Engine

The KS8995M features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KS8995M has a 64kB internal frame buffer. This resource is shared between all five ports. The buffer sharing mode can be programmed through Register 2. See *"Register 2."* In one mode, ports are allowed to use any free buffers in the buffer pool. In the second mode, each port is only allowed to use 1/5 of the total buffer pool. There are a total of 512 buffers available. Each buffer is sized at 128B.

## MAC (Media Access Controller) Operation

The KS8995M strictly abides by IEEE 802.3 standards to maximize compatibility.

### Inter-Packet Gap (IPG)

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

### Backoff Algorithm

The KS8995M implements the IEEE Std 802.3 binary exponential back-off algorithm, and optional "aggressive mode" back off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration in register 3. See *"Register 3."*

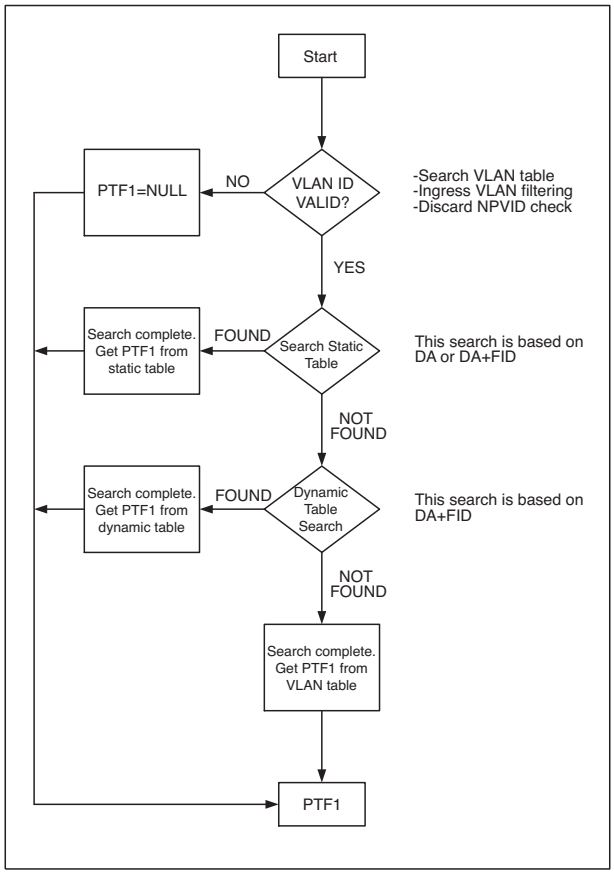



**Figure 5. DA Look-Up Flowchart–Stage 1**

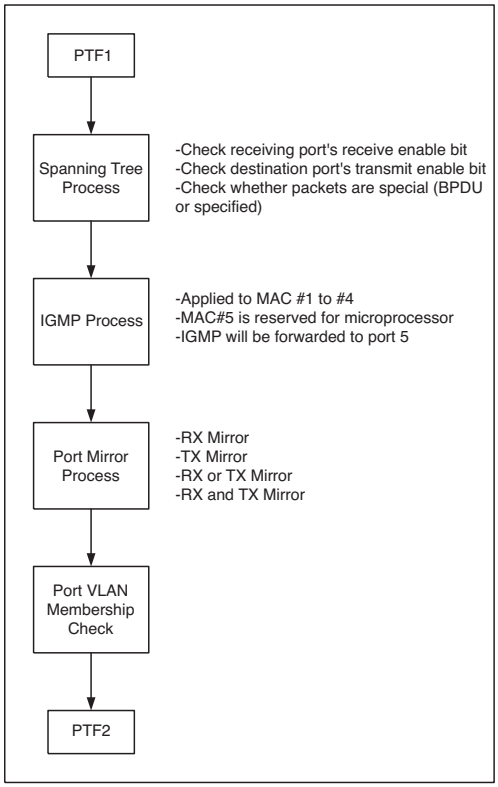



**Figure 6. DA Resolution Flowchart–Stage 2**