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# KS8995XA

## Integrated 5-Port 10/100 QoS Switch

Rev 2.6

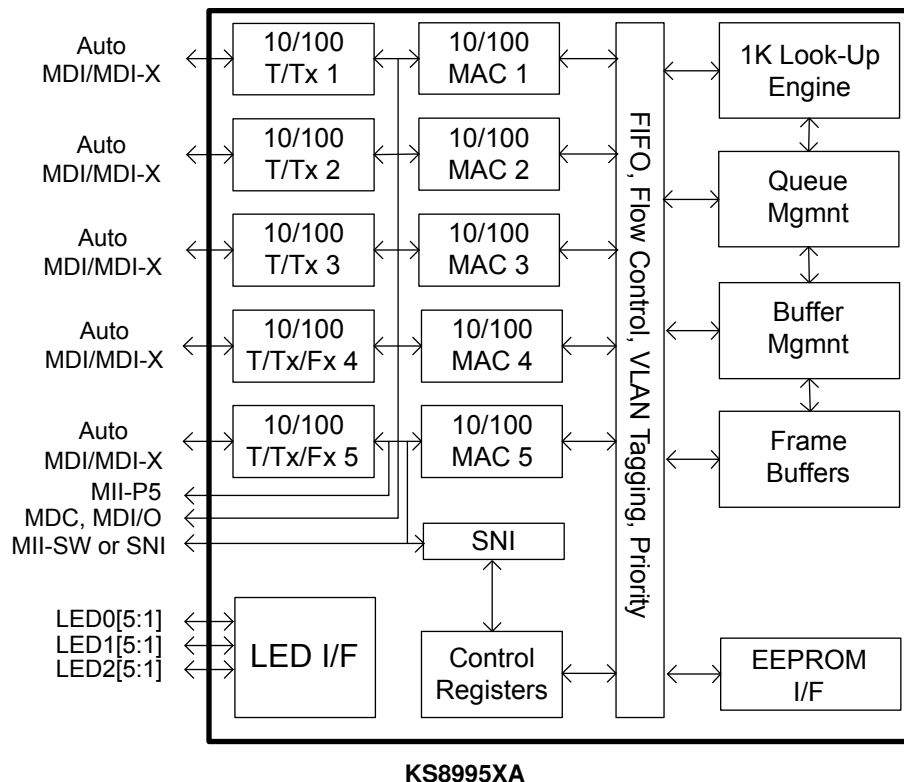
### General Description

The KS8995XA is a highly integrated Layer-2 quality of service (QoS) switch with optimized bill of materials (BOM) cost for low port count, cost-sensitive 10/100Mbps switch systems. It also provides an extensive feature set including three different QoS priority schemes, a dual MII interface for BOM cost reduction, rate limiting to offload CPU tasks, software and hardware power-down, a MDC/MDIO control interface and port mirroring/monitoring to effectively address both current and emerging Fast Ethernet applications.

The KS8995XA contains five 10/100 transceivers with patented mixed-signal low-power technology, five media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

All PHY units support 10BASE-T and 100BASE-TX. In addition, two of the PHY units support 100BaseFX (Ports 4 and 5).

### Functional Diagram



## Features

- Integrated switch with five MACs and five Fast Ethernet transceivers fully compliant to IEEE 802.3u standard
- Shared memory based switch fabric with fully nonblocking configuration
- 10BASE-T, 100BASE-TX and 100BASE-FX modes (FX in Ports 4 and 5)
- Dual MII configuration: MII-Switch (MAC or PHY mode MII) and MII-P5 (PHY mode MII)
- VLAN ID tag/untag options, per-port basis
- Enable/disable option for huge frame size up to 1916 bytes per frame
- Broadcast storm protection with percent control – global and per-port basis
- Optimization for fiber-to-copper media conversion
- Full-chip hardware power-down support (register configuration not saved)
- Per-port-based software power-save on PHY (idle link detection, register configuration preserved)
- QoS/CoS packets prioritization supports: per port, 802.1p and DiffServ-based
- 802.1p/q tag insertion or removal on a per-port basis (egress)
- Port-based VLAN support
- MDC and MDI/O interface support to access the MII PHY control registers (not all control registers)
- MII local loopback support
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table)
- 1.4Gbps high performance memory bandwidth
- Wire-speed reception and transmission
- Integrated look-up engine with dedicated 1K unicast MAC addresses
- Automatic address learning, address aging and address migration
- Full-duplex IEEE 802.3x and half-duplex back pressure flow control
- Comprehensive LED support
- 7-wire SNI support for legacy MAC interface
- Automatic MDI/MDI-X crossover for plug-and-play
- Disable automatic MDI/MDI-X option
- Low power
  - Core: 1.8V
  - Digital I/O: 3.3V
  - Analog I/O: 2.5 or 3.3V
- 0.18 $\mu$ m CMOS technology
- Commercial temperature range: 0°C to +70°C
- Available in 128-pin PQFP package

## Applications

- Broadband gateway/firewall/VPN
- Integrated DSL or cable modem multi-port router
- Wireless LAN access point plus gateway
- Home networking expansion
- Standalone 10/100 switch
- Hotel/campus/MxU gateway
- Enterprise VoIP gateway/phone
- FTTx customer premise equipment
- Media converter

## Ordering Information

Part Number		Temperature Range	Package
Standard	Pb-Free		
KS8995XA	KSZ8995XA	0°C to +70°C	128-Pin PQFP

## Revision History

Revision	Date	Summary of Changes
2.0	10/15/03	Created.
2.1	4/1/04	Editorial changes on TTL input and output electrical characteristics.
2.2	1/19/05	Insert recommended reset circuit.
2.3	4/13/05	Switched pins names for pins 7 & 8 on page 16. Changed VDDIO to 3.3V. Changed Jitter to 16 ns Max.
2.4	7/14/06	Update pin description for PCRS, PCOL, etc. Update the description of the register and MIIM register for the loop-back, etc. And update the MII timing diagram.
2.5	6/01/07	Add package thermal information in the operating rating and the transformer power consumption information in the electrical characteristics note.
2.6	9/15/08	Add description for the revision ID and LED mode, etc.

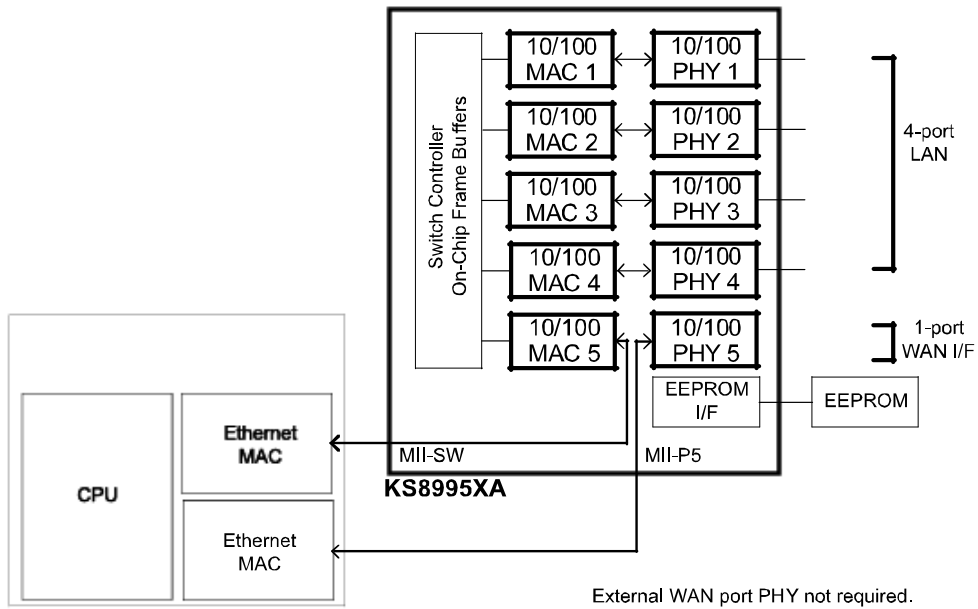
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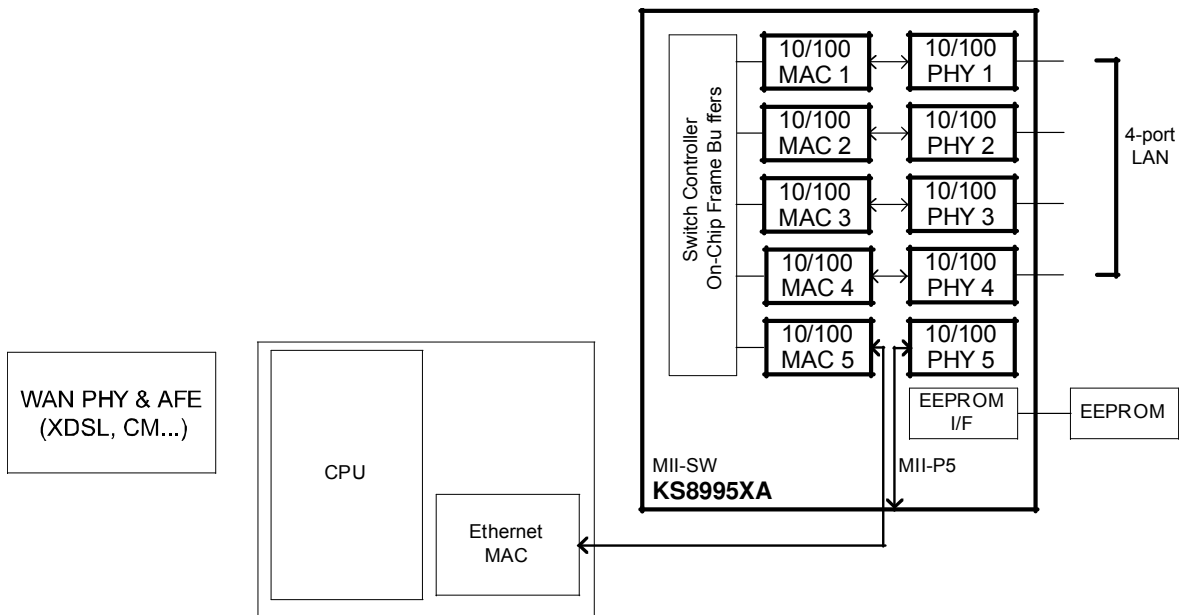


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# System Level Applications



**Figure 1. Broadband Gateway**



**Figure 2. Integrated Broadband Router**

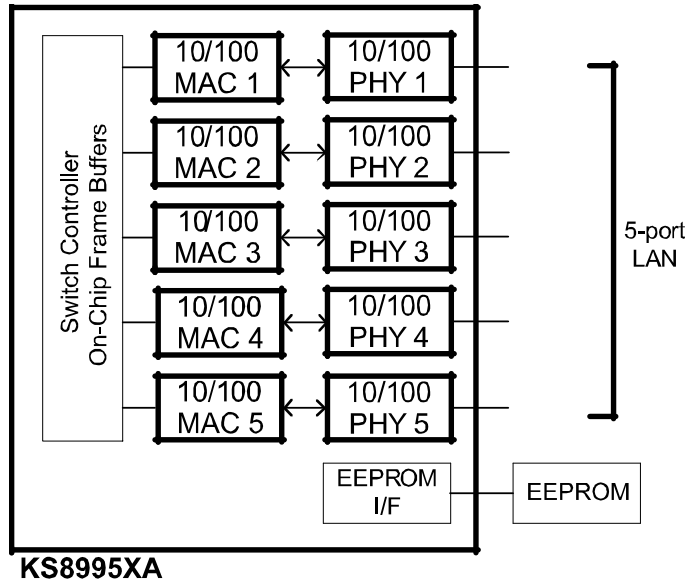


Figure 3. Standalone Switch





## Pin Description (by Number)

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function <sup>(2)</sup>
1	MDI-XDIS	lpd	1-5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GND A	Gnd		Analog ground.
3	VDDAR	P		1.8V analog V <sub>DD</sub> .
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal – (differential).
6	GND A	Gnd		Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal – (differential).
9	VDDAT	P		2.5V or 3.3V analog V <sub>DD</sub> .
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal – (differential).
12	GND A	Gnd		Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
15	VDDAR	P		1.8V analog V <sub>DD</sub> .
16	GND A	Gnd		Analog ground.
17	IS E T			Set physical transmit output current. Pull-down with a 3.01kΩ1% resistor.
18	VDDAT	P		2.5V or 3.3V analog V <sub>DD</sub> .
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal - (differential).
21	GND A	Gnd		Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
24	VDDAT	P		2.5V or 3.3V analog V <sub>DD</sub> .
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal - (differential).
27	GND A	Gnd		Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
30	GND A	Gnd		Analog ground.

### Notes:

- P = Power supply.
  - I = Input.
  - O = Output.
  - I/O = Bidirectional.
  - Gnd = Ground.
  - Ipu = Input w/internal pull-up.
  - Ipd = Input w/internal pull-down.
  - Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
  - Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
- PU = Strap pin pull-up.
  - PD = Strap pull-down.
  - Otri = Output tristated.

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function <sup>(2)</sup>
31	VDDAR	P		1.8V analog V <sub>DD</sub> .
32	RXP5	I	5	Physical receive signal + (differential).
33	RXM5	I	5	Physical receive signal – (differential).
34	GND A	Gnd		Analog ground.
35	TXP5	O	5	Physical transmit signal + (differential).
36	TXM5	O	5	Physical transmit signal – (differential).
37	VDDAT	P		2.5V or 3.3V analog V <sub>DD</sub> .
38	FXSD5	I	5	Fiber signal detect/factory test pin.
39	FXSD4	I	4	Fiber signal detect/factory test pin.
40	GND A	Gnd		Analog ground.
41	VDDAR	P		1.8V analog V <sub>DD</sub> .
42	GND A	Gnd		Analog ground.
43	VDDAR	P		1.8V analog V <sub>DD</sub> .
44	GND A	Gnd		Analog ground.
45	NC / MUX1	I		No connect. Factory test pin.
46	NC / MUX2	I		No connect. Factory test pin.
47	PWRDN_N	Ipu		Full-chip power down. Active low.
48	RESERVE/NC			Reserved pin. No connect.
49	GNDD	Gnd		Digital ground.
50	VDDC	P		1.8V digital core V <sub>DD</sub> .
51	PMTXEN	Ipd	5	PHY[5] MII transmit enable.
52	PMTXD3	Ipd	5	PHY[5] MII transmit bit 3.
53	PMTXD2	Ipd	5	PHY[5] MII transmit bit 2.
54	PMTXD1	Ipd	5	PHY[5] MII transmit bit 1.
55	PMTXD0	Ipd	5	PHY[5] MII transmit bit 0.
56	PMTXER	Ipd	5	PHY[5] MII transmit error.
57	PMTXC	O	5	PHY[5] MII transmit clock. PHY mode MII.
58	GNDD	Gnd		Digital ground.
59	VDDIO	P		3.3V digital V <sub>DD</sub> for digital I/O circuitry.
60	PMRXC	O	5	PHY[5] MII receive clock. PHY mode MII.

**Notes:**

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  - Gnd = Ground.
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  - Ipd = Input w/internal pull-down.
  - Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
  - Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
- PU = Strap pin pull-up.
  - PD = Strap pull-down.
  - Otri = Output tristated.

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function <sup>(2)</sup>
61	PMRXDV	lpd/O	5	PHY[5] MII receive data valid.
62	PMRXD3	lpd/O	5	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
63	PMRXD2	lpd/O	5	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
64	PMRXD1	lpd/O	5	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
65	PMRXD0	lpd/O	5	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
66	PMRXER	lpd/O	5	PHY[5] MII receive error. Strap option: PD (default) = packet size 1518/1522 bytes; PU = 1536 bytes.
67	PCRS	lpd/O	5	PHY[5] MII carrier sense/strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
68	PCOL	lpd/O	5	PHY[5] MII collision detect/ strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.
69	SMTXEN	lpd		Switch MII transmit enable.
70	SMTXD3	lpd		Switch MII transmit bit 3.
71	SMTXD2	lpd		Switch MII transmit bit 2.
72	SMTXD1	lpd		Switch MII transmit bit 1.
73	SMTXD0	lpd		Switch MII transmit bit 0.
74	SMTXER	lpd		Switch MII transmit error.
75	SMTXC	I/O		Switch MII transmit clock. PHY or MAC mode MII.
76	GNDD	Gnd		Digital ground.
77	VDDIO	P		3.3V digital V <sub>DD</sub> for digital I/O circuitry.
78	SMRXC	I/O		Switch MII receive clock. PHY or MAC mode MII.
79	SMRXDV	lpd/O		Switch MII receive data valid.
80	SMRXD3	lpd/O		Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control.
81	SMRXD2	lpd/O		Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full-duplex mode; PU = Switch MII in half-duplex mode.
82	SMRXD1	lpd/O		Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode.
83	SMRXD0	lpd/O		Switch MII receive bit 0; Strap option: see "Register 11[1]."
84	SCOL	lpd/O		Switch MII collision detect.
85	SCRS	lpd/O		Switch mode carrier sense.

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 Gnd = Ground.  
 lpu = Input w/internal pull-up.  
 lpd = Input w/internal pull-down.  
 lpd/O = Input w/internal pull-down during reset, output pin otherwise.  
 lpu/O = Input w/internal pull-up during reset, output pin otherwise.
- PU = Strap pin pull-up.  
 PD = Strap pull-down.  
 Otri = Output tristated.

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function <sup>(2)</sup>		
86	SCONF1	Ipd		Dual MII configuration pin.		
				<b>Pin# (91, 86, 87):</b>	<b>Switch MII</b>	<b>PHY [5] MII</b>
				000	Disable, Otri	Disable, Otri
				001	PHY Mode MII	Disable, Otri
				010	MAC Mode MII	Disable, Otri
				011	PHY Mode SNI	Disable, Otri
				100	Disable	Disable
				101	PHY Mode MII	PHY Mode MII
				110	MAC Mode MII	PHY Mode MII
111	PHY Mode SNI	PHY Mode MII				
87	SCONF0	Ipd		Dual MII configuration pin.		
88	GNDD	Gnd		Digital ground.		
89	VDDC	P		1.8V digital core V <sub>DD</sub> .		
90	LED5-2	Ipu/O	5	LED indicator 2. Aging setup. See "Aging" section.		
91	LED5-1	Ipu/O	5	LED indicator 1. Strap option: PU (default): enable PHY[5] MII I/F. PD: tristate all PHY[5] MII output. See "Pin# 86 SCONF1."		
92	LED5-0	Ipu/O	5	LED indicator 0.		
93	LED4-2	Ipu/O	4	LED indicator 2.		
94	LED4-1	Ipu/O	4	LED indicator 1.		
95	LED4-0	Ipu/O	4	LED indicator 0.		
96	LED3-2	Ipu/O	3	LED indicator 2.		
97	LED3-1	Ipu/O	3	LED indicator 1.		
98	LED3-0	Ipu/O	3	LED indicator 0.		
99	GNDD	Gnd		Digital ground.		
100	VDDIO	P		3.3V digital V <sub>DD</sub> for digital I/O.		
101	LED2-2	Ipu/O	2	LED indicator 2.		
102	LED2-1	Ipu/O	2	LED indicator 1.		
103	LED2-0	Ipu/O	2	LED indicator 0.		
104	LED1-2	Ipu/O	1	LED indicator 2.		
105	LED1-1	Ipu/O	1	LED indicator 1.		
106	LED1-0	Ipu/O	1	LED indicator 0.		

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  - Gnd = Ground.
  - Ipu = Input w/internal pull-up.
  - Ipd = Input w/internal pull-down.
  - Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
  - Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
  - NC = No connect.
- PU = Strap pin pull-up.
  - PD = Strap pull-down.
  - Otri = Output tristated.

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function
106	LED1-0	Ipu/O	1	LED indicator 0. <sup>(2)</sup>
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock. <sup>(2)</sup>
108	MDIO	Ipu/O	All	Switch or PHY[5] MII management data I/O.
109	Reserved		All	No connect.
110	SCL	I/O	All	Output clock at 81kHz in I <sup>2</sup> C master mode.
111	SDA	I/O	All	Serial data input/output in I <sup>2</sup> C master mode.
112	Reserved		All	No connect
113	PS1	Ipd		No connect or pull-down.
114	PS0	Ipd		No connect or pull-down.
115	RST_N	Ipu		Reset the KS8995XA. Active low.
116	GNDD	Gnd		Digital ground.
117	VDDC	P		1.8V digital core V <sub>DD</sub> .
118	TESTEN	Ipd		Factory test pin.
119	SCANEN	Ipd		Factory test pin.
120	NC	NC		No connection.
121	X1	I		25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be ±100ppm.
122	X2	O		25MHz crystal clock connection.
123	VDDAP	P		1.8V analog V <sub>DD</sub> for PLL.
124	GNDA	Gnd		Analog ground.
125	VDDAR	P		1.8V analog V <sub>DD</sub> .
126	GNDA	Gnd		Analog ground.
127	GNDA	Gnd		Analog ground.
128	TEST2			Factory test pin.

**Notes:**

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  - Ipu = Input w/internal pull-up.
  - Ipd = Input w/internal pull-down.
  - Ipd/O = Input w/internal pull-down during reset, output pin otherwise.
  - Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
  - NC = No connect.
- PU = Strap pin pull-up.
  - PD = Strap pull-down.
  - Otri = Output tristated.

## Pin Description (by Name)

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function
39	FXSD4	I	4	Fiber signal detect/factory test pin.
38	FXSD5	I	5	Fiber signal detect/factory test pin.
2	GND A	Gnd		Analog ground.
6	GND A	Gnd		Analog ground.
12	GND A	Gnd		Analog ground.
16	GND A	Gnd		Analog ground.
21	GND A	Gnd		Analog ground.
27	GND A	Gnd		Analog ground.
30	GND A	Gnd		Analog ground.
34	GND A	Gnd		Analog ground.
40	GND A	Gnd		Analog ground.
42	GND A	Gnd		Analog ground.
44	GND A	Gnd		Analog ground.
120	NC	NC		No connection.
124	GND A	Gnd		Analog ground.
126	GND A	Gnd		Analog ground.
127	GND A	Gnd		Analog ground.
49	GND D	Gnd		Digital ground.
58	GND D	Gnd		Digital ground.
76	GND D	Gnd		Digital ground.
88	GND D	Gnd		Digital ground.
99	GND D	Gnd		Digital ground.
116	GND D	Gnd		Digital ground.
17	IS ET			Set physical transmit output current. Pull down with a 3.01kΩ1% resistor.
106	LED1-0	Ipu/O	1	LED indicator 0.
105	LED1-1	Ipu/O	1	LED indicator 1.
104	LED1-2	Ipu/O	1	LED indicator 2.
103	LED2-0	Ipu/O	2	LED indicator 0.
102	LED2-1	Ipu/O	2	LED indicator 1.
101	LED2-2	Ipu/O	2	LED indicator 2.
98	LED3-0	Ipu/O	3	LED indicator 0.
97	LED3-1	Ipu/O	3	LED indicator 1.

### Notes:

- P = Power supply.  
 I = Input.  
 O = Output.  
 I/O = Bidirectional.  
 Gnd = Ground.  
 Ipu = Input w/internal pull-up.  
 Ipd = Input w/internal pull-down.  
 Ipd/O = Input w/internal pull-down during reset, output pin otherwise.  
 Ipu/O = Input w/internal pull-up during reset, output pin otherwise.  
 NC = No connect.



Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function <sup>(2)</sup>
96	LED3-2	Ipu/O	3	LED indicator 2.
95	LED4-0	Ipu/O	4	LED indicator 0.
94	LED4-1	Ipu/O	4	LED indicator 1.
93	LED4-2	Ipu/O	4	LED indicator 2.
92	LED5-0	Ipu/O	5	LED indicator 0.
91	LED5-1	Ipu/O	5	LED indicator 1. Strap option: PU (default): enable PHY MII I/F Pd: tristate all PHY MII output. See "Pin# 86 SCONF1."
90	LED5-2	Ipu/O	5	LED indicator 2. Aging setup. See "Aging" section.
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock.
108	MDIO	Ipu/O	All	Switch or PHY[5] MII management data I/O.
45	NC / MUX1		I	No connect. Factory test pin.
46	NC / MUX2		I	No connect. Factory test pin.
68	PCOL	Ipd/O	5	PHY[5] MII collision detect/ strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.
67	PCRS	Ipd/O	5	PHY[5] MII carrier sense/strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
60	PMRXC	O	5	PHY[5] MII receive clock. PHY mode MII.
65	PMRXD0	Ipd/O	5	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
64	PMRXD1	Ipd/O	5	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
63	PMRXD2	Ipd/O	5	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
62	PMRXD3	Ipd/O	5	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
61	PMRXDV	Ipd/O	5	PHY[5] MII receive data valid.
66	PMRXER	Ipd/O	5	PHY[5] MII receive error. Strap option: PD (default) = packet size 1518/1522 bytes; PU = 1536 bytes.
57	PMTXC	O	5	PHY[5] MII transmit clock. PHY mode MII.
55	PMTXD0	Ipd	5	PHY[5] MII transmit bit 0.
54	PMTXD1	Ipd	5	PHY[5] MII transmit bit 1.
53	PMTXD2	Ipd	5	PHY[5] MII transmit bit 2.
52	PMTXD3	Ipd	5	PHY[5] MII transmit bit 3.
51	PMTXEN	Ipd	5	PHY[5] MII transmit enable.
56	PMTXER	Ipd	5	PHY[5] MII transmit error.
114	PS0	Ipd		No connect or pull down.
113	PS1	Ipd		No connect or pull down.

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I/O = Bidirectional.  
Gnd = Ground.  
Ipu = Input w/internal pull-up.  
Ipd = Input w/internal pull-down.  
Ipd/O = Input w/internal pull-down during reset, output pin otherwise.  
Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
- PU = Strap pin pull-up.  
PD = Strap pull-down.

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function <sup>(2)</sup>		
47	PWRDN_N	lpu		Full-chip power down. Active low.		
48	RESERVE/NC			Reserved pin. No connect.		
109	Reserved		All	No connect.		
112	Reserved		All	No connect.		
115	RST_N	lpu		Reset the KS8995X. Active low.		
5	RXM1	I	1	Physical receive signal - (differential).		
11	RXM2	I	2	Physical receive signal - (differential).		
20	RXM3	I	3	Physical receive signal - (differential).		
26	RXM4	I	4	Physical receive signal - (differential).		
33	RXM5	I	5	Physical receive signal - (differential).		
4	RXP1	I	1	Physical receive signal + (differential).		
10	RXP2	I	2	Physical receive signal + (differential).		
19	RXP3	I	3	Physical receive signal + (differential).		
25	RXP4	I	4	Physical receive signal + (differential).		
32	RXP5	I	5	Physical receive signal + (differential).		
119	SCANEN	lpd		Factory test pin.		
110	SCL	I/O	All	Output clock at 81kHz in I <sup>2</sup> C master mode. See "Pin# 113."		
84	SCOL	lpd/O		Switch MII collision detect.		
87	SCONF0	lpd		Dual MII configuration pin.		
86	SCONF1	lpd		Dual MII configuration pin.		
				<b>Pin# (91, 86, 87):</b>	<b>Switch MII</b>	<b>PHY [5] MII</b>
				000	Disable, Otri	Disable, Otri
				001	PHY Mode MII	Disable, Otri
				010	MAC Mode MII	Disable, Otri
				011	PHY Mode SNI	Disable, Otri
				100	Disable	Disable
				101	PHY Mode MII	PHY Mode MII
				110	MAC Mode MII	PHY Mode MII
111	PHY Mode SNI	PHY Mode MII				
85	SCRS	lpd/O		Switch MII carrier sense.		
111	SDA	I/O	All	Serial data input/output in I <sup>2</sup> C master mode. See "Pin# 113."		
78	SMRXC	I/O		Switch MII receive clock. PHY or MAC mode MII.		
83	SMRXD0	lpd/O		Switch MII receive bit 0; strap option: see "Register 11[1]."		

**Notes:**

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 Gnd = Ground.  
 lpu = Input w/internal pull-up.  
 lpd = Input w/internal pull-down.  
 lpd/O = Input w/internal pull-down during reset, output pin otherwise.  
 lpu/O = Input w/internal pull-up during reset, output pin otherwise.

- Otri = Output tristated.

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function <sup>(2)</sup>
82	SMRXD1	lpd/O		Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode.
81	SMRXD2	lpd/O		Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full-duplex mode; PU = Switch MII in half-duplex mode.
80	SMRXD3	lpd/O		Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control.
79	SMRXDV	lpd/O		Switch MII receive data valid.
75	SMTXC	I/O		Switch MII transmit clock. PHY or MAC mode MII.
73	SMTXD0	lpd		Switch MII transmit bit 0.
72	SMTXD1	lpd		Switch MII transmit bit 1.
71	SMTXD2	lpd		Switch MII transmit bit 2.
70	SMTXD3	lpd		Switch MII transmit bit 3.
69	SMTXEN	lpd		Switch MII transmit enable.
74	SMTXER	lpd		Switch MII transmit error.
1	MDIXDIS	lpd	1-5	Disable auto MDI/MDI-X.
128	TEST2			Factory test pin.
118	TESTEN	lpd		Factory test pin.
7	TXP1	O	1	Physical transmit signal + (differential).
13	TXP2	O	2	Physical transmit signal + (differential).
22	TXP3	O	3	Physical transmit signal + (differential).
28	TXP4	O	4	Physical transmit signal + (differential).
35	TXP5	O	5	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal – (differential).
14	TXM2	O	2	Physical transmit signal – (differential).
23	TXM3	O	3	Physical transmit signal – (differential).
29	TXM4	O	4	Physical transmit signal – (differential).
36	TXM5	O	5	Physical transmit signal – (differential).
123	VDDAP	P		1.8V analog V <sub>DD</sub> for PLL.
3	VDDAR	P		1.8V analog V <sub>DD</sub> .
15	VDDAR	P		1.8V analog V <sub>DD</sub> .
31	VDDAR	P		1.8V analog V <sub>DD</sub> .
41	VDDAR	P		1.8V analog V <sub>DD</sub> .
43	VDDAR	P		1.8V analog V <sub>DD</sub> .
125	VDDAR	P		1.8V analog V <sub>DD</sub> .

**Notes:**

- P = Power supply.  
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 O = Output.  
 I/O = Bidirectional.  
 Gnd = Ground.  
 Ipu = Input w/internal pull-up.  
 Ipd = Input w/internal pull-down.  
 Ipd/O = Input w/internal pull-down during reset, output pin otherwise.  
 Ipu/O = Input w/internal pull-up during reset, output pin otherwise.
- PU = Strap pin pull-up.  
 PD = Strap pull-down.

Pin Number	Pin Name	Type <sup>(1)</sup>	Port	Pin Function
9	VDDAT	P		2.5V or 3.3V analog V <sub>DD</sub> .
18	VDDAT	P		2.5V or 3.3V analog V <sub>DD</sub> .
24	VDDAT	P		2.5V or 3.3V analog V <sub>DD</sub> .
37	VDDAT	P		2.5V or 3.3V analog V <sub>DD</sub> .
50	VDDC	P		1.8V digital core V <sub>DD</sub> .
89	VDDC	P		1.8V digital core V <sub>DD</sub> .
117	VDDC	P		1.8V digital core V <sub>DD</sub> .
59	VDDIO	P		3.3V digital V <sub>DD</sub> for digital I/O circuitry.
77	VDDIO	P		3.3V digital V <sub>DD</sub> for digital I/O circuitry.
100	VDDIO	P		3.3V digital V <sub>DD</sub> for digital I/O circuitry.
121	X1	I		25MHz crystal clock connection/or 3.3V tolerant oscillator input. Oscillator should be $\pm 100$ ppm.
122	X2	O		25MHz crystal clock connection.

**Notes:**

1. P = Power supply.  
I = Input.  
O = Output.

## Introduction

The KS8995XA contains five 10/100 physical layer transceivers and five media access control (MAC) units with an integrated Layer 2 switch. The device runs in three modes. The first mode is as a five-port integrated switch. The second is as a five-port switch with the fifth port decoupled from the physical port. In this mode access to the fifth MAC is provided through a media independent interface (MII) . This is useful for implementing an integrated broadband router. The third mode uses the dual MII feature to recover the use of the fifth PHY. This allows the additional broadband gateway configuration, where the fifth PHY may be accessed through the MII-P5 port.

The KS8995XA is optimized for an unmanaged design in which the configuration is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KS8995XA supports IEEE 802.3 10BASE-T, 100BASE-TX on all ports, and 100BASE-FX on ports 4 and 5. The KS8995XA can be used as two separate media converters.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

The major enhancements from the KS8995E to the KS8995XA are support for programmable rate limiting, a dual MII interface, MDC/MDIO control interface for IEEE 802.3-defined register configuration (not all the registers), per-port broadcast storm protection, local loopback and lower power consumption.

The KS8995XA is pin-compatible to the managed switch, the KS8995M.

## Functional Overview: Physical Layer Transceiver

### 100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01k $\Omega$  resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

### 100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then it tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

### PLL Clock Synthesizer

The KS8995XA generates 125MHz, 42MHz, 25MHz, and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal.

### Scrambler/De-Scrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline

wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit nonrepetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

### **100BASE-FX Operation**

100BASE-FX operation is very similar to 100BASE-TX operation except that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode the auto-negotiation feature is bypassed since there is no standard that supports fiber auto-negotiation.

### **100BASE-FX Signal Detection**

The physical port runs in 100BASE-FX mode if FXSDx >0.6V for ports 4 and 5 only. This signal is internally referenced to 1.25V. The fiber module interface should be set by a voltage divider such that FXSDx 'H' is above this 1.25V reference, indicating signal detect, and FXSDx 'L' is below the 1.25V reference to indicate no signal. When FXSDx is below 0.6V then 100BASE-FX mode is disabled.

### **100BASE-FX Far End Fault**

Far end fault occurs when the signal detection is logically false from the receive fiber module. When this occurs, the transmission side signals the other end of the link by sending 84 1's followed by a zero in the idle period between frames. The far end fault may be disabled through register settings.

### **10BASE-T Transmit**

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

### **10BASE-T Receive**

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulsewidths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8995XA decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

### **Power Management**

The KS8995XA features a per port power down mode. To save power the user can power down ports that are not in use by setting port control registers or MII control registers. In addition, it also supports full chip power down mode. When activated, the entire chip will be shutdown.

### **MDI/MDI-X Auto Crossover**

The KS8995XA supports MDI/MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the Micrel device. This can be highly useful when end users are unaware of cable types and can also save on an additional uplink configuration connection. The auto crossover feature may be disabled through the port control registers.

### **Auto-Negotiation**

The KS8995XA conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation the link partners advertise capabilities across the link to each other. If auto-negotiation is not supported or the link partner to the KS8995XA is forced to bypass auto-negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The flow for the link set up is depicted in Figure 4.

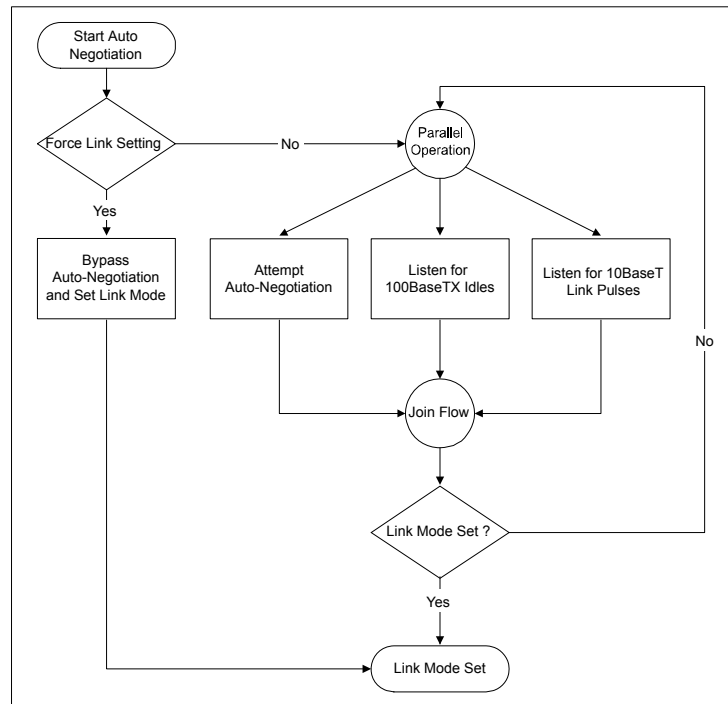


Figure 4. Auto-Negotiation

## Functional Overview: Switch Core

### Address Look-Up

The internal look-up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KS8995XA is guaranteed to learn 1K addresses and distinguishes itself from hash-based look-up tables which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

### Learning

The internal look-up engine will update its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will insert the qualified SA into the table, along with the port number, time stamp. If the table is full, the last entry of the table will be deleted first to make room for the new entry.

### Migration

The internal look-up engine also monitors whether a station is moved. If it happens, it will update the table accordingly.

Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

### Aging

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 ±75 seconds. This feature can be enabled or disabled through register 3 or by external pull-up or pull-down resistors on LED[5][2]. See "Register 3" section.



## Switching Engine

The KS8995XA features a high performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KS8995XA has a 64kB internal frame buffer. This resource is shared between all five ports. The buffer sharing mode can be programmed through Register 2. See "Register 2." In one mode, ports are allowed to use any free buffers in the buffer pool.

In the second mode, each port is only allowed to use 1/5 of the total buffer pool. There are a total of 512 buffers available. Each buffer is sized at 128B.

## Media Access Controller (MAC) Operation

The KS8995XA strictly abides by IEEE 802.3 standards to maximize compatibility.

### *Inter-Packet Gap (IPG)*

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

### *Backoff Algorithm*

The KS8995XA implements the IEEE Std. 802.3 binary exponential back-off algorithm, and optional "aggressive mode" back off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration in Register 3. See "Register 3."

### *Late Collision*

If a transmit packet experiences collisions after 512-bit times of the transmission, the packet will be dropped.

### *Illegal Frames*

The KS8995XA discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Register 4. For special applications, the KS8995XA can also be programmed to accept frames up to 1916 bytes in Register 4. Since the KS8995XA supports VLAN tags, the maximum sizing is adjusted when these tags are present.

### *Flow Control*

The KS8995XA supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KS8995XA receives a pause control frame, the KS8995XA will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KS8995XA will be transmitted.

On the transmit side, the KS8995XA has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KS8995XA will flow control a port, which just received a packet, if the destination port resource is being used up. The KS8995XA will issue a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KS8995XA will send out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being activated and deactivated too many times.

The KS8995XA will flow control all ports if the receive queue becomes full.

### *Half-Duplex Back Pressure*

A half-duplex back pressure option (note: not in 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full-duplex mode. If back pressure is required, the KS8995XA will send preambles to defer the other stations' transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier-sense-type back pressure will be interrupted and those packets will be transmitted instead. If there are no

more packets to send, carrier-sense-type back pressure will be active again until switch resources are free. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive backoff (register 3, bit 0)
- No excessive collision drop (register 4, bit 3)
- Back pressure (register 4, bit 5)

These bits are not set as the default because this is not the IEEE standard.

#### *Broadcast Storm Protection*

The KS8995XA has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets will be forwarded to all ports except the source port, and thus use too many switch resources (bandwidth and available space in transmit queues). The KS8995XA has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 50ms interval for 100BT and a 500ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Register 6 and Register 7. The default setting for registers 6 and 7 is 0x4A, which is 74 decimal. This is equal to a rate of 1%, calculated as follows:

$$148,800 \text{ frames/sec} \times 50\text{ms/interval} \times 1\% = 74 \text{ frames/interval (approx.)} = 0x4$$

## MII Interface Operation

The media independent interface (MII) is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. The KS8995XA provides two such interfaces. The MII-P5 interface is used to connect to the fifth PHY, whereas the MII-SW interface is used to connect to the fifth MAC. Each of these MII interfaces contains two distinct groups of signals, one for transmission and the other for receiving. The table below describes the signals used in the MII-P5 interface.

The MII-P5 interface operates in PHY mode only, while the MII-SW interface operates in either MAC mode or PHY mode. These interfaces are nibble-wide data interfaces and therefore run at 1/4 the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors. For half-duplex operation, there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the MII-SW interface for PHY mode operation and the signal MTXER is not provided on the MII-SW interface for MAC mode operation. Normally MRXER would indicate a receive error coming from the physical layer device. MTXER would indicate a transmit error from the MAC device. These signals are not appropriate for this configuration. For PHY mode operation, if the device interfacing with the KS8995XA has an MRXER pin, it should be tied low. For MAC mode operation, if the device interfacing with the KS8995XA has an MTXER pin, it should be tied low.

MII Signal	Description	KS8995XA Signal
MTXEN	Transmit enable	PMTXEN
MTXER	Transmit error	PMTXER
MTXD3	Transmit data bit 3	PMTXD[3]
MTXD2	Transmit data bit 2	PMTXD[2]
MTXD1	Transmit data bit 1	PMTXD[1]
MTXD0	Transmit data bit 0	PMTXD[0]
MTXC	Transmit clock	PMTXC
MCOL	Collision detection	PCOL
MCRS	Carrier sense	PCRS
MRXDV	Receive data valid	PMRXDV
MRXER	Receive error	PMRXER
MRXD3	Receive data bit 3	PMRXD[3]
MRXD2	Receive data bit 2	PMRXD[2]
MRXD1	Receive data bit 1	PMRXD[1]
MRXD0	Receive data bit 0	PMRXD[0]
MRXC	Receive clock	PMRXC
MDC	Management data clock	MDC
MDIO	Management data I/O	MDIO

**Table 1. MII – P5 Signals (PHY Mode)**

PHY Mode Connection		Description	MAC Mode Connection	
External MAC	KS8995XA Signal		External PHY	KS8995XA Signal
MTXEN	SMTXEN	Transmit enable	MTXEN	SMRXDV
MTXER	SMTXER	Transmit error	MTXER	Not used
MTXD3	SMTXD[3]	Transmit data bit 3	MTXD3	SMRXD[3]
MTXD2	SMTXD[2]	Transmit data bit 2	MTXD2	SMRXD[2]
MTXD1	SMTXD[1]	Transmit data bit 1	MTXD1	SMRXD[1]
MTXD0	SMTXD[0]	Transmit data bit 0	MTXD0	SMRXD[0]
MTXC	SMTXC	Transmit clock	MTXC	SMRXC
MCOL	SCOL	Collision detection	MCOL	SCOL
MCRS	SCRS	Carrier sense	MCRS	SCRS
MRXDV	SMRXDV	Receive data valid	MRXDV	SMTXEN
MRXER	Not used	Receive error	MRXER	SMTXER
MRXD3	SMRXD[3]	Receive data bit 3	MRXD3	SMTXD[3]
MRXD2	SMRXD[2]	Receive data bit 2	MRXD2	SMTXD[2]
MRXD1	SMRXD[1]	Receive data bit 1	MRXD1	SMTXD[1]
MRXD0	SMRXD[0]	Receive data bit 0	MRXD0	SMTXD[0]
MRXC	SMRXC	Receive clock	MRXC	SMTXC

**Table 2. MII – SW Signals**