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# KSZ9021RL/RN

## Gigabit Ethernet Transceiver with RGMII Support

**Revision 1.2**

## General Description

The KSZ9021RL is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ9021RL provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000Mbps speed.

The KSZ9021RL reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

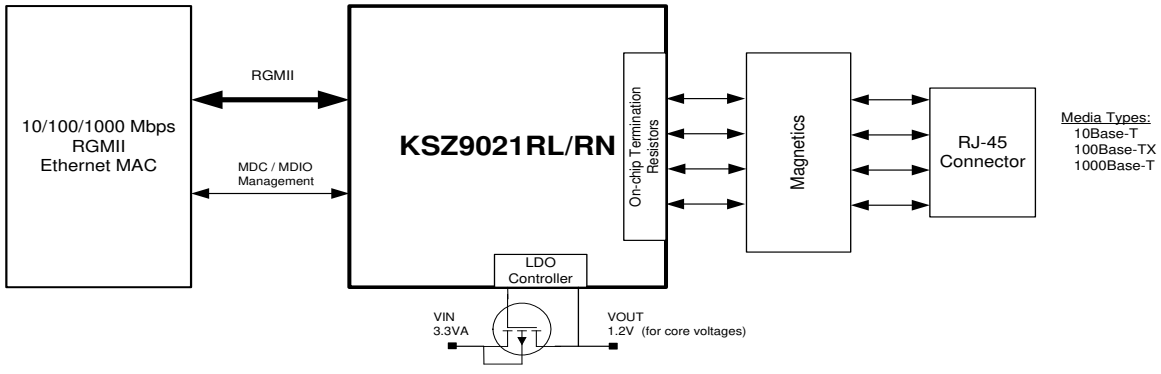
The KSZ9021RL provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9021 I/Os and board. Micrel LinkMD® TDR-based cable diagnostics permit identification of faulty copper cabling. Remote and local loopback functions provide verification of analog and digital data paths.

The KSZ9021RL is available in a 64-pin, lead-free E-LQFP package, and is offered as the KSZ9021RN in the smaller 48-pin QFN package (See Ordering Information).

## Features

- Single-chip 10/100/1000Mbps IEEE 802.3 compliant Ethernet Transceiver
- RGMII interface compliant to RGMII Version 1.3
- RGMII I/Os with 3.3V/2.5V tolerant and programmable timings to adjust and correct delays on both Tx and Rx paths
- Auto-negotiation to automatically select the highest link up speed (10/100/100Mbps) and duplex (half/full)
- On-chip termination resistors for the differential pairs
- On-chip LDO controller to support single 3.3V supply operation – requires only external FET to generate 1.2V for the core
- Jumbo frame support up to 16KB
- 125MHz Reference Clock Output
- Programmable LED outputs for link, activity and speed
- Baseline Wander Correction
- LinkMD® TDR-based cable diagnostics for identification of faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and board.
- Loopback modes for diagnostics

## Functional Diagram




LinkMD is a registered trademark of Micrel, Inc.

## More Features

- Automatic MDI/MDI-X crossover for detection and correction of pair swap at all speeds of operation
- Automatic detection and correction of pair swap, pair skew and pair polarity
- MDC/MDIO Management Interface for PHY register configuration
- Interrupt pin option
- Power down and power saving modes
- Operating Voltages
  - Core: 1.2V (external FET or regulator)
  - I/O: 3.3V or 2.5V
  - Transceiver: 3.3V
- Available packages
  - 64-pin E-LQFP (10mm x 10mm): KSZ9021RL
  - 48-pin QFN (7mm x 7mm): KSZ9021RN

## Applications

- Laser/Network printer
- Network attached storage (NAS)
- Network server
- Gigabit LAN on motherboard (GLOM)
- Broadband gateway
- Gigabit SOHO/SMB router
- IPTV
- IP Set-top box
- Game console
- Triple-play (data, voice, video) media center
- Media converter

## Ordering Information

| Part Number | Temp. Range | Package | Lead Finish | Description |
|---|---|---|---|---|
| KSZ9021RL | 0°C to +70°C | 64-Pin E-LQFP | Pb-Free | RGMII, Commercial Temperature, 64-E-LQFP |
| KSZ9021RLI (1) | –40°C to +85°C | 64-Pin E-LQFP | Pb-Free | RGMII, Industrial Temperature, 64-E-LQFP |
| KSZ9021RN | 0°C to +70°C | 48-Pin QFN | Pb-Free | RGMII, Commercial Temperature, 48-QFN |
| KSZ9021RNI (1) | –40°C to +85°C | 48-Pin QFN | Pb-Free | RGMII, Industrial Temperature, 48-QFN |

**Note:**

1. Contact factory for availability.

## Revision History

| Revision | Date | Summary of Changes |
|---|---|---|
| 1.0 | 1/16/09 | Data sheet created. |
| 1.1 | 10/13/09 | Updated current consumption in Electrical Characteristics section.<br>Corrected data sheet omission of register 1 bit 8 for 1000Base-T Extended Status information.<br>Added the following register bits to provide further power saving during software power down: Tri-state all digital I/Os (reg. 258.7), LDO disable (reg. 263.15), Low frequency oscillator mode (reg. 263.8).<br>Added KSZ9021RN device and updated entire data sheet accordingly.<br>Added 48-Pin QFN package information. |
| 1.2 | 2/13/14 | Added RGMII Pad Skew Registers section.<br>Corrected pad skew steps in Registers 260 (104h) and 261 (105h). Datasheet values are incorrect. There is no change to the silicon.<br>Added Register 262 (106h) for RGMII TX Data Pad Skew.<br>Updated boilerplate. |

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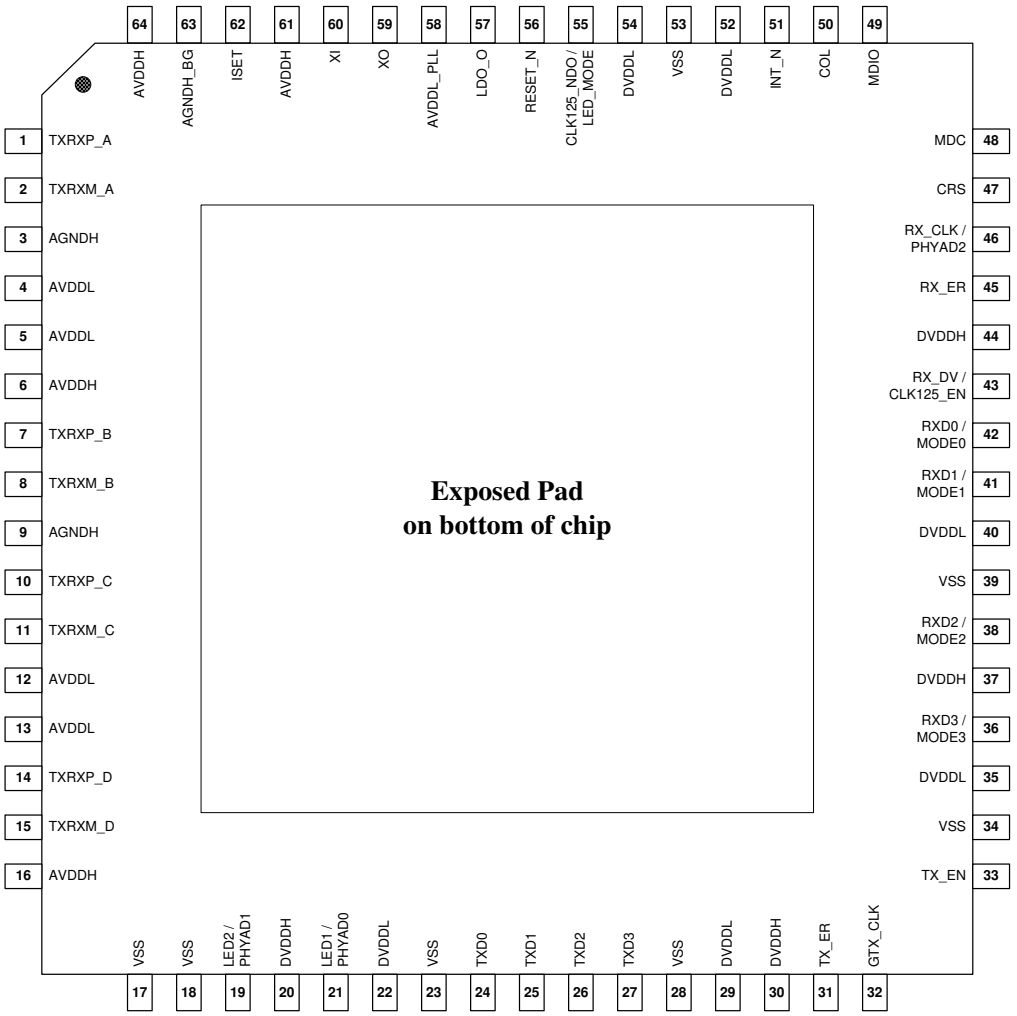
## Pin Configuration – KSZ9021RL




**64-Pin E-LQFP**
**(Top View)**

## Pin Description – KSZ9021RL

| Pin Number | Pin Name | Type[1] | Pin Function |
|---|---|---|---|
| 1 | TXRXP_A | I/O | Media Dependent Interface[0], positive signal of differential pair<br>1000Base-T Mode:<br>TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively. |
| 2 | TXRXM_A | I/O | Media Dependent Interface[0], negative signal of differential pair<br>1000Base-T Mode:<br>TXRXM_A corresponds to BI_DA- for MDI configuration and BI_DB- for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXM_A is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively. |
| 3 | AGNDH | Gnd | Analog ground |
| 4 | AVDDL | P | 1.2V analog $V_{DD}$ |
| 5 | AVDDL | P | 1.2V analog $V_{DD}$ |
| 6 | AVDDH | P | 3.3V analog $V_{DD}$ |
| 7 | TXRXP_B | I/O | Media Dependent Interface[1], positive signal of differential pair<br>1000Base-T Mode:<br>TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively. |
| 8 | TXRXM_B | I/O | Media Dependent Interface[1], negative signal of differential pair<br>1000Base-T Mode:<br>TXRXM_B corresponds to BI_DB- for MDI configuration and BI_DA- for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXM_B is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively. |
| 9 | AGNDH | Gnd | Analog ground |
| 10 | TXRXP_C | I/O | Media Dependent Interface[2], positive signal of differential pair<br>1000Base-T Mode:<br>TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXP_C is not used. |
| 11 | TXRXM_C | I/O | Media Dependent Interface[2], negative signal of differential pair<br>1000Base-T Mode:<br>TXRXM_C corresponds to BI_DC- for MDI configuration and BI_DD- for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXM_C is not used. |
| 12 | AVDDL | P | 1.2V analog $V_{DD}$ |

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>13</td><td>AVDDL</td><td>P</td><td>1.2V analog $V_{DD}$</td></tr>
<tr><td>14</td><td>TXRXP_D</td><td>I/O</td><td>Media Dependent Interface[3], positive signal of differential pair<br>1000Base-T Mode:<br>TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXP_D is not used.</td></tr>
<tr><td>15</td><td>TXRXM_D</td><td>I/O</td><td>Media Dependent Interface[3], negative signal of differential pair<br>1000Base-T Mode:<br>TXRXM_D corresponds to BI_DD- for MDI configuration and BI_DC- for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXM_D is not used.</td></tr>
<tr><td>16</td><td>AVDDH</td><td>P</td><td>3.3V analog $V_{DD}$</td></tr>
<tr><td>17</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>18</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>19</td><td>LED2 /<br>PHYAD1</td><td>I/O</td><td>LED Output: Programmable LED2 Output /<br>Config Mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up/reset. See “Strapping Options” section for details.<br>The LED2 pin is programmed by the LED_MODE strapping option (pin 55), and is defined as follows.<br><br>Single LED Mode
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>Link off</td><td>H</td><td>OFF</td></tr>
<tr><td>Link on (any speed)</td><td>L</td><td>ON</td></tr>
</table>
Tri-color Dual LED Mode
<table>
<tr><th rowspan="2">Link / Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For Tri-color Dual LED Mode, LED2 works in conjunction with LED1 (pin 21) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>20</td><td>DVDDH</td><td>P</td><td>3.3V/2.5V digital $V_{DD}$</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>21</td><td>LED1 /<br>PHYAD0</td><td>I/O</td><td>LED Output: Programmable LED1 Output /<br>Config Mode: The pull-up/pull-down value is latched as PHYAD[0] during power-up/reset. See “Strapping Options” section for details.<br>The LED1 pin is programmed by the LED_MODE strapping option (pin 55), and is defined as follows.<br><br>Single LED Mode
<table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity (RX, TX)</td><td>Toggle</td><td>Blinking</td></tr>
</table>
Tri-color Dual LED Mode
<table>
<tr><th rowspan="2">Link / Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For Tri-color Dual LED Mode, LED1 works in conjunction with LED2 (pin 19) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>22</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>23</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>RGMII Mode: RGMII TD0 (Transmit Data 0) Input</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>RGMII Mode: RGMII TD1 (Transmit Data 1) Input</td></tr>
<tr><td>26</td><td>TXD2</td><td>I</td><td>RGMII Mode: RGMII TD2 (Transmit Data 2) Input</td></tr>
<tr><td>27</td><td>TXD3</td><td>I</td><td>RGMII Mode: RGMII TD3 (Transmit Data 3) Input</td></tr>
<tr><td>28</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>29</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>30</td><td>DVDDH</td><td>P</td><td>3.3V/2.5V digital $V_{DD}$</td></tr>
<tr><td>31</td><td>TX_ER</td><td>I</td><td>RGMII Mode: This pin is not used and should be left as a no connect.</td></tr>
<tr><td>32</td><td>GTX_CLK</td><td>I</td><td>RGMII Mode: RGMII TXC (Transmit Reference Clock) Input</td></tr>
<tr><td>33</td><td>TX_EN</td><td>I</td><td>RGMII Mode: RGMII TX_CTL (Transmit Control) Input</td></tr>
<tr><td>34</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>35</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
</table>

| Pin Number | Pin Name | Type[1] | Pin Function |
|---|---|---|---|
| 36 | RXD3 / MODE3 | I/O | RGMII Mode: RGMII RD3 (Receive Data 3) Output /<br>Config Mode: The pull-up/pull-down value is latched as MODE3 during power-up/reset. See “Strapping Options” section for details. |
| 37 | DVDDH | P | 3.3V/2.5V digital $V_{DD}$ |
| 38 | RXD2 / MODE2 | I/O | RGMII Mode: RGMII RD2 (Receive Data 2) Output /<br>Config Mode: The pull-up/pull-down value is latched as MODE2 during power-up/reset. See “Strapping Options” section for details. |
| 39 | VSS | Gnd | Digital ground |
| 40 | DVDDL | P | 1.2V digital $V_{DD}$ |
| 41 | RXD1 / MODE1 | I/O | RGMII Mode: RGMII RD1 (Receive Data 1) Output /<br>Config Mode: The pull-up/pull-down value is latched as MODE1 during power-up/reset. See “Strapping Options” section for details. |
| 42 | RXD0 / MODE0 | I/O | RGMII Mode: RGMII RD0 (Receive Data 0) Output /<br>Config Mode: The pull-up/pull-down value is latched as MODE0 during power-up/reset. See “Strapping Options” section for details. |
| 43 | RX_DV / CLK125_EN | I/O | RGMII Mode: RGMII RX_CTL (Receive Control) Output /<br>Config Mode: Latched as CLK125_NDO Output Enable during power-up/reset. See “Strapping Options” section for details. |
| 44 | DVDDH | P | 3.3V/2.5V digital $V_{DD}$ |
| 45 | RX_ER | O | RGMII Mode: This pin is not used and should be left as a no connect. |
| 46 | RX_CLK / PHYAD2 | I/O | RGMII Mode: RGMII RXC (Receive Reference Clock) Output /<br>Config Mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up/reset. See “Strapping Options” section for details. |
| 47 | CRS | O | RGMII Mode: This pin is not used and should be left as a no connect. |
| 48 | MDC | Ipu | Management Data Clock Input<br>This pin is the input reference clock for MDIO (pin 49). |
| 49 | MDIO | Ipu/O | Management Data Input/Output<br>This pin is synchronous to MDC (pin 48) and requires an external pull-up resistor to 3.3V/2.5V digital $V_{DD}$ in a range from 1.0kΩ to 4.7kΩ. |
| 50 | COL | O | RGMII Mode: This pin is not used and should be left as a no connect. |
| 51 | INT_N | O | Interrupt Output<br>This pin provides a programmable interrupt output and requires an external pull-up resistor to 3.3V/2.5V digital $V_{DD}$ in a range from 1.0kΩ to 4.7kΩ when active low.<br>Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 14 sets the interrupt output to active low (default) or active high. |
| 52 | DVDDL | P | 1.2V digital $V_{DD}$ |
| 53 | VSS | Gnd | Digital ground |
| 54 | DVDDL | P | 1.2V digital $V_{DD}$ |
| 55 | CLK125_NDO / LED_MODE | I/O | 125MHz Clock Output<br>This pin provides a 125MHz reference clock output option for use by the MAC. /<br>Config Mode: The pull-up/pull-down value is latched as LED_MODE during power-up/reset. See “Strapping Options” section for details. |

| Pin Number | Pin Name | Type(1) | Pin Function |
|---|---|---|---|
| 56 | RESET_N | Ipu | Chip Reset (active low)<br>Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See “Strapping Options” section for more details. |
| 57 | LDO_O | O | On-chip 1.2V LDO Controller Output<br>This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip’s core voltages. If 1.2V is provided by the system and this pin is not used, it can be left floating. |
| 58 | AVDDL_PLL | P | 1.2V analog $V_{DD}$ for PLL |
| 59 | XO | O | 25MHz Crystal feedback<br>This pin is a no connect if oscillator or external clock source is used. |
| 60 | XI | I | Crystal / Oscillator / External Clock Input<br>25MHz ±50ppm tolerance |
| 61 | AVDDH | P | 3.3V analog $V_{DD}$ |
| 62 | ISET | I/O | Set transmit output level<br>Connect a 4.99KΩ 1% resistor to ground on this pin. |
| 63 | AGNDH_BG | Gnd | Analog ground |
| 64 | AVDDH | P | 3.3V analog $V_{DD}$ |
| E-PAD | E-PAD | Gnd | Exposed Pad on bottom of chip<br>Connect E-PAD to ground. |

**Note:**

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up.
   Ipu/O = Input with internal pull-up / Output.

## Strapping Options – KSZ9021RL

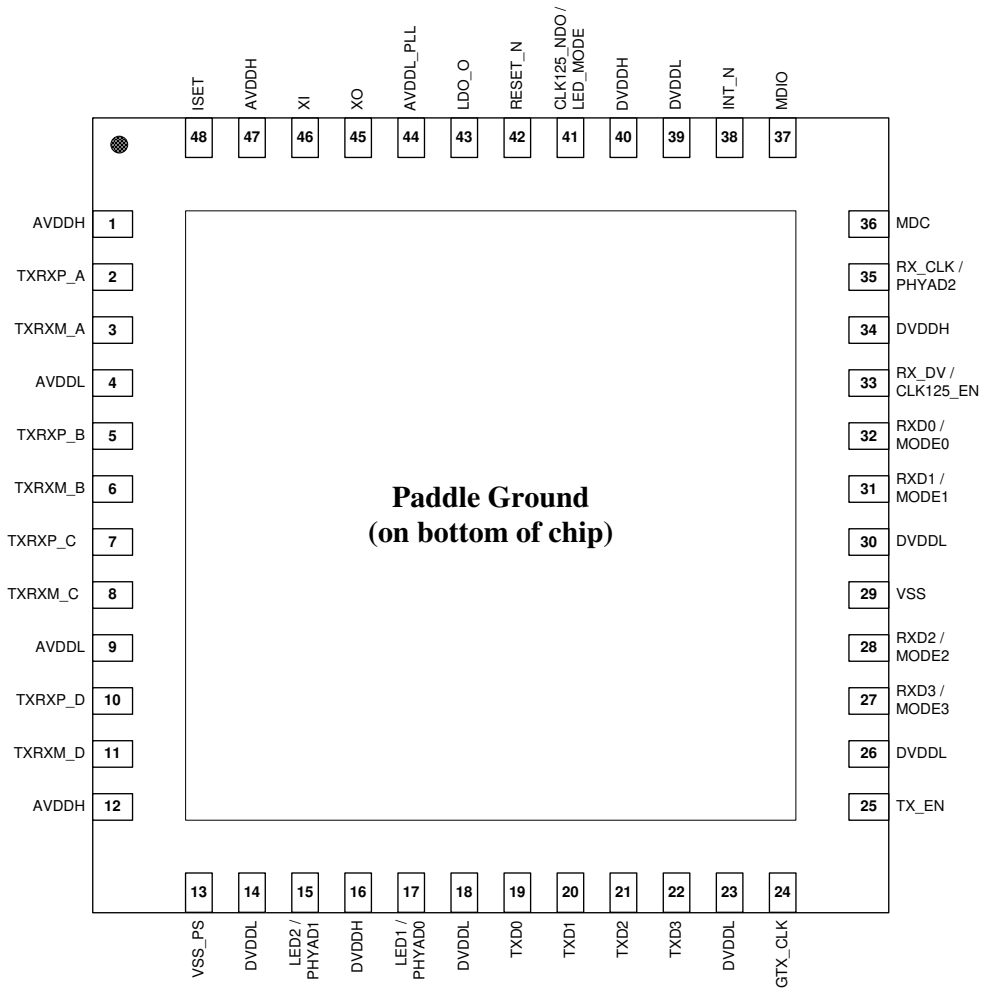
<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>46<br>19<br>21</td><td>PHYAD2<br>PHYAD1<br>PHYAD0</td><td>I/O<br>I/O<br>I/O</td><td>The PHY Address, PHYAD[2:0], is latched at power-up/reset and is configurable to any value from 1 to 7. Each PHY address bit is configured as follows:<br>Pull-up = 1<br>Pull-down = 0<br>PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>36<br>38<br>41<br>42</td><td>MODE3<br>MODE2<br>MODE1<br>MODE0</td><td>I/O<br>I/O<br>I/O<br>I/O</td><td>The MODE[3:0] strap-in pins are latched at power-up/reset and are defined as follows:
<table>
<tr><th>MODE[3:0]</th><th>Mode</th></tr>
<tr><td>0000</td><td>Reserved – not used</td></tr>
<tr><td>0001</td><td>Reserved – not used</td></tr>
<tr><td>0010</td><td>Reserved – not used</td></tr>
<tr><td>0011</td><td>Reserved – not used</td></tr>
<tr><td>0100</td><td>NAND Tree Mode</td></tr>
<tr><td>0101</td><td>Reserved – not used</td></tr>
<tr><td>0110</td><td>Reserved – not used</td></tr>
<tr><td>0111</td><td>Chip Power Down Mode</td></tr>
<tr><td>1000</td><td>Reserved – not used</td></tr>
<tr><td>1001</td><td>Reserved – not used</td></tr>
<tr><td>1010</td><td>Reserved – not used</td></tr>
<tr><td>1011</td><td>Reserved – not used</td></tr>
<tr><td>1100</td><td>RGMII Mode – advertise 1000Base-T full-duplex only</td></tr>
<tr><td>1101</td><td>RGMII Mode – advertise 1000Base-T full and half-duplex only</td></tr>
<tr><td>1110</td><td>RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex),except 1000Base-T half-duplex</td></tr>
<tr><td>1111</td><td>RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex)</td></tr>
</table></td></tr>
<tr><td>43</td><td>CLK125_EN</td><td>I/O</td><td>CLK125_EN is latched at power-up/reset and is defined as follows:<br>Pull-up = Enable 125MHz Clock Output<br>Pull-down = Disable 125MHz Clock Output<br>Pin 55 (CLK125_NDO) provides the 125MHz reference clock output option for use by the MAC.</td></tr>
<tr><td>55</td><td>LED_MODE</td><td>I/O</td><td>LED_MODE is latched at power-up/reset and is defined as follows:<br>Pull-up = Single LED Mode<br>Pull-down = Tri-color Dual LED Mode</td></tr>
</table>

**Note:**

1. I/O = Bi-directional.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the RGMII signals to be latched to the incorrect configuration. In this case, it is recommended to add external pull-ups/pull-downs on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

## Pin Configuration – KSZ9021RN




**48-Pin QFN**
**(Top View)**

## Pin Description – KSZ9021RN

| Pin Number | Pin Name | Type[1] | Pin Function |
|---|---|---|---|
| 1 | AVDDH | P | 3.3V analog $V_{DD}$ |
| 2 | TXRXP_A | I/O | Media Dependent Interface[0], positive signal of differential pair<br>1000Base-T Mode:<br>TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively. |
| 3 | TXRXM_A | I/O | Media Dependent Interface[0], negative signal of differential pair<br>1000Base-T Mode:<br>TXRXM_A corresponds to BI_DA- for MDI configuration and BI_DB- for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXM_A is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively. |
| 4 | AVDDL | P | 1.2V analog $V_{DD}$ |
| 5 | TXRXP_B | I/O | Media Dependent Interface[1], positive signal of differential pair<br>1000Base-T Mode:<br>TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively. |
| 6 | TXRXM_B | I/O | Media Dependent Interface[1], negative signal of differential pair<br>1000Base-T Mode:<br>TXRXM_B corresponds to BI_DB- for MDI configuration and BI_DA- for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXM_B is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively. |
| 7 | TXRXP_C | I/O | Media Dependent Interface[2], positive signal of differential pair<br>1000Base-T Mode:<br>TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXP_C is not used. |
| 8 | TXRXM_C | I/O | Media Dependent Interface[2], negative signal of differential pair<br>1000Base-T Mode:<br>TXRXM_C corresponds to BI_DC- for MDI configuration and BI_DD- for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXM_C is not used. |
| 9 | AVDDL | P | 1.2V analog $V_{DD}$ |

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>10</td><td>TXRXP_D</td><td>I/O</td><td>Media Dependent Interface[3], positive signal of differential pair<br>1000Base-T Mode:<br>TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXP_D is not used.</td></tr>
<tr><td>11</td><td>TXRXM_D</td><td>I/O</td><td>Media Dependent Interface[3], negative signal of differential pair<br>1000Base-T Mode:<br>TXRXM_D corresponds to BI_DD- for MDI configuration and BI_DC- for MDI-X configuration, respectively.<br>10Base-T/100Base-TX Mode:<br>TXRXM_D is not used.</td></tr>
<tr><td>12</td><td>AVDDH</td><td>P</td><td>3.3V analog $V_{DD}$</td></tr>
<tr><td>13</td><td>VSS_PS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>14</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>15</td><td>LED2 /<br>PHYAD1</td><td>I/O</td><td>LED Output: Programmable LED2 Output /<br>Config Mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up/reset. See “Strapping Options” section for details.<br>The LED2 pin is programmed by the LED_MODE strapping option (pin 41), and is defined as follows.<br><br>Single LED Mode
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>Link off</td><td>H</td><td>OFF</td></tr>
<tr><td>Link on (any speed)</td><td>L</td><td>ON</td></tr>
</table>
Tri-color Dual LED Mode
<table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For Tri-color Dual LED Mode, LED2 works in conjunction with LED1 (pin 17) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>16</td><td>DVDDH</td><td>P</td><td>3.3V/2.5V digital $V_{DD}$</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>17</td><td>LED1 /<br>PHYAD0</td><td>I/O</td><td>LED Output: Programmable LED1 Output /<br>Config Mode: The pull-up/pull-down value is latched as PHYAD[0] during power-up/reset. See “Strapping Options” section for details.<br>The LED1 pin is programmed by the LED_MODE strapping option (pin 41), and is defined as follows.<br><br>Single LED Mode
<table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity (RX, TX)</td><td>Toggle</td><td>Blinking</td></tr>
</table>
Tri-color Dual LED Mode
<table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For Tri-color Dual LED Mode, LED1 works in conjunction with LED2 (pin 15) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>18</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>19</td><td>TXD0</td><td>I</td><td>RGMII Mode: RGMII TD0 (Transmit Data 0) Input</td></tr>
<tr><td>20</td><td>TXD1</td><td>I</td><td>RGMII Mode: RGMII TD1 (Transmit Data 1) Input</td></tr>
<tr><td>21</td><td>TXD2</td><td>I</td><td>RGMII Mode: RGMII TD2 (Transmit Data 2) Input</td></tr>
<tr><td>22</td><td>TXD3</td><td>I</td><td>RGMII Mode: RGMII TD3 (Transmit Data 3) Input</td></tr>
<tr><td>23</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>24</td><td>GTX_CLK</td><td>I</td><td>RGMII Mode: RGMII TXC (Transmit Reference Clock) Input</td></tr>
<tr><td>25</td><td>TX_EN</td><td>I</td><td>RGMII Mode: RGMII TX_CTL (Transmit Control) Input</td></tr>
<tr><td>26</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>27</td><td>RXD3 /<br>MODE3</td><td>I/O</td><td>RGMII Mode: RGMII RD3 (Receive Data 3) Output /<br>Config Mode: The pull-up/pull-down value is latched as MODE3 during power-up/reset. See “Strapping Options” section for details.</td></tr>
<tr><td>28</td><td>RXD2 /<br>MODE2</td><td>I/O</td><td>RGMII Mode: RGMII RD2 (Receive Data 2) Output /<br>Config Mode: The pull-up/pull-down value is latched as MODE2 during power-up/reset. See “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>30</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>31</td><td>RXD1 /<br>MODE1</td><td>I/O</td><td>RGMII Mode: RGMII RD1 (Receive Data 1) Output /<br>Config Mode: The pull-up/pull-down value is latched as MODE1 during power-up/reset. See “Strapping Options” section for details.</td></tr>
</table>

| Pin Number | Pin Name | Type(1) | Pin Function |
|---|---|---|---|
| 32 | RXD0 / MODE0 | I/O | RGMII Mode: RGMII RD0 (Receive Data 0) Output /<br>Config Mode: The pull-up/pull-down value is latched as MODE0 during power-up/reset. See “Strapping Options” section for details. |
| 33 | RX_DV / CLK125_EN | I/O | RGMII Mode: RGMII RX_CTL (Receive Control) Output /<br>Config Mode: Latched as CLK125_NDO Output Enable during power-up/ reset. See “Strapping Options” section for details. |
| 34 | DVDDH | P | 3.3V/2.5V digital $V_{DD}$ |
| 35 | RX_CLK / PHYAD2 | I/O | RGMII Mode: RGMII RXC (Receive Reference Clock) Output /<br>Config Mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up/reset. See “Strapping Options” section for details. |
| 36 | MDC | Ipu | Management Data Clock Input<br>This pin is the input reference clock for MDIO (pin 37). |
| 37 | MDIO | Ipu/O | Management Data Input/Output<br>This pin is synchronous to MDC (pin 36) and requires an external pull-up resistor to 3.3V/2.5V digital $V_{DD}$ in a range from 1.0kΩ to 4.7kΩ. |
| 38 | INT_N | O | Interrupt Output<br>This pin provides a programmable interrupt output and requires an external pull-up resistor to 3.3V/2.5V digital $V_{DD}$ in a range from 1.0kΩ to 4.7kΩ when active low.<br>Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 14 sets the interrupt output to active low (default) or active high. |
| 39 | DVDDL | P | 1.2V digital $V_{DD}$ |
| 40 | DVDDH | P | 3.3V/2.5V digital $V_{DD}$ |
| 41 | CLK125_NDO / LED_MODE | I/O | 125MHz Clock Output<br>This pin provides a 125MHz reference clock output option for use by the MAC. /<br>Config Mode: The pull-up/pull-down value is latched as LED_MODE during power-up/reset. See “Strapping Options” section for details. |
| 42 | RESET_N | Ipu | Chip Reset (active low)<br>Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See “Strapping Options” section for more details. |
| 43 | LDO_O | O | On-chip 1.2V LDO Controller Output<br>This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip’s core voltages. If 1.2V is provided by the system and this pin is not used, it can be left floating. |
| 44 | AVDDL_PLL | P | 1.2V analog $V_{DD}$ for PLL |
| 45 | XO | O | 25MHz Crystal feedback<br>This pin is a no connect if oscillator or external clock source is used. |
| 46 | XI | I | Crystal / Oscillator / External Clock Input<br>25MHz ±50ppm tolerance |
| 47 | AVDDH | P | 3.3V analog $V_{DD}$ |
| 48 | ISET | I/O | Set transmit output level<br>Connect a 4.99kΩ 1% resistor to ground on this pin. |
| PADDLE | P_GND | Gnd | Exposed Paddle on bottom of chip<br>Connect P_GND to ground. |

**Note:**

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up.
   Ipu/O = Input with internal pull-up / Output.

## Strapping Options – KSZ9021RN

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>35<br>15<br>17</td><td>PHYAD2<br>PHYAD1<br>PHYAD0</td><td>I/O<br>I/O<br>I/O</td><td>The PHY Address, PHYAD[2:0], is latched at power-up/reset and is configurable to any value from 1 to 7. Each PHY address bit is configured as follows:<br>Pull-up = 1<br>Pull-down = 0<br>PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>27<br>28<br>31<br>32</td><td>MODE3<br>MODE2<br>MODE1<br>MODE0</td><td>I/O<br>I/O<br>I/O<br>I/O</td><td>The MODE[3:0] strap-in pins are latched at power-up/reset and are defined as follows:
<table>
<tr><th>MODE[3:0]</th><th>Mode</th></tr>
<tr><td>0000</td><td>Reserved – not used</td></tr>
<tr><td>0001</td><td>Reserved – not used</td></tr>
<tr><td>0010</td><td>Reserved – not used</td></tr>
<tr><td>0011</td><td>Reserved – not used</td></tr>
<tr><td>0100</td><td>NAND Tree Mode</td></tr>
<tr><td>0101</td><td>Reserved – not used</td></tr>
<tr><td>0110</td><td>Reserved – not used</td></tr>
<tr><td>0111</td><td>Chip Power Down Mode</td></tr>
<tr><td>1000</td><td>Reserved – not used</td></tr>
<tr><td>1001</td><td>Reserved – not used</td></tr>
<tr><td>1010</td><td>Reserved – not used</td></tr>
<tr><td>1011</td><td>Reserved – not used</td></tr>
<tr><td>1100</td><td>RGMII Mode – advertise 1000Base-T full-duplex only</td></tr>
<tr><td>1101</td><td>RGMII Mode – advertise 1000Base-T full and half-duplex only</td></tr>
<tr><td>1110</td><td>RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex), except 1000Base-T half-duplex</td></tr>
<tr><td>1111</td><td>RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex)</td></tr>
</table></td></tr>
<tr><td>33</td><td>CLK125_EN</td><td>I/O</td><td>CLK125_EN is latched at power-up/reset and is defined as follows:<br>Pull-up = Enable 125MHz Clock Output<br>Pull-down = Disable 125MHz Clock Output<br>Pin 41 (CLK125_NDO) provides the 125MHz reference clock output option for use by the MAC.</td></tr>
<tr><td>41</td><td>LED_MODE</td><td>I/O</td><td>LED_MODE is latched at power-up/reset and is defined as follows:<br>Pull-up = Single LED Mode<br>Pull-down = Tri-color Dual LED Mode</td></tr>
</table>

**Note:**

1. I/O = Bi-directional.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the RGMII signals to be latched to the incorrect configuration. In this case, it is recommended to add external pull-ups/pull-downs on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

## Functional Overview

The KSZ9021RL/RN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable. Its on-chip proprietary 1000Base-T transceiver and Manchester/MLT-3 signaling-based 10Base-T/100Base-TX transceivers are all IEEE 802.3 compliant.

The KSZ9021RL/RN reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9021RL/RN can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

The KSZ9021RL/RN provides the RGMII interface for a direct and seamless connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000Mbps speed.

The following figure shows a high-level block diagram of the KSZ9021RL/RN.

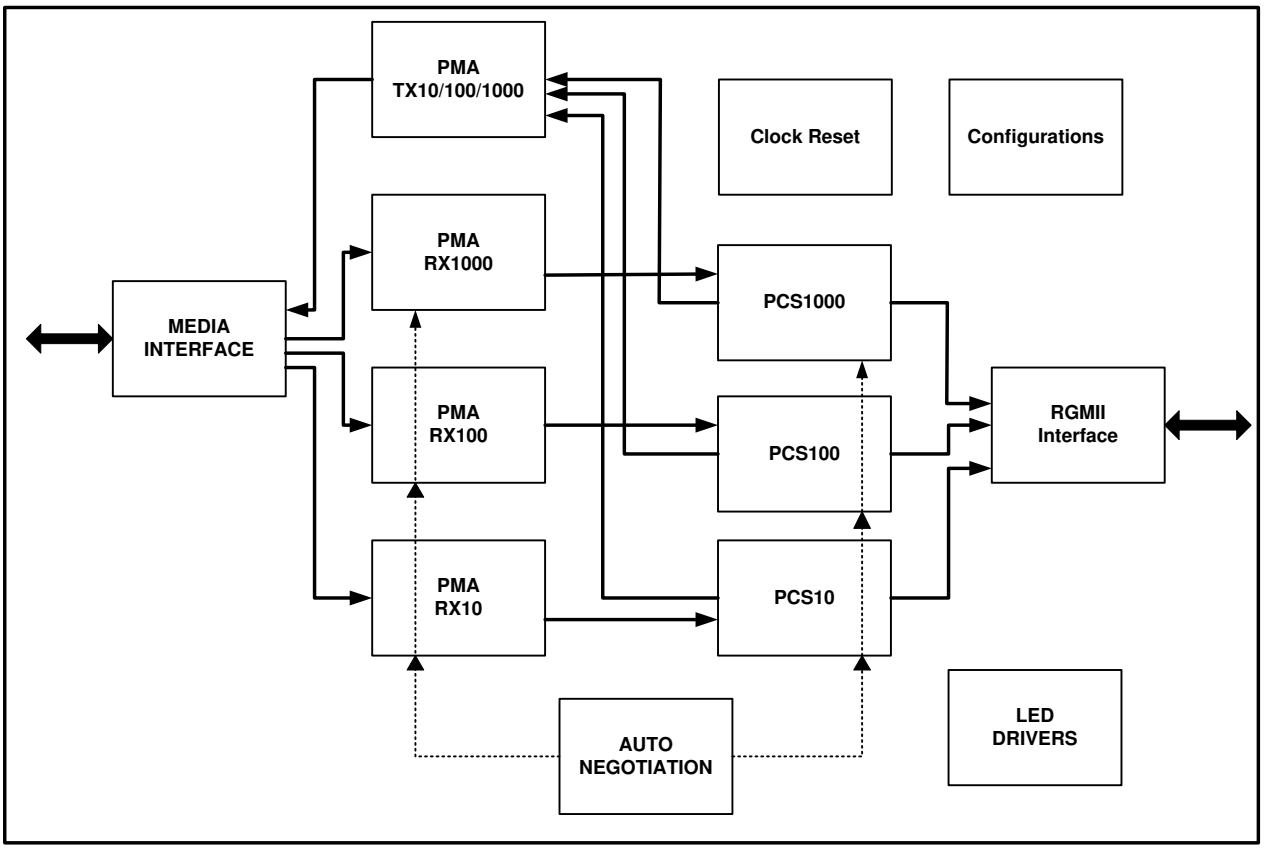



**Figure 1. KSZ9021RL/RN Block Diagram**

# Functional Description: 10Base-T/100Base-TX Transceiver

### 100Base-TX Transmit

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the RGMII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 4.99kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

### 100Base-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RGMII format and provided as the input data to the MAC.

### Scrambler/De-scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

### 10Base-T Transmit

The output 10Base-T driver is incorporated into the 100Base-TX driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into typical outputs of 2.5V amplitude. The harmonic contents are at least 31 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

### 10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths in order to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9021RL/RN decodes a data frame. The receiver clock is maintained active during idle periods in between receiving data frames.

## Functional Description: 1000Base-T Transceiver

The 1000Base-T transceiver is based on a mixed-signal/digital signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancellers, cross-talk cancellers, precision clock recovery scheme, and power efficient line drivers.

The following figure shows a high-level block diagram of a single channel of the 1000Base-T transceiver for one of the four differential pairs.

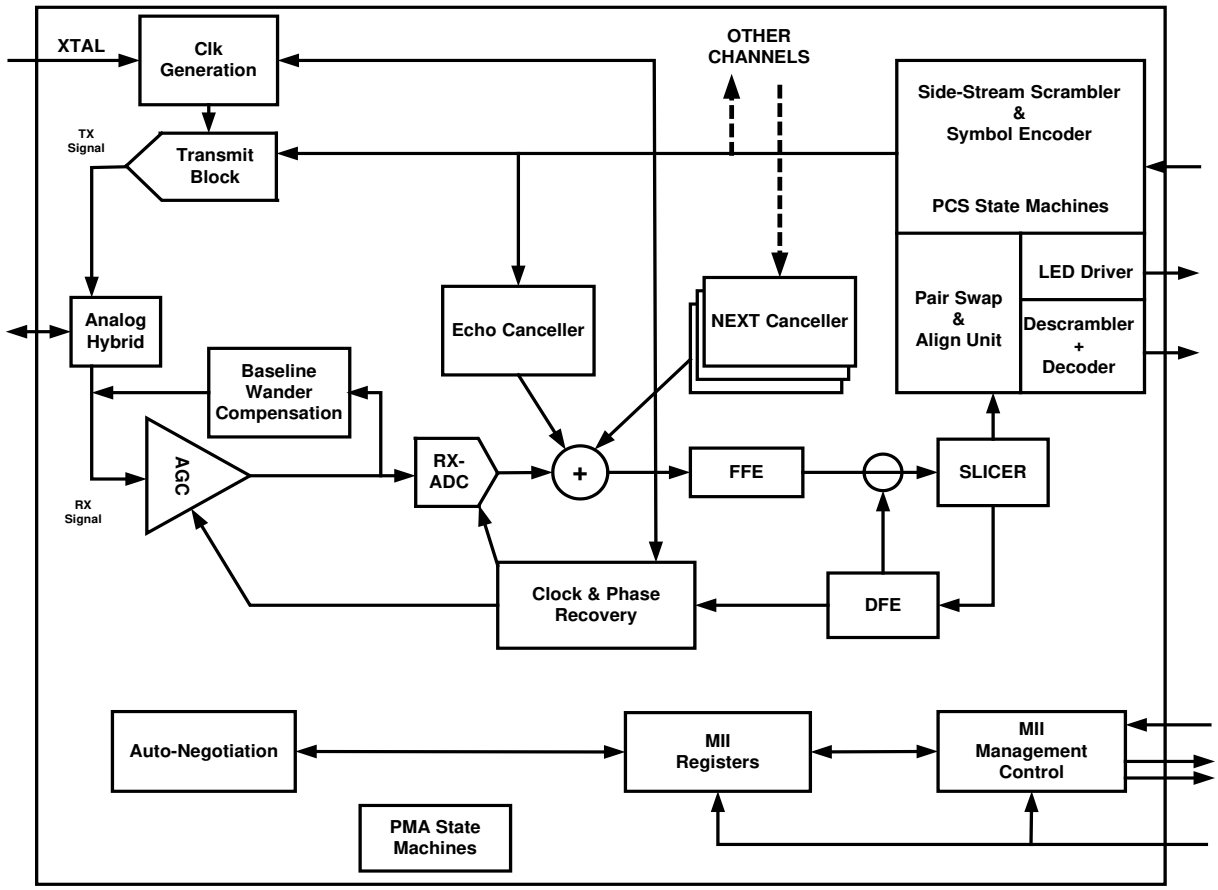



**Figure 2. KSZ9021RL/RN 1000Base-T Block Diagram – Single Channel**

### Analog Echo Cancellation Circuit

In 1000Base-T mode, the analog echo cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10Base-T/100Base-TX mode.

### Automatic Gain Control (AGC)

In 1000Base-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

### Analog-to-Digital Converter (ADC)

In 1000Base-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10Base-T/100Base-TX mode.

### Timing Recovery Circuit

In 1000Base-T mode, the mixed-signal clock recovery circuit, together with the digital phase locked loop, is used to recover and track the incoming timing information from the received data. The digital phase locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000Base-T slave PHY is required to transmit the exact receive clock frequency recovered from the received data back to the 1000Base-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. Additionally, this helps to facilitate echo cancellation and NEXT removal.

### Adaptive Equalizer

In 1000Base-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid and echo due to impedance mismatch. The KSZ9021RL/RN employs a digital echo canceller to further reduce echo components on the receive signal.

In 1000Base-T mode, the data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high frequency cross-talk coming from adjacent wires. The KSZ9021RL/RN employs three NEXT cancellers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10Base-T/100Base-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

### Trellis Encoder and Decoder

In 1000Base-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9021RL/RN is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order and polarity have to be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and then de-scrambled into 8-bit data.

## Functional Description: 10/100/1000 Transceiver Features

### Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9021RL/RN and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and then assigns the MDI/MDI-X pair mapping of the KSZ9021RL/RN accordingly.

The following table shows the KSZ9021RL/RN 10/100/1000 pin-out assignments for MDI/MDI-X pin mapping.

| Pin (RJ-45 pair) | MDI | | | MDI-X | | |
|---|---|---|---|---|---|---|
| | 1000Base-T | 100Base-TX | 10Base-T | 1000Base-T | 100Base-TX | 10Base-T |
| TXRXP/M_A (1,2) | A+/- | TX+/- | TX+/- | B+/- | RX+/- | RX+/- |
| TXRXP/M_B (3,6) | B+/- | RX+/- | RX+/- | A+/- | TX+/- | TX+/- |
| TXRXP/M_C (4,5) | C+/- | Not used | Not used | D+/- | Not used | Not used |
| TXRXP/M_D (7,8) | D+/- | Not used | Not used | C+/- | Not used | Not used |

**Table 1. MDI/MDI-X Pin Mapping**

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 28 (1Ch) bit 6. MDI and MDI-X mode is set by register 28 (1Ch) bit 7 if auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X.