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KSZ9031MNX

Gigabit Ethernet Transceiver with GMII/MII Support

Features

- Single-Chip 10/100/1000 Mbps Ethernet Transceiver Suitable for IEEE 802.3 Applications
- GMII/MII Standard Interface with 3.3V/2.5V/1.8V Tolerant I/Os
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100/1000 Mbps) and Duplex (Half/Full)
- On-Chip Termination Resistors for the Differential Pairs
- On-Chip LDO Controller to Support Single 3.3V Supply Operation
- Jumbo Frame Support Up to 16 KB
- 125 MHz Reference Clock Output
- Energy-Detect Power-Down Mode for Reduced Power Consumption When the Cable is Not Attached
- Wake-On-LAN (WOL) Support with Robust Custom-Packet Detection
- Programmable LED Outputs for Link, Activity, and Speed
- Baseline Wander Correction
- LinkMD TDR-based Cable Diagnostic to Identify Faulty Copper Cabling
- Parametric NAND Tree Support to Detect Faults Between Chip I/Os and Board
- Loopback Modes for Diagnostics
- Automatic MDI/MDI-X Crossover to Detect and Correct Pair Swap at All Speeds of Operation
- Automatic Detection and Correction of Pair Swaps, Pair Skew, and Pair Polarity
- MDC/MDIO Management Interface for PHY Register Configuration
- Interrupt Pin Option
- Power-Down and Power-Saving Modes
- Operating Voltages
  - Core (DVDDL, AVDDL, AVDDL_PLL): 1.2V (External FET or Regulator)
  - VDD I/O (DVDDH): 3.3V, 2.5V, or 1.8V
  - Transceiver (AVDDH): 3.3V or 2.5V (Commercial Temp.)
- 64-pin QFN (8 mm × 8 mm) Package

Target Applications

- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-Top Box
- Game Console
- IP Camera
- Triple-Play (Data, Voice, Video) Media Center
- Media Converter

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

The KSZ9031MNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical-layer transceiver for transmission and reception of data on standard CAT-5 unshielded twisted pair (UTP) cable.

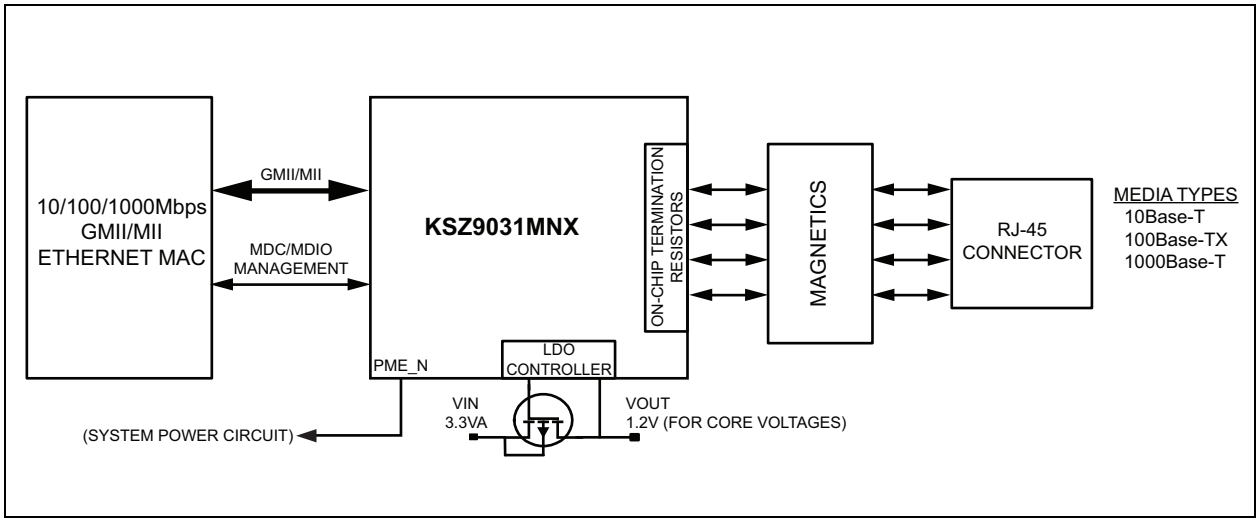
The KSZ9031MNX offers the industry-standard GMII/MII (Gigabit Media Independent Interface/Media Independent Interface) for connection to GMII/MII MACs in Gigabit Ethernet processors and switches for data transfer at 1000 Mbps or 10/100 Mbps.

The KSZ9031MNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

The KSZ9031MNX offers diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9031MNX I/Os and the board. The LinkMD® TDR-based cable diagnostic identifies faulty copper cabling. Remote and local loopback functions verify analog and digital data paths.

The KSZ9031MNX is available in a 64-pin, lead-free QFN package.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 64-QFN PIN ASSIGNMENT (TOP VIEW)

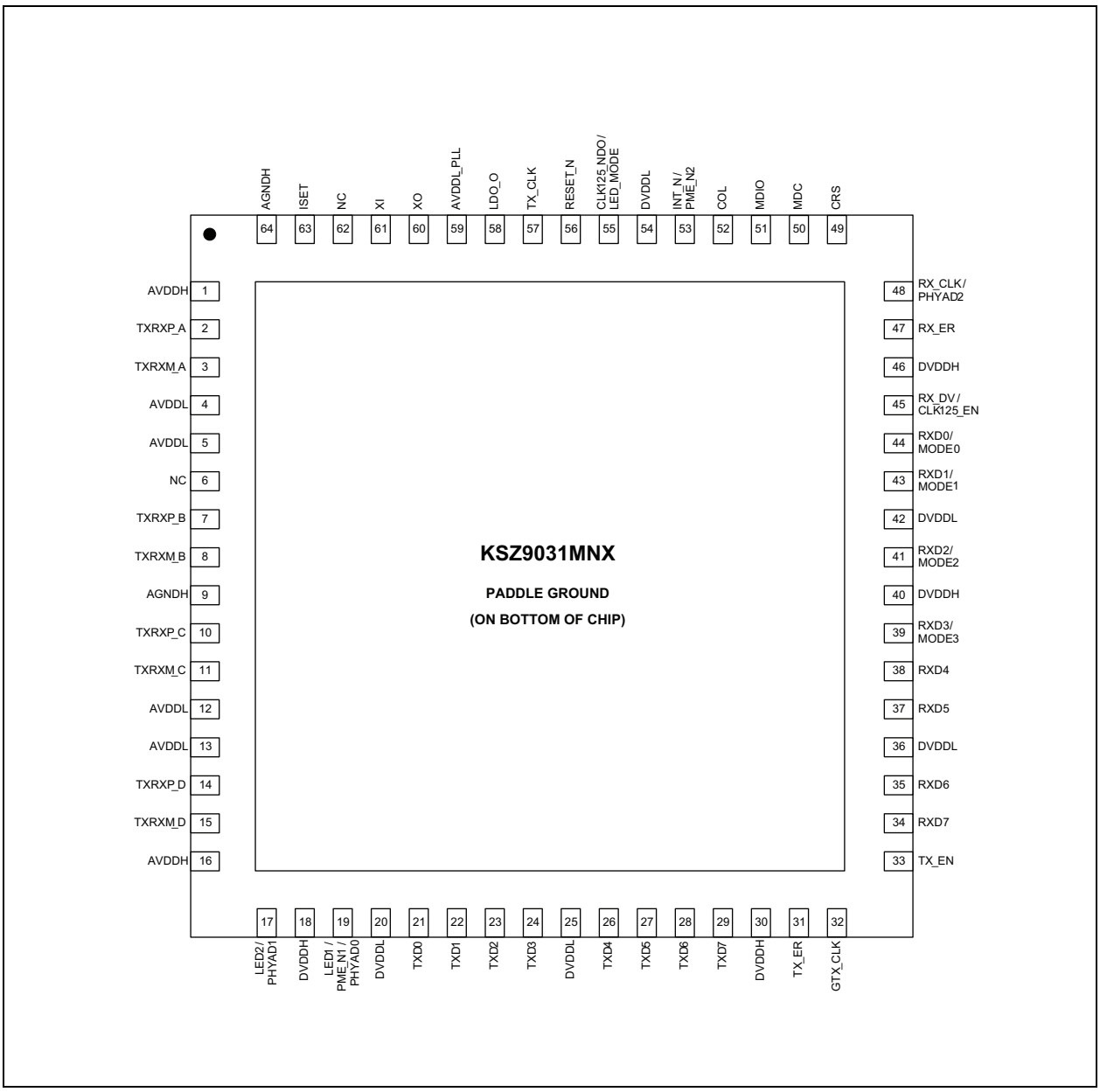


TABLE 2-1: SIGNALS - KSZ9031MNX

Pin Number	Pin Name	Type Note 2-1	Description
1	AVDDH	P	3.3V/2.5V (commercial temperature only) analog V_{DD}
2	TXRXP_A	I/O	Media Dependent Interface[0], positive signal of differential pair 1000BASE-T mode: TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively.
3	TXRXM_A	I/O	Media Dependent Interface[0], negative signal of differential pair 1000BASE-T mode: TXRXM_A corresponds to BI_DA– for MDI configuration and BI_DB– for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXM_A is the negative transmit signal (TX–) for MDI configuration and the negative receive signal (RX–) for MDI-X configuration, respectively.
4	AVDDL	P	1.2V analog V_{DD}
5	AVDDL	P	1.2V analog V_{DD}
6	NC	—	No connect
7	TXRXP_B	I/O	Media Dependent Interface[1], positive signal of differential pair 1000BASE-T mode: TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively.
8	TXRXM_B	I/O	Media Dependent Interface[1], negative signal of differential pair 1000BASE-T mode: TXRXM_B corresponds to BI_DB– for MDI configuration and BI_DA– for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXM_B is the negative receive signal (RX–) for MDI configuration and the negative transmit signal (TX–) for MDI-X configuration, respectively.
9	AGNDH	GND	Analog ground
10	TXRXP_C	I/O	Media Dependent Interface[2], positive signal of differential pair 1000BASE-T mode: TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXP_C is not used.
11	TXRXM_C	I/O	Media Dependent Interface[2], negative signal of differential pair 1000BASE-T mode: TXRXM_C corresponds to BI_DC– for MDI configuration and BI_DD– for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXM_C is not used.
12	AVDDL	P	1.2V analog V_{DD}
13	AVDDL	P	1.2V analog V_{DD}

TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td>14</td><td>TXRXP_D</td><td>I/O</td><td>Media Dependent Interface[3], positive signal of differential pair
1000BASE-T mode: TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively.
10BASE-T/100BASE-TX mode: TXRXP_D is not used.</td></tr>
<tr><td>15</td><td>TXRXM_D</td><td>I/O</td><td>Media Dependent Interface[3], negative signal of differential pair
1000BASE-T mode: TXRXM_D corresponds to BI_DD– for MDI configuration and BI_DC– for MDI-X configuration, respectively.
10BASE-T/100BASE-TX mode: TXRXM_D is not used.</td></tr>
<tr><td>16</td><td>AVDDH</td><td>P</td><td>3.3V/2.5V (commercial temperature only) analog V_{DD}</td></tr>
<tr><td>17</td><td>LED2/
PHYAD1</td><td>I/O</td><td>LED2 output: Programmable LED2 output
Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of PHYAD[1]. See the Strapping Options - KSZ9031MNX section for details.
The LED2 pin is programmed by the LED_MODE strapping option (Pin 55), and is defined as follows:
Single-LED Mode
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>Link Off</td><td>H</td><td>OFF</td></tr>
<tr><td>Link On (any speed)</td><td>L</td><td>ON</td></tr>
</table>
Tri-Color Dual-LED Mode
<table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link Off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link/No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link/Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link/No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link/Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link/No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link/Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For tri-color dual-LED mode, LED2 works in conjunction with LED1 (Pin 19) to indicate 10 Mbps link and activity.</td></tr>
<tr><td>18</td><td>DVDDH</td><td>P</td><td>3.3V, 2.5V, or 1.8V digital V_{DD_IO}</td></tr>
</table>

TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td rowspan="20">19</td><td rowspan="20">LED1/
PHYAD0/
PME_N1</td><td rowspan="20">I/O</td><td>LED1 output: Programmable LED1 output
Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of PHYAD[0]. See the Strapping Options - KSZ9031MNX section for details.
PME_N output: Programmable PME_N output (pin option 1). This pin function requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0 kΩ to 4.7 kΩ. When asserted low, this pin signals that a WOL event has occurred.
This pin is not an open-drain for all operating modes.
The LED1 pin is programmed by the LED_MODE strapping option (Pin 55), and is defined as follows:</td></tr>
<tr><td>Single-LED Mode</td></tr>
<tr><td><table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity (RX, TX)</td><td>Toggle</td><td>Blinking</td></tr>
</table></td></tr>
<tr><td>Tri-Color Dual-LED Mode</td></tr>
<tr><td><table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link Off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link/No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link/Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link/No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link/Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link/No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link/Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table></td></tr>
<tr><td>For tri-color dual-LED mode, LED1 works in conjunction with LED2 (Pin 17) to indicate 10 Mbps link and activity.</td></tr>
<tr><td>20</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>21</td><td>TXD0</td><td>I</td><td>GMII mode: GMII TXD0 (Transmit Data 0) input
MII mode: MII TXD0 (Transmit Data 0) input</td></tr>
<tr><td>22</td><td>TXD1</td><td>I</td><td>GMII mode: GMII TXD1 (Transmit Data 1) input
MII mode: MII TXD1 (Transmit Data 1) input</td></tr>
<tr><td>23</td><td>TXD2</td><td>I</td><td>GMII mode: GMII TXD2 (Transmit Data 2) input
MII mode: MII TXD2 (Transmit Data 2) Input</td></tr>
</table>

TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
24	TXD3	I	GMII mode: GMII TXD3 (Transmit Data 3) input MII mode: MII TXD3 (Transmit Data 3) input
25	DVDDL	P	1.2V digital V_{DD}
26	TXD4	I	GMII mode: GMII TXD4 (Transmit Data 4) input MII mode: This pin is not used and can be driven high or low.
27	TXD5	I	GMII mode: GMII TXD5 (Transmit Data 5) input MII mode: This pin is not used and can be driven high or low.
28	TXD6	I	GMII mode: GMII TXD6 (Transmit Data 6) input MII Mode: This pin is not used and can be driven high or low.
29	TXD7	I	GMII mode: GMII TXD7 (Transmit Data 7) input MII mode: This pin is not used and can be driven high or low.
30	DVDDH	P	3.3V, 2.5V, or 1.8V digital V_{DD_IO}
31	TX_ER	I	GMII mode: GMII TX_ER (Transmit Error) input MII mode: MII TX_ER (Transmit Error) input If the GMII/MII MAC does not provide the TX_ER output signal, this pin should be tied low.
32	GTX_CLK	I	GMII mode: GMII GTX_CLK (Transmit Reference Clock) input
33	TX_EN	I	GMII mode: GMII TX_EN (Transmit Enable) input MII mode: MII TX_EN (Transmit Enable) input
34	RXD7	O	GMII mode: GMII RXD7 (Receive Data 7) output MII mode: This pin is not used and is driven low.
35	RXD6	O	GMII mode: GMII RXD6 (Receive Data 6) output MII mode: This pin is not used and is driven low.
36	DVDDL	P	1.2V digital V_{DD}
37	RXD5	O	GMII mode: GMII RXD5 (Receive Data 5) output MII mode: This pin is not used and is driven low.
38	RXD4	O	GMII mode: GMII RXD4 (Receive Data 4) output MII mode: This pin is not used and is driven low.
39	RXD3/ MODE3	I/O	GMII mode: GMII RXD3 (Receive Data 3) output MII mode: MII RXD3 (Receive Data 3) output Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of MODE3. See the Strapping Options - KSZ9031MNX section for details.
40	DVDDH	P	3.3V, 2.5V, or 1.8V digital V_{DD_IO}
41	RXD2/ MODE2	I/O	GMII mode: GMII RXD2 (Receive Data 2) output MII mode: MII RXD2 (Receive Data 2) output Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of MODE2. See the Strapping Options - KSZ9031MNX section for details.
42	DVDDL	P	1.2V digital V_{DD}

TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
43	RXD1/ MODE1	I/O	GMII mode: GMII RXD1 (Receive Data 1) output MII mode: MII RXD1 (Receive Data 1) output Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of MODE1. See the Strapping Options - KSZ9031MNX section for details.
44	RXD0/ MODE0	I/O	GMII mode: GMII RXD0 (Receive Data 0) output MII mode: MII RXD0 (Receive Data 0) output Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of MODE0. See the Strapping Options - KSZ9031MNX section for details.
45	RX_DV/ CLK125_EN	I/O	GMII mode: GMII RX_DV (Receive Data Valid) output MII mode: MII RX_DV (Receive Data Valid) output Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of CLK125_EN. See the Strapping Options - KSZ9031MNX section for details.
46	DVDDH	P	3.3V, 2.5V, or 1.8V digital V_{DD_IO}
47	RX_ER	O	GMII mode: GMII RX_ER (Receive Error) output MII mode: MII RX_ER (Receive Error) output
48	RX_CLK/ PHYAD2	I/O	GMII mode: GMII RX_CLK (Receive Reference Clock) output MII mode: MII RX_CLK (Receive Reference Clock) output Config mode: The voltage on this pin is sampled and latched during the power up/reset process to determine the value of PHYAD[2]. See the Strapping Options - KSZ9031MNX section for details.
49	CRS	O	GMII mode: GMII CRS (Carrier Sense) output MII mode: MII CRS (Carrier Sense) output
50	MDC	Ipu	Management data clock input This pin is the input reference clock for MDIO (Pin 51).
51	MDIO	Ipu/O	Management data input/output This pin is synchronous to MDC (Pin 50) and requires an external pull-up resistor to DVDDH (digital V_{DD_IO}) in a range from 1.0 kΩ to 4.7 kΩ.
52	COL	O	GMII mode: GMII COL (Collision Detected) output MII mode: MII COL (Collision Detected) output
53	INT_N/ PME_N2	O	Interrupt output: Programmable interrupt output, with Register 1Bh as the Interrupt Control/Status Register, for programming the interrupt conditions and reading the interrupt status. Register 1Fh, Bit [14] sets the interrupt output to active low (default) or active high. PME_N output: Programmable PME_N output (pin option 2). When asserted low, this pin signals that a WOL event has occurred. For Interrupt (when active low) and PME functions, this pin requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0 kΩ to 4.7 kΩ. This pin is not an open-drain for all operating modes.
54	DVDDL	P	1.2V digital V_{DD}

TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
55	CLK125_NDO/ LED_MODE	I/O	125 MHz clock output This pin provides a 125 MHz reference clock output option for use by the MAC. Config mode: The voltage on this pin is sampled during the power-up/reset process to determine the value of LED_MODE. See the Strapping Options - KSZ9031MNX section for details.
56	RESET_N	Ipu	Chip reset (active low) Hardware pin configurations are strapped-in (sampled and latched) at the de-assertion (rising edge) of RESET_N. See the Strapping Options - KSZ9031MNX section for details.
57	TX_CLK	O	MII mode: MII TX_CLK (Transmit Reference Clock) output
58	LDO_O	O	On-chip 1.2V LDO controller output This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip's core voltages. If the system provides 1.2V and this pin is not used, it can be left floating.
59	AVDDL_PLL	P	1.2V analog V_{DD} for PLL
60	XO	O	25 MHz crystal feedback This pin connects to one end of an external 25 MHz crystal. This pin is a no connect if an oscillator or other external (non-crystal) clock source is used.
61	XI	I	Crystal/Oscillator/External Clock input This pin connects to one end of an external 25 MHz crystal or to the output of an oscillator or other external (non-crystal) clock source. 25 MHz ±50 ppm tolerance
62	NC	—	No connect This pin is not bonded and can be connected to AVDDH power for footprint compatibility with the KSZ9021GN Gigabit PHY.
63	ISET	I/O	Set the transmit output level. Connect a 12.1 kΩ 1% resistor to ground on this pin.
64	AGNDH	GND	Analog ground.
Paddle	P_GND	GND	Exposed paddle on bottom of chip. Connect P_GND to ground.

Note 2-1 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Electrical Characteristics for value).
Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during the power-up or reset process, and consequently cause the PHY strap-in pins on the GMII/MII signals to be latched to the incorrect configuration. In this case, external pull-up or pull-down resistors should be added on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

TABLE 2-2: STRAPPING OPTIONS - KSZ9031MNX

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type
Note 2-1</th><th>Description</th></tr>
<tr><td>48
17
19</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>I/O
I/O
I/O</td><td>The PHY address, PHYAD[2:0], is sampled and latched at power-up/reset and is configurable to any value from 0 to 7. Each PHY address bit is configured as follows:
Pull-up = 1
Pull-down = 0
PHY Address Bits [4:3] are always set to ‘00’.</td></tr>
<tr><td rowspan="18">39
41
43
44</td><td rowspan="18">MODE3
MODE2
MODE1
MODE0</td><td rowspan="18">I/O
I/O
I/O
I/O</td><td>The MODE[3:0] strap-in pins are sampled and latched at power-up/reset and are defined as follows:</td></tr>
<tr><td>
<table>
<tr><th>MODE[3:0]</th><th>Mode</th></tr>
<tr><td>0000</td><td>Reserved - not used</td></tr>
<tr><td>0001</td><td>GMII/MII mode</td></tr>
<tr><td>0010</td><td>Reserved - not used</td></tr>
<tr><td>0011</td><td>Reserved - not used</td></tr>
<tr><td>0100</td><td>NAND tree mode</td></tr>
<tr><td>0101</td><td>Reserved - not used</td></tr>
<tr><td>0110</td><td>Reserved - not used</td></tr>
<tr><td>0111</td><td>Chip power-down mode</td></tr>
<tr><td>1000</td><td>Reserved - not used</td></tr>
<tr><td>1001</td><td>Reserved - not used</td></tr>
<tr><td>1010</td><td>Reserved - not used</td></tr>
<tr><td>1011</td><td>Reserved - not used</td></tr>
<tr><td>1100</td><td>Reserved - not used</td></tr>
<tr><td>1101</td><td>Reserved - not used</td></tr>
<tr><td>1110</td><td>Reserved - not used</td></tr>
<tr><td>1111</td><td>Reserved - not used</td></tr>
</table>
</td></tr>
<tr><td>45</td><td>CLK125_EN</td><td>I/O</td><td>CLK125_EN is sampled and latched at power-up/reset and is defined as follows:
Pull-up (1) = Enable 125 MHz clock output
Pull-down (0) = Disable 125 MHz clock output
Pin 55 (CLK125_NDO) provides the 125 MHz reference clock output option for use by the MAC.</td></tr>
<tr><td>55</td><td>LED_MODE</td><td>I/O</td><td>LED_MODE is sampled and latched at power-up/reset and is defined as follows:
Pull-up (1) = Single-LED mode
Pull-down (0) = Tri-color dual-LED mode</td></tr>
</table>

Note 2-1 I/O = Bi-directional.

3.0 FUNCTIONAL DESCRIPTION

The KSZ9031MNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable.

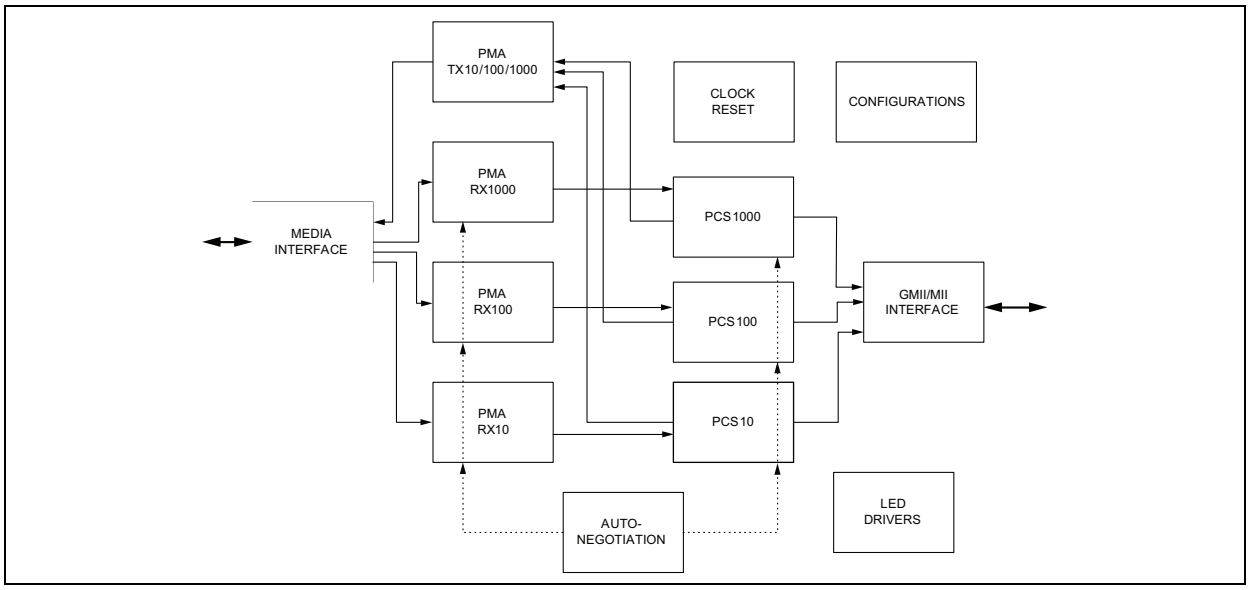
The KSZ9031MNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9031MNX can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000BASE-T operation.

The KSZ9031MNX provides the GMII/MII interface for connection to GMACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000Mbps.

Figure 3-1 shows a high-level block diagram of the KSZ9031MNX.

FIGURE 3-1: KSZ9031MNX BLOCK DIAGRAM



3.1 10BASE-T/100BASE-TX Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 12.1 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, and overshoot. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the GMII/MII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled using an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.1.4 10BASE-T TRANSMIT

The 10BASE-T output drivers are incorporated into the 100BASE-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/10BASE-Te signals have harmonic contents that are at least 31 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level-detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9031MNX decodes a data frame. The receiver clock is maintained active during idle periods between receiving data frames.

The KSZ9031MNX removes all 7 bytes of the preamble and presents the received frame starting with the SFD (start of frame delimiter) to the MAC.

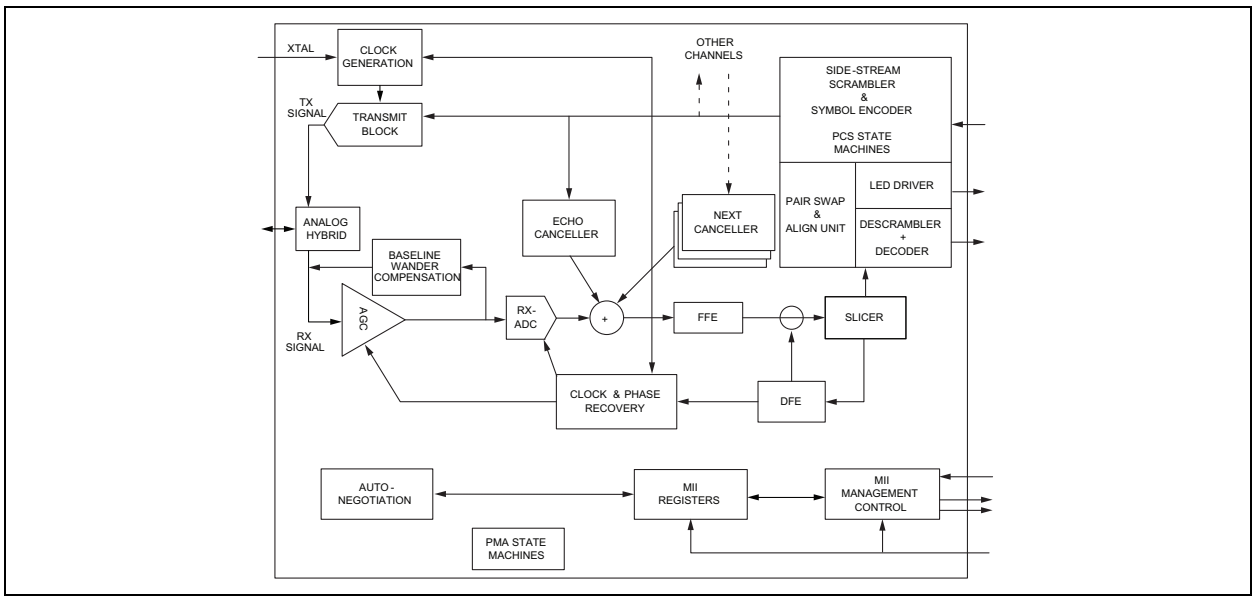
Auto-polarity correction is provided for the receiving differential pair to automatically swap and fix the incorrect +/– polarity wiring in the cabling.

3.2 1000BASE-T Transceiver

The 1000BASE-T transceiver is based-on a mixed-signal/digital-signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancelers, cross-talk cancelers, precision clock recovery scheme, and power-efficient line drivers.

Figure 3-2 shows a high-level block diagram of a single channel of the 1000BASE-T transceiver for one of the four differential pairs.

FIGURE 3-2: KSZ9031MNX 1000BASE-T BLOCK DIAGRAM - SINGLE CHANNEL



3.2.1 ANALOG ECHO-CANCELLATION CIRCUIT

In 1000BASE-T mode, the analog echo-cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

3.2.2 AUTOMATIC GAIN CONTROL (AGC)

In 1000BASE-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

3.2.3 ANALOG-TO-DIGITAL CONVERTER (ADC)

In 1000BASE-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

3.2.4 TIMING RECOVERY CIRCUIT

In 1000BASE-T mode, the mixed-signal clock recovery circuit together with the digital phase-locked loop is used to recover and track the incoming timing information from the received data. The digital phase-locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000BASE-T slave PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000BASE-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

3.2.5 ADAPTIVE EQUALIZER

In 1000BASE-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The KSZ9031MNX uses a digital echo canceler to further reduce echo components on the receive signal.

In 1000BASE-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The KSZ9031MNX uses three NEXT cancelers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10BASE-T/100BASE-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

3.2.6 TRELLIS ENCODER AND DECODER

In 1000BASE-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9031MNX is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order, and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

3.3 Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9031MNX and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the KSZ9031MNX accordingly.

Table 3-1 shows the KSZ9031MNX 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

TABLE 3-1: MDI/MDI-X PIN MAPPING

Pin (RJ-45 Pair)	MDI			MDI-X		
	1000BASE-T	100BASE-T	10BASE-T	1000BASE-T	100BASE-T	10BASE-T
TXRXP/M_A (1, 2)	A+/–	TX+/–	TX+/–	B+/–	RX+/–	RX+/–
TXRXP/M_B (3, 6)	B+/–	RX+/–	RX+/–	A+/–	TX+/–	TX+/–
TXRXP/M_C (4, 5)	C+/–	Not Used	Not Used	D+/–	Not Used	Not Used
TXRXP/M_D (7, 8)	D+/–	Not Used	Not Used	C+/–	Not Used	Not Used

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to Register 1Ch, Bit [6]. MDI and MDI-X mode is set by Register 1Ch, Bit [7] if Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

3.4 Pair-Swap, Alignment, and Polarity Check

In 1000BASE-T mode, the KSZ9031MNX

- Detects incorrect channel order and automatically restores the pair order for the A, B, C, D pairs (four channels).
- Supports 50 ns ±10 ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized.

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

3.5 Wave Shaping, Slew-Rate Control, and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000BASE-T, a special partial-response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-T, pre-emphasis is used to extend the signal quality through the cable.

3.6 PLL Clock Synthesizer

The KSZ9031MNX generates 125 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from the external 25 MHz crystal or reference clock.

3.7 Auto-Negotiation

The KSZ9031MNX conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (unshielded twisted pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the operating mode.

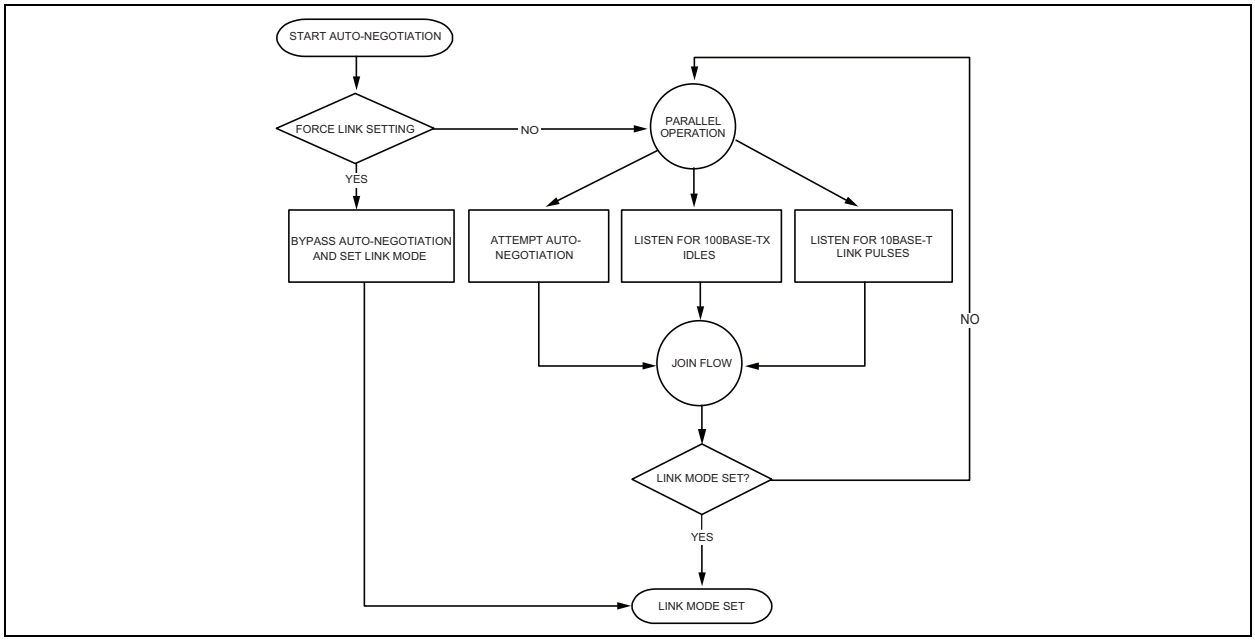
The following list shows the speed and duplex operation mode from highest-to-lowest:

- Priority 1: 1000BASE-T, full-duplex
- Priority 2: 1000BASE-T, half-duplex
- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 100BASE-TX, half-duplex
- Priority 5: 10BASE-T, full-duplex
- Priority 6: 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ9031MNX link partner is forced to bypass auto-negotiation for 10BASE-T and 100BASE-TX modes, the KSZ9031MNX sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9031MNX to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION FLOW CHART



For 1000BASE-T mode, auto-negotiation is required and always used to establish a link. During 1000BASE-T auto-negotiation, the master and slave configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled through Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bits [6, 13] and the duplex is set by Register 0h, Bit [8].

If the speed is changed on the fly, the link goes down and either auto-negotiation or parallel detection initiates until a common speed between KSZ9031MNX and its link partner is re-established for a link.

If the link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through Register 0h, Bit [9], or a link-down to link-up transition occurs (that is, disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in Register 1h, Bit [2], and the link partner capabilities are updated in Registers 5h, 6h, and Ah.

The auto-negotiation finite state machines use interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions is summarized in Table 3-2.

TABLE 3-2: AUTO-NEGOTIATION TIMERS

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst Interval	16 ms
Transmit Pulse Interval	68 µs
FLP Detect Minimum Time	17.2 µs
FLP Detect Maximum Time	185 µs
Receive Minimum Burst Interval	6.8 ms
Receive Maximum Burst Interval	112 ms
Data Detect Minimum Interval	35.4 µs
Data Detect Maximum Interval	95 µs
NLP Test Minimum Interval	4.5 ms
NLP Test Maximum Interval	30 ms
Link Loss Time	52 ms
Break Link Time	1480 ms
Parallel Detection Wait Time	830 ms
Link Enable Wait Time	1000 ms

3.8 10/100 Mbps Speeds Only

Some applications require link-up to be limited to 10/100 Mbps speeds only.

After power-up/reset, the KSZ9031MNX can be restricted to auto-negotiate and link-up to 10/100 Mbps speeds only by programming the following register settings:

1. Set Register 0h, Bit [6] = ‘0’ to remove 1000 Mbps speed.
2. Set Register 9h, Bits [9:8] = ‘00’ to remove Auto-Negotiation advertisements for 1000 Mbps full/half duplex.
3. Write a ‘1’ to Register 0h, Bit [9], a self-clearing bit, to force a restart of Auto-Negotiation.

Auto-Negotiation and 10BASE-T/100BASE-TX speeds use only differential pairs A (pins 2, 3) and B (pins 7, 8). Differential pairs C (pins 10, 11) and D (pins 14, 15) can be left as no connects.

3.9 GMII Interface

The Gigabit Media Independent Interface (GMII) is compliant to the IEEE 802.3 Specification. It provides a common interface between GMII PHYs and MACs, and has the following key characteristics:

- Pin count is 24 pins (11 pins for data transmission, 11 pins for data reception, and 2 pins for carrier and collision indication).
- 1000 Mbps is supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 8 bits wide, a byte.

In GMII operation, the GMII pins function as follows:

- The MAC sources the transmit reference clock, GTX_CLK, at 125 MHz for 1000 Mbps.
- The PHY recovers and sources the receive reference clock, RX_CLK, at 125 MHz for 1000 Mbps.
- TX_EN, TXD[7:0], and TX_ER are sampled by the KSZ9031MNX on the rising edge of GTX_CLK.
- RX_DV, RXD[7:0], and RX_ER are sampled by the MAC on the rising edge of RX_CLK.
- CRS and COL are driven by the KSZ9031MNX and do not have to transition synchronously with respect to either GTX_CLK or RX_CLK.

The KSZ9031MNX combines GMII mode with MII mode to form GMII/MII mode to support data transfer at 10/100/1000 Mbps. After power-up or reset, the KSZ9031MNX is configured to GMII/MII mode if the MODE[3:0] strap-in pins are set to '0001'. See the Strapping Options - KSZ9031MNX section.

The KSZ9031MNX has the option to output a 125 MHz reference clock on CLK125_NDO (Pin 55). This clock provides a lower-cost reference clock alternative for GMII/MII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

The KSZ9031MNX provides a dedicated transmit clock input pin (GTX_CLK, Pin 32) for GMII mode, which is sourced by the MAC for 1000 Mbps speed.

3.9.1 GMII SIGNAL DEFINITION

Table 3-3 describes the GMII signals. Refer to Clause 35 of the IEEE 802.3 Specification for more detailed information.

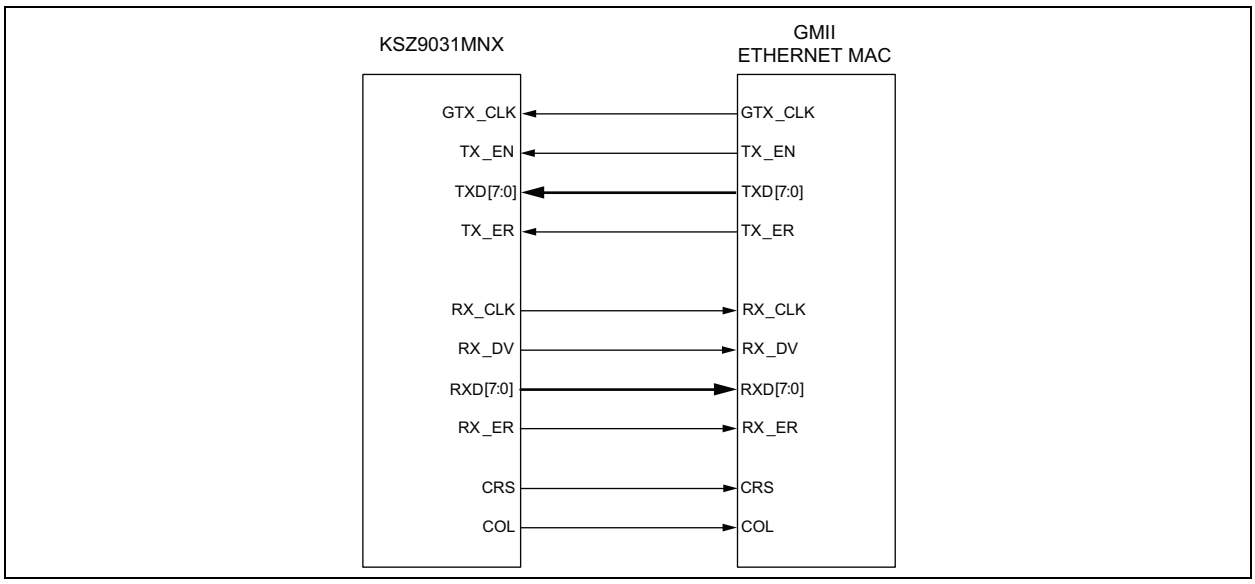
TABLE 3-3: GMII SIGNAL DEFINITION

GMII Signal Name (per spec)	GMII Signal Name (per KSZ9031MNX)	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
GTX_CLK	GTX_CLK	Input	Output	Transmit Reference Clock (125 MHz for 1000 Mbps)
TX_EN	TX_EN	Input	Output	Transmit Enable
TXD[7:0]	TXD[7:0]	Input	Output	Transmit Data[7:0]
TX_ER	TX_ER	Input	Output	Transmit Error
RX_CLK	RX_CLK	Output	Input	Receive Reference Clock (125 MHz for 1000 Mbps)
RX_DV	RX_DV	Output	Input	Receive Data Valid
RXD[7:0]	RXD[7:0]	Output	Input	Receive Data[7:0]
RX_ER	RX_ER	Output	Input	Receive Error
CRS	CRS	Output	Input	Carrier Sense
COL	COL	Output	Input	Collision Detected

3.9.2 GMII SIGNAL DIAGRAM

The KSZ9031MNX GMII pin connections to the MAC are shown in Figure 3-4.

FIGURE 3-4: KSZ9031MNX GMII INTERFACE



3.10 MII Interface

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 16 pins (7 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10 Mbps and 100 Mbps are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4 bits wide, a nibble.

In MII operation, the MII pins function as follows:

- The PHY sources the transmit reference clock, TX_CLK, at 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- The PHY recovers and sources the receive reference clock, RX_CLK, at 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- TX_EN, TXD[3:0], and TX_ER are driven by the MAC and transition synchronously with respect to TX_CLK.
- RX_DV, RXD[3:0], and RX_ER are driven by the KSZ9031MNX and transition synchronously with respect to RX_CLK.
- CRS and COL are driven by the KSZ9031MNX and do not have to transition synchronously with respect to either TX_CLK or RX_CLK.

The KSZ9031MNX combines GMII mode with MII mode to form GMII/MII mode to support data transfer at 10/100/1000 Mbps. After power-up or reset, the KSZ9031MNX is configured to GMII/MII mode if the MODE[3:0] strap-in pins are set to ‘0001’. See the Strapping Options - KSZ9031MNX section.

The KSZ9031MNX has the option to output a 125 MHz reference clock on CLK125_NDO (Pin 55). This clock provides a lower-cost reference clock alternative for GMII/MII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

The KSZ9031MNX provides a dedicated transmit clock output pin (TX_CLK, Pin 57) for MII mode, which is sourced by the KSZ9031MNX for 10/100 Mbps speed.

3.10.1 MII SIGNAL DEFINITION

Table 3-4 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

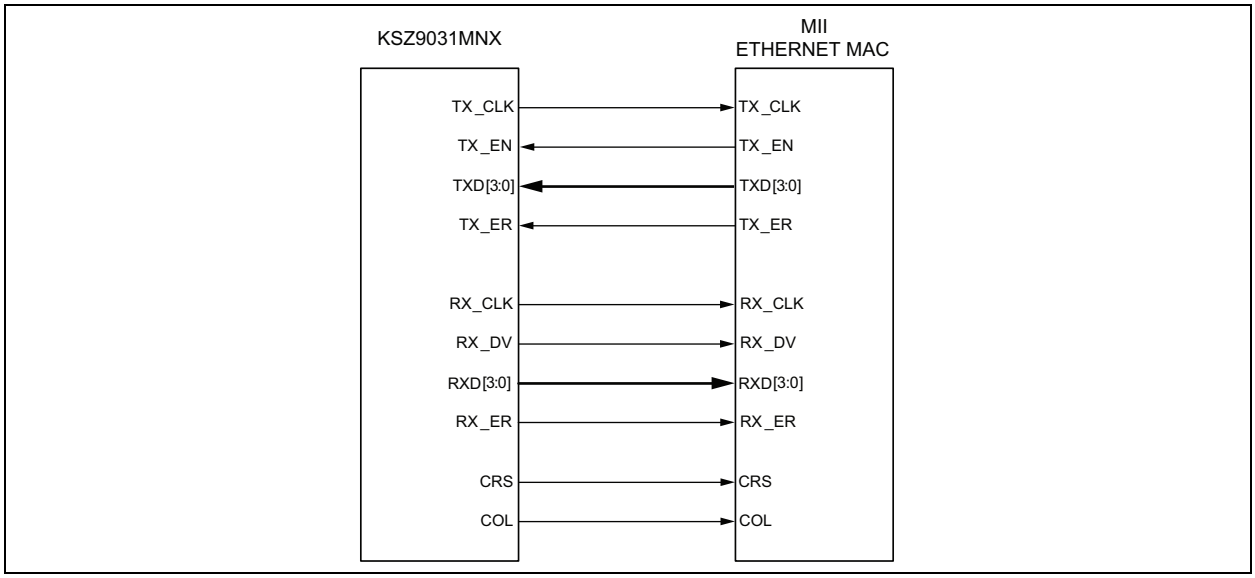
TABLE 3-4: MII SIGNAL DEFINITION

MII Signal Name (per spec)	MII Signal Name (per KSZ9031MNX)	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
TX_CLK	TX_CLK	Output	Input	Transmit Reference Clock (25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
TX_EN	TX_EN	Input	Output	Transmit Enable
TXD[3:0]	TXD[3:0]	Input	Output	Transmit Data[3:0]
TX_ER	TX_ER	Input	Output	Transmit Error
RX_CLK	RX_CLK	Output	Input	Receive Reference Clock (25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
RX_DV	RX_DV	Output	Input	Receive Data Valid
RXD[3:0]	RXD[3:0]	Output	Input	Receive Data[3:0]
RX_ER	RX_ER	Output	Input	Receive Error
CRS	CRS	Output	Input	Carrier Sense
COL	COL	Output	Input	Collision Detection

3.10.2 MII SIGNAL DIAGRAM

The KSZ9031MNX MII pin connections to the MAC are shown in Figure 3-5.

FIGURE 3-5: KSZ9031MNX MII INTERFACE



3.11 MII Management (MIIM) Interface

The KSZ9031MNX supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9031MNX. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows an external controller to communicate with one or more KSZ9031MNX devices. Each KSZ9031MNX device is assigned a unique PHY address between 0h and 7h by the PHYAD[2:0] strapping pins.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers. See the Register Map section.

PHY Address 0h is supported as the unique PHY address only; it is not supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set Register 0h to a value of 0x1940 to set Bit [11] to a value of one to enable software power-down). Instead, separate write commands are used to program each PHY device.

Table 3-5 shows the MII management frame format for the KSZ9031MNX.

TABLE 3-5: MII MANAGEMENT FRAME FORMAT FOR THE KSZ9031MNX

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.12 Interrupt (INT_N)

The INT_N pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9031MNX PHY register. Bits [15:8] of Register 1Bh are the interrupt control bits that enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of Register 1Bh are the interrupt status bits that indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [14] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ9031MNX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

3.13 LED Mode

The KSZ9031MNX provides two programmable LED output pins, LED2 and LED1, which are configurable to support two LED modes. The LED mode is configured by the LED_MODE strap-in (Pin 55). It is latched at power-up/reset and is defined as follows:

- Pull-Up: Single-LED Mode
- Pull-Down: Tri-Color Dual-LED Mode

Each LED output pin can directly drive an LED with a series resistor (typically 220Ω to 470Ω).

3.13.1 SINGLE-LED MODE

In single-LED mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in Table 3-6.

TABLE 3-6: SINGLE-LED MODE - PIN DEFINITION

LED Pin	Pin State	LED Definition	Link/Activity
LED2	H	OFF	Link Off
	L	ON	Link On (any speed)
LED1	H	OFF	No Activity
	Toggle	Blinking	Activity (RX, TX)

3.13.2 TRI-COLOR DUAL-LED MODE

In tri-color dual-LED mode, the link and activity status are indicated by the LED2 pin for 1000BASE-T; by the LED1 pin for 100BASE-TX; and by both LED2 and LED1 pins, working in conjunction, for 10BASE-T. This is summarized in Table 3-7.

TABLE 3-7: TRI-COLOR DUAL-LED MODE - PIN DEFINITION

LED Pin (State)		LED Pin (Definition)		Link/Activity
LED2	LED1	LED2	LED1	
H	H	OFF	OFF	Link Off
L	H	ON	OFF	1000 Link/No Activity
Toggle	H	Blinking	OFF	1000 Link/Activity (RX, TX)
H	L	OFF	ON	100 Link/No Activity
H	Toggle	OFF	Blinking	100 Link/Activity (RX, TX)
L	L	ON	ON	10 Link/No Activity
Toggle	Toggle	Blinking	Blinking	10 Link/Activity (RX, TX)

3.14 Loopback Mode

The KSZ9031MNX supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

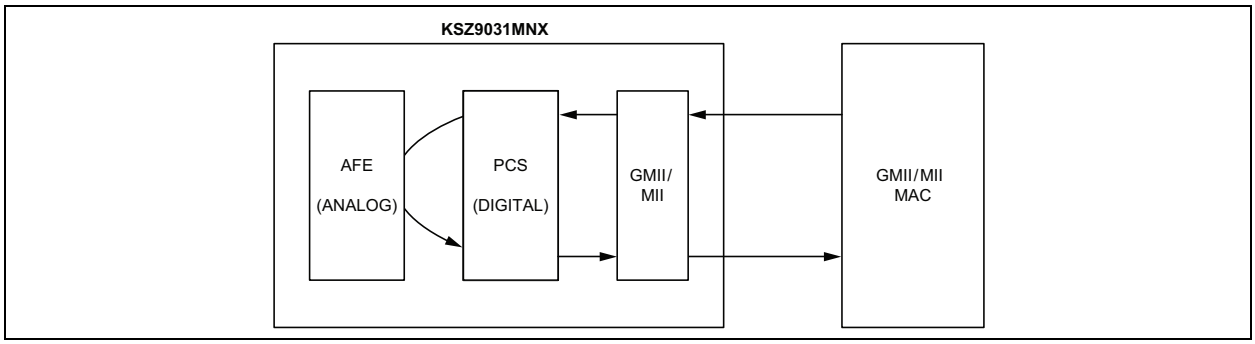
3.14.1 LOCAL (DIGITAL) LOOPBACK

This loopback mode checks the GMII/MII transmit and receive data paths between KSZ9031MNX and external MAC, and is supported for all three speeds (10/100/1000 Mbps) at full-duplex.

The loopback data path is shown in Figure 3-6.

1. GMII/MII MAC transmits frames to KSZ9031MNX.
2. Frames are wrapped around inside KSZ9031MNX.
3. KSZ9031MNX transmits frames back to GMII/MII MAC.

FIGURE 3-6: LOCAL (DIGITAL) LOOPBACK



The following programming steps and register settings are used for local loopback mode.

For 1000 Mbps loopback,

1. Set Register 0h,
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode
2. Set Register 9h,
   - Bit [12] = 1 // Enable master-slave manual configuration
   - Bit [11] = 0 // Select slave configuration (required for loopback mode)

For 10/100 Mbps loopback,

1. Set Register 0h,
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 00 / 01 // Select 10 Mbps/100 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

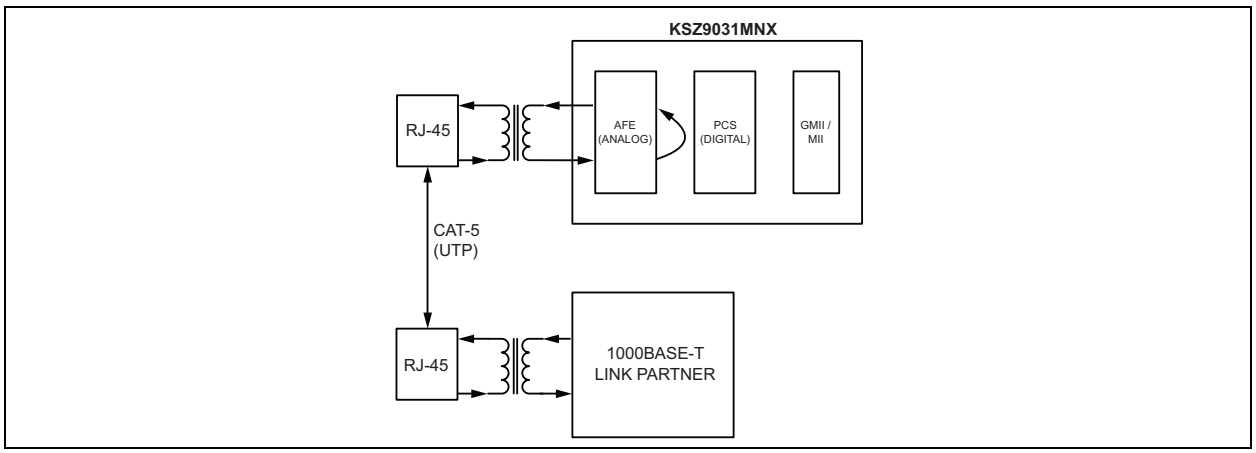
3.14.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between KSZ9031MNX and its link partner, and is supported for 1000BASE-T full-duplex mode only.

The loopback data path is shown in Figure 3-7.

1. The Gigabit PHY link partner transmits frames to KSZ9031MNX.
2. Frames are wrapped around inside KSZ9031MNX.
3. KSZ9031MNX transmits frames back to the Gigabit PHY link partner.

FIGURE 3-7: REMOTE (ANALOG) LOOPBACK



The following programming steps and register settings are used for remote loopback mode.

1. Set Register 0h,
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

   Or just auto-negotiate and link up at 1000BASE-T full-duplex mode with the link partner.
2. Set Register 11h,
   - Bit [8] = 1 // Enable remote loopback mode

3.15 LinkMD® Cable Diagnostic

The LinkMD function uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches.

LinkMD operates by sending a pulse of known amplitude and duration down the selected differential pair, then analyzing the polarity and shape of the reflected signal to determine the type of fault: open circuit for a positive/non-inverted amplitude reflection and short circuit for a negative/inverted amplitude reflection. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing Register 12h, the LinkMD – Cable Diagnostic register, in conjunction with Register 1Ch, the Auto MDI/MDI-X register. The latter register is needed to disable the Auto MDI/MDI-X function before running the LinkMD test. Additionally, a software reset (Reg. 0h, Bit [15] = 1) should be performed before and after running the LinkMD test. The reset helps to ensure the KSZ9031MNX is in the normal operating state before and after the test.

3.16 NAND Tree Support

The KSZ9031MNX provides parametric NAND tree support for fault detection between chip I/Os and board. NAND tree mode is enabled at power-up/reset with the MODE[3:0] strap-in pins set to ‘0100’. Table 3-8 lists the NAND tree pin order.

TABLE 3-8: NAND TREE TEST PIN ORDER FOR KSZ9031MNX

Pin	Description
LED2	Input
LED1/PME_N1	Input
TXD0	Input
TXD1	Input
TXD2	Input
TXD3	Input

TABLE 3-8: NAND TREE TEST PIN ORDER FOR KSZ9031MNX (CONTINUED)

Pin	Description
TX_ER	Input
GTX_CLK	Input
TX_EN	Input
RX_DV	Input
RX_ER	Input
RX_CLK	Input
CRS	Input
COL	Input
INT_/PME_N2	Input
MDC	Input
MDIO	Input
CLK125_NDO	Output

3.17 Power Management

The KSZ9031MNX incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

3.17.1 ENERGY-DETECT POWER-DOWN MODE

Energy-detect power-down (EDPD) mode is used to further reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a one to MMD Address 1Ch, Register 23h, Bit [0], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In EDPD Mode, the KSZ9031MNX shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Power can be reduced further by extending the time interval between the transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the KSZ9031MNX and its link partner, when operating in the same low-power state and with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them. By default, EDPD mode is disabled after power-up.

3.17.2 SOFTWARE POWER-DOWN MODE

This mode is used to power down the KSZ9031MNX device when it is not in use after power-up. Software power-down (SPD) mode is enabled by writing a one to Register 0h, Bit [11]. In the SPD state, the KSZ9031MNX disables all internal functions, except for the MII management interface. The KSZ9031MNX exits the SPD state after a zero is written to Register 0h, Bit [11].

3.17.3 CHIP POWER-DOWN MODE

This mode provides the lowest power state for the KSZ9031MNX device when it is mounted on the board but not in use. Chip power-down (CPD) mode is enabled after power-up/reset with the MODE[3:0] strap-in pins set to ‘0111’. The KSZ9031MNX exits CPD mode after a hardware reset is applied to the RESET_N pin (Pin 56) with the MODE[3:0] strap-in pins set to an operating mode other than CPD.

3.18 Wake-On-LAN

Wake-On-LAN (WOL) is normally a MAC-based function to wake up a host system (for example, an Ethernet end device, such as a PC) that is in standby power mode. Wake-up is triggered by receiving and detecting a special packet (commonly referred to as the “magic packet”) that is sent by the remote link partner. The KSZ9031MNX can perform the same WOL function if the MAC address of its associated MAC device is entered into the KSZ9031MNX PHY registers for magic-packet detection. When the KSZ9031MNX detects the magic packet, it wakes up the host by driving its power management event (PME) output pin low.

By default, the WOL function is disabled. It is enabled by setting the enabling bit and configuring the associated registers for the selected PME wake-up detection method.

The KSZ9031MNX provides three methods to trigger a PME wake-up:

- Magic-packet detection