Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

KSZ9031RNX

Gigabit Ethernet Transceiver with RGMII Support

Features

- Single-Chip 10/100/1000 Mbps Ethernet Transceiver Suitable for IEEE 802.3 Applications
- RGMII Timing Supports On-Chip Delay According to RGMII Version 2.0, with Programming Options for External Delay and Making Adjustments and Corrections to TX and RX Timing Paths
- RGMII with 3.3V/2.5V/1.8V Tolerant I/Os
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100/1000 Mbps) and Duplex (Half/Full)
- On-Chip Termination Resistors for the Differential Pairs
- On-Chip LDO Controller to Support Single 3.3V Supply Operation – Requires Only One External FET to Generate 1.2V for the Core
- Jumbo Frame Support up to 16 KB
- 125 MHz Reference Clock Output
- Energy Detect Power-Down Mode for Reduced Power Consumption When the Cable is Not Attached
- Wake-On-LAN (WOL) Support with Robust Custom-Packet Detection
- AEC-Q100 Grade 3 (KSZ9031RNXUA) and Grade 2 (KSZ9031RNXVA) Qualified for Automotive Applications
- Programmable LED Outputs for Link, Activity, and Speed
- Baseline Wander Correction
- LinkMD TDR-Based Cable Diagnostic to Identify Faulty Copper Cabling
- Parametric NAND Tree Support to Detect Faults Between Chip I/Os and Board
- Loopback Modes for Diagnostics
- Automatic MDI/MDI-X Crossover to Detect and Correct Pair Swap at all Speeds of Operation
- Automatic Detection and Correction of Pair Swaps, Pair Skew, and Pair Polarity
- MDC/MDIO Management Interface for PHY Register Configuration
- Interrupt Pin Option
- Power-Down and Power-Saving Modes
- Operating Voltages
  - Core (DVDDL, AVDDL, AVDDL_PLL): 1.2V (External FET or Regulator)
  - VDD I/O (DVDDH): 3.3V, 2.5V, or 1.8V
  - Transceiver (AVDDH): 3.3V or 2.5V (Commercial Temp.)
- 48-pin QFN (7 mm × 7 mm) Package

Target Applications

- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Gigabit LAN on Motherboard (GLOM)
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-Top Box
- Game Console
- Triple-Play (Data, Voice, Video) Media Center
- Media Converter
- Automotive In-Vehicle Networking

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 Introduction 4
2.0 Pin Description and Configuration 5
3.0 Functional Description 13
4.0 Register Descriptions 31
5.0 Operational Characteristics 52
6.0 Electrical Characteristics 53
7.0 Timing Diagrams 57
8.0 Reset Circuit 63
9.0 Reference Circuits — LED Strap-In Pins 65
10.0 Reference Clock - Connection and Selection 66
11.0 On-Chip LDO Controller - MOSFET Selection 66
12.0 Magnetic - Connection and Selection 67
13.0 Package Outlines 69
Appendix A: Data Sheet Revision History 74
The Microchip Web Site 75
Customer Change Notification Service 75
Customer Support 75
Product Identification System 76

1.0 INTRODUCTION

1.1 General Description

The KSZ9031RNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical-layer transceiver for transmission and reception of data on standard CAT-5 unshielded twisted pair (UTP) cable.

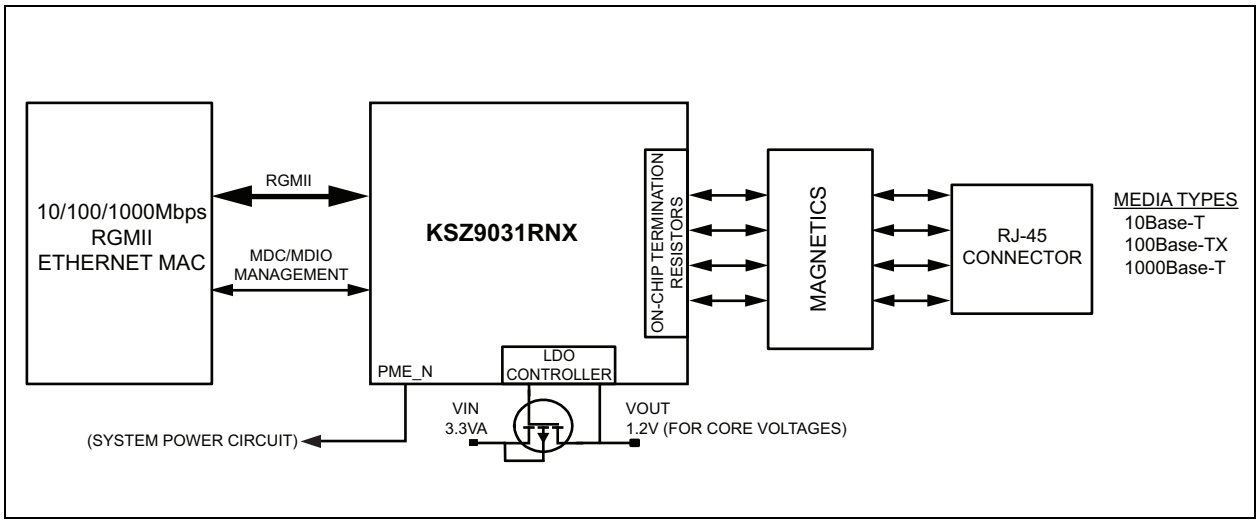
The KSZ9031RNX provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000 Mbps.

The KSZ9031RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

The KSZ9031RNX offers diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9031 I/Os and the board. The LinkMD® TDR-based cable diagnostic identifies faulty copper cabling. Remote and local loopback functions verify analog and digital data paths.

The standard KSZ9031RNX is available in a 48-pin, lead-free QFN package, and the AEC-Q100 automotive qualified parts, KSZ9031RNXUA and KSZ9031RNXVA, are available in a 48-pin lead-free WQFN package.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 48-QFN PIN ASSIGNMENT (TOP VIEW)

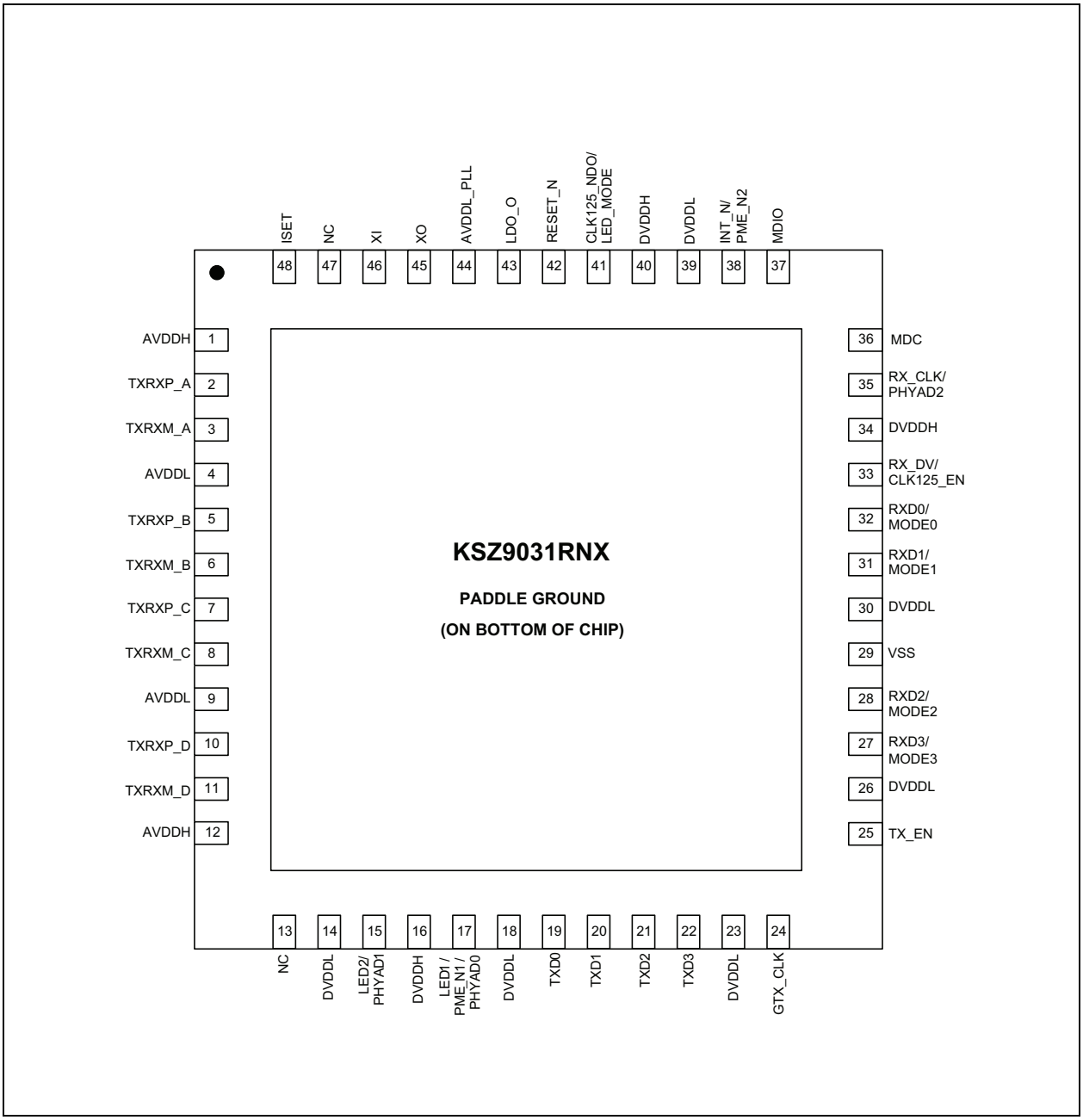


TABLE 2-1: SIGNALS - KSZ9031RNX

Pin Number	Pin Name	Type Note 2-1	Description
1	AVDDH	P	3.3V/2.5V (commercial temp only) analog V_{DD}
2	TXRXP_A	I/O	Media Dependent Interface[0], positive signal of differential pair 1000BASE-T mode: TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively.
3	TXRXM_A	I/O	Media Dependent Interface[0], negative signal of differential pair 1000BASE-T mode: TXRXM_A corresponds to BI_DA– for MDI configuration and BI_DB– for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXM_A is the negative transmit signal (TX–) for MDI configuration and the negative receive signal (RX–) for MDI-X configuration, respectively.
4	AVDDL	P	1.2V analog V_{DD}
5	TXRXP_B	I/O	Media Dependent Interface[1], positive signal of differential pair 1000BASE-T mode: TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively.
6	TXRXM_B	I/O	Media Dependent Interface[1], negative signal of differential pair 1000BASE-T mode: TXRXM_B corresponds to BI_DB– for MDI configuration and BI_DA– for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXM_B is the negative receive signal (RX–) for MDI configuration and the negative transmit signal (TX–) for MDI-X configuration, respectively.
7	TXRXP_C	I/O	Media Dependent Interface[2], positive signal of differential pair 1000BASE-T mode: TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXP_C is not used.
8	TXRXM_C	I/O	Media Dependent Interface[2], negative signal of differential pair 1000BASE-T mode: TXRXM_C corresponds to BI_DC– for MDI configuration and BI_DD– for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXM_C is not used.
9	AVDDL	P	1.2V analog V_{DD}

TABLE 2-1: SIGNALS - KSZ9031RNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
10	TXRXP_D	I/O	Media Dependent Interface[3], positive signal of differential pair 1000BASE-T mode: TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXP_D is not used.
11	TXRXM_D	I/O	Media Dependent Interface[3], negative signal of differential pair 1000BASE-T mode: TXRXM_D corresponds to BI_DD– for MDI configuration and BI_DC– for MDI-X configuration, respectively. 10BASE-T/100BASE-TX mode: TXRXM_D is not used.
12	AVDDH	P	3.3V/2.5V (commercial temp only) analog V_{DD}
13	NC	—	No connect. This pin is not bonded and can be connected to digital ground for footprint compatibility with the KSZ9021RN Gigabit PHY.
14	DVDDL	P	1.2V digital V_{DD}

TABLE 2-1: SIGNALS - KSZ9031RNX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td rowspan="16">15</td><td rowspan="16">LED2/
PHYAD1</td><td rowspan="16">I/O</td><td>LED output: Programmable LED2 output
Config mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up/reset. See the Strap-In Options - KSZ9031RNX section for details. The LED2 pin is programmed by the LED_MODE strapping option (Pin 41), and is defined as follows:
Single-LED Mode</td></tr>
<tr><td><table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>Link Off</td><td>H</td><td>OFF</td></tr>
<tr><td>Link On (any speed)</td><td>L</td><td>ON</td></tr>
</table></td></tr>
<tr><td>Tri-Color Dual-LED Mode</td></tr>
<tr><td><table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link Off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link/No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link/Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link/No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link/Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link/No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link/Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table></td></tr>
<tr><td>For tri-color dual-LED mode, LED2 works in conjunction with LED1 (Pin 17) to indicate 10 Mbps link and activity.</td></tr>
<tr><td>16</td><td>DVDDH</td><td>P</td><td>3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$</td></tr>
</table>

TABLE 2-1: SIGNALS - KSZ9031RNX (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td rowspan="19">17</td><td rowspan="19">LED1/
PHYAD0/
PME_N1</td><td rowspan="19">I/O</td><td>LED1 output: Programmable LED1 output
Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of PHYAD[0]. See the Strap-In Options - KSZ9031RNX section for details.
PME_N output: Programmable PME_N output (pin option 1). This pin function requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0 kΩ to 4.7 kΩ. When asserted low, this pin signals that a WOL event has occurred.
This pin is not an open-drain for all operating modes.
The LED1 pin is programmed by the LED_MODE strapping option (Pin 41), and is defined as follows:</td></tr>
<tr><td>Single-LED Mode</td></tr>
<tr><td>Activity | Pin State | LED Definition
No Activity | H | OFF
Activity (RX, TX) | Toggle | Blinking</td></tr>
<tr><td>Tri-Color Dual-LED Mode</td></tr>
<tr><td>Link/Activity | Pin State | LED Definition
LED2 | LED1 | LED2 | LED1
Link Off | H | H | OFF | OFF
1000 Link/No Activity | L | H | ON | OFF
1000 Link/Activity (RX, TX) | Toggle | H | Blinking | OFF
100 Link/No Activity | H | L | OFF | ON
100 Link/Activity (RX, TX) | H | Toggle | OFF | Blinking
10 Link/No Activity | L | L | ON | ON
10 Link/Activity (RX, TX) | Toggle | Toggle | Blinking | Blinking</td></tr>
<tr><td>For tri-color dual-LED mode, LED1 works in conjunction with LED2 (Pin 15) to indicate 10 Mbps link and activity.</td></tr>
<tr><td>18</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>19</td><td>TXD0</td><td>I</td><td>RGMII mode: RGMII TD0 (Transmit Data 0) input</td></tr>
<tr><td>20</td><td>TXD1</td><td>I</td><td>RGMII mode: RGMII TD1 (Transmit Data 1) input</td></tr>
<tr><td>21</td><td>TXD2</td><td>I</td><td>RGMII mode: RGMII TD2 (Transmit Data 2) input</td></tr>
<tr><td>22</td><td>TXD3</td><td>I</td><td>RGMII mode: RGMII TD3 (Transmit Data 3) input</td></tr>
<tr><td>23</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>24</td><td>GTX_CLK</td><td>I</td><td>RGMII mode: RGMII TXC (Transmit Reference Clock) input</td></tr>
</table>

TABLE 2-1: SIGNALS - KSZ9031RNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
25	TX_EN	I	RGMII mode: RGMII TX_CTL (Transmit Control) input
26	DVDDL	P	1.2V digital V_{DD}
27	RXD3/ MODE3	I/O	RGMII mode: RGMII RD3 (Receive Data 3) output Config mode: The pull-up/pull-down value is latched as MODE3 during power-up/reset. See the Strap-In Options - KSZ9031RNX section for details.
28	RXD2/ MODE2	I/O	RGMII mode: RGMII RD2 (Receive Data 2) output Config mode: The pull-up/pull-down value is latched as MODE2 during power-up/reset. See the Strap-In Options - KSZ9031RNX section for details.
29	VSS	GND	Digital ground
30	DVDDL	P	1.2V digital V_{DD}
31	RXD1/ MODE1	I/O	RGMII mode: RGMII RD1 (Receive Data 1) output Config mode: The pull-up/pull-down value is latched as MODE1 during power-up/reset. See the Strap-In Options - KSZ9031RNX section for details.
32	RXD0/ MODE0	I/O	RGMII mode: RGMII RD0 (Receive Data 0) output Config mode: The pull-up/pull-down value is latched as MODE0 during power-up/reset. See the Strap-In Options - KSZ9031RNX section for details.
33	RX_DV/ CLK125_EN	I/O	RGMII mode: RGMII RX_CTL (Receive Control) output Config mode: Latched as CLK125_NDO Output Enable during power-up/reset. See the Strap-In Options - KSZ9031RNX section for details.
34	DVDDH	P	3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$
35	RX_CLK/ PHYAD2	I/O	RGMII mode: RGMII RXC (Receive Reference Clock) output Config mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up/reset. See the Strap-In Options - KSZ9031RNX section for details.
36	MDC	Ipu	Management data clock input This pin is the input reference clock for MDIO (Pin 37).
37	MDIO	Ipu/O	Management data input/output This pin is synchronous to MDC (Pin 36) and requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0 kΩ to 4.7 kΩ.
38	INT_N/ PME_N2	O	Interrupt output: Programmable interrupt output, with Register 1Bh as the Interrupt Control/Status register, for programming the interrupt conditions and reading the interrupt status. Register 1Fh, Bit [14] sets the interrupt output to active low (default) or active high. PME_N output: Programmable PME_N output (pin option 2). When asserted low, this pin signals that a WOL event has occurred. For Interrupt (when active low) and PME functions, this pin requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0 kΩ to 4.7 kΩ. This pin is not an open-drain for all operating modes.
39	DVDDL	P	1.2V digital V_{DD}
40	DVDDH	P	3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$

TABLE 2-1: SIGNALS - KSZ9031RNX (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
41	CLK125_NDO/ LED_MODE	I/O	125 MHz clock output This pin provides a 125 MHz reference clock output option for use by the MAC. Config mode: The pull-up/pull-down value is latched as LED_MODE during power-up/reset. See the Strap-In Options - KSZ9031RNX section for details.
42	RESET_N	Ipu	Chip reset (active low) Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See the Strap-In Options - KSZ9031RNX section for details.
43	LDO_O	O	On-chip 1.2V LDO controller output This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip's core voltages. If the system provides 1.2V and this pin is not used, it can be left floating.
44	AVDDL_PLL	P	1.2V analog V_{DD} for PLL
45	XO	O	25 MHz crystal feedback This pin is a no connect if an oscillator or external clock source is used.
46	XI	I	Crystal/Oscillator/External Clock input 25 MHz ±50 ppm tolerance
47	NC	—	No connect This pin is not bonded and can be connected to AVDDH power for footprint compatibility with the KSZ9021RN Gigabit PHY.
48	ISET	I/O	Set the transmit output level Connect a 12.1 kΩ 1% resistor to ground on this pin.
Paddle	P_GND	GND	Exposed paddle on bottom of chip Connect P_GND to ground.

Note 2-1 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value).
Ipu/O = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the RGMII signals to be latched to an incorrect configuration. In this case, external pull-up or pull-down resistors should be added on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

TABLE 2-2: STRAP-IN OPTIONS - KSZ9031RNX

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type
Note 2-2</th><th colspan="2">Description</th></tr>
<tr><td>35
15
17</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>I/O
I/O
I/O</td><td colspan="2">The PHY address, PHYAD[2:0], is sampled and latched at power-up/reset and is configurable to any value from 0 to 7. Each PHY address bit is configured as follows:
Pull-up = 1
Pull-down = 0
PHY Address Bits [4:3] are always set to ‘00’.</td></tr>
<tr><td rowspan="18">27
28
31
32</td><td rowspan="18">MODE3
MODE2
MODE1
MODE0</td><td rowspan="18">I/O
I/O
I/O
I/O</td><td colspan="2">The MODE[3:0] strap-in pins are sampled and latched at power-up/reset and are defined as follows:</td></tr>
<tr><td>MODE[3:0]</td><td>Mode</td></tr>
<tr><td>0000</td><td>Reserved - not used</td></tr>
<tr><td>0001</td><td>Reserved - not used</td></tr>
<tr><td>0010</td><td>Reserved - not used</td></tr>
<tr><td>0011</td><td>Reserved - not used</td></tr>
<tr><td>0100</td><td>NAND tree mode</td></tr>
<tr><td>0101</td><td>Reserved - not used</td></tr>
<tr><td>0110</td><td>Reserved - not used</td></tr>
<tr><td>0111</td><td>Chip power-down mode</td></tr>
<tr><td>1000</td><td>Reserved - not used</td></tr>
<tr><td>1001</td><td>Reserved - not used</td></tr>
<tr><td>1010</td><td>Reserved - not used</td></tr>
<tr><td>1011</td><td>Reserved - not used</td></tr>
<tr><td>1100</td><td>RGMII mode - Advertise 1000BASE-T full-duplex only</td></tr>
<tr><td>1101</td><td>RGMII mode - Advertise 1000BASE-T full- and half-duplex only</td></tr>
<tr><td>1110</td><td>RGMII mode - Advertise all capabilities (10/100/1000 speed half-/full-duplex), except 1000BASE-T half-duplex</td></tr>
<tr><td>1111</td><td>RGMII mode - Advertise all capabilities (10/100/1000 speed half-/full-duplex)</td></tr>
<tr><td>33</td><td>CLK125_EN</td><td>I/O</td><td colspan="2">CLK125_EN is sampled and latched at power-up/reset and is defined as follows:
Pull-up (1) = Enable 125 MHz clock output
Pull-down (0) = Disable 125 MHz clock output
Pin 41 (CLK125_NDO) provides the 125 MHz reference clock output option for use by the MAC.</td></tr>
<tr><td>41</td><td>LED_MODE</td><td>I/O</td><td colspan="2">LED_MODE is sampled and latched at power-up/reset and is defined as follows:
Pull-up (1) = Single-LED mode
Pull-down (0) = Tri-color dual-LED mode</td></tr>
</table>

Note 2-2 I/O = Bi-directional.

3.0 FUNCTIONAL DESCRIPTION

The KSZ9031RNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable.

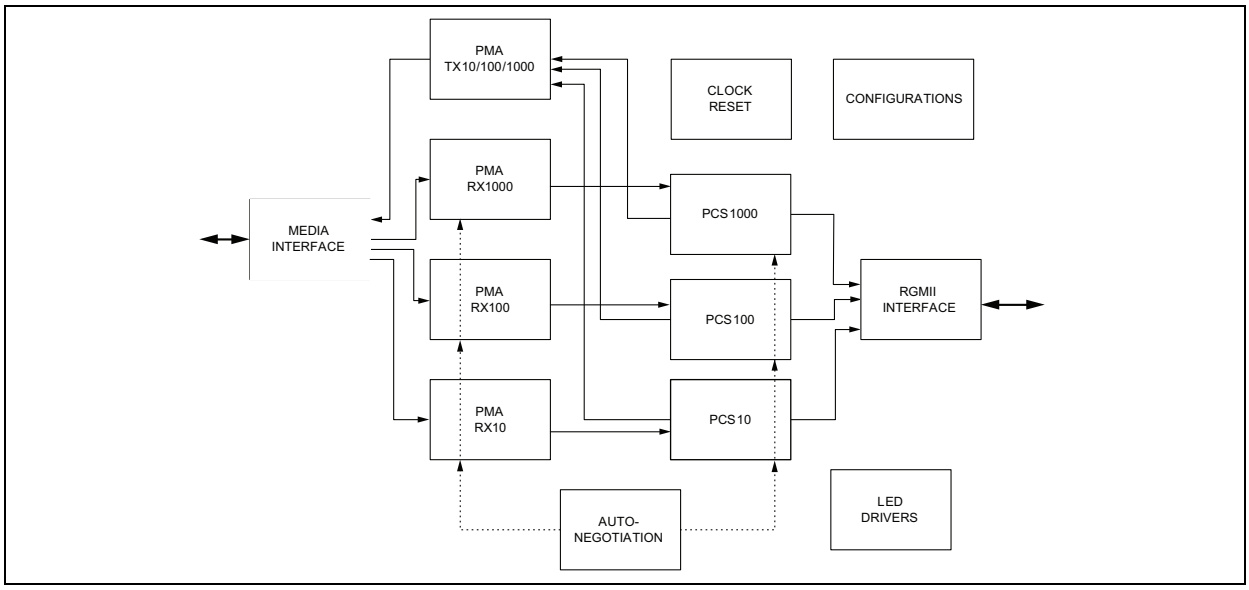
The KSZ9031RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9031RNX can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000BASE-T operation.

The KSZ9031RNX provides the RGMII interface for connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000 Mbps.

Figure 3-1 shows a high-level block diagram of the KSZ9031RNX.

FIGURE 3-1: KSZ9031RNX BLOCK DIAGRAM



3.1 10BASE-T/100BASE-TX Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 12.1 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, and overshoot. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RGMII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled using an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.1.4 10BASE-T TRANSMIT

The 10BASE-T output drivers are incorporated into the 100BASE-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/10BASE-Te signals have harmonic contents that are at least 31 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level-detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9031RNX decodes a data frame. The receiver clock is maintained active during idle periods between receiving data frames.

The KSZ9031RNX removes all 7 bytes of the preamble and presents the received frame starting with the SFD (start of frame delimiter) to the MAC.

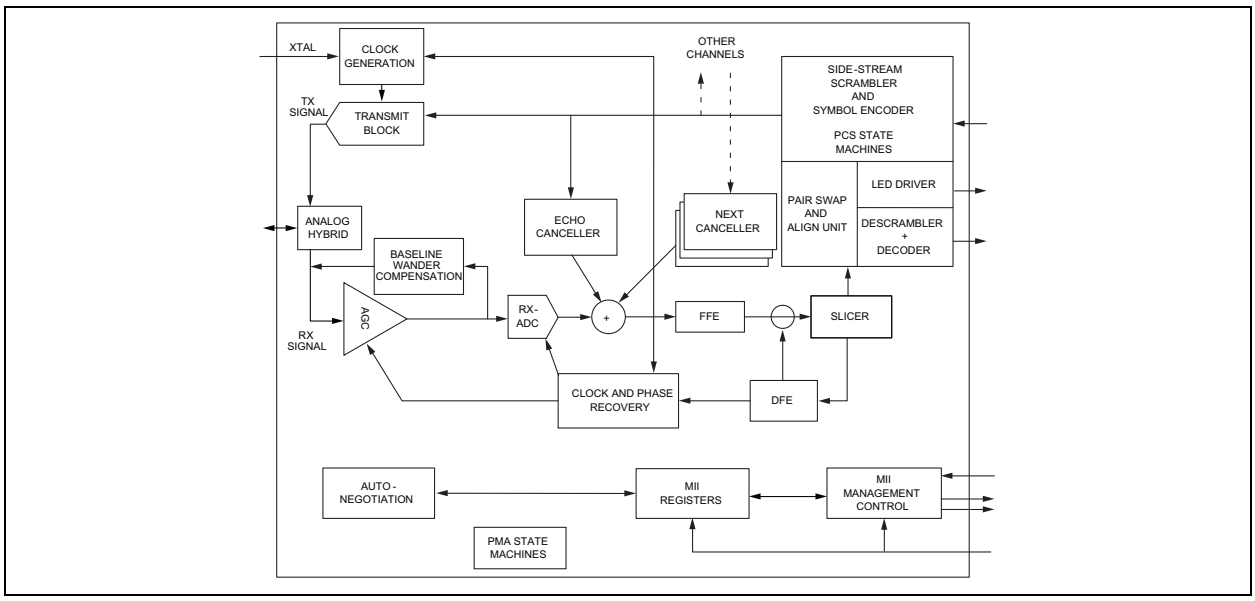
Auto-polarity correction is provided for the receiving differential pair to automatically swap and fix the incorrect +/– polarity wiring in the cabling.

3.2 1000BASE-T Transceiver

The 1000BASE-T transceiver is based-on a mixed-signal/digital-signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancelers, cross-talk cancelers, precision clock recovery scheme, and power-efficient line drivers.

Figure 3-2 shows a high-level block diagram of a single channel of the 1000BASE-T transceiver for one of the four differential pairs.

FIGURE 3-2: KSZ9031RNX 1000BASE-T BLOCK DIAGRAM - SINGLE CHANNEL



3.2.1 ANALOG ECHO-CANCELLATION CIRCUIT

In 1000BASE-T mode, the analog echo-cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

3.2.2 AUTOMATIC GAIN CONTROL (AGC)

In 1000BASE-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

3.2.3 ANALOG-TO-DIGITAL CONVERTER (ADC)

In 1000BASE-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

3.2.4 TIMING RECOVERY CIRCUIT

In 1000BASE-T mode, the mixed-signal clock recovery circuit together with the digital phase-locked loop is used to recover and track the incoming timing information from the received data. The digital phase-locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000BASE-T slave PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000BASE-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

3.2.5 ADAPTIVE EQUALIZER

In 1000BASE-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The KSZ9031RNX uses a digital echo canceler to further reduce echo components on the receive signal.

In 1000BASE-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The KSZ9031RNX uses three NEXT cancelers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10BASE-T/100BASE-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

3.2.6 TRELLIS ENCODER AND DECODER

In 1000BASE-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9031RNX is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order, and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

3.3 Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9031RNX and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the KSZ9031RNX accordingly.

Table 3-1 shows the KSZ9031RNX 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

TABLE 3-1: MDI/MDI-X PIN MAPPING

Pin (RJ-45 Pair)	MDI			MDI-X		
	1000BASE-T	100BASE-T	10BASE-T	1000BASE-T	100BASE-T	10BASE-T
TXRXP/M_A (1, 2)	A+/–	TX+/–	TX+/–	B+/–	RX+/–	RX+/–
TXRXP/M_B (3, 6)	B+/–	RX+/–	RX+/–	A+/–	TX+/–	TX+/–
TXRXP/M_C (4, 5)	C+/–	Not Used	Not Used	D+/–	Not Used	Not Used
TXRXP/M_D (7, 8)	D+/–	Not Used	Not Used	C+/–	Not Used	Not Used

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to Register 1Ch, Bit [6]. MDI and MDI-X mode is set by Register 1Ch, Bit [7] if Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

3.4 Pair-Swap, Alignment, and Polarity Check

In 1000BASE-T mode, the KSZ9031RNX

- Detects incorrect channel order and automatically restores the pair order for the A, B, C, D pairs (four channels).
- Supports 50 ns ±10 ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized.

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

3.5 Wave Shaping, Slew-Rate Control, and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000BASE-T, a special partial-response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-T, pre-emphasis is used to extend the signal quality through the cable.

3.6 PLL Clock Synthesizer

The KSZ9031RNX generates 125 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from the external 25 MHz crystal or reference clock.

3.7 Auto-Negotiation

The KSZ9031RNX conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (unshielded twisted pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the operating mode.

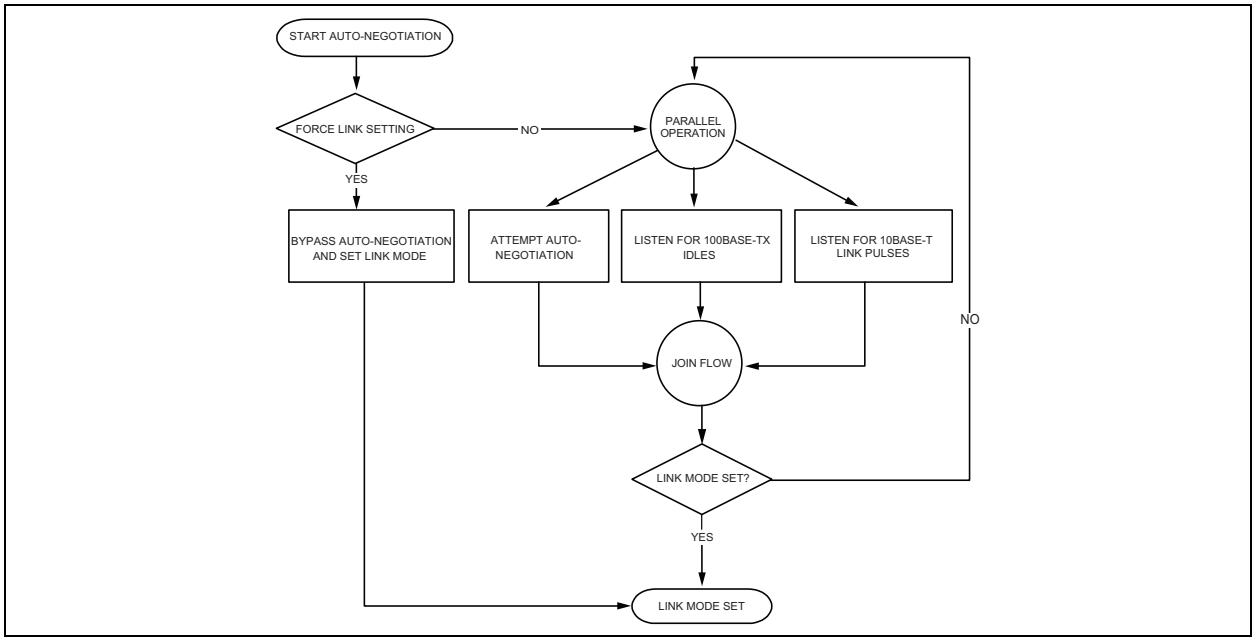
The following list shows the speed and duplex operation mode from highest-to-lowest:

- Priority 1: 1000BASE-T, full-duplex
- Priority 2: 1000BASE-T, half-duplex
- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 100BASE-TX, half-duplex
- Priority 5: 10BASE-T, full-duplex
- Priority 6: 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ9031RNX link partner is forced to bypass auto-negotiation for 10BASE-T and 100BASE-TX modes, the KSZ9031RNX sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9031RNX to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION FLOW CHART



For 1000BASE-T mode, auto-negotiation is required and always used to establish a link. During 1000BASE-T auto-negotiation, the master and slave configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled through Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bits [6, 13] and the duplex is set by Register 0h, Bit [8].

If the speed is changed on the fly, the link goes down and auto-negotiation and parallel detection initiate until a common speed between KSZ9031RNX and its link partner is re-established for a link.

If the link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through Register 0h, Bit [9], or a link-down to link-up transition occurs (that is, disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in Register 1h, Bit [2], and the link partner capabilities are updated in Registers 5h, 6h, 8h, and Ah.

The auto-negotiation finite state machines use interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions is summarized in Table 3-2.

TABLE 3-2: AUTO-NEGOTIATION TIMERS

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst Interval	16 ms
Transmit Pulse Interval	68 µs
FLP Detect Minimum Time	17.2 µs
FLP Detect Maximum Time	185 µs
Receive Minimum Burst Interval	6.8 ms
Receive Maximum Burst Interval	112 ms
Data Detect Minimum Interval	35.4 µs
Data Detect Maximum Interval	95 µs
NLP Test Minimum Interval	4.5 ms
NLP Test Maximum Interval	30 ms
Link Loss Time	52 ms
Break Link Time	1480 ms
Parallel Detection Wait Time	830 ms
Link Enable Wait Time	1000 ms

3.8 10/100 Mbps Speeds Only

Some applications require link-up to be limited to 10/100 Mbps speeds only.

After power-up/reset, the KSZ9031RNX can be restricted to auto-negotiate and link-up to 10/100 Mbps speeds only by programming the following register settings:

1. Set Register 0h, Bit [6] = ‘0’ to remove 1000 Mbps speed.
2. Set Register 9h, Bits [9:8] = ‘00’ to remove Auto-Negotiation advertisements for 1000 Mbps full-/half-duplex.
3. Write a ‘1’ to Register 0h, Bit [9], a self-clearing bit, to force a restart of Auto-Negotiation.

Auto-Negotiation and 10BASE-T/100BASE-TX speeds use only differential pairs A (pins 2, 3) and B (pins 5, 6). Differential pairs C (pins 7, 8) and D (pins 10, 11) can be left as no connects.

3.9 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) supports on-chip data-to-clock delay timing according to the RGMII Version 2.0 Specification, with programming options for external delay timing and to adjust and correct TX and RX timing paths.

RGMII provides a common interface between RGMII PHYs and MACs, and has the following key characteristics:

- Pin count is reduced from 24 pins for the IEEE Gigabit Media Independent Interface (GMII) to 12 pins for RGMII.
- All speeds (10 Mbps, 100 Mbps, and 1000 Mbps) are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each four bits wide, a nibble.

In RGMII operation, the RGMII pins function as follows:

- The MAC sources the transmit reference clock, TXC, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps.
- The PHY recovers and sources the receive reference clock, RXC, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps.
- For 1000BASE-T, the transmit data, TXD[3:0], is presented on both edges of TXC, and the received data, RXD[3:0], is clocked out on both edges of the recovered 125 MHz clock, RXC.
- For 10BASE-T/100BASE-TX, the MAC holds TX_CTL low until both PHY and MAC operate at the same speed.

During the speed transition, the receive clock is stretched on either a positive or negative pulse to ensure that no clock glitch is presented to the MAC.

- TX_ER and RX_ER are combined with TX_EN and RX_DV, respectively, to form TX_CTL and RX_CTL. These two RGMII control signals are valid at the falling clock edge.

After power-up or reset, the KSZ9031RNX is configured to RGMII mode if the MODE[3:0] strap-in pins are set to one of the RGMII mode capability options. See the Strap-In Options - KSZ9031RNX section.

The KSZ9031RNX has the option to output a 125 MHz reference clock on the CLK125_NDO pin. This clock provides a lower-cost reference clock alternative for RGMII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

3.9.1 RGMII SIGNAL DEFINITION

Table 3-3 describes the RGMII signals. Refer to the RGMII Version 2.0 Specification for more detailed information.

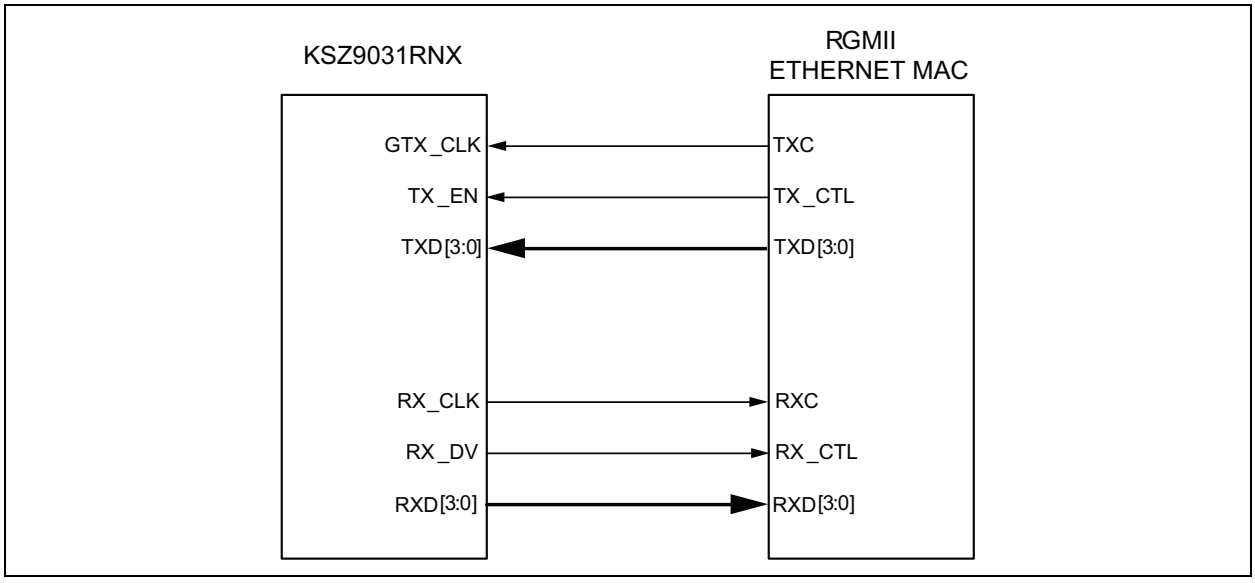
TABLE 3-3: RGMII SIGNAL DEFINITION

RGMII Signal Name (per spec)	RGMII Signal Name (per KSZ9031RNX)	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
TXC	GTX_CLK	Input	Output	Transmit Reference Clock (125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps)
TX_CTL	TX_EN	Input	Output	Transmit Control
TXD[3:0]	TXD[3:0]	Input	Output	Transmit Data[3:0]
RXC	RX_CLK	Output	Input	Receive Reference Clock (125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
RX_CTL	RX_DV	Output	Input	Receive Control
RXD[3:0]	RXD[3:0]	Output	Input	Receive Data[3:0]

3.9.2 RGMII SIGNAL DIAGRAM

The KSZ9031RNX RGMII pin connections to the MAC are shown in Figure 3-4.

FIGURE 3-4: KSZ9031RNX RGMII INTERFACE



3.9.3 RGMII PAD SKEW REGISTERS

Pad skew registers are available for all RGMII pins (clocks, control signals, and data bits) to provide programming options to adjust or correct the timing relationship for each RGMII pin. Because RGMII is a source-synchronous bus interface, the timing relationship needs to be maintained only within the RGMII pin's respective timing group.

- RGMII transmit timing group pins: GTX_CLK, TX_EN, TXD[3:0]
- RGMII receive timing group pins: RX_CLK, RX_DV, RXD[3:0]

Table 3-4 details the four registers located at MMD Address 2h that are provided for pad skew programming.

TABLE 3-4: RGMII PAD SKEW REGISTERS

Address	Name	Description	Mode	Default
MMD Address 2h, Register 4h – RGMII Control Signal Pad Skew				
2.4.15:8	Reserved	Reserved	RW	0000_0000
2.4.7:4	RX_DV Pad Skew	RGMII RX_CTL output pad skew control (0.06 ns/ step)	RW	0111
2.4.3:0	TX_EN Pad Skew	RGMII TX_CTL input pad skew control (0.06 ns/ step)	RW	0111
MMD Address 2h, Register 5h – RGMII RX Data Pad Skew				
2.5.15:12	RXD3 Pad Skew	RGMII RXD3 output pad skew control (0.06 ns/ step)	RW	0111
2.5.11:8	RXD2 Pad Skew	RGMII RXD2 output pad skew control (0.06 ns/ step)	RW	0111
2.5.7:4	RXD1 Pad Skew	RGMII RXD1 output pad skew control (0.06 ns/ step)	RW	0111
2.5.3:0	RXD0 Pad Skew	RGMII RXD0 output pad skew control (0.06 ns/ step)	RW	0111
MMD Address 2h, Register 6h – RGMII TX Data Pad Skew				
2.6.15:12	TXD3 Pad Skew	RGMII TXD3 input pad skew control (0.06 ns/step)	RW	0111
2.6.11:8	TXD2 Pad Skew	RGMII TXD2 input pad skew control (0.06 ns/step)	RW	0111
2.6.7:4	TXD1 Pad Skew	RGMII TXD1 input pad skew control (0.06 ns/step)	RW	0111
2.6.3:0	TXD0 Pad Skew	RGMII TXD0 input pad skew control (0.06 ns/step)	RW	0111
MMD Address 2h, Register 8h – RGMII Clock Pad Skew				
2.8.15:10	Reserved	Reserved	RW	0000_00
2.8.9:5	GTX_CLK Pad Skew	RGMII GTX_CLK input pad skew control (0.06 ns/ step)	RW	01_111
2.8.4:0	RX_CLK Pad Skew	RGMII RX_CLK output pad skew control (0.06 ns/ step)	RW	0_1111

The RGMII control signals and data bits have 4-bit skew settings, while the RGMII clocks have 5-bit skew settings.

Each register bit is approximately a 0.06 ns step change. A single-bit decrement decreases the delay by approximately 0.06 ns, while a single-bit increment increases the delay by approximately 0.06 ns.

Table 3-5 and Table 3-6 list the approximate absolute delay for each pad skew (value) setting.

TABLE 3-5: ABSOLUTE DELAY FOR 5-BIT PAD SKEW SETTING

Pad Skew Value	Delay (ns)
0_0000	–0.90
0_0001	–0.84
0_0010	–0.78
0_0011	–0.72
0_0100	–0.66
0_0101	–0.60
0_0110	–0.54
0_0111	–0.48
0_1000	–0.42
0_1001	–0.36
0_1010	–0.30
0_1011	–0.24
0_1100	–0.18
0_1101	–0.12
0_1110	–0.06
0_1111	No delay adjustment (default value)
1_0000	+0.06
1_0001	+0.12
1_0010	+0.18
1_0011	+0.24
1_0100	+0.30
1_0101	+0.36
1_0110	+0.42
1_0111	+0.48
1_1000	+0.54
1_1001	+0.60
1_1010	+0.66
1_1011	+0.72
1_1100	+0.78
1_1101	+0.84
1_1110	+0.90
1_1111	+0.96

TABLE 3-6: ABSOLUTE DELAY FOR 4-BIT PAD SKEW SETTING

Pad Skew Value	Delay (ns)
0000	–0.42
0001	–0.36
0010	–0.30
0011	–0.24
0100	–0.18
0101	–0.12
0110	–0.06
0111	No delay adjustment (default value)
1000	+0.06
1001	+0.12
1010	+0.18
1011	+0.24
1100	+0.30
1101	+0.36
1110	+0.42
1111	+0.48

When computing the RGMII timing relationships, delays along the entire data path must be aggregated to determine the total delay to be used for comparison between RGMII pins within their respective timing group. For the transmit data path, total delay includes MAC output delay, MAC-to-PHY PCB routing delay, and PHY (KSZ9031RNX) input delay and skew setting (if any). For the receive data path, the total delay includes PHY (KSZ9031RNX) output delay, PHY-to-MAC PCB routing delay, and MAC input delay and skew setting (if any).

As the default, after power-up or reset, the KSZ9031RNX RGMII timing conforms to the timing requirements in the RGMII Version 2.0 Specification for internal PHY chip delay.

For the transmit path (MAC to KSZ9031RNX), the KSZ9031RNX does not add any delay locally at its GTX_CLK, TX_EN and TXD[3:0] input pins, and expects the GTX_CLK delay to be provided on-chip by the MAC. If MAC does not provide any delay or insufficient delay for the GTX_CLK, the KSZ9031RNX has pad skew registers that can provide up to 1.38 ns on-chip delay.

For the receive path (KSZ9031RNX to MAC), the KSZ9031RNX adds 1.2ns typical delay to the RX_CLK output pin with respect to RX_DV and RXD[3:0] output pins. If necessary, the KSZ9031RNX has pad skew registers that can adjust the RX_CLK on-chip delay up to 2.58 ns from the 1.2 ns default delay.

The above default RGMII timings imply:

- RX_CLK clock skew is set by the KSZ9031RNX default register settings.
- GTX_CLK clock skew is provided by the MAC.
- No PCB delay is required for GTX_CLK and RX_CLK clocks.

The following examples show how to read/write to MMD Address 2h, Register 8h for the RGMII GTX_CLK and RX_CLK skew settings. MMD register access is through the direct portal Registers Dh and Eh. For more programming details, refer to the MMD Registers section.

- Read back value of MMD Address 2h, Register 8h.
  - Write Register 0xD = 0x0002 // Select MMD Device Address 2h
  - Write Register 0xE = 0x0008 // Select Register 8h of MMD Device Address 2h
  - Write Register 0xD = 0x4002 // Select register data for MMD Device Address 2h, Register 8h
  - Read Register 0xE // Read value of MMD Device Address 2h, Register 8h

- Write value 0x03FF (delay GTX_CLK and RX_CLK pad skews to their maximum values) to MMD Address 2h, Register 8h
  - Write Register 0xD = 0x0002 // Select MMD Device Address 2h
  - Write Register 0xE = 0x0008 // Select Register 8h of MMD Device Address 2h
  - Write Register 0xD = 0x4002 // Select register data for MMD Device Address 2h, Register 8h
  - Write Register 0xE = 0x03FF // Write value 0x03FF to MMD Device Address 2h, Register 8h

3.9.4 RGMII IN-BAND STATUS

The KSZ9031RNX provides in-band status to the MAC during the inter-frame gap when RX_DV is de-asserted. RGMII in-band status is always enabled after power-up.

The in-band status is sent to the MAC using the RXD[3:0] data pins, and is described in Table 3-7.

TABLE 3-7: RGMII IN-BAND STATUS

RX_DV	RXD3	RXD[2:1]	RXD0
0 (valid only when RX_DV is low)	Duplex Status 0 = Half-duplex 1 = Full-duplex	RX_CLK clock speed 00 = 2.5 MHz (10 Mbps) 01 = 25 MHz (100 Mbps) 10 = 125 MHz (1000 Mbps) 11 = Reserved	Link Status 0 = Link down 1 = Link up

3.10 MII Management (MIIM) Interface

The KSZ9031RNX supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9031RNX. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows an external controller to communicate with one or more KSZ9031RNX devices. Each KSZ9031RNX device is assigned a unique PHY address between 0h and 7h by the PHYAD[2:0] strapping pins.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers. See the Register Map section.

PHY Address 0h is supported as the unique PHY address only; it is not supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set Register 0h to a value of 0x1940 to set Bit [11] to a value of one to enable software power-down). Instead, separate write commands are used to program each PHY device.

Table 3-8 shows the MII management frame format for the KSZ9031RNX.

TABLE 3-8: MII MANAGEMENT FRAME FORMAT FOR THE KSZ9031RNX

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.11 Interrupt (INT_N)

The INT_N pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9031RNX PHY register. Bits [15:8] of Register 1Bh are the interrupt control bits that enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of Register 1Bh are the interrupt status bits that indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [14] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ9031RNX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

3.12 LED Mode

The KSZ9031RNX provides two programmable LED output pins, LED2 and LED1, which are configurable to support two LED modes. The LED mode is configured by the LED_MODE strap-in (Pin 41). It is latched at power-up/reset and is defined as follows:

- Pull-Up: Single-LED Mode
- Pull-Down: Tri-Color Dual-LED Mode

Each LED output pin can directly drive an LED with a series resistor (typically 220Ω to 470Ω).

3.12.1 SINGLE-LED MODE

In single-LED mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in Table 3-9.

TABLE 3-9: SINGLE-LED MODE - PIN DEFINITION

LED Pin	Pin State	LED Definition	Link/Activity
LED2	H	OFF	Link Off
	L	ON	Link On (any speed)
LED1	H	OFF	No Activity
	Toggle	Blinking	Activity (RX, TX)

3.12.2 TRI-COLOR DUAL-LED MODE

In tri-color dual-LED mode, the link and activity status are indicated by the LED2 pin for 1000BASE-T; by the LED1 pin for 100BASE-TX; and by both LED2 and LED1 pins, working in conjunction, for 10BASE-T. This is summarized in Table 3-10.

TABLE 3-10: TRI-COLOR DUAL-LED MODE - PIN DEFINITION

LED Pin (State)		LED Pin (Definition)		Link/Activity
LED2	LED1	LED2	LED1	
H	H	OFF	OFF	Link Off
L	H	ON	OFF	1000 Link/No Activity
Toggle	H	Blinking	OFF	1000 Link/Activity (RX, TX)
H	L	OFF	ON	100 Link/No Activity
H	Toggle	OFF	Blinking	100 Link/Activity (RX, TX)
L	L	ON	ON	10 Link/No Activity
Toggle	Toggle	Blinking	Blinking	10 Link/Activity (RX, TX)

3.13 Loopback Mode

The KSZ9031RNX supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

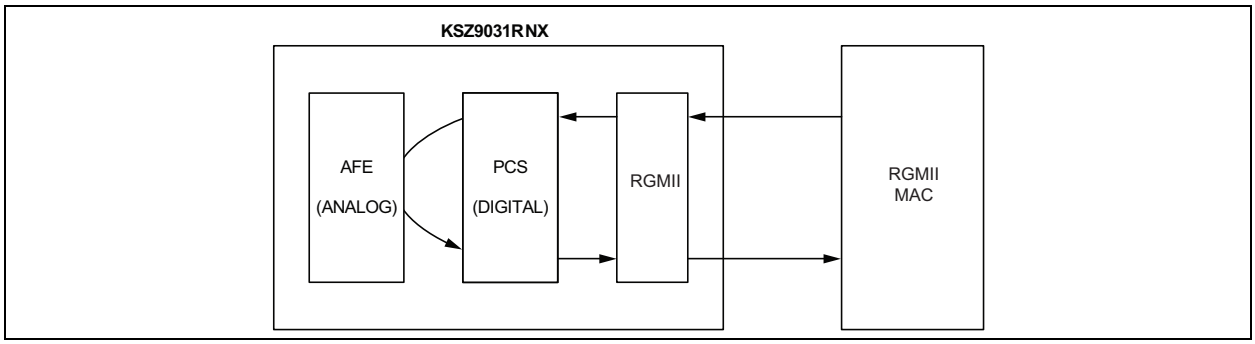
3.13.1 LOCAL (DIGITAL) LOOPBACK

This loopback mode checks the RGMII transmit and receive data paths between KSZ9031RNX and external MAC, and is supported for all three speeds (10/100/1000 Mbps) at full-duplex.

The loopback data path is shown in Figure 3-5.

1. RGMII MAC transmits frames to KSZ9031RNX.
2. Frames are wrapped around inside KSZ9031RNX.
3. KSZ9031RNX transmits frames back to RGMII MAC.

FIGURE 3-5: LOCAL (DIGITAL) LOOPBACK



The following programming steps and register settings are used for local loopback mode.

For 1000 Mbps loopback,

1. Set Register 0h,
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode
2. Set Register 9h,
   - Bit [12] = 1 // Enable master-slave manual configuration
   - Bit [11] = 0 // Select slave configuration (required for loopback mode)

For 10/100 Mbps loopback,

1. Set Register 0h,
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 00 / 01 // Select 10 Mbps/100 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

3.13.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between KSZ9031RNX and its link partner, and is supported for 1000BASE-T full-duplex mode only.

The loopback data path is shown in Figure 3-6.

1. The Gigabit PHY link partner transmits frames to KSZ9031RNX.
2. Frames are wrapped around inside KSZ9031RNX.
3. KSZ9031RNX transmits frames back to the Gigabit PHY link partner.