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7-Port Gigabit Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interfaces

Highlights

- One port with 10/100/1000 Ethernet MAC and SGMII interface
- One port with 10/100/1000 Ethernet MAC and configurable RGMII/MII/RMII interface
- EtherSynch® with full support for IEEE 1588v2 Precision Time Protocol (PTP)
- IEEE 802.1AS/Qav Audio Video Bridging (AVB)
- IEEE 802.1X access control support
- Five ports with integrated 10/100/1000BASE-T PHY transceivers
- Non-blocking wire-speed Ethernet switching fabric
- Full-featured forwarding and filtering control, including Access Control List (ACL) filtering
- Full VLAN and QoS support
- EtherGreen™ power management features, including low power standby
- Flexible management interface options: SPI, I²C, MIIM, and in-band management via any port
- Industrial temperature range support
- 128-pin TQFP-EP (14 x 14mm) RoHS compliant pkg

Target Applications

- Industrial Ethernet (Profinet, MODBUS, Ethernet/IP)
- Real-time Ethernet networks
- IEC 61850 networks w/ power substation automation
- Industrial control/automation switches
- Networked measurement and control systems
- Test and measurement equipment

Features

- Switch Management Capabilities
 - 10/100/1000Mbps Ethernet switch basic functions: frame buffer management, address look-up table, queue management, MIB counters
 - Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 4096 entry forwarding table with 256kByte frame buffer
 - Jumbo packet support up to 9000 bytes
 - Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
 - Rapid spanning tree protocol (RSTP) support for topology management and ring/linear recovery
 - Multiple spanning tree protocol (MSTP) support
- One External MAC Port with SGMII
- One External MAC Port with RGMII/MII/RMII
 - RGMII v2.0, RMII v1.2 with 50MHz reference clock input/output option, MII in PHY/MAC mode

- Five Integrated PHY Ports
 - 1000BASE-T/100BASE-TX/10BASE-Te IEEE 802.3
 - Fast Link-up option significantly reduces link-up time
 - Auto-negotiation and Auto-MDI/MDI-X support
 - On-chip termination resistors and internal biasing for differential pairs to reduce power
 - LinkMD® cable diagnostic capabilities for determining cable opens, shorts, and length
- Advanced Switch Capabilities
 - IEEE 802.1Q VLAN support for 128 active VLAN groups and the full range of 4096 VLAN IDs
 - IEEE 802.1p/Q tag insertion/removal on per port basis
 - VLAN ID on per port or VLAN basis
 - IEEE 802.3x full-duplex flow control and half-duplex back pressure collision control
 - IEEE 802.1X access control (Port-based and MAC address based)
 - IGMP v1/v2/v3 snooping for multicast packet filtering
 - IPv6 multicast listener discovery (MLD) snooping
 - IPv4/IPv6 QoS support, QoS/CoS packet prioritization
 - 802.1p QoS packet classification with 4 priority queues
 - Programmable rate limiting at ingress/egress ports
- IEEE 1588v2 PTP and Clock Synchronization
 - Transparent Clock (TC) with auto correction update
 - Master and slave Ordinary Clock (OC) support
 - End-to-end (E2E) or peer-to-peer (P2P)
 - PTP multicast and unicast message support
 - PTP message transport over IPv4/v6 and IEEE 802.3
 - IEEE 1588v2 PTP packet filtering
 - Synchronous Ethernet support via recovered clock
- Audio Video Bridging (AVB)
 - Compliant with IEEE 802.1BA/AS/Qat/Qav standards
 - Priority queuing, Low latency cut-through mode
 - gPTP time synchronization, credit-based traffic shaper
 - Time aware traffic scheduler per port
- Comprehensive Configuration Registers Access
 - High-speed 4-wire SPI (up to 50MHz), I²C interfaces provide access to all internal registers
 - MII Management (MIIM, MDC/MDIO 2-wire) Interface provides access to all PHY registers
 - In-band management via any of the data ports
 - I/O pin strapping facility to set certain register bits from I/O pins at reset time
- Power Management
 - Energy detect power-down mode on cable disconnect
 - Dynamic clock tree control
 - Unused ports can be individually powered down
 - Full-chip software power-down
 - Wake-on-LAN (WoL) standby power mode with PME interrupt output for system wake upon triggered events

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Table of Contents

1.0 Preface	4
2.0 Introduction	8
3.0 Pin Descriptions and Configuration	9
4.0 Functional Description	18
5.0 Device Registers	63
6.0 Operational Characteristics	203
7.0 Design Guidelines	220
8.0 Package Information	223
Appendix A: Data Sheet Revision History	225
The Microchip Web Site	226
Customer Change Notification Service	226
Customer Support	226
Product Identification System	227

KSZ9567S

1.0 PREFACE

1.1 Glossary of Terms

TABLE 1-1: GENERAL TERMS

Term	Description
10BASE-Te	10 Mbps Ethernet, 2.5V signaling, IEEE 802.3 compliant
100BASE-TX	100 Mbps Fast Ethernet, IEEE 802.3u compliant
1000BASE-T	1000 Mbps Gigabit Ethernet, IEEE 802.3ab compliant
ADC	Analog-to-Digital Converter
AN	Auto-Negotiation
AVB	Audio Video Bridging (IEEE 802.1BA, 802.1AS, 802.1Qat, 802.1Qav)
BLW	Baseline Wander
BPDU	Bridge Protocol Data Unit. Messages which carry the Spanning Tree Protocol information.
Byte	8 bits
CRC	Cyclic Redundancy Check. A common technique for detection data transmission errors. CRC for Ethernet is 32 bits long.
CSR	Control and Status Registers
DA	Destination Address
DWORD	32 bits
FCS	Frame Check Sequence. The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FID	Frame or Filter ID. Specifies the frame identifier. Alternately is the filter identifier.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol. Defined by RFC 1112, RFC 2236, and RFC 4604 to establish multicast group membership in IPv4 networks.
IPG	Inter-Packet Gap. A time delay between successive data packets mandated by the network standard for protocol reasons.
Jumbo Packet	A packet larger than the standard Ethernet packet (1518 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.
lsb	Least Significant Bit
LSB	Least Significant Byte
MAC	Media Access Controller. A functional block responsible for implementing the media access control layer, which is a sublayer of the data link layer.
MDI	Medium Dependent Interface. An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable.
MDIX	Media Independent Interface with Crossover. An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable.
MIB	Management Information Base. The MIB comprises the management portion of network devices. This can include monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII	Media Independent Interface. The MII accesses PHY registers as defined in the IEEE 802.3 specification.

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
MIIM	Media Independent Interface Management
MLD	Multicast Listening Discovery. This protocol is defined by RFC 3810 and RFC 4604 to establish multicast group membership in IPv6 networks.
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit "1" and the logic output remaining at the same level represents a code bit "0".
msb	Most Significant Bit
MSB	Most Significant Byte
NRZ	Non Return to Zero. A type of signal data encoding whereby the signal does not return to a zero state in between bits.
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a "1" and leaves the signal unchanged for a "0"
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
PHY	A device or function block which performs the physical layer interface function in a network.
PLL	Phase Locked Loop. A electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal.
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter. The 8-bit value indicating the end of the preamble of an Ethernet frame.
SQE	Signal Quality Error (also known as "heartbeat")
SSD	Start of Stream Delimiter
TCP	Transmission Control Protocol
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UTP	Unshielded Twisted Pair. Commonly a cable containing 4 twisted pairs of wire.
UUID	Universally Unique IDentifier
VLAN	Virtual Local Area Network
WORD	16 bits

KSZ9567S

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
I	Input
IPU	Input with internal pull-up (58 k Ω \pm 30%)
IPU/O	Input with internal pull-up (58 k Ω \pm 30%) during power-up/reset; output pin during normal operation
IPD	Input with internal pull-down (58 k Ω \pm 30%)
IPD/O	Input with internal pull-down (58 k Ω \pm 30%) during power-up/reset; output pin during normal operation
O8	Output with 8 mA sink and 8 mA source
O24	Output with 24 mA sink and 24 mA source
OPU	Output (8mA) with internal pull-up (58 k Ω \pm 30%)
OPD	Output (8mA) with internal pull-down (58 k Ω \pm 30%)
SGMII-I	SGMII Input
SGMII-O	SGMII Output
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power
GND	Ground

Note: Refer to [Section 6.3, "Electrical Characteristics,"](#) on page 204 for the electrical characteristics of the various buffers.

1.3 Register Nomenclature

TABLE 1-3: REGISTER NOMENCLATURE

Register Bit Type Notation	Register Bit Description
R	Read: A register or bit with this attribute can be read.
W	Write: A register or bit with this attribute can be written.
RO	Read only: Read only. Writes have no effect.
RC	Read to Clear: Contents is cleared after the read. Writes have no effect.
WO	Write only: If a register or bit is write-only, reads will return unspecified data.
WC	Write One to Clear: Writing a one clears the value. Writing a zero has no effect.
LL	Latch Low: Applies to certain RO status bits. If a status condition causes this bit to go low, it will maintain the low state until read, even if the status condition changes. A read clears the latch, allowing the bit to go high if dictated by the status condition.
LH	Latch High: Applies to certain RO status bits. If a status condition causes this bit to go high, it will maintain the high state until read, even if the status condition changes. A read clears the latch, allowing the bit to go low if dictated by the status condition.
SC	Self-Clearing: Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
RESERVED	Reserved Field: Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

1.4 References

- NXP I²C-Bus Specification (UM10204, April 4, 2014): www.nxp.com/documents/user_manual/UM10204.pdf

KSZ9567S

2.0 INTRODUCTION

2.1 General Description

The KSZ9567S is a highly-integrated, IEEE 802.3 compliant networking device that incorporates a layer-2 managed Gigabit Ethernet switch, five 10BASE-T_e/100BASE-TX/1000BASE-T physical layer transceivers (PHYs) and associated MAC units, and two individually configurable MAC ports (one SGMII interface, one RGMII/MII/RMII interface) for direct connection to a host processor/controller, another Ethernet switch, or an Ethernet PHY transceiver. The SGMII port may be connected to a fiber optic transceiver.

The KSZ9567S is built upon industry-leading Ethernet technology, with features designed to offload host processing and streamline the overall design:

- Non-blocking wire-speed Ethernet switch fabric
- Full-featured forwarding and filtering control, including port-based Access Control List (ACL) filtering
- Full VLAN and QoS support
- Traffic prioritization with per-port ingress/egress queues and by traffic classification
- Spanning Tree support
- IEEE 802.1X access control support

As a member of the EtherSynch product family, the KSZ9567S incorporates full hardware support for the IEEE 1588v2 Precision Time Protocol (PTP), including hardware time-stamping at all PHY-MAC interfaces, and a high-resolution hardware “PTP clock”. IEEE 1588 provides sub-microsecond synchronization for a range of industrial Ethernet applications.

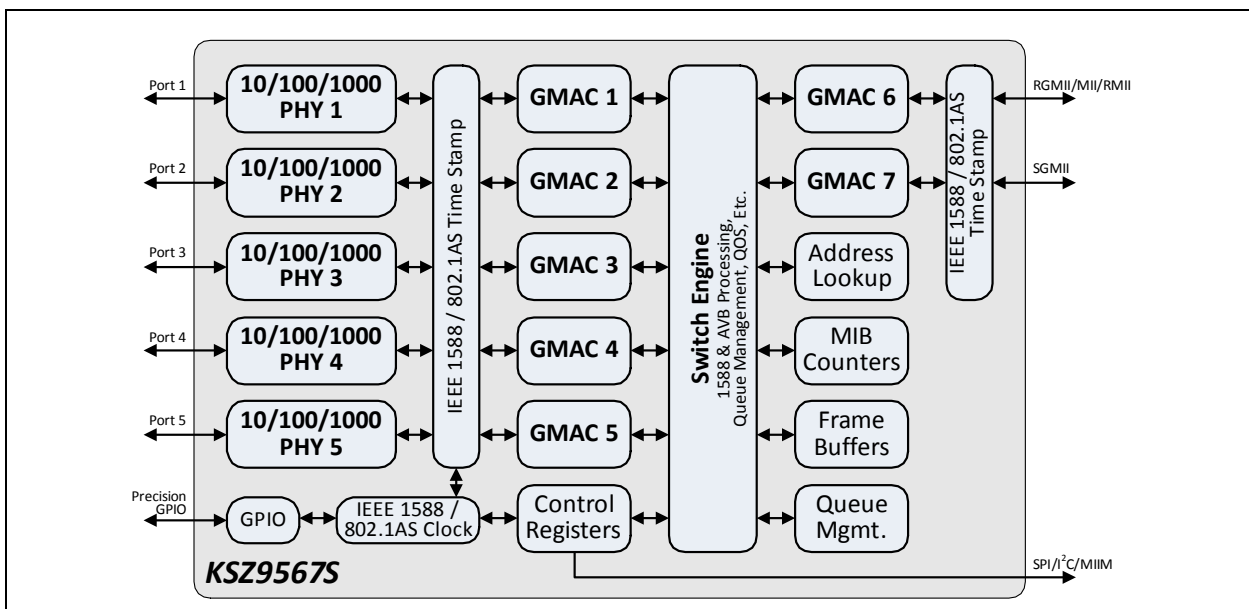
The KSZ9567S fully supports the IEEE family of Audio Video Bridging (AVB) standards, which provides high Quality of Service (QoS) for latency sensitive traffic streams over Ethernet. Time-stamping and time-keeping features support IEEE 802.1AS time synchronization. All ports feature credit based traffic shapers for IEEE 802.1Qav, and a time aware scheduler as proposed for IEEE 802.1Qbv.

A host processor can access all KSZ9567S registers for control over all PHY, MAC, and switch functions. Full register access is available via the integrated SPI or I²C interfaces, and by in-band management via any one of the data ports. PHY register access is provided by a MIIM interface. Flexible digital I/O voltage allows the MAC port to interface directly with a 1.8/2.5/3.3V host processor/controller/FPGA.

Additionally, a robust assortment of power-management features including Wake-on-LAN (WoL) for low power standby operation, have been designed to satisfy energy-efficient system requirements.

The KSZ9567S is available in an industrial (-40°C to +85°C) temperature range. An internal block diagram of the KSZ9567S is shown in [Figure 2-1](#).

FIGURE 2-1: INTERNAL BLOCK DIAGRAM

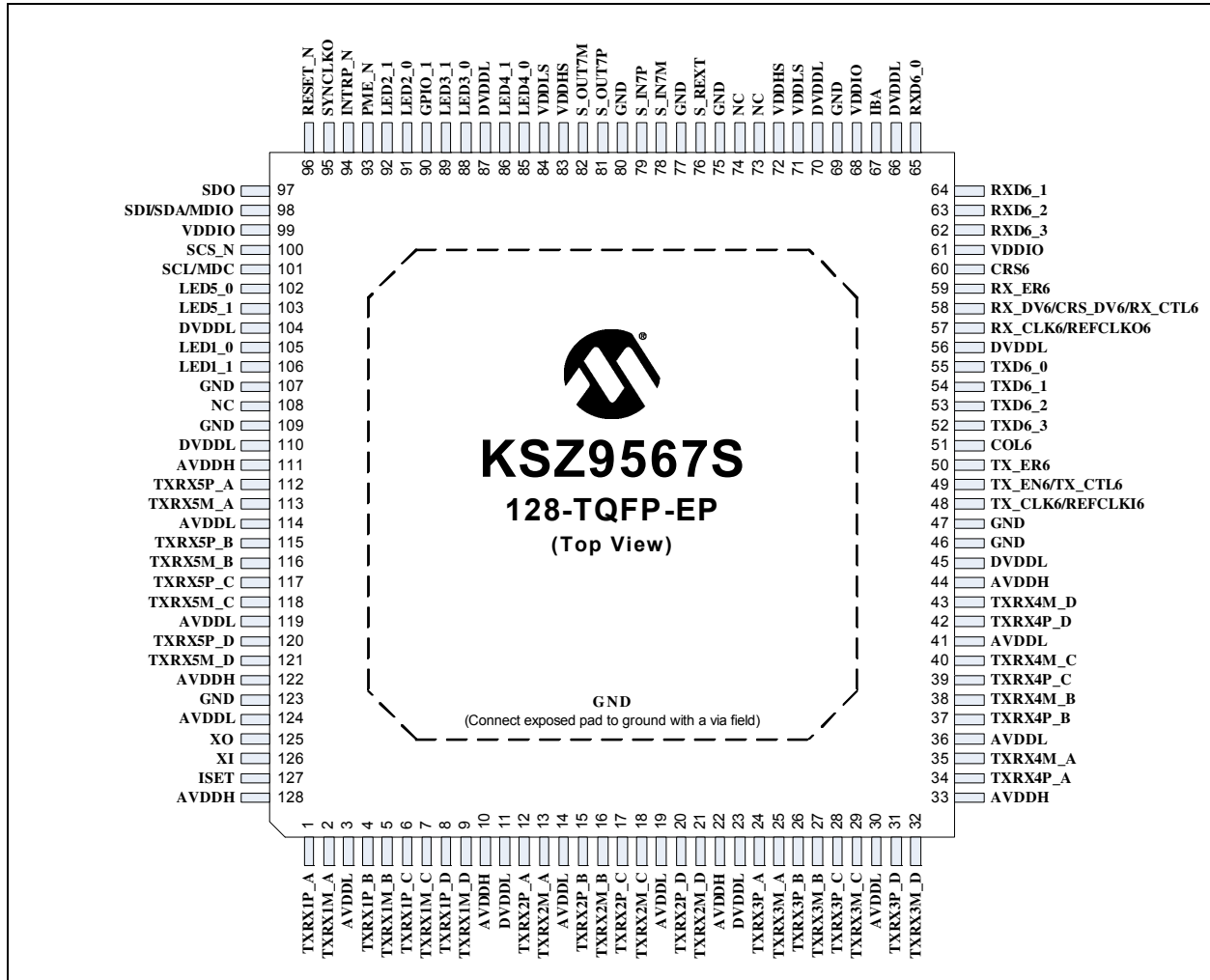


3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

The device pin diagram for the KSZ9567S can be seen in [Figure 3-1](#). [Table 3-1](#) provides a KSZ9567S pin assignment table. Pin descriptions are provided in [Section 3.2, "Pin Descriptions"](#).

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note: When an “_N” is used at the end of the signal name, it indicates that the signal is active low. For example, RESET_N indicates that the reset signal is active low.

The buffer type for each signal is indicated in the “Buffer Type” column of the pin description tables in [Section 3.2, "Pin Descriptions"](#). A description of the buffer types is provided in [Section 1.2, "Buffer Types"](#).

KSZ9567S

TABLE 3-1: PIN ASSIGNMENTS

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	TXRX1P_A	33	AVDDH	65	RXD6_0 (Note 3-1)	97	SDO
2	TXRX1M_A	34	TXRX4P_A	66	DVDDL	98	SDI/SDA/MDIO
3	AVDDL	35	TXRX4M_A	67	IBA (Note 3-1)	99	VDDIO
4	TXRX1P_B	36	AVDDL	68	VDDIO	100	SCS_N
5	TXRX1M_B	37	TXRX4P_B	69	GND	101	SCL/MDC
6	TXRX1P_C	38	TXRX4M_B	70	DVDDL	102	LED5_0
7	TXRX1M_C	39	TXRX4P_C	71	VDDLS	103	LED5_1 (Note 3-1)
8	TXRX1P_D	40	TXRX4M_C	72	VDDHS	104	DVDDL
9	TXRX1M_D	41	AVDDL	73	NC	105	LED1_0
10	AVDDH	42	TXRX4P_D	74	NC	106	LED1_1 (Note 3-1)
11	DVDDL	43	TXRX4M_D	75	GND	107	GND
12	TXRX2P_A	44	AVDDH	76	S_REXT	108	NC
13	TXRX2M_A	45	DVDDL	77	GND	109	GND
14	AVDDL	46	GND	78	S_IN7M	110	DVDDL
15	TXRX2P_B	47	GND	79	S_IN7P	111	AVDDH
16	TXRX2M_B	48	TX_CLK6/REFCLKI6	80	GND	112	TXRX5P_A
17	TXRX2P_C	49	TX_EN6/TX_CTL6	81	S_OUT7P	113	TXRX5M_A
18	TXRX2M_C	50	TX_ER6	82	S_OUT7M	114	AVDDL
19	AVDDL	51	COL6	83	VDDHS	115	TXRX5P_B
20	TXRX2P_D	52	TXD6_3	84	VDDLS	116	TXRX5M_B
21	TXRX2M_D	53	TXD6_2	85	LED4_0 (Note 3-1)	117	TXRX5P_C
22	AVDDH	54	TXD6_1	86	LED4_1 (Note 3-1)	118	TXRX5M_C
23	DVDDL	55	TXD6_0	87	DVDDL	119	AVDDL
24	TXRX3P_A	56	DVDDL	88	LED3_0	120	TXRX5P_D
25	TXRX3M_A	57	RX_CLK6/REFCLKO6	89	LED3_1 (Note 3-1)	121	TXRX5M_D
26	TXRX3P_B	58	RX_DV6/CRS_DV6/ RX_CTL6	90	GPIO_1	122	AVDDH
27	TXRX3M_B	59	RX_ER6	91	LED2_0 (Note 3-1)	123	GND
28	TXRX3P_C	60	CRS6	92	LED2_1 (Note 3-1)	124	AVDDL
29	TXRX3M_C	61	VDDIO	93	PME_N	125	XO
30	AVDDL	62	RXD6_3 (Note 3-1)	94	INTRP_N	126	XI
31	TXRX3P_D	63	RXD6_2 (Note 3-1)	95	SYNCLKO	127	ISSET
32	TXRX3M_D	64	RXD6_1 (Note 3-1)	96	RESET_N	128	AVDDH

Exposed Pad Must be Connected to GND

Note 3-1 This pin provides configuration strap functions during hardware/software resets. Refer to [Section 3.2.1, "Configuration Straps"](#) for additional information.

3.2 Pin Descriptions

This sections details the functions of the various device signals.

TABLE 3-2: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Ports 5-1 Gigabit Ethernet Pins			
Port 5-1 Ethernet TX/RX Pair A +	TXRX[5:1]P_A	AIO	Port 5-1 1000BASE-T Differential Data Pair A (+) Note: 100BASE-TX and 10BASE-Te are also supported on the A and B pairs.
Port 5-1 Ethernet TX/RX Pair A -	TXRX[5:1]M_A	AIO	Port 5-1 1000BASE-T Differential Data Pair A (-) Note: 100BASE-TX and 10BASE-Te are also supported on the A and B pairs.
Port 5-1 Ethernet TX/RX Pair B +	TXRX[5:1]P_B	AIO	Port 5-1 1000BASE-T Differential Data Pair B (+) Note: 100BASE-TX and 10BASE-Te are also supported on the A and B pairs.
Port 5-1 Ethernet TX/RX Pair B -	TXRX[5:1]M_B	AIO	Port 5-1 1000BASE-T Differential Data Pair B (-) Note: 100BASE-TX and 10BASE-Te are also supported on the A and B pairs.
Port 5-1 Ethernet TX/RX Pair C +	TXRX[5:1]P_C	AIO	Port 5-1 1000BASE-T Differential Data Pair C (+)
Port 5-1 Ethernet TX/RX Pair C -	TXRX[5:1]M_C	AIO	Port 5-1 1000BASE-T Differential Data Pair C (-)
Port 5-1 Ethernet TX/RX Pair D +	TXRX[5:1]P_D	AIO	Port 5-1 1000BASE-T Differential Data Pair D (+)
Port 5-1 Ethernet TX/RX Pair D -	TXRX[5:1]M_D	AIO	Port 5-1 1000BASE-T Differential Data Pair D (-)
Port 6 RGMII/MII/RMII Pins			
Port 6 Transmit/Reference Clock	TX_CLK6/ REFCLKI6	I/O8	MII Mode: TX_CLK6 is the Port 6 25/2.5MHz Transmit Clock. In PHY mode this pin is an output, in MAC mode it is an input. RMII Mode: REFCLKI6 is the Port 6 50MHz Reference Clock input when in RMII Normal mode. This pin is unused when in RMII Clock mode. RGMII Mode: TX_CLK6 is the Port 6 125/25/2.5MHz Transmit Clock input.
Port 6 Transmit Enable/Control	TX_EN6/ TX_CTL6	IPD	MII/RMII Modes: TX_EN6 is the Port 6 Transmit Enable. RGMII Mode: TX_CTL6 is the Port 6 Transmit Control.
Port 6 Transmit Error	TX_ER6	IPD	MII Mode: Port 6 Transmit Error input. RMII/RGMII Modes: Not used. Do not connect this pin in these modes of operation.

KSZ9567S

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port 6 Collision Detect	COL6	IPD/O8	MII Mode: Port 6 Collision Detect. In PHY mode this pin is an output, in MAC mode it is an input. RMII/RGMII Modes: Not used. Do not connect this pin in these modes of operation.
Port 6 Transmit Data 3	TXD6_3	IPD	MII/RGMII Modes: Port 6 Transmit Data bus bit 3. RMII Mode: Not used. Do not connect this pin in this mode of operation.
Port 6 Transmit Data 2	TXD6_2	IPD	MII/RGMII Modes: Port 6 Transmit Data bus bit 2. RMII Mode: Not used. Do not connect this pin in this mode of operation.
Port 6 Transmit Data 1	TXD6_1	IPD	MII/RMII/RGMII Modes: Port 6 Transmit Data bus bit 1.
Port 6 Transmit Data 0	TXD6_0	IPD	MII/RMII/RGMII Modes: Port 6 Transmit Data bus bit 0.
Port 6 Receive/Reference Clock	RX_CLK6/ REFCLKO6	I/O24	MII Mode: RX_CLK6 is the Port 6 25/2.5MHz Receive Clock. In PHY mode this pin is an output, in MAC mode it is an input. RMII Mode: REFCLKO6 is the Port 6 50MHz Reference Clock output when in RMII Clock mode. This pin is unused when in RMII Normal mode. RGMII Mode: RX_CLK6 is the Port 6 125/25/2.5MHz Receive Clock output.
Port 6 Receive Data Valid / Carrier Sense / Control	RX_DV6/ CRS_DV6/ RX_CTL6	IPD/O24	MII Mode: RX_DV6 is the Port 6 Received Data Valid output. RMII Mode: CRS_DV6 is the Carrier Sense / Receive Data Valid output. RGMII Mode: RX_CTL6 is the Receive Control output.
Port 6 Receive Error	RX_ER6	IPD/O24	MII Mode: Port 6 Receive Error output. RMII/RGMII Modes: Not used. Do not connect this pin in these modes of operation.
Port 6 Carrier Sense	CRS6	IPD/O8	MII Mode: Port 6 Carrier Sense. In PHY mode this pin is an output, in MAC mode it is an input. RMII/RGMII Modes: Not used. Do not connect this pin in these modes of operation.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port 6 Receive Data 3	RXD6_3	IPD/O24	<p>MII/RGMII Modes: Port 6 Receive Data bus bit 3.</p> <p>RGMII Mode: Not used. Do not connect this pin in this mode of operation.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>
Port 6 Receive Data 2	RXD6_2	IPD/O24	<p>MII/RGMII Modes: Port 6 Receive Data bus bit 2.</p> <p>RGMII Mode: Not used. Do not connect this pin in this mode of operation.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>
Port 6 Receive Data 1	RXD6_1	IPD/O24	<p>MII/RGMII/RGMII Modes: Port 6 Receive Data bus bit 1.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>
Port 6 Receive Data 0	RXD6_0	IPD/O24	<p>MII/RGMII/RGMII Modes: Port 6 Receive Data bus bit 0.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>
Port 7 SGMII Pins			
Port 7 SGMII Differential Input Data +	S_IN7P	SGMII-I	Port 7 SGMII Differential Input Data +
Port 7 SGMII Differential Input Data -	S_IN7M	SGMII-I	Port 7 SGMII Differential Input Data -
Port 7 SGMII Differential Output Data +	S_OUT7P	SGMII-O	Port 7 SGMII Differential Output Data +
Port 7 SGMII Differential Output Data -	S_OUT7M	SGMII-O	Port 7 SGMII Differential Output Data -
Port 7 SGMII Reference Resistor	S_REXT	A	SGMII reference resistor. Connect a 191Ω 1% resistor between this pin and GND using a short trace to avoid noise coupling.
SPI/I²C/MIIM Interface Pins			
SPI/I ² C/MIIM Serial Clock	SCL/MDC	IPU	<p>SPI/I²C Modes: SCL serial clock.</p> <p>MIIM Mode: MDC serial clock.</p>
SPI Data Out	SDO	O8	<p>SPI Mode: Data out (also known as MISO).</p> <p>I²C/MIIM Modes: Not used.</p>

KSZ9567S

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
SPI Data In / I ² C/MIIM Data In/Out	SDI/SDA/MDIO	IPU/O8	<p>SPI Mode: SDI Data In (also known as MOSI).</p> <p>I²C Mode: SDA Data In/Out.</p> <p>MIIM Mode: MDIO Data In/Out.</p> <p>SDI and MDIO are open-drain signals when in the output state. An external pull-up resistor to VDDIO (1.0kΩ to 4.7kΩ) is required.</p>
SPI Chip Select	SCS_N	IPU	<p>SPI Mode: Chip Select (active low).</p> <p>I²C/MIIM Modes: Not used.</p>
LED Pins			
Port 1 LED Indicator 0	LED1_0	IPU/O8	<p>Port 1 LED Indicator 0. Active low output sinks current to light an external LED.</p>
Port 1 LED Indicator 1	LED1_1	IPU/O8	<p>Port 1 LED Indicator 1. Active low output sinks current to light an external LED.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>
Port 2 LED Indicator 0	LED2_0	IPU/O8	<p>Port 2 LED Indicator 0. Active low output sinks current to light an external LED.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>
Port 2 LED Indicator 1	LED2_1	IPU/O8	<p>Port 2 LED Indicator 1. Active low output sinks current to light an external LED.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>
Port 3 LED Indicator 0	LED3_0	IPU/O8	<p>Port 3 LED Indicator 0. Active low output sinks current to light an external LED.</p>
Port 3 LED Indicator 1	LED3_1	IPU/O8	<p>Port 3 LED Indicator 1. Active low output sinks current to light an external LED.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>
Port 4 LED Indicator 0	LED4_0	IPU/O8	<p>Port 4 LED Indicator 0. Active low output sinks current to light an external LED.</p> <p>Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.</p>

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port 4 LED Indicator 1	LED4_1	IPU/O8	Port 4 LED Indicator 1. Active low output sinks current to light an external LED. Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Port 5 LED Indicator 0	LED5_0	IPU/O8	Port 5 LED Indicator 0. Active low output sinks current to light an external LED.
Port 5 LED Indicator 1	LED5_1	IPU/O8	Port 5 LED Indicator 1. Active low output sinks current to light an external LED. Note: This pin also provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
Miscellaneous Pins			
Interrupt	INTRP_N	OPU	Active low, open-drain interrupt. Note: This pin requires an external pull-up resistor.
Power Management Event	PME_N	O8	Power Management Event. This output signal indicates that an energy detect event has occurred. It is intended to wake up the system from a low power mode. Note: The assertion polarity is programmable (default active low). An external pull-up resistor is required for active-low operation; an external pull-down resistor is required for active-high operation.
System Reset	RESET_N	IPU	Active low system reset. The device must be reset either during or after power-on. An RC circuit is suggested for power-on reset.
Crystal Clock / Oscillator Input	XI	ICLK	Crystal clock / oscillator input. When using a 25MHz crystal, this input is connected to one lead of the crystal. When using an oscillator, this pin is the input from the oscillator. The crystal oscillator should have a tolerance of ± 50 ppm.
Crystal Clock Output	XO	OCLK	Crystal clock / oscillator output. When using a 25MHz crystal, this output is connected to one lead of the crystal. When using an oscillator, this pin is left unconnected.
25/125MHz Reference Clock Output	SYNCLKO	IPU/O24	25/125MHz reference clock output, derived from the crystal input or the recovered clock of any PHY. This signal may be used for Synchronous Ethernet.
General Purpose Input/Output 1	GPIO_1	IPU/O8	This signal can be used as an input or output for use by the IEEE 1588 event trigger or timestamp capture units. It will be synchronized to the internal IEEE 1588 clock. This pin can also be controlled (as an output) or sampled (as an input) via device registers.
Transmit Output Current Set Resistor	ISSET	A	Transmit output current set resistor. This pin configures the physical transmit output current. It must be connected to GND through a 6.04k Ω 1% resistor.

KSZ9567S

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
In-Band Management Configuration Strap	IBA	IPD	In-Band Management Configuration strap. This pin provides configuration strap functions during hardware/software resets. Refer to Section 3.2.1, "Configuration Straps" for additional information.
No Connect	NC	-	No Connect. For proper operation, this pin must be left unconnected.
Power/Ground Pins			
+3.3/2.5/1.8V I/O Power	VDDIO	P	+3.3V / +2.5V / +1.8V I/O Power
+2.5V Analog Power	AVDDH	P	+2.5V Analog Power
+1.2V Analog Power	AVDDL	P	+1.2V Analog Power
+1.2V Digital Power	DVDDL	P	+1.2V Digital Power
+1.2V SGMII Core Power	VDDL	P	+1.2V SGMII Core Power
+2.5V SGMII I/O Power	VDDHS	P	+2.5V SGMII I/O Power
Ground	GND	GND	Ground (pins and pad)

3.2.1 CONFIGURATION STRAPS

The KSZ9567S utilizes configuration strap pins to configure the device for different modes. While **RESET_N** is low, these pins are hi-Z. Pull-up/down resistors are used to create high or low states on these pins, which are internally sampled at the rising edge of **RESET_N**. All of these pins have a weak internal pull-up or pull-down resistor which provides a default level for strapping. To strap an LED pin low, use a 750Ω to 1kΩ external pull-down resistor. To strap a non-LED pin high, use an external 1kΩ to 10kΩ pull-up resistor to **VDDIO**. Once **RESET_N** is high, all of these pins become driven outputs.

Because the internal pull-up/down resistors are not strong, consideration must be given to any other pull-up/down resistors which may reside on the board or inside a device connected to these pins.

When an LED pin is directly driving an LED, the effect of the LED and LED load resistor on the strapping level must be considered. This is the reason for using a small value resistor to pull an LED pin low. This is especially true when an LED is powered from a voltage that is higher than **VDDIO**.

The configuration strap pins and their associated functions are detailed in [Table 3-3](#).

TABLE 3-3: CONFIGURATION STRAP DESCRIPTIONS

Configuration Strap Pin	Description
LED1_1	Flow Control (All Ports) 0: Flow control disabled 1: Flow control enabled (Default)
LED2_1	Link-up Mode (All PHYs) 0: Fast Link-up: Auto-negotiation and auto MDI/MDI-X are disabled 1: Normal Link-up: Auto-negotiation and auto MDI/MDI-X are enabled (Default) Note: Since Fast Link-up disables auto-negotiation and auto-crossover, it is suitable only for specialized applications.

TABLE 3-3: CONFIGURATION STRAP DESCRIPTIONS (CONTINUED)

Configuration Strap Pin	Description
LED2_0, LED4_0	<p>When LED2_1 = 1 at strap-in (Normal Link-up): [LED2_0, LED4_0]: Auto-Negotiation Enable (All PHYs) / NAND Tree Test Mode 00: Reserved 01: Auto-negotiation disabled 10: NAND Tree test mode 11: Auto-negotiation enabled (Default)</p> <p>When LED2_1 = 0 at strap-in (Fast Link-up; All PHYs Full-Duplex): LED2_0: 1000BASE-T Master/Slave Mode, 10/100BASE-T MDI/MDI-X Mode (All PHYs) 0: 1000BASE-T: Slave Mode 10/100BASE-T: MDI-X 1: 1000BASE-T: Master Mode (Default) 10/100BASE-T: MDI (Default)</p> <p>LED4_0: PHY Speed Select (All PHYs) 0: 1000BASE-T 1: 100BASE-TX (Default)</p>
LED4_1, LED3_1	<p>[LED4_1, LED3_1]: Management Interface Mode 00: MIIM (MDIO) 01: I²C 1x: SPI (Default)</p>
LED5_1	<p>Switch Enable at Startup 0: Start Switch is disabled. The switch will not forward packets until the Start Switch bit is set in the Switch Operation Register. 1: Start Switch is enabled. The switch will forward packets immediately after reset. (Default)</p>
RXD6_3, RXD6_2	<p>[RXD6_3, RXD6_2]: Port 6 Mode 00: RGMII (Default) 01: RMII 10: Reserved 11: MII</p>
RXD6_1	<p>Port 6 MII/RMII Mode 0: MII: PHY Mode (Default) RMII: Clock Mode. RMII 50MHz reference clock is output on REFCLKO6. (Default) RGMII: No effect 1: MII: MAC Mode RMII: Normal Mode. RMII 50MHz reference clock is input on REFCLKI6. RGMII: No effect</p>
RXD6_0	<p>Port 6 Speed Select 0: 1000Mbps Mode (Default) 1: 10/100Mbps Mode</p> <p>Note: If Port 6 is configured for MII or RMII, set the speed to 100Mbps.</p>
IBA	<p>In-Band Management 0: Disable In-Band Management (Default) 1: Enable In-Band Management</p>

KSZ9567S

4.0 FUNCTIONAL DESCRIPTION

This section provides functional descriptions for the following:

- [Physical Layer Transceiver \(PHY\)](#)
- [LEDs](#)
- [Media Access Controller \(MAC\)](#)
- [Switch](#)
- [IEEE 1588 Precision Time Protocol](#)
- [Audio Video Bridging and Time Sensitive Networks](#)
- [NAND Tree Support](#)
- [Clocking](#)
- [Power](#)
- [Power Management](#)
- [Management Interface](#)
- [In-Band Management](#)
- [MAC Interface \(Ports 6 and 7\)](#)

4.1 Physical Layer Transceiver (PHY)

Ports 1 through 5 include completely integrated triple-speed (10BASE-T_e, 100BASE-TX, 1000BASE-T) Ethernet physical layer transceivers for transmission and reception of data over standard four-pair unshielded twisted pair (UTP), CAT-5 or better Ethernet cable.

The device reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs, eliminating the need for external termination resistors. The internal chip termination and biasing provides significant power savings when compared with using external biasing and termination resistors.

The device can automatically detect and correct for differential pair misplacements and polarity reversals, and correct for propagation delay differences between the four differential pairs, as specified in the IEEE 802.3 standard for 1000BASE-T operation.

4.1.1 1000BASE-T TRANSCEIVER

The 1000BASE-T transceiver is based on a mixed-signal/digital signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancelers, cross-talk cancelers, a precision clock recovery scheme, and power-efficient line drivers.

4.1.1.1 Analog Echo Cancellation Circuit

In 1000BASE-T mode, the analog echo cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer. This circuit is disabled in 10BASE-T_e/100BASE-TX mode.

4.1.1.2 Automatic Gain Control (AGC)

In 1000BASE-T mode, the automatic gain control circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

4.1.1.3 Analog-to-Digital Converter (ADC)

In 1000BASE-T mode, the analog-to-digital converter digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver. This circuit is disabled in 10BASE-T_e/100BASE-TX mode.

4.1.1.4 Timing Recovery Circuit

In 1000BASE-T mode, the mixed signal clock recovery circuit, together with the digital phase locked loop (PLL), is used to recover and track the incoming timing information from the received data. The digital PLL has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000BASE-T slave PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000BASE-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

4.1.1.5 Adaptive Equalizer

In 1000BASE-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The device uses a digital echo canceler to further reduce echo components on the receive signal.

In 1000BASE-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The device uses three NEXT cancelers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10BASE-Te/100BASE-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

4.1.1.6 Trellis Encoder and Decoder

In 1000BASE-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

4.1.2 100BASE-TX TRANSCEIVER

4.1.2.1 100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external ISET resistor sets the output current for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-Te output driver is also incorporated into the 100BASE-TX driver.

4.1.2.2 100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

4.1.2.3 Scrambler/De-Scrambler

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. The scrambler is used only for 100BASE-TX.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

KSZ9567S

4.1.3 10BASE-Te TRANSCEIVER

10BASE-Te is an energy-efficient version of 10BASE-T which is powered from a 2.5V supply. It has a reduced transmit signal amplitude and requires Cat5 cable. It is inter-operable to 100m with 10BASE-T when Cat5 cable is used.

4.1.3.1 10BASE-Te Transmit

The 10BASE-Te driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with typical 1.75V amplitude (compared to the typical transmit amplitude of 2.5V for 10BASE-T). The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

4.1.3.2 10BASE-Te Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP1 or RXM1 input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the device decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

4.1.4 AUTO MDI/MDI-X

The automatic MDI/MDI-X feature, also known as auto crossover, eliminates the need to determine whether to use a straight cable or a crossover cable between the device and its link partner. The auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the device accordingly. [Table 4-1](#) shows the device's 10/100/1000 Mbps pin configuration assignments for MDI and MDI-X pin mapping.

TABLE 4-1: MDI/MDI-X PIN DEFINITIONS

Pin (RJ45 pair)	MDI			MDI-X		
	1000BASE-T	100BASE-TX	10BASE-Te	1000BASE-T	100BASE-TX	10BASE-Te
TXRXxP/M_A (1,2)	A+/-	TX+/-	TX+/-	B+/-	RX+/-	RX+/-
TXRXxP/M_B (3,6)	B+/-	RX+/-	RX+/-	A+/-	TX+/-	TX+/-
TXRXxP/M_C (4,5)	C+/-	Not used	Not used	D+/-	Not used	Not used
TXRXxP/M_D (7,8)	D+/-	Not used	Not used	C+/-	Not used	Not used

Auto MDI/MDI-X is enabled by default. It can be disabled through the port control registers. If Auto MDI/MDI-X is disabled, the port control register can also be used to select between MDI and MDI-X settings.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

4.1.5 PAIR-SWAP, ALIGNMENT, AND POLARITY CHECK

In 1000BASE-T mode, the device:

- Detects incorrect channel order and automatically restores the pair order for the A, B, C, D pairs (four channels).
- Supports 50±10ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized.

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

4.1.6 WAVE SHAPING, SLEW-RATE CONTROL, AND PARTIAL RESPONSE

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000BASE-T, a special partial-response signaling method is used to provide the bandwidth-limiting feature for the transmission path.
- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-Te, pre-emphasis is used to extend the signal quality through the cable.

4.1.7 AUTO-NEGOTIATION

The device conforms to the auto-negotiation protocol as described by IEEE 802.3. Auto-negotiation allows each port to operate at either 10BASE-Te, 100BASE-TX or 1000BASE-T by allowing link partners to select the best common mode of operation. During auto-negotiation, the link partners advertise capabilities across the link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

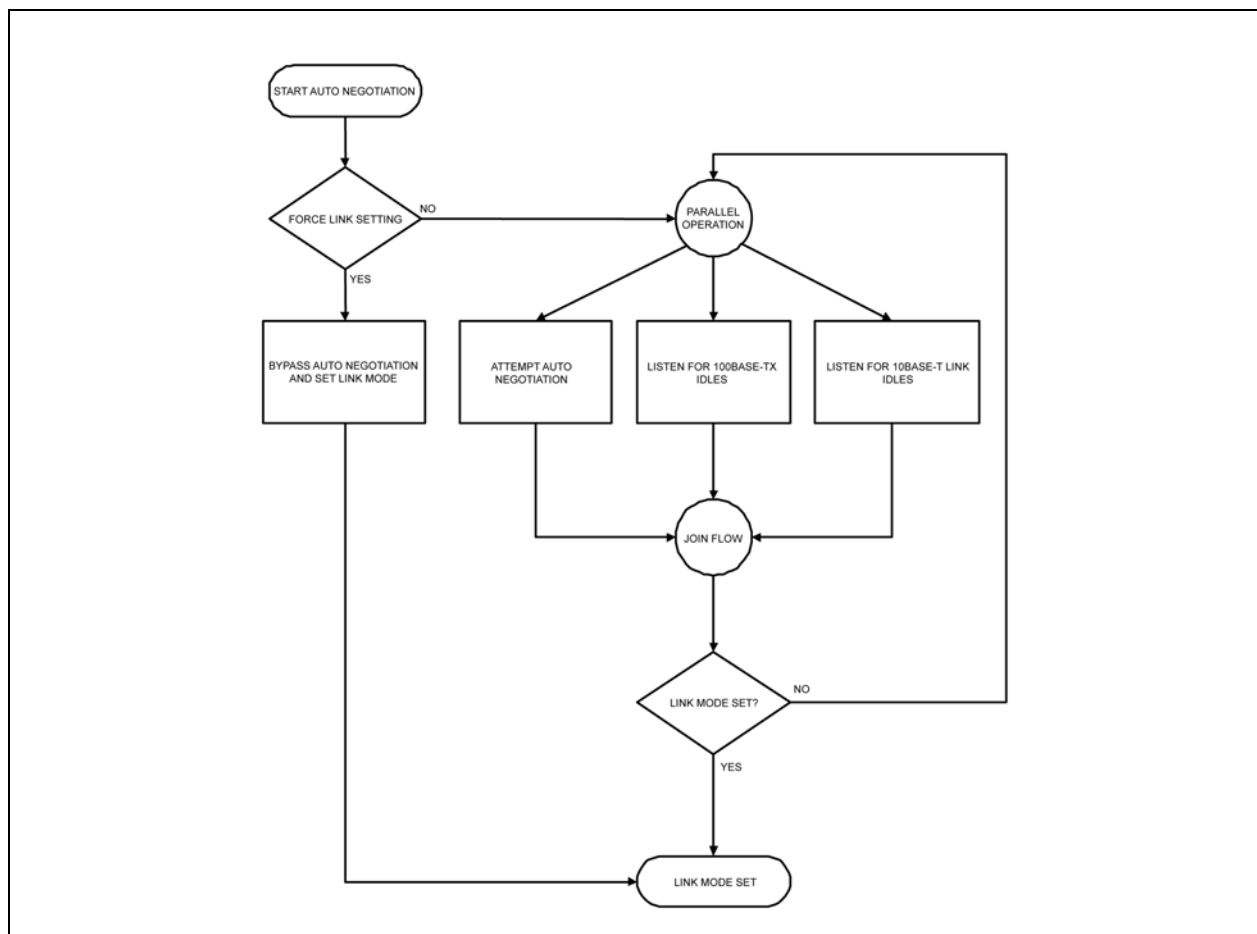
The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 1000BASE-T, full-duplex
- Priority 2: 1000BASE-T, half-duplex
- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 100BASE-TX, half-duplex
- Priority 5: 10BASE-Te, full-duplex
- Priority 6: 10BASE-Te, half-duplex

If the KSZ9567S link partner doesn't support auto-negotiation or is forced to bypass auto-negotiation for 10BASE-Te and 100BASE-TX modes, the KSZ9567S port sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ9567S to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in [Figure 4-1](#).

FIGURE 4-1: AUTO-NEGOTIATION AND PARALLEL OPERATION



For 1000BASE-T mode, auto-negotiation is always required to establish a link. During 1000BASE-T auto-negotiation, the master and slave configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

KSZ9567S

Auto-negotiation is enabled by default after power-up or hardware reset. Afterwards, auto-negotiation can be enabled or disabled via bit 12 of the [PHY Basic Control Register](#). If auto-negotiation is disabled, the speed is set by bits 6 and 13 of the [PHY Basic Control Register](#), and the duplex is set by bit 8.

If the speed is changed on the fly, the link goes down and either auto-negotiation or parallel detection initiate until a common speed between the KSZ9567S and its link partner is re-established for a link.

If link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through bit 9 of the [PHY Basic Control Register](#), or a link-down to link-up transition occurs (i.e. disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in the [PHY Basic Status Register](#), and the link partner capabilities are updated in the [PHY Auto-Negotiation Link Partner Ability Register](#), [PHY Auto-Negotiation Expansion Status Register](#), and [PHY 100BASE-T Status Register](#).

4.1.8 FAST LINK-UP

Link up time is normally determined by the time it takes to complete auto-negotiation. Additional time may be added by the auto MDI/MDI-X feature. The total link up time from power-up or cable connect is typically a second or more.

Fast Link-up mode significantly reduces 100BASE-TX link-up time by disabling both auto-negotiation and auto MDI/MDI-X, and fixing the TX and RX channels. This mode is enabled or disabled by the **LED2_1** strapping option. It is not set by registers, so fast link-up is available immediately upon power-up. Fast Link-up is available at power-up only for 100BASE-TX link speed, which is selected by strapping the **LED4_0** pin high. Fast Link-up is also available for 10BASE-T, but this link speed must first be selected via a register write.

Fast Link-up is intended for specialized applications where both link partners are known in advance. The link must also be known so that the fixed transmit channel of one device connects to the fixed receive channel of the other device, and vice versa. The TX and RX channel assignments are determined by the MDI/MDI-X strapping option on **LED2_0**.

If a device in Fast Link-up mode is connected to a normal device (auto-negotiate and auto-MDI/MDI-X), there will be no problems linking, but the speed advantage of Fast Link-up will not be realized.

For more information on configuration straps, refer to [Section 3.2.1, "Configuration Straps," on page 16](#).

4.1.9 LinkMD® CABLE DIAGNOSTICS

The LinkMD® function utilizes Time Domain Reflectometry (TDR) to analyze the cabling for common cabling problems, such as open circuits, short circuits and impedance mismatches.

LinkMD® works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, and then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD® function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

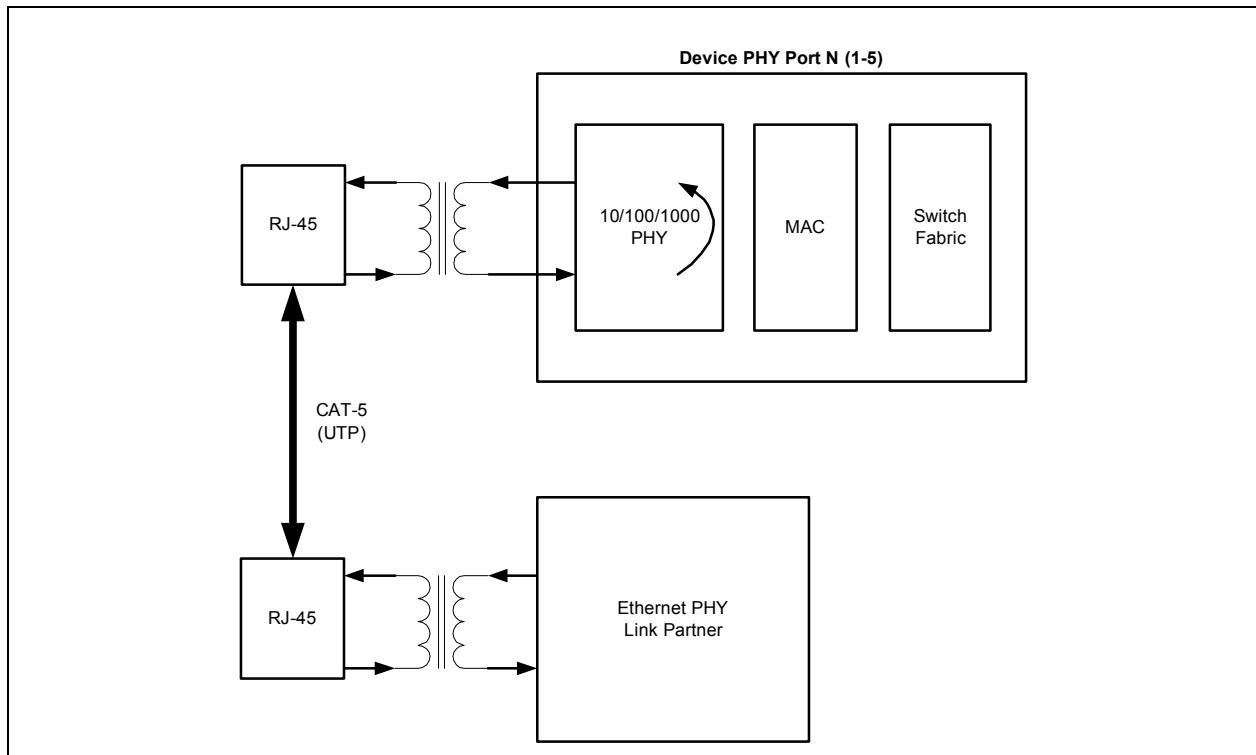
4.1.10 REMOTE PHY LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ9567S and its Ethernet PHY link partner, and is supported for 10/100/1000 Mbps at full-duplex.

The loopback data path is shown in [Figure 4-2](#) and functions as follows:

- The Ethernet PHY link partner transmits data to the KSZ9567S PHY port.
- Data received at the external pins of the PHY port is looped back without passing through the MAC and internal switch fabric.
- The same KSZ9567S PHY port transmits data back to the Ethernet PHY link partner.

FIGURE 4-2: REMOTE PHY LOOPBACK



The following programming steps and register settings are for remote PHY loopback mode for 1000BASE-T Master Mode, 1000BASE-T Slave Mode, 100BASE-TX Mode, and 10BASE-T Mode.

- 1000BASE-T Master Mode
 - Set Port N (1-5), [PHY 1000BASE-T Control Register](#) = 0x1F00
 - Set Port N (1-5), [PHY Remote Loopback Register](#) = 0x01F0
 - Set Port N (1-5), [PHY Basic Control Register](#) = 0x1340

- 1000BASE-T Slave Mode
 - Set Port N (1-5), [PHY 1000BASE-T Control Register](#) = 0x1300
 - Set Port N (1-5), [PHY Remote Loopback Register](#) = 0x01F0
 - Set Port N (1-5), [PHY Basic Control Register](#) = 0x1340

- 100BASE-TX Mode
 - Set Port N (1-5), [PHY Auto-Negotiation Advertisement Register](#) = 0x0181
 - Set Port N (1-5), [PHY 1000BASE-T Control Register](#) = 0x0C00
 - Set Port N (1-5), [PHY Remote Loopback Register](#) = 0x01F0
 - Set Port N (1-5), [PHY Basic Control Register](#) = 0x3300

- 10BASE-T Mode
 - Set Port N (1-5), [PHY Auto-Negotiation Advertisement Register](#) = 0x0061
 - Set Port N (1-5), [PHY 1000BASE-T Control Register](#) = 0x0C00
 - Set Port N (1-5), [PHY Remote Loopback Register](#) = 0x01F0
 - Set Port N (1-5), [PHY Basic Control Register](#) = 0x3300

KSZ9567S

4.2 LEDs

Each PHY port has two programmable LED output pins, **LEDx_0** and **LEDx_1**, to indicate the PHY link and activity status. Two different LED modes are available. The LED mode can be changed individually for each PHY port by writing to the PHY Mode bit in the PHY indirect register: MMD 2, address 0, bit 4:

- 1 = [Single-LED Mode](#)
- 0 = [Tri-Color Dual-LED Mode](#) (Default)

Each LED output pin can directly drive an LED with a series resistor (typically 220Ω to 470Ω). LED outputs are active-low.

4.2.1 SINGLE-LED MODE

In single-LED mode, the **LEDx_1** pin indicates the link status while the **LEDx_0** pin indicates the activity status, as shown in [Figure 4-2](#).

TABLE 4-2: SINGLE-LED MODE PIN DEFINITION

LED Pin	Pin State	Pin LED Definition	Link/Activity
LEDx_1	H	OFF	Link Off
	L	ON	Link On (any speed)
LEDx_0	H	OFF	No Activity
	Toggle	Blinking	Activity (RX,TX)

4.2.2 TRI-COLOR DUAL-LED MODE

In tri-color dual-LED mode, the link and activity status are indicated by the **LEDx_1** pin for 1000BASE-T; by the **LEDx_0** pin for 100BASE-TX; and by both **LEDx_1** and **LEDx_0** pins, working in conjunction, for 10BASE-T. This behavior is summarized in [Figure 4-3](#).

TABLE 4-3: TRI-COLOR DUAL-LED MODE PIN DEFINITION

LED Pin (State)		LED Pin (Definition)		Link/Activity
LEDx_1	LEDx_0	LEDx_1	LEDx_0	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000Mbps Link / No Activity
Toggle	H	Blinking	OFF	1000Mbps Link / Activity (RX,TX)
H	L	OFF	ON	100Mbps Link / No Activity
H	Toggle	OFF	Blinking	100Mbps Link / Activity (RX,TX)
L	L	ON	ON	10Mbps Link / No Activity
Toggle	Toggle	Blinking	Blinking	10Mbps Link / Activity (RX,TX)

4.3 Media Access Controller (MAC)

4.3.1 MAC OPERATION

The device strictly abides by IEEE 802.3 standards to maximize compatibility. Additionally, there is an added MAC filtering function to filter unicast packets. The MAC filtering function is useful in applications, such as VoIP, where restricting certain packets reduces congestion and thus improves performance.

The transmit MAC takes data from the egress buffer and creates full Ethernet frames by adding the preamble and the start-of-frame delimiter ahead of the data, and generates the FCS that is appended to the end of the frame. It also sends flow control packets as needed.

The receive MAC accepts data via the integrated PHY or via the SGMII/MII/RMII/RGMII interface. It decodes the data bytes, strips off the preamble and SFD of each frame. The destination and source addresses and VLAN tag are extracted for use in filtering and address/ID lookup, and the MAC also calculates the CRC of the received frame, which is compared to the FCS field. The MAC can discard frames that are the wrong size, that have an FCS error, or when the source MAC address matches the Switch MAC address.

The receive MAC also implements the Wake on LAN (WoL) feature. This system power saving feature is described in detail in the [Section 4.10, "Power Management"](#).

MIB statistics are collected in both receive and transmit directions.

4.3.2 INTER-PACKET GAP (IPG)

If a frame is successfully transmitted, then the minimum 96-bit time for IPG is specified as being between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bit time for IPG is specified as being from carrier sense (CRS) to the next transmit packet.

4.3.3 BACK-OFF ALGORITHM

The device implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

4.3.4 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

4.3.5 LEGAL PACKET SIZE

On all ports, the device discards received packets smaller than 64 bytes (excluding VLAN tag, including FCS) or larger than the maximum size. The default maximum size is the IEEE standard of 1518 bytes, but can be programmed to 2000 bytes. Ports operating at 1000Mbps may be programmed to accept jumbo packets up to 9000 bytes, but for performance reasons it is recommended that no more than two ports be enabled simultaneously for jumbo packets.

4.3.6 FLOW CONTROL

The device supports standard MAC Control PAUSE (802.3x flow control) frames in both the transmit and receive directions for full-duplex connections.

In the receive direction, if a PAUSE control frame is received on any port, the device will not transmit the next normal frame on that port until the timer, specified in the PAUSE control frame, expires. If another PAUSE frame is received before the current timer expires, the timer will then update with the new value in the second PAUSE frame. During this period (while it is flow controlled), only flow control packets from the device are transmitted.

In the transmit direction, the device has intelligent and efficient ways to determine when to invoke flow control and send PAUSE frames. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The device issues a PAUSE frame containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the device sends out another flow control frame with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

4.3.7 HALF-DUPLEX BACK PRESSURE

A half-duplex back pressure option (non-IEEE 802.3 standard) is also provided. The activation and deactivation conditions are the same as in full-duplex mode. If back pressure is required, the device sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the device discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier sense type back pressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type back pressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collision and carrier sense is maintained to prevent packet reception.