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KSZ9692PB, KSZ9692PB-S

Integrated Gigabit Networking and Communications Controller

Rev. 5.0

General Description

The KSZ9692PB, KSZ9692PB-S is a highly integrated System-on-Chip (SoC) containing an ARM 922T 32-bit processor and a rich set of peripherals to address the cost-sensitive, high-performance needs of a wide variety of high bandwidth networking and communications applications.

The KSZ9692PB-S is a small package version of KSZ9692PB and it supports 16 bit DDR data width.

Features

ARM 922T High-Performance Processor Core

- 250 MHz ARM 922T RISC processor core
- 8KB I-cache and 8KB D-cache
- Configurable Memory Management Unit (MMU) for Linux and WinCE

Memory Controller

- 8/16-bit external bus interface for FLASH, ROM, SRAM, and external I/O
- NAND FLASH controller with boot option
- 200MHz 32-bit DDR controller
- Two JEDEC Specification JESD82-1 compliant differential clock drivers for a glueless DDR interface solution

Ethernet Interfaces

- Two Gb (10/100/1000 Mbps) MACs
- MII or RGMII interface
- Fully compliant with IEEE 802.3 Ethernet standards

IP Security Engine

- Hardware IPSec Engine guarantees 100Mbps VPN
- Secure Socket Layer Support
- DES/3DES/AES/RC4 Cyphers
- MD-5, SHA-1, SHA-256 Hashing Algorithms
- HMAC
- SSLMAC

PCI Interface

- Version PCI 2.3
- 32-bit 33/66MHz
- Integrated PCI Arbiter supports three external masters
- Configurable as Host bridge or Guest device
- Glueless Support for mini-PCI or CardBus devices

Dual High-Speed USB 2.0 Interfaces

- Two USB2.0 ports with integrated PHY
- Can be configured as 2-port host, or host + device

SDIO/SD Host Controller

- Meets SD Host Controller Standard Specification Version 1.0
- Meets SDIO card specification Version 1.0

DMA Controllers

- Dedicated DMA channels for PCI, USB, IPSec, SDIO and Ethernet ports.

Peripherals

- Four high-speed UART ports up to 5 Mbps
- Two programmable 32-bit timers with watchdog timer capability
- Interrupt Controller
- Twenty GPIO ports
- One shared SPI/I2C interface
- One I2S port

Debugging

- ARM9 JTAG debug interface
- JTAG Boundary Scan Support

Power Management

- CPU and system clock speed step-down options
- Ethernet port Wake-on-LAN
- DDR and PCI power down

Operating Voltage

- 1.3V power for core
- 3.3V power for I/O
- 2.5V or 2.6V power for DDR memory interface

Reference Hardware and Software Evaluation Kit

- Hardware evaluation Kit
- Software Evaluation Kit includes WinCE BSP, Open WRT BSP, Linux based SOHO Router packages

Applications

- Enhanced residential gateways
- High-end printer servers
- Voice-over-Internet Protocol (VoIP) systems
- IP-based multimedia systems
- Wireless Access Points or Mesh Nodes
- USB device servers
- Industrial control
- Video surveillance systems
- SMB/SME Network Security Applications, including VPN Routers

Ordering Information

Part Number	Temp. Range	Package	Lead Finish
KSZ9692PB	0°C to 70°C	400-Pin PBGA	Pb-Free
KSZ9692PBI	-40°C to 85°C	400-Pin PBGA	Pb-Free
KSZ9692PB-S	0°C to 70°C	400-Pin PBGA	Pb-Free

Block Diagram

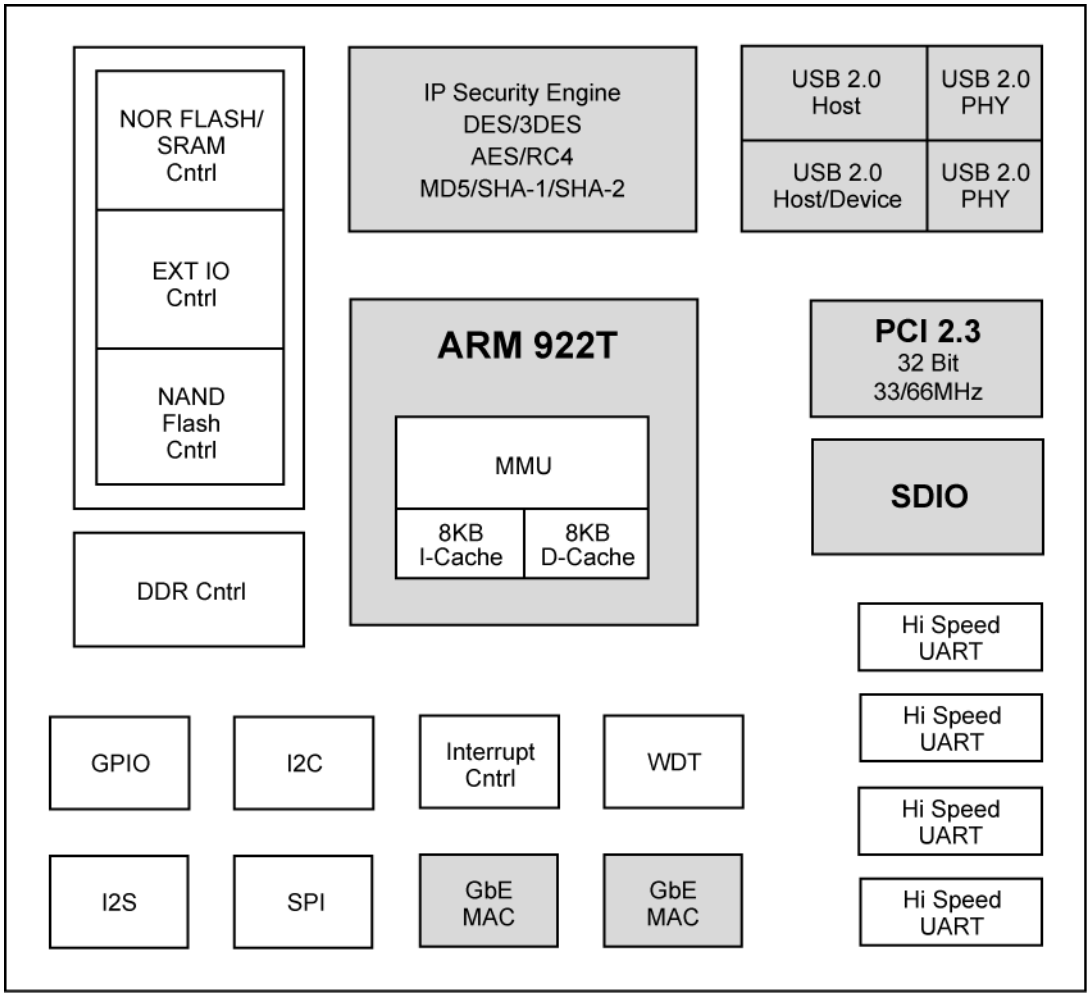

Figure 1. KSZ9692PB, KSZ9692PB-S Block Diagram

Revision History

Revision	Date	Summary of Changes
1.0	10/14/08	Initial Release
2.0	3/10/09	Power Sequencing, Added A1 (PMEN) to pin list, 1.3V Supply for Core, Power Consumption table
3.0	8/10/09	DDR Data Width Changed to 16-bit
4.0	01/28/10	DDR Data Width Changed to 32-bit
4.1	06/10/10	Remove NAND Boot support
5.0	04/14/11	Add small packet device KSZ9692PB-S
	09/13/11	Change the USB Port 0 to Port 2 in Figure 12 and 13. Change RSVD to DATA[31..16] in Figure 20.

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System Level Applications

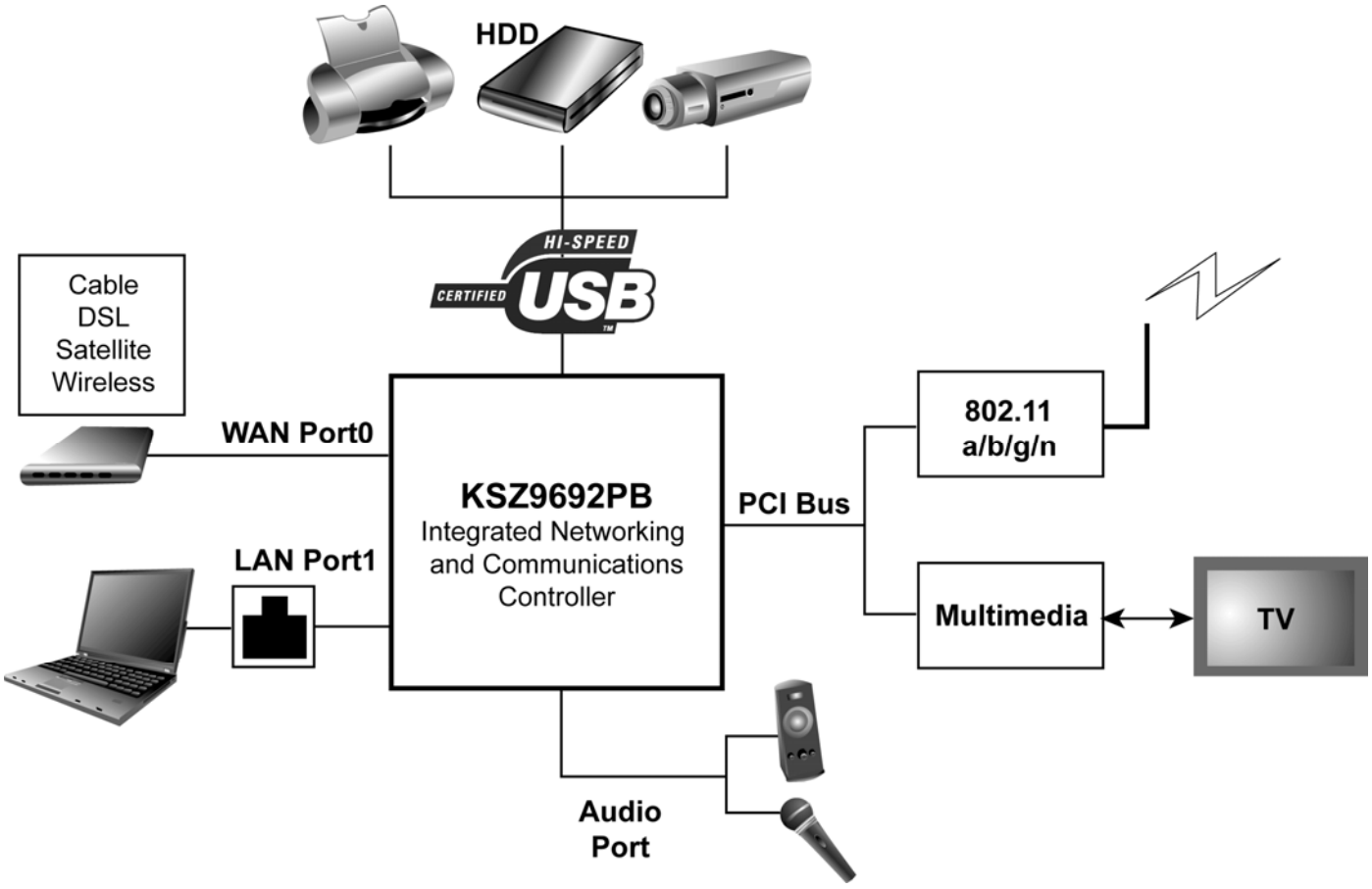

Figure 2. Peripheral Options and Examples

Pin Description: Signal Descriptions by Group

Pin Number	Pin Name	Pin Type	Pin Description
System Interface			
R5	RESETN	I	Reset, asserted Low. RESETN will force the KSZ9692PB, KSZ9692PB-S to reset ARM9 CPU and all functional blocks. Once asserted, RESETN must remain asserted for a minimum duration of 256 system clock cycles. When in the reset state, all the output pins are put into Tri-state and all open drain signals are floated.
N5	WRSTO	O	Watchdog Timer Reset Output When the Watchdog Timer expires, this signal will be asserted for at least 200 msec.
W1	XCLK2	I	System Clock Input 2. External crystal or clock input 2. The clock frequency should be 25MHz ± 50ppm.
Y1	XCLK1	I	System Clock Input 1. Used with XCLK1 pin when other polarity of crystal is needed. This is unused for a normal clock input.
H19	CLK25MHz	O	25MHz output to external PHY
Y15, Y14	DDCLKO[1:0]	O	DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
W15, W14	DDCLKON[1:0]	O	The negative of differential pair of DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
U13	SDCLKEO	O	Clock Enable output for SDRAM (for Power Down Mode)
T7, U7	VREF	I	Reference Voltage for SSTL interface. Must be half of the voltage for the DDR VDD supply. See EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5V, SSTL_2)
W3	SDOCLK	O	DDR Clock Out for loopback from De-skew PLL
Y3	SDICLK	I	DDR Clock In from loopback to De-skew PLL. This pin must connect to SDOCLK with appropriate de-skew length. See Engineering Evaluation Design Kit for detailed implementation.
Y17, Y16	DDCLKO[3:2]	O	Factory Reserved.
W17, W16	DDCLKON[3:2]	O	Factory Reserved.
NAND/SRAM/ROM/EXIO Interface			
L2, K1, K2, J3, H5, H4, J2, H3, J1, H2, G5, H1, G3, G4, G2, F1, G1, F2, F3, F5, F4, E1, E2, E3	SADDR[23..0]	O	SRAM Address Bus. The 24-bit address bus covers 16M word memory space of ROM/SRAM/FLASH, and 16M byte external I/O banks. This address bus is shared between ROM/SRAM/FLASH/EXTIO devices.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
T2, U1, L5, N4, P3, R2, T1, M4, K5, N3, P2, R1, L4, M3, P1, K4	SDATA[15..0]	Ipu/O	SRAM DATA Bus. Bidirectional Bus for 16-bit DATA In and DATA Out. The KSZ9692PB, KSZ9692PB-S also supports 8-bit data bus for ROM/SRAM/FLASH/EXTIO cycles. This data bus is shared between NAND, ROM/SRAM/FLASH/EXTIO devices.
L3	ECS2	O	External I/O Chip Select 2, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
N1	ECS1	O	External I/O Chip Select 1, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
M2	ECS0	O	External I/O Chip Select 0, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
K3	RCSN1	O	ROM/SRAM/FLASH(NOR) Chip select 1, asserted Low. The KSZ9692PB, KSZ9692PB-S can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks.
L1	RCSN0	O	ROM/SRAM/FLASH(NOR) Chip select 0, asserted Low. The KSZ9692PB, KSZ9692PB-S can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks. This bank is configurable as boot option
N2	EWAITN	I	External Wait asserted Low. This signal is asserted when an external I/O device or ROM/SRAM/FLASH(NOR) bank needs more access cycles than those defined in the corresponding control register.
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device.
J5	ERWEN1	O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[15..8] for ROM/SRAM/FLASH and EXTIO access.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[7..0 or 15..0] for ROM/SRAM/FLASH and EXTIO access.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash.
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash.
T3	NCEN1	O	NAND Bank Chip Enable 1, asserted low NAND device bank 1 selection control.
V3	NCEN0	O	NAND Bank Chip Enable 0, asserted low NAND device bank 0 selection control.
R4	NREN	Ipu/O	NAND Read Enable, asserted low
T4	NWEN	Ipu/O	NAND Write Enable, asserted low
U3	NWPN	Ipu/O	NAND Write Protection, asserted low
P4, U4	NRBN[1:0]	I	NAND Ready/Busy, asserted low for busy.
DDR Interface			

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
T17, V18, U17, T16, W20, W19, Y20, Y19, W18, V17, U16, T15, Y18, V16	DADDR[13..0]	O	DDR Address Bus.
V13, U11, V12, W13, Y13, W12, V11, U10, V10, Y11, W10, U9, Y10, V9, W9, Y9, W8, Y8, Y7, W7, V7, Y6, W6, V6, Y5, V5, W5, U5, T5, Y4, V4, W4	DDATA[31..0]	I/O	DDR Data Bus.
T13, V14	BA[1:0]	O	DDR Bank Address.
U14	CSN	O	DDR Chip Select, asserted Low. Chip select pins for DDR, the KSZ9692PB, KSZ9692PB-S supports only one DDR bank.
T14	RASN	O	DDR Row Address Strobe, asserted Low. The Row Address Strobe pin for DDR.
U15	CASN	O	DDR Column Address Strobe, asserted Low. The Column Address Strobe pin for DDR.
V15	WEN	O	DDR Write Enable, asserted Low. The write enable signal for DDR.
U8, T6 T12,Y12	DM[3:0]	O	Data Input/Output mask signals for DDR. DM is sampled High and is an output mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a Write cycle. DM0 corresponds to DDATA[7:0], DM1 corresponds to DDATA[15:8], DM2 corresponds to DDATA[23:16] and DM3 corresponds to DDATA[31:24].
V8, U6 U12,W11	DQS[3:0]	I/O	DDR only Data Strobe Input with read data, output with write data. DQS0 corresponds to DDATA[7:0], DQS1 corresponds to DDATA[15:8].

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
Ethernet Port 0			
M16	P0_RXC	Ipd/O	MAC mode MII: input RX clock / PHY mode MII: output RX clock RGMII mode: input RX clock
P18, N17, P17, N16	P0_RXD[3:0]	I	RX data[3:0]
N18	P0_RXDV	I	MII mode: RX data valid RGMII mode: as RX_CTL. RXDV on rising edge of RXC, logic derivative of RXDV and RXER on falling edge of RXC
P19	P0_RXER	I	MII mode: RX error RGMII mode: input SEL
M17	P0_CRS	I	MAC mode MII: input carrier sense RGMII mode: not used
P20	P0_COL	I	MAC mode MII: input collision RGMII mode: not used
M18	P0_TXC	Ipd/O	MAC mode MII: input TX clock / PHY mode MII: output TX clock RGMII mode: output TX clock
L17, M19, N20, N19	P0_TXD[3:0]	O	TX data[3:0]
L16	P0_TXEN	O	MII: TX enable RGMII: as TX_CTL input. TXEN on rising edge of TXC, logic derivative of TXEN and TXER on falling edge of TXC.
Ethernet Port 1			
K19	P1_RXC	Ipd/O	MAC mode MII: input RX clock / PHY mode MII: output RX clock RGMII mode: input RX clock
L20, L19, L18, M20	P1_RXD[3:0]	I	RX data[3:0]
K16	P1_RXDV	I	MII mode: RX data valid RGMII mode: as RX_CTL. RXDV on rising edge of RXC, logic derivative of RXDV and RXER on falling edge of RXC
K17	P1_RXER	I	MII mode: RX error RGMII mode: input SEL
K18	P1_CRS	I	MAC mode MII: input carrier sense RGMII mode: not used
K20	P1_COL	I	MAC mode MII: input collision RGMII mode: not used
J17	P1_TXC	Ipd/O	MAC mode MII: input TX clock / PHY mode MII: output TX clock RGMII mode: output TX clock
H20, J19, J18, J20	P1_TXD[3:0]	O	TX data[3:0] output.
J16	P1_TXEN	O	MII: TX enable RGMII: as TX_CTL input. TXEN on rising edge of TXC, logic derivative of TXEN and TXER on falling edge of TXC.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
USB Interface			
G19	U1P	I/O (analog)	USB port 1 differential + signal
G20	U1M	I/O (analog)	USB port 1 differential - signal
F19	U2P	I/O (analog)	USB port 2 differential + signal
F20	U2M	I/O (analog)	USB port 2 differential - signal
G17	USBXI	I (analog)	Crystal in for USB PLL
G18	USBXO	O (analog)	Crystal out for USB PLL
H16	USBREXT	I (analog)	Connect to an external resistor 3.4K ohm to GND
G16	USBTEST	O (Analog)	USB analog test output (factory reserved)
G15	USBCFG	I	USB port 2 configuration "1" = port 2 is host "0" = port 2 is device (port 1 is always host)
F18	USBHOVC0	I	Over current sensing input for Host Controller downstream port 1.
F15	USBHOVC1	I	Over current sensing input for Host Controller downstream port 2.
F17	USBHPWR0	Ipu/O (open drain)	Power switching control output for downstream port 1; open drain output.
F16	USBHPWR1	Ipu/O (open drain)	Power switching control output for downstream port 2; open drain output.
SDIO Interface			
D14	KCMD	Ipd/O	SD 4-bit mode: Command line SD 1-bit mode: Command line
C18	KCLK	Ipd/O	SDIO/SD Clock
C15	KDATA3	I/O	SD 4-bit mode : data line 3 SD 1-bit mode : not used
C16	KDATA2	I/O	SD 4-bit mode : data line 2 or read wait (optional) SD 1-bit mode : read wait (optional)
E13	KDATA1	I/O	SD 4-bit mode : data line 1 or interrupt (optional) SD 1-bit mode : interrupt
C17	KDATA0	I/O	SD 4-bit mode : data line 0 SD 1-bit mode : data line
C14	KSDCDN	I	Active low used for Card Detection

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
D13	KSDWP	I	Active high used for Card write protection
General Purpose I/O			
B14	SLED/GPIO[19]	I/O	SDIO Line Status LED output or General Purpose I/O Pin[19]
B15	CPUINTN/ GPIO[18]	I/O	Internal CPU interrupt request or General Purpose I/O Pin[18] As CPUINTN, any interrupt generated to ARM CPU asserts logic low on this pin. Useful for software development.
B16, B17, B18, D18, E15, D19	GPIO[17:12]	I/O	General Purpose I/O Pin[17:12]
F14	UART 4 RTSN /GPIO[11]	I/O	UART 4 RTS or general purpose I/O Pin[11]
E16	UART 4 CTSN /GPIO[10]	I/O	UART 4 CTS or general purpose I/O Pin[10]
E17	UART 3 RTSN /GPIO[9]	I/O	UART 3 RTS or general purpose I/O Pin[9]
E19	UART 3 CTSN /GPIO[8]	I/O	UART 3 CTS or general purpose I/O Pin[8]
E20	UART 2 RTSN /GPIO[7]	I/O	UART 2 RTS or general purpose I/O Pin[7]
E18	UART 2 CTSN /GPIO[6]	I/O	UART 2 CTS or general purpose I/O Pin[6]
U20, U19	TOUT[1:0]/ GPIO[5:4]	I/O	Timer 1/0 out or General Purpose I/O Pin[5:4]
V20, T18, V19, U18	EINT[3:0]/ GPIO[3:0]	I/O	External Interrupt Request or General Purpose I/O Pin[3:0]
I2S Interface			
C20	SCKIN	I	External crystal or clock input for I2S clock The maximum supported frequency is 49.2MHz
D20	SCKOUT	O	External Crystal out for I2S clock
C19	I2S_MCLK	O	I2S master clock out This clock is of same frequency as SCKIN
B20	I2S_BCLK	O	I2S bit clock out
B19	I2S_LRCLK	O	Left/right select
A19	I2S_SDO	O	Serial data out
A20	I2S_SDI	I	Serial data in
MDIO/MDC Interface			
H18	MDC	Ipu/O	Clock for station management
H17	MDIO	Ipu/O	Serial data for station management
I2C/SPI Interface			

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
E14	SPCK_SCL	Ipu/O	SPI mode: master clock output I2C mode: serial clock output
D17	SPMOSI_SDA	Ipu/O	SPI mode: master data out,slave data in I2C mode: serial data
D16	SPMISO	I	SPI master data in, slave data out
D15	SPICS	Ipu/O	SPI chip select
F13	SPI_RDY	I	Micrel SPI mode ready signal
PCI Interface Signals			
C3	PRSTN	I	PCI Reset, asserted Low In Host Bridge Mode, the PCI Reset pin is an input. This pin as well as the reset pin of all the devices on the PCI bus could be driven by WRSTO. In Guest Bridge Mode, this pin is input. The system reset to drive this pin.
B2	PCLK	I	PCI Bus Clock input. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz, or 66MHz.
E4	GNT3N	O	PCI Bus Grant 3 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ3N. In Guest Bridge Mode, this is unused.
D4	GNT2N	O	PCI Bus Grant 2 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ2N. In Guest Bridge Mode, this is unused.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
B1	GNT1N	O	PCI Bus Grant 1 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ1N. In Guest Bridge Mode, this is an output signal to indicate to the external PCI bus arbiter that KSZ9692PB, KSZ9692PB-S is requesting access to the PCI bus.
D3	REQ3N	I	PCI Bus Request 3 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this is unused.
E6	REQ2N	I	PCI Bus Request 2 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this is unused.
C1	REQ1N	I	PCI Bus Request 1 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this signal comes from the external arbiter to indicate that the bus is granted to KSZ9692PB, KSZ9692PB-S.
B3, E7, D6, A2, B4, A3, D7, C5, C6, B5, A4, A5, B6, E8, C7, D8, D10, B10, A11, B11, C11, A12, E11, D11, B12, A13, C12, B13, F12, C13, D12, E12	PAD[31..0]	I/O	32-bit PCI address and data lines Addresses and data bits are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the PAD bus contains the first clock cycle of a PCI transaction, the PAD bus contains the physical address. During subsequent clock cycles, these lines contain the 32-bit data to be transferred. Depending on the type of the transaction, the source of the data will be the KSZ9692PB, KSZ9692PB-S if it initiates a PCI write transaction, or the data source will be the target if it is a PCI Read transaction. The KSZ9692PB, KSZ9692PB-S bus transaction consists of an address phase followed by one or more data phases. The KSZ9692PB, KSZ9692PB-S supports both Read and Write burst transactions. In case of a Read transaction, a special data turn around cycle is needed between the address phase and the data phase.
A6, A7, E10, C10	CBEN[3..0]	I/O	PCI Commands and Byte Enable, asserted Low. The PCI command and byte enable signals are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the CBEN bus contains the command for the transaction. The PCI transaction consists of the address phases and one or more data phases. During the data phases of the transaction, the bus carries the byte enable for the current data phases.
C8	PAR	I/O	Parity PCI Bus parity is even across PAD[31:0] and CBEN[3:0]. The KSZ9692PB, KSZ9692PB-S generates PAR during the address phase and write data phases as a bus master, and during read data phases as a target. It checks for correct PAR during read data phase as a bus master, during every address phase as a bus slave, and during write data phases as a target.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
D9	FRAMEN	I/O	PCI Bus Frame signal, asserted Low. FRAMEN is an indication of an active PCI bus cycle. It is asserted at the beginning of a PCI transaction, i.e. the address phase, and de-asserted before the final transfer of the data phase of the transaction.
B8	IRDYN	I/O	PCI Initiator Ready signal, asserted Low. This signal is asserted by a PCI master to indicate a valid data phase on the PAD bus during data phases of a write transaction. In a read transaction, it indicates that the master is ready to accept data from the target. A target will monitor the IRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together.
E9	TRDYN	I/O	PCI Target Ready signal, asserted Low. This signal is asserted by a PCI slave to indicate a valid data phase on the PAD bus during data phases of a read transaction. In a write transaction, it indicates that the slave is ready to accept data from the target. A PCI initiator will monitor the TRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together.
A9	DEVSELN	I/O	PCI Device Select signal, asserted Low. This signal is asserted when the KSZ9692PB, KSZ9692PB-S is selected as a target during a bus transaction. When the KSZ9692PB, KSZ9692PB-S is the initiator of the current bus access, it expects the target to assert DEVSELN within 5 PCI bus cycles, confirming the access. If the target does not assert DEVSELN within the required bus cycles, the KSZ9692PB, KSZ9692PB-S aborts the bus cycle. As a target, the KSZ9692PB, KSZ9692PB-S asserts this signal in a medium speed decode timing. (2 bus cycle)
B7	IDSEL	I	Initialization Device Select. It is used as a chip select during configuration read and write transactions.
B9	STOPN	I/O	PCI Stop signal, asserted Low. This signal is asserted by the PCI target to indicate to the bus master that it is terminating the current transaction. The KSZ9692PB, KSZ9692PB-S responds to the assertion of STOPN when it is the bus master, either to disconnect, retry, or abort.
A10	PERRN	I/O	PCI Parity Error signal, asserted Low. The KSZ9692PB, KSZ9692PB-S asserts PERRN when it checks and detects a bus parity error. When it generates the PAR output, the KSZ9692PB, KSZ9692PB-S monitors for any reported parity error on PERRN. When the KSZ9692PB, KSZ9692PB-S is the bus master and a parity error is detected, the KSZ9692PB, KSZ9692PB-S sets error bits on the control status registers. It completes the current data burst transaction, then stop the operation. After the Host clears the system error, the KSZ9692PB, KSZ9692PB-S continues its operation.
C9	SERRN	O (open drain)	PCI System Error signal, asserted Low. If an address parity error is detected, the KSZ9692PB, KSZ9692PB-S asserts the SERRN signal two clocks after the failing address.
C4	M66EN	I	PCI 66MHz Enable When asserted, this signal indicates the PCI Bus segment is operating at 66MHz. This pin is mainly used in Guest bridge mode when the PCLK is driven by the Host bridge.
F6	PCLKOUT3	O	PCI Clock output 3

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
D1	PCLKOUT2	O	PCI Clock output 2
D2	PCLKOUT1	O	PCI Clock output 1
E5	PCLKOUT0	O	PCI Clock output 0. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz, or 66MHz. In Host Bridge Mode, this is an output signal for all the devices on the PCI bus to sample data and control signals. Connect this clock to drive PCLK input. In Guest Bridge Mode, this is not used.
A8	CLKRUNN	I/O	This is a CardBus only signal. The CLKRUNN signal is used by portable CardBus devices to request the system to turn on the bus clock. Output is not generated.
C2	MPCIACTN	I/O	Mini-PCI active. This signal is asserted by the PCI device to indicate that its current function requires full system performance. MPCIACTN is an open drain output signal.
D5	PBMS	I	PCI Bridge Mode Select Select the operating mode of the PCI Bridge. When PBMS is High, the Host Bridge Mode is selected and on chip PCI bus arbiter is enabled. When PBMS is Low, the Guest Bridge Mode is selected and the on-chip arbiter is disabled.
A1	PMEN	O (open drain)	PCI Power Management Enable (active low) This pin is to inform the external PCI host that KSZ9692PB, KSZ9692PB-S has detected a wake-up event.
UART Signals			
P16	U1RXD	Ipd	UART 1 Receive Data
R16	U1TXD	O (Tri-State)	UART 1Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
R19	U1CTSN	Ipd	UART 1Clear to Send
R20	U1DCDN	Ipd	UART 1 Data Carrier Detect
P15	U1DSRN	Ipd	UART 1 Data Set Ready
R15	U2RXD	Ipd	UART 2 Receive Data
R17	U2TXD	O (Tri-State)	UART 2 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
R18	U3RXD	Ipd	UART 3 Receive Data
N15	U3TXD	O (Tri-State)	UART 3 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
T19	U4RXD	Ipd	UART 4 Receive Data
T20	U4TXD	O (Tri-State)	UART 4 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
TAP Control Signals			
A18	TCK	I	JTAG Test Clock
A17	TMS	I	JTAG Test Mode Select
A16	TDI	I	JTAG Test Data In
A15	TDO	O	JTAG Test Data Out
A14	TRSTN	I	JTAG Test Reset, asserted Low
Test Signals			
P5	SCANEN	Ipd	1 = Scan Enable (Factory reserved) 0 = Normal Operation
V2	TESTEN	Ipd	1 = Test Enable (Factory reserved) 0 = Normal Operation
V1	TESTEN1	Ipd	1 = Test Enable1 (Factory reserved) 0 = Normal Operation
Y2	TEST1	O (analog)	Factory reserved
W2	TEST2	O (analog)	Factory reserved
Power and Ground (96)			
N6, M6, M7, G7, G8, G9, M14, M15, N14, P11, P12, P13, P14	VDD1.2	P	Digital power supply 1.3V (13)
G6, H6, J6, K6, F7, F8, F9, F10, F11, G10, G11, H14, J14, K14, K15, L15	VDD3.3	P	Digital power supply 3.3V (16)
R6, R7, R8, R9, R10, R11, R12, R13, R14, T8, T9, T10, T11	VDD2.5	P	DDR Pad Driver 2.5V or 2.6V Power Supply. (13)
H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, K12, L7, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, N9, N10, N11, N12, N13, P7, P8, P9, P10	GND	GROUND	Digital Ground. (37)

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
L6	PLLVDDA3.3	P	Band Gap Reference Analog Power. (1)
M8	PLLVSSA3.3	GROUND	Band Gap Reference Analog Ground. (1)
P6	PLLDVDD1.2	P	De-skew PLL Analog and Digital Power. (1)
M5	PLLSVDD1.2	P	System PLL Analog and Digital Power. (1)
N7, N8	PLLVSS1.2	GROUND	De-skew PLL and System PLL Ground. (2)
L8	PLLVSSISO	GROUND	Ground Isolation PLL and other circuit. (1)
G12	USB1VDDA3.3	P	Analog Power for USB Channel 1. (1)
G13	USBCVDDA3.3	P	Analog Power for Common Circuit of USB Channel 1 and 2. (1)
G14	USB2VDDA3.3	P	Analog Power for USB Channel 2. (1)
H13, J13, K13	USBVSSA3.3	GROUND	Analog Ground for both USB Channels Analog Circuit. (3)
J15	USB1VDD1.2	P	Digital Power for USB Channel 1 Controller. (1)
H15	USB2VDD1.2	P	Digital Power for USB Channel 2 Controller. (1)
J12	USBVSS1	GROUND	Digital Ground for USB Channel 1 Controller. (1)
H12	USBVSS2	GROUND	Digital Ground for USB Channel 2 Controller. (1)

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   O/I = Output in normal mode; input pin during reset.
   Ipu = Internal 55kΩ pull-up resistor.
   Ipd = Internal 55kΩ pull-down resistor.

Pin Description: Power-up Strapping Options

Certain pins are sampled upon power up or reset to initialize KSZ9692PB, KSZ9692PB-S system registers per system configuration requirements.

Pin Number	Pin Name	Pin Type	Pin Description
E3	SADDR[0]	Ipd/O	During reset, this pin is the input strap option for NAND Boot small page size 0 = 512 Bytes (default) 1 = 528 Bytes (Not support NAND Boot)
E1, E2	SADDR[2:1]	Ipd/O	During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [7:6]. These pins are used to specify number of active banks (CE#) in cascade. 00 = 1 bank (default) 01 = 2 banks
F4	SADDR[3]	Ipd/O	During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [8], NAND Flash type. This pin is used to specify using large or small block NAND Flash as a boot bank as follows: “0” = small block (default) “1” = large block (Not support NAND Boot)
F5	SADDR[4]	Ipd/O	During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [4], NAND Flash type. This pin is used to specify number of NAND Flash in parallel for combined data width as follows: “0” = 1 NAND Flash (default) “1” = 2 NAND Flash
F3	SADDR[5]	Ipu/O	During reset, this is the input strap option to enter ARM9 tic test mode 0: ARM tic test mode (factory reserved) 1: Normal mode (default)
F2	SADDR[6]	Ipd/O	During reset, this pin is the input strap option for NAND FLASH device support automatic page crossing 0: NAND FLASH device does not support automatic page crossing (default) 1: NAND FLASH device supports automatic page crossing
G1	SADDR[7]	Ipd/O	During reset, this pin is a strapping option for B0SIZE, Bank 0 Data Access Size. This is applicable to ROM/SRAM/FLASH boot and NAND boot bank. Bank 0 is used for boot program. This pin is used to specify the size of the bank 0 data bus width as follow: “0” = one byte (default) “1” = half word
F1	SADDR[8]	Ipd/O	During reset, this pin is a strapping option for BTSEL: “0” = Boot select from NOR flash (default) “1” = Boot select from NAND flash (Not support NAND Boot)
G2	SADDR[9]	Ipd/O	During reset this pin is a strapping option for BYP_SYSPLL: “0” = Use systems PLL (default) “1” = Bypass systems PLL, use external clock (factory reserved)
G4	SADDR[10]	Ipd/O	During reset this pin is a strapping option for BYP_CLKSEL: “0” = Select 200MHz external clock (default) “1” = Select 250MHz external clock (factory reserved)

Pin Description: Power-up Strapping Options (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
G3	SADDR[11]	Ipd/O	During reset, this pin is input strap option to enable either MII or RGMII mode at port1 (LAN port) 0: MII mode (default) 1: RGMII mode
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device. During reset, this pin is used for Watchdog Timer Reset Polarity Select. This is a power strapping option pin for watchdog reset output polarity. “0” = WRSTO is selected as active high (default) “1” = WRSTO is selected as active low. This pin is shared with the EROEN pin.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, these signals control the byte write enable of the memory device for ROM/SRAM/FLASH and EXTIO access. During ARM tic test mode, this pin is TESTACK. During reset, this pin is the input strap option to enable either MII or RGMII mode at port0 (WAN port) 0: MII mode (default) 1: RGMII mode
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash. During reset, this pin is input strap option for NAND Flash configuration register (0x8054) bit [2]. This bit along with configuration register bits [1:0] is used for boot program. This pin along with NALE and NWEN is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit (Not support NAND Boot)

Pin Description: Power-up Strapping Options (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash. During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [1]. This bit along with configuration register bits [2], [0] is used for boot program. This pin along with NCLE and NWEN is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit (Not support NAND Boot)
T4	NWEN	Ipu/O	NAND Write Enable, asserted low During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [0]. This bit along with configuration register bits [2:1] is used for boot program. This pin along with NCLE and NALE is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit (Not support NAND Boot)
U3	NWPN	Ipu/O	NAND Write Protection, asserted low During reset, this pin is the input strap option to enable test modes. This pin along with TESTEN, TESTEN1 form different test modes. {TESTEN, TESTEN1, NWPN} = 011: ARM Scan test mode 010: USB Analog Bits test mode others: refer to TESTEN and TESTEN1 pin description (factory reserved)
G15	USBCFG	I	USB port 2 configuration “1” = port 2 is host “0” = port 2 is device (port 1 is always host)