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Kionix®	**± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX022-1020 Rev. 12.0 5-Apr-16**

Product Description

The KX022 is a tri-axis ±2g, ±4g or ±8g silicon micromachined accelerometer with integrated 256 byte buffer, orientation, tap/double tap, and activity detecting algorithms. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable application algorithms. The accelerometer is delivered in a 2 x 2 x 0.9 mm LGA plastic package operating from a 1.71 – 3.6V DC supply. Voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics over the range of input supply voltages and virtually undetectable ratiometric error. I^2C or SPI digital protocol is used to communicate with the chip to configure and check for updates to the orientation, Directional Tap™ detection and activity monitoring algorithms.

Features

- 2 x 2 x 0.9 mm LGA
- User-selectable g Range and Output Data Rate
- User-selectable low power or high resolution mode
- Digital High-Pass Filter Outputs
- Embedded FIFO/FILO buffer
- Low Power Consumption with FlexSet™ Performance Optimization
- Internal voltage regulator
- Enhanced integrated Directional Tap/Double-Tap™, and Device-orientation Algorithms
- User-configurable wake-up function
- Digital I^2C up to 3.4MHz
- Digital SPI up to 10MHz
- Lead-free Solderability
- Excellent Temperature Performance
- High Shock Survivability
- Factory Programmed Offset and Sensitivity
- Self-test Function

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Kionix®	**± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX022-1020 Rev. 12.0 5-Apr-16**

Table of Contents

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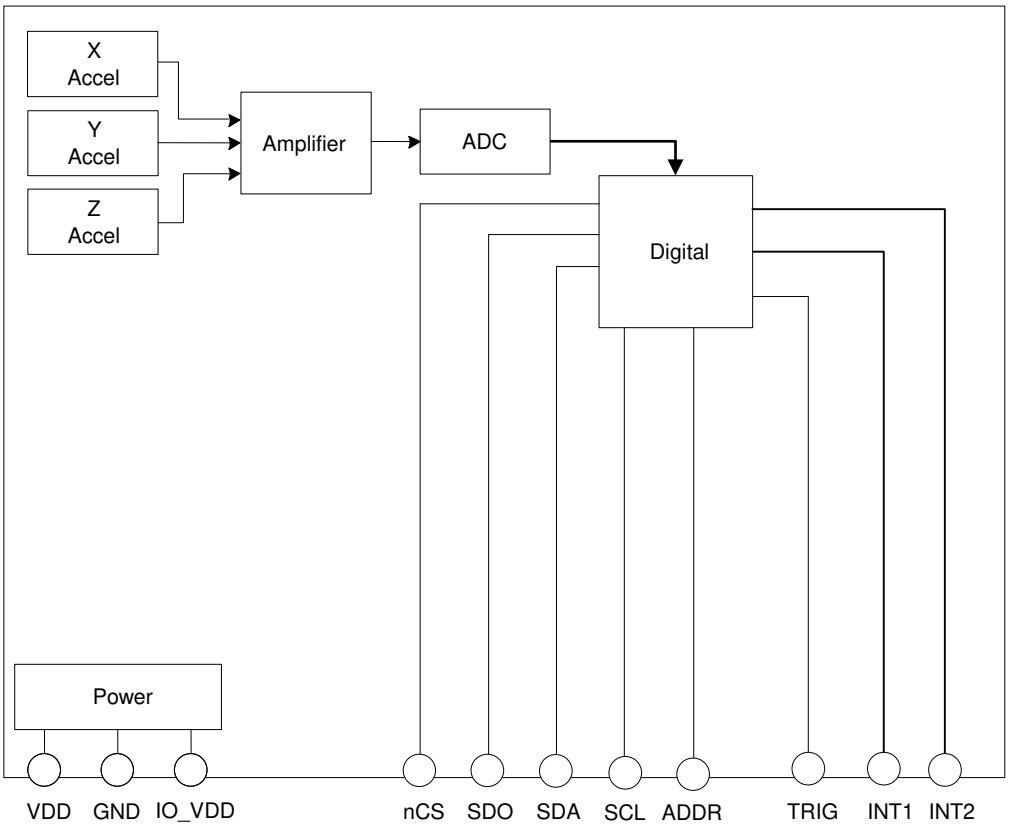
Functional Diagram



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Product Specifications

Mechanical

(Specifications are for operation at VDD = 2.5V and T = RT = 25°C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	85
Zero-g Offset		mg		±25	±90
Zero-g Offset Variation from RT over Temp.		mg/°C		0.2	
Sensitivity[1]	GSEL1=0, GSEL0=0 (± 2g)	counts/g	15401	16384	17367
	GSEL1=0, GSEL0=1 (± 4g)		7700	8192	8684
	GSEL1=1, GSEL0=0 (± 8g)		3850	4096	4342
Sensitivity (Buffer 8-bit mode)[1,2]	GSEL1=0, GSEL0=0 (± 2g)	counts/g	60	64	68
	GSEL1=0, GSEL0=1 (± 4g)		30	32	34
	GSEL1=1, GSEL0=0 (± 8g)		15	16	17
Sensitivity Variation from RT over Temp.		%/°C		0.01	
Positive Self-Test Output change on Activation[5]		g	0.35	0.5	0.65
Mechanical Resonance (-3dB)[3]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.6	
Cross Axis Sensitivity		%		2	
Noise (RMS at 50Hz with low-pass filter = ODR/9)[4]		mg		0.75	

Table 1: Mechanical Specifications

Notes:

1. Resolution and acceleration ranges are user selectable via I²C or SPI.
2. Sensitivity is proportional to BRES in BUF_CNTL2.
3. Resonance as defined by the dampened mechanical sensor.
4. Noise varies with Output Data Rate (ODR) and Current Consumption settings. Contact Kionix Engineering for additional details on FlexSet™ Performance Optimization.
5. Requires changing of STPOL bit in INC1 register to 1 prior to performing self-test.

Electrical

(Specifications are for operation at VDD = 2.5V and T = 25°C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.71	2.5	3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.7		VDD
Current Consumption	High Resolution Mode (RES = 1)	µA		145	
	Low Power Mode[1] (RES = 0)			10	
	Standby			0.9	
Output Low Voltage (IO_VDD < 2V)[2]		V	-	-	0.2 * IO_VDD
Output Low Voltage (IO_VDD ≥ 2V)[2]		V	-	-	0.4
Output High Voltage		V	0.8 * IO_VDD	-	-
Input Low Voltage		V	-	-	0.2 * IO_VDD
Input High Voltage		V	0.8 * IO_VDD	-	-
Input Pull-down Current		µA		0	
Start Up Time[3]		ms	2.0		650
Power Up Time[4]		ms		10	
I²C Communication Rate		MHz			3.4
SPI Communication Rate		MHz			10
Output Data Rate (ODR)[5]		Hz	0.781	50	1600
Bandwidth (-3dB)[6]	RES = 0	Hz		800	
	RES = 1	Hz		ODR/2	

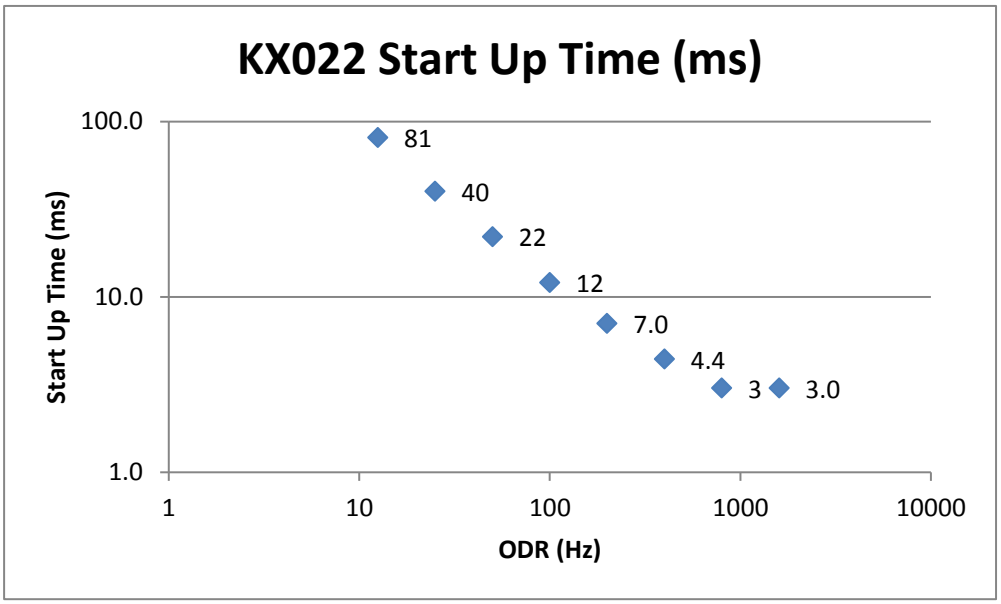
Table 2: Electrical Specifications

Notes:

1. Current varies with Output Data Rate (ODR) as shown the chart below, and with Noise level settings. Contact Kionix Engineering for additional details on FlexSet™ Performance Optimization.
2. For I²C communication, this assumes a minimum 1.5KΩ pull-up resistor on SCL and SDA pins.
3. Startup time is from PC1 set to valid outputs. Time varies with Output Data Rate (ODR); see chart below
4. Power up time is from VDD valid to device boot completion.
5. User selectable through I²C or SPI.
6. User selectable and dependent on ODR and RES.

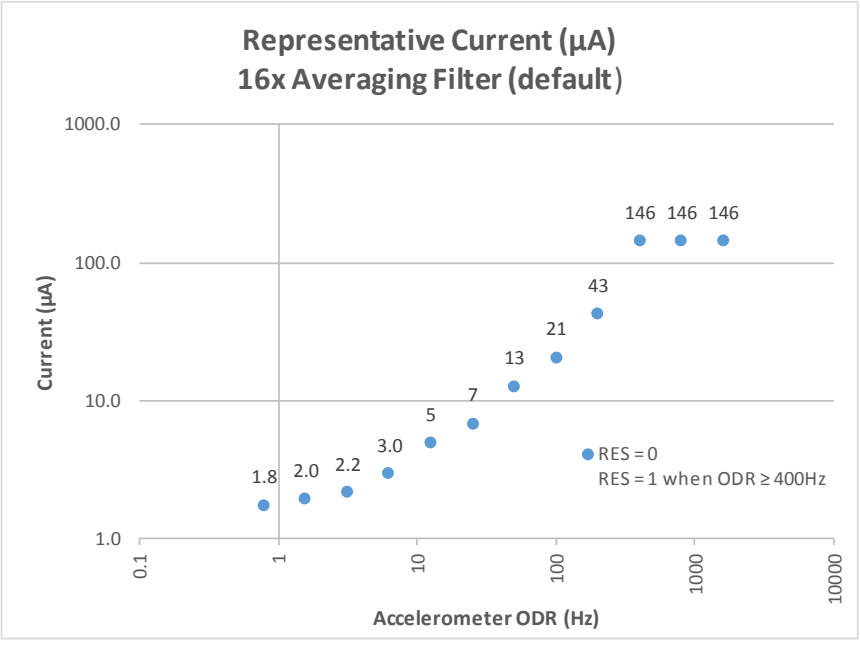
Start Up Time Profile

KX022 Start Up Time	
ODR (Hz)	Time (ms)
1600	3.0
800	3.0
400	4.4
200	7.0
100	12
50	22
25	40
12.5	81



Current Profile

Representative Current Profile		
ODR (Hz)	RES	Current (µA)
0	Standby	0.9
0.781	0	1.8
1.563	0	2.0
3.125	0	2.2
6.25	0	3.0
12.5	0	5
25	0	7
50	0	13
100	0	21
200	0	43
400	1	146
800	1	146
1600	1	146



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Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD_{Low}**, **T_{VDD}** (rise time), and **T_{VDD_Off}** profile of individual applications. It is recommended to minimize **VDD_{Low}**, and **T_{VDD}**, and maximize **T_{VDD_Off}**. It is also advised that the **VDD** ramp up time **T_{VDD}** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD_{Low}, T_{VDD}, T_{VDD_Off} and temperature as POR performance can vary depending on these parameters.

Please refer to Technical Note ***TN014 KX022, KX023 Accelerometer Power-On Procedure*** for more information.

Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.5	-	3.63
Operating Temperature Range		°C	-40	-	85
Storage Temperature Range		°C	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Table 3: Environmental Specifications

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

These products conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are “of uniform composition throughout”. The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.

Applicable Exemption: *7C-I - Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix compound.*

These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-161) as identified by the European Chemicals Agency as of 17 December 2014.

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Terminology

g

A unit of acceleration equal to the acceleration of gravity at the earth's surface.

$$1g = 9.8\frac{m}{s^2}$$

One thousandth of a g (0.0098 m/ s^2) is referred to as 1 milli-g (1 mg).

Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal VDD and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

$$Sensitivity = \frac{(Output\ @+1g - Output\ @-1g)}{2g}$$

The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25ºC), the sensitivity will vary by the amount shown in Table 1.

Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the OUTX, OUTY, OUTZ registers = 00h, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 00h. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified Table 1, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

Functionality

Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

ASIC interface

A separate ASIC device packaged with the sense element provides all of the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I^2C digital communications provided by the ASIC. In addition, the ASIC contains all of the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic. Plus, there are two programmable state machines which allow the user to create unique embedded functions based on changes in acceleration.

Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in nonvolatile memory (OTP). Additionally, all functional register default values are also programmed into the nonvolatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.

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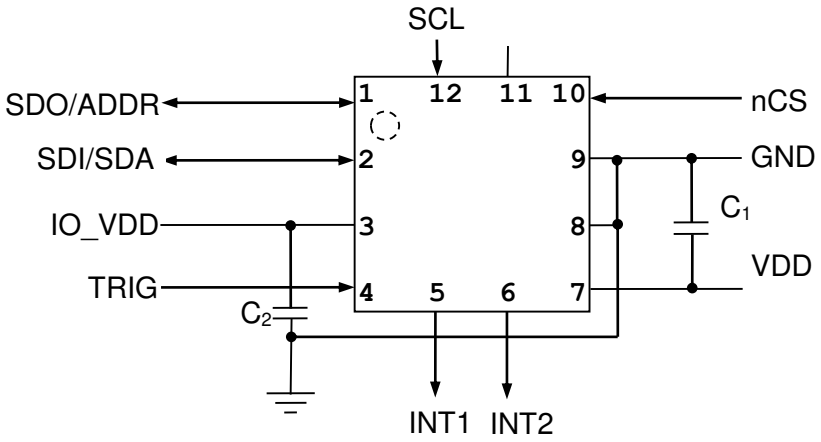
Application Schematic



Pin Descriptions

Pin	Name	Description
1	SDO/ADDR	Serial Data Out pin during 4 wire SPI communication and part of the device address during I2C communication.
2	SDI/SDA	SPI Data input / I2C Serial Data
3	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
4	TRIG	Trigger pin for FIFO buffer control – Connect to GND when not using external trigger option
5	INT1	Physical Interrupt 1. Leave floating if not used.
6	INT2	Physical Interrupt 2. Leave floating if not used.
7	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
8	GND	Ground
9	GND	Ground
10	nCS	SPI enable / I2C mode select. Connect to GND for SPI enabled, I2C communication disabled. Connect to IO_VDD for SPI disabled, I2C communication enabled. Do not leave floating.
11	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
12	SCLK/SCL	SPI and I^2C Serial Clock

Table 4: Pin Descriptions

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Test Specifications

***Special Characteristics**:*

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

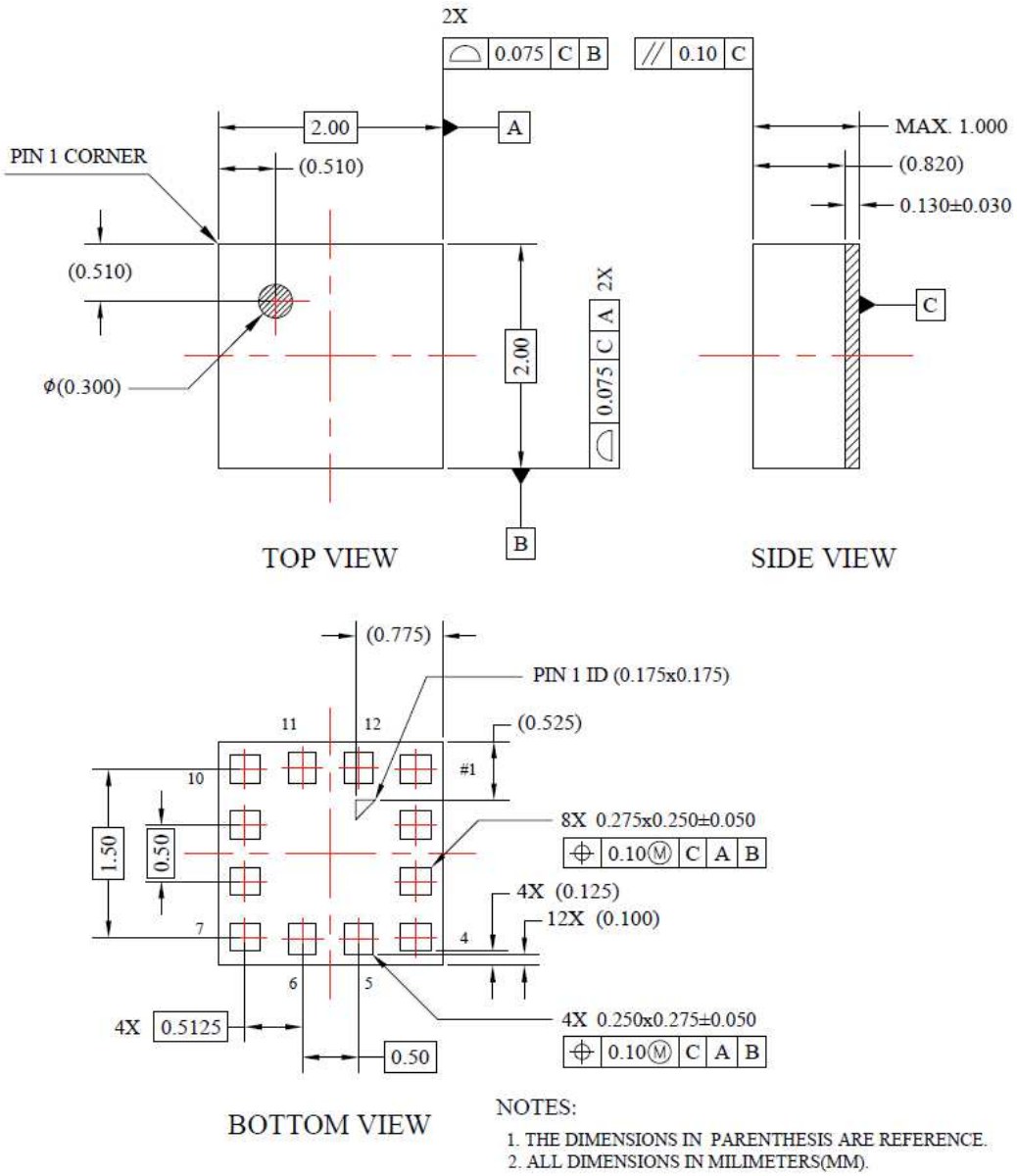
Parameter	Specification	Test Conditions
Zero-g Offset @ RT[1] (2g range)	0 ± 1475 counts	25°C, VDD = 2.5 V
Sensitivity @ RT[1] (2g range)	16384 ± 983 counts/g	25°C, VDD = 2.5 V

Table 5: Test Specifications

[1]Room Temperature = 25°C

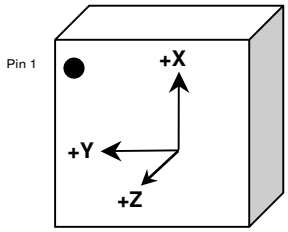
Package Dimensions and Orientation

Dimensions
2 x 2 x 0.9 mm LGA



All dimensions and tolerances conform to ASME Y14.5M-1994

Orientation

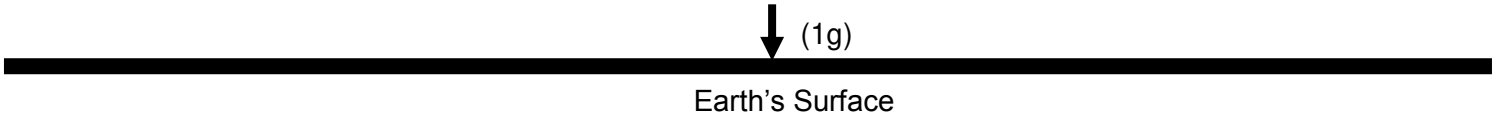


When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0 (± 2g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top Bottom		Bottom Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	16384	64	0	0	-16384	-64	0	0	0	0	0	0
Y (counts)	0	0	-16384	-64	0	0	16384	64	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	16384	64	-16384	-64
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



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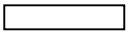
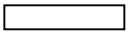
Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1 (± 4g)

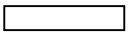
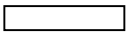
Position	1		2		3		4		5		6	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	8192	32	0	0	-8192	-32	0	0	0	0	0	0
Y (counts)	0	0	-8192	-32	0	0	8192	32	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	8192	32	-8192	-32
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

 (1g)

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0 (± 8g)

Position	1		2		3		4		5		6	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	4096	16	0	0	-4096	-16	0	0	0	0	0	0
Y (counts)	0	0	-4096	-16	0	0	4096	16	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	4096	16	-4096	-16
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

 (1g)

Earth's Surface

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Digital Interface

The Kionix KX022 digital accelerometer has the ability to communicate via the I²C and SPI digital serial interface protocols. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 6: Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KX022 has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KX022 always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are high.

The I2C interface is compliant with high-speed mode, fast mode and standard mode I2C protocols.

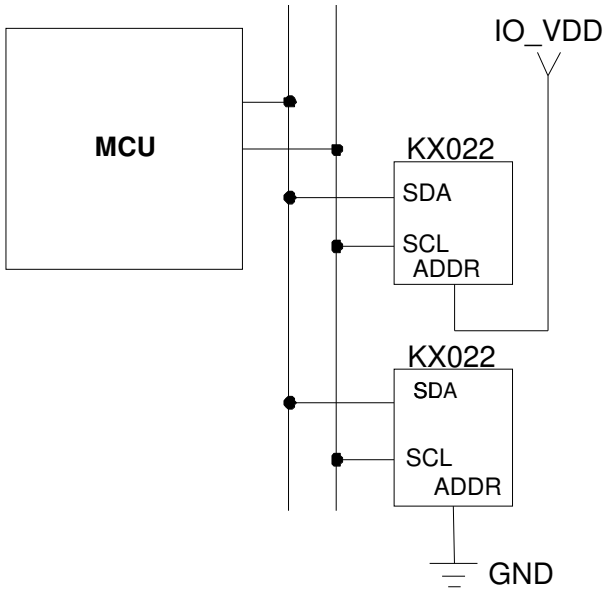

Figure 1: Multiple KX022 I²C Connection

I²C Address

Description	Address Pad	7 bit Address	Address	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
I2C Wr	IO_VDD	1Fh	3Eh	0	0	1	1	1	1	1	0
I2C Rd	IO_VDD	1Fh	3Fh	0	0	1	1	1	1	1	1
I2C Wr	GND	1Eh	3Ch	0	0	1	1	1	1	0	0
I2C Rd	GND	1Eh	3Dh	0	0	1	1	1	1	0	1

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The KX022's Slave Address is comprised of a programmable part and a fixed part, which allows for connection of multiple KX022's to the same I²C bus. The Slave Address associated with the KX022 is 001111X, where the programmable bit, X, is determined by the assignment of ADDR (pin 1) to GND or IO_VDD. Figure 1 above shows how two KX022's would be implemented on an I²C bus.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free. Note that if the KX022 is accessed through I^2C protocol before the startup is finished a NACK signal is sent.

Writing to 8-bit Register

Upon power up, the Master must write to the KX022's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KX022 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KX022 to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the MSB of the RA command should always be zero (0). The KX022 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KX022 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KX022 is now stored in the appropriate register. The KX022 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.
Note** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it may alter the content of the affected registers.

Reading from 8-bit Register

When reading data from a KX022 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KX022 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KX022 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KX022 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KX022 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command.
Note** Accelerometer's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I²C bus and how the Master and Slave interact during these transfers. Table 7 defines the I²C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 7: I²C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5. HS-mode data transfer of the Master writing multiple bytes to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	Sr	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

n bytes + ack.

Sequence 6. HS-mode data transfer of the Master receiving multiple bytes of data from the Slave.

Speed	FS-mode			HS-mode				
Master	S	M-code	NACK	Sr	SAD + W		RA	
Slave						ACK		ACK

Speed	HS-mode								FS-mode
Master	Sr	SAD + R					NACK	P	
Slave			ACK	DATA	ACK	DATA			

(n-1) bytes + ack.

I²C Timing Diagram

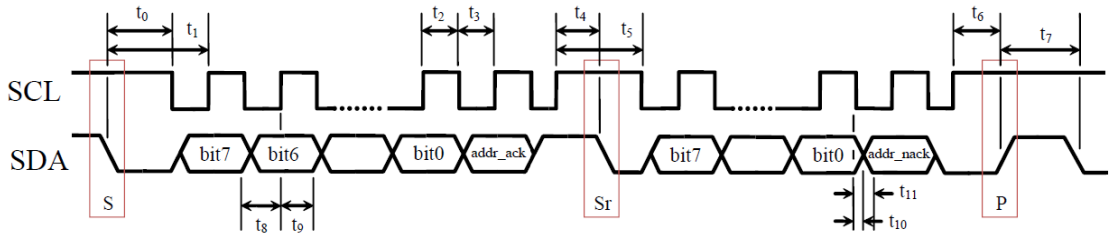

Table 8: I²C Timing (Fast Mode)

Number	Description	MIN	MAX	Units
t_0	SDA low to SCL low transition (Start event)	50	-	ns
t_1	SDA low to first SCL rising edge	100	-	ns
t_2	SCL pulse width: high	100	-	ns
t_3	SCL pulse width: low	100	-	ns
t_4	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: high during a S/Sr/P event	100	-	ns
t_6	SCL high before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: high	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I²C CLK	2.5	-	us

SPI Communications

4-Wire SPI Interface

The KX022 also utilizes an integrated 4-Wire Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The KX022 always operates as a Slave device during standard Master-Slave SPI operation.

4-wire SPI is a synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDI or MOSI) and the Data Input (SDO or MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in Figure 2 below.

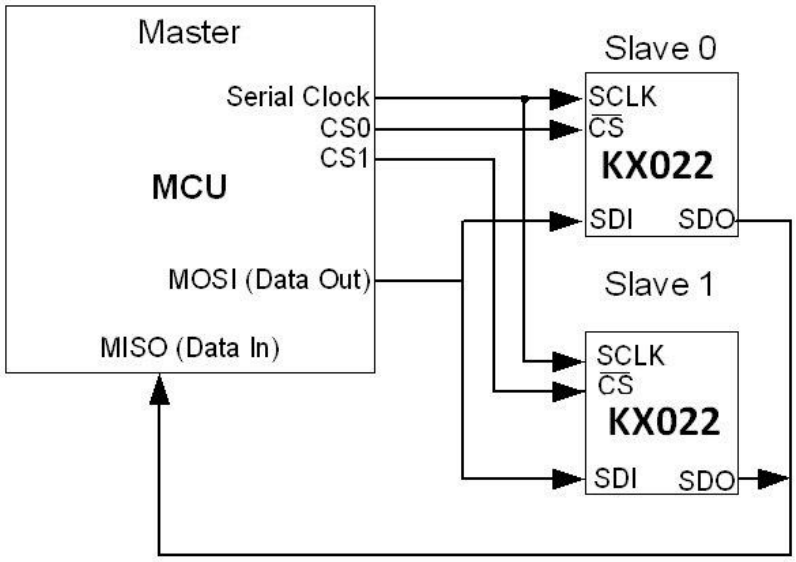

Figure 2: 4-wire SPI Connections