



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# XC228x

16/32-Bit Single-Chip Microcontroller with  
32-Bit Performance

Microcontrollers



Never stop thinking

**Edition 2008-08**

**Published by  
Infineon Technologies AG  
81726 München, Germany**

**© Infineon Technologies AG 2008.  
All Rights Reserved.**

### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffheitsgarantie"). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

### **Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### **Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

# XC228x

16/32-Bit Single-Chip Microcontroller with  
32-Bit Performance

Microcontrollers



Never stop thinking

**XC228x**

**Revision History: V2.1, 2008-08**

Previous Version(s):

V2.0, 2008-03, Preliminary

V0.91, 2007-02, Preliminary

V0.9, 2006-11, Preliminary

<b>Page</b>	<b>Subjects (major changes since last revision)</b>
several	Maximum frequency changed to 80 MHz
<b>34</b>	Voltage domain for XTAL1/XTAL2 corrected to M
<b>75</b>	Coupling factors corrected
<b>80, 82</b>	Improved leakage parameters
<b>81, 83</b>	Pin leakage formula corrected
<b>89</b>	Improved ADC error values
<b>102f</b>	Improved definition of external clock parameters
<b>118</b>	JTAG clock speed corrected

**We Listen to Your Comments**

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document.

Please send your proposal (including a reference to this document) to:

[mcdocu.comments@infineon.com](mailto:mcdocu.comments@infineon.com)



<b>1</b>	<b>Summary of Features</b>	<b>4</b>
<b>2</b>	<b>General Device Information</b>	<b>9</b>
2.1	Pin Configuration and Definition	10
<b>3</b>	<b>Functional Description</b>	<b>37</b>
3.1	Memory Subsystem and Organization	38
3.2	External Bus Controller	41
3.3	Central Processing Unit (CPU)	42
3.4	Interrupt System	44
3.5	On-Chip Debug Support (OCDS)	50
3.6	Capture/Compare Unit (CAPCOM2)	51
3.7	Capture/Compare Units CCU6x	54
3.8	General Purpose Timer (GPT12E) Unit	56
3.9	Real Time Clock	60
3.10	A/D Converters	62
3.11	Universal Serial Interface Channel Modules (USIC)	63
3.12	MultiCAN Module	65
3.13	Watchdog Timer	67
3.14	Clock Generation	67
3.15	Parallel Ports	68
3.16	Power Management	70
3.17	Instruction Set Summary	71
<b>4</b>	<b>Electrical Parameters</b>	<b>74</b>
4.1	General Parameters	74
4.2	DC Parameters	78
4.2.1	DC Parameters for Upper Voltage Area	80
4.2.2	DC Parameters for Lower Voltage Area	82
4.2.3	Power Consumption	84
4.3	Analog/Digital Converter Parameters	89
4.4	System Parameters	92
4.5	Flash Memory Parameters	94
4.6	AC Parameters	96
4.6.1	Testing Waveforms	96
4.6.2	Definition of Internal Timing	97
4.6.3	External Clock Input Parameters	102
4.6.4	External Bus Timing	104
4.6.5	Synchronous Serial Interface Timing	115
4.6.6	JTAG Interface Timing	118
<b>5</b>	<b>Package and Reliability</b>	<b>120</b>
5.1	Packaging	120
5.2	Thermal Considerations	122

## **1 Summary of Features**

For a quick overview and easy reference, the features of the XC228x are summarized here.

- High-performance CPU with five-stage pipeline
  - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1024 Bytes on-chip special function register area (C166 Family compatible)
- Interrupt system with 16 priority levels for up to 87 sources
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- On-chip memory modules
  - 1 Kbyte on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 64 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 768 Kbytes on-chip program memory (Flash memory)
- On-Chip Peripheral Modules
  - Two Synchronizable A/D Converters with up to 24 channels, 10-bit resolution, conversion time below 1 μs, optional data preprocessing (data reduction, range check)
  - 16-channel general purpose capture/compare unit (CAPCOM2)
  - Up to four capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers

**Summary of Features**

- Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
- On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 5 CAN nodes and gateway functionality
- On-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Five programmable chip-select signals
  - Hold- and hold-acknowledge bus arbitration support
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable watchdog timer and oscillator watchdog
- Up to 118 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via JTAG interface
- 144-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

**Ordering Information**

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For ordering codes for the XC228x please contact your sales representative or local distributor.

This document describes several derivatives of the XC228x group. **Table 1** lists these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity the term **XC228x** is used for all derivatives throughout this document.



**Summary of Features**
**Table 1 XC228x Derivative Synopsis**

<b>Derivative<sup>1)</sup></b>	<b>Temp. Range</b>	<b>Program Memory<sup>2)</sup></b>	<b>PSRAM<sup>3)</sup></b>	<b>CCU6 Mod.</b>	<b>ADC<sup>4)</sup> Chan.</b>	<b>Interfaces<sup>4)</sup></b>
SAK-XC2287-96FxxL	-40 °C to 125 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XC2287-96FxxL	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAK-XC2287-72FxxL	-40 °C to 125 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XC2287-72FxxL	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAK-XC2287-56FxxL	-40 °C to 125 °C	448 Kbytes Flash	16 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XC2287-56FxxL	-40 °C to 85 °C	448 Kbytes Flash	16 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAK-XC2286-96FxxL	-40 °C to 125 °C	768 Kbytes Flash	64 Kbytes	0, 1	16 + 8	3 CAN Nodes, 6 Serial Chan.
SAF-XC2286-96FxxL	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	16 + 8	3 CAN Nodes, 6 Serial Chan.
SAK-XC2286-72FxxL	-40 °C to 125 °C	576 Kbytes Flash	32 Kbytes	0, 1	16 + 8	3 CAN Nodes, 6 Serial Chan.
SAF-XC2286-72FxxL	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	16 + 8	3 CAN Nodes, 6 Serial Chan.
SAK-XC2286-56FxxL	-40 °C to 125 °C	448 Kbytes Flash	16 Kbytes	0, 1	16 + 8	3 CAN Nodes, 6 Serial Chan.
SAF-XC2286-56FxxL	-40 °C to 85 °C	448 Kbytes Flash	16 Kbytes	0, 1	16 + 8	3 CAN Nodes, 6 Serial Chan.
SAK-XC2285-96FxxL	-40 °C to 125 °C	768 Kbytes Flash	64 Kbytes	0, 1	16	2 CAN Nodes, 4 Serial Chan.
SAF-XC2285-96FxxL	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	16	2 CAN Nodes, 4 Serial Chan.
SAK-XC2285-72FxxL	-40 °C to 125 °C	576 Kbytes Flash	32 Kbytes	0, 1	16	2 CAN Nodes, 4 Serial Chan.
SAF-XC2285-72FxxL	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	16	2 CAN Nodes, 4 Serial Chan.

**Summary of Features**

**Table 1 XC228x Derivative Synopsis (cont'd)**

<b>Derivative<sup>1)</sup></b>	<b>Temp. Range</b>	<b>Program Memory<sup>2)</sup></b>	<b>PSRAM<sup>3)</sup></b>	<b>CCU6 Mod.</b>	<b>ADC<sup>4)</sup> Chan.</b>	<b>Interfaces<sup>4)</sup></b>
SAK-XC2285-56FxxL	-40 °C to 125 °C	448 Kbytes Flash	16 Kbytes	0, 1	16	2 CAN Nodes, 4 Serial Chan.
SAF-XC2285-56FxxL	-40 °C to 85 °C	448 Kbytes Flash	16 Kbytes	0, 1	16	2 CAN Nodes, 4 Serial Chan.

1) This Data Sheet is valid for devices starting with and including design step AC.

2) Specific information about the on-chip Flash memory in [Table 2](#).

3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM.

4) Specific information about the available channels in [Table 3](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

**Summary of Features**

The XC228x types are offered with several Flash memory sizes. **Table 2** describes the location of the available memory areas for each Flash memory size.

**Table 2 Flash Memory Allocation**

<b>Total Flash Size</b>	<b>Flash Area A<sup>1)</sup></b>	<b>Flash Area B</b>	<b>Flash Area C</b>
768 Kbytes	C0'0000 <sub>H</sub> ... C0'FFFF <sub>H</sub>	C1'0000 <sub>H</sub> ... CB'FFFF <sub>H</sub>	n.a.
576 Kbytes	C0'0000 <sub>H</sub> ... C0'FFFF <sub>H</sub>	C1'0000 <sub>H</sub> ... C8'FFFF <sub>H</sub>	n.a.
448 Kbytes	C0'0000 <sub>H</sub> ... C0'FFFF <sub>H</sub>	C1'0000 <sub>H</sub> ... C5'FFFF <sub>H</sub>	C8'0000 <sub>H</sub> ... C8'FFFF <sub>H</sub>

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000<sub>H</sub> to C0'FFFF<sub>H</sub>).

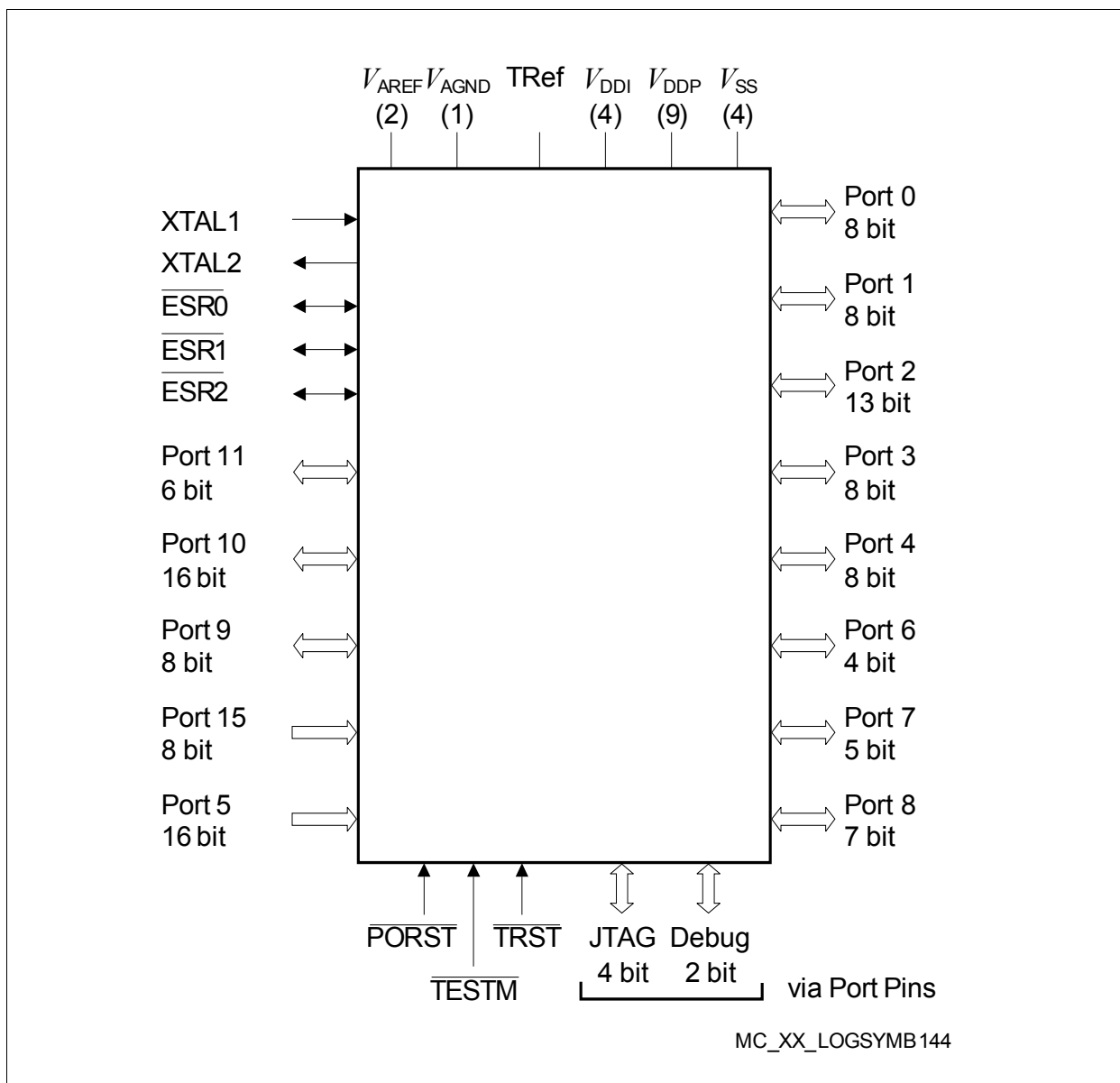
The XC228x types are offered with different interface options. **Table 3** lists the available channels for each option.

**Table 3 Interface Channel Association**

<b>Total Number</b>	<b>Available Channels</b>
16 ADC0 channels	CH0 ... CH15
8 ADC1 channels	CH0 ... CH7
5 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4
3 CAN nodes	CAN0, CAN1, CAN2
2 CAN nodes	CAN0, CAN1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1
4 serial channels	U0C0, U0C1, U1C0, U1C1

## 2 General Device Information

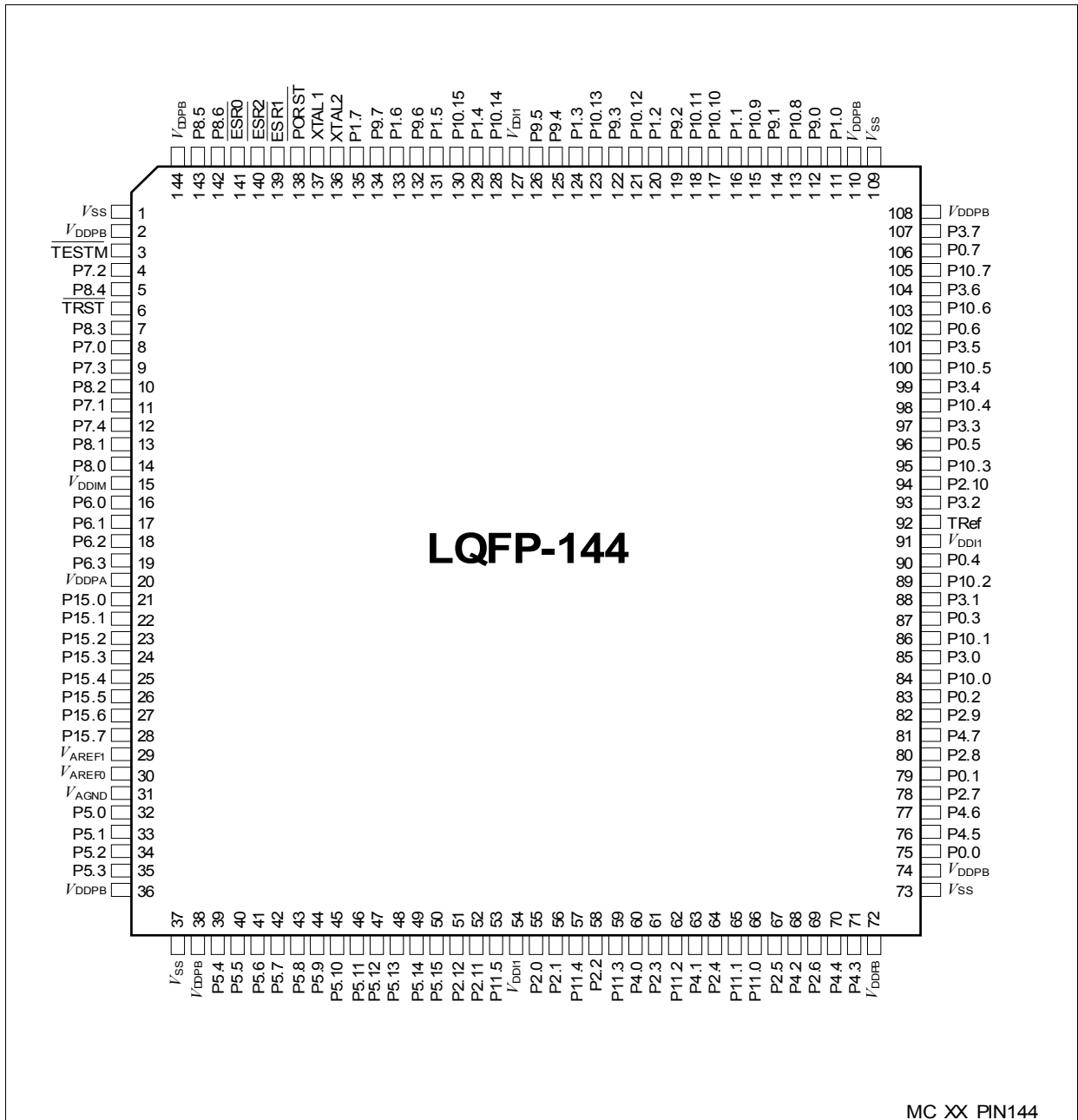
The XC228x derivatives are high-performance members of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.



**Figure 1 Logic Symbol**

## 2.1 Pin Configuration and Definition

The pins of the XC228x are described in detail in [Table 4](#), which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. [Figure 2](#) summarizes all pins, showing their locations on the four sides of the package.



**Figure 2 Pin Configuration (top view)**

**Notes to Pin Definitions**

1. **Ctrl.:** The output signal for a port pin is selected by bitfield PC in the associated register Px\_IOCry. Output O0 is selected by setting the respective bitfield PC to 1x00<sub>B</sub>, output O1 is selected by 1x01<sub>B</sub>, etc.  
Output signal OH is controlled by hardware.
2. **Type:** Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).

**Table 4 Pin Definitions and Functions**

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	<b>Testmode Enable</b> Enables factory test modes, must be held HIGH for normal operation (connect to $V_{\text{DDPB}}$ ). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	<b>Bit 2 of Port 7, General Purpose Input/Output</b>
	EMUX0	O1	St/B	<b>External Analog MUX Control Output 0 (ADC1)</b>
	TxDC4	O2	St/B	<b>CAN Node 4 Transmit Data Output</b>
	CCU62_ CCPOS0A	I	St/B	<b>CCU62 Position Input 0</b>
	TDI_C	I	St/B	<b>JTAG Test Data Input</b>
5	P8.4	O0 / I	St/B	<b>Bit 4 of Port 8, General Purpose Input/Output</b>
	CCU60_ COUT61	O1	St/B	<b>CCU60 Channel 1 Output</b>
	TMS_D	I	St/B	<b>JTAG Test Mode Selection Input</b>
6	$\overline{\text{TRST}}$	I	In/B	<b>Test-System Reset Input</b> For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC228x's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	<b>Bit 3 of Port 8, General Purpose Input/Output</b>
	CCU60_ COUT60	O1	St/B	<b>CCU60 Channel 0 Output</b>
	TDI_D	I	St/B	<b>JTAG Test Data Input</b>

**Table 4 Pin Definitions and Functions (cont'd)**

<b>Pin</b>	<b>Symbol</b>	<b>Ctrl.</b>	<b>Type</b>	<b>Function</b>
8	P7.0	O0 / I	St/B	<b>Bit 0 of Port 7, General Purpose Input/Output</b>
	T3OUT	O1	St/B	<b>GPT1 Timer T3 Toggle Latch Output</b>
	T6OUT	O2	St/B	<b>GPT2 Timer T6 Toggle Latch Output</b>
	TDO_A	OH	St/B	<b>JTAG Test Data Output</b>
	ESR2_1	I	St/B	<b>ESR2 Trigger Input 1</b>
	RxDC4B	I	St/B	<b>CAN Node 4 Receive Data Input</b>
9	P7.3	O0 / I	St/B	<b>Bit 3 of Port 7, General Purpose Input/Output</b>
	EMUX1	O1	St/B	<b>External Analog MUX Control Output 1 (ADC1)</b>
	U0C1_DOUT	O2	St/B	<b>USIC0 Channel 1 Shift Data Output</b>
	U0C0_DOUT	O3	St/B	<b>USIC0 Channel 0 Shift Data Output</b>
	CCU62_ CCPOS1A	I	St/B	<b>CCU62 Position Input 1</b>
	TMS_C	I	St/B	<b>JTAG Test Mode Selection Input</b>
	U0C1_DX0F	I	St/B	<b>USIC0 Channel 1 Shift Data Input</b>
10	P8.2	O0 / I	St/B	<b>Bit 2 of Port 8, General Purpose Input/Output</b>
	CCU60_ CC62	O1 / I	St/B	<b>CCU60 Channel 2 Input/Output</b>
11	P7.1	O0 / I	St/B	<b>Bit 1 of Port 7, General Purpose Input/Output</b>
	EXTCLK	O1	St/B	<b>Programmable Clock Signal Output</b>
	TxDC4	O2	St/B	<b>CAN Node 4 Transmit Data Output</b>
	CCU62_ CTRAPA	I	St/B	<b>CCU62 Emergency Trap Input</b>
	BRKIN_C	I	St/B	<b>OCDS Break Signal Input</b>

**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
12	P7.4	O0 / I	St/B	<b>Bit 4 of Port 7, General Purpose Input/Output</b>
	EMUX2	O1	St/B	<b>External Analog MUX Control Output 2 (ADC1)</b>
	U0C1_DOUT	O2	St/B	<b>USIC0 Channel 1 Shift Data Output</b>
	U0C1_SCLKOUT	O3	St/B	<b>USIC0 Channel 1 Shift Clock Output</b>
	CCU62_CCPOS2A	I	St/B	<b>CCU62 Position Input 2</b>
	TCK_C	I	St/B	<b>JTAG Clock Input</b>
	U0C0_DX0D	I	St/B	<b>USIC0 Channel 0 Shift Data Input</b>
	U0C1_DX1E	I	St/B	<b>USIC0 Channel 1 Shift Clock Input</b>
13	P8.1	O0 / I	St/B	<b>Bit 1 of Port 8, General Purpose Input/Output</b>
	CCU60_CC61	O1 / I	St/B	<b>CCU60 Channel 1 Input/Output</b>
14	P8.0	O0 / I	St/B	<b>Bit 0 of Port 8, General Purpose Input/Output</b>
	CCU60_CC60	O1 / I	St/B	<b>CCU60 Channel 0 Input/Output</b>
16	P6.0	O0 / I	St/A	<b>Bit 0 of Port 6, General Purpose Input/Output</b>
	EMUX0	O1	St/A	<b>External Analog MUX Control Output 0 (ADC0)</b>
	$\overline{\text{BRKOUT}}$	O3	St/A	<b>OCDS Break Signal Output</b>
	ADCx_REQGTyC	I	St/A	<b>External Request Gate Input for ADC0/1</b>
	U1C1_DX0E	I	St/A	<b>USIC1 Channel 1 Shift Data Input</b>
17	P6.1	O0 / I	St/A	<b>Bit 1 of Port 6, General Purpose Input/Output</b>
	EMUX1	O1	St/A	<b>External Analog MUX Control Output 1 (ADC0)</b>
	T3OUT	O2	St/A	<b>GPT1 Timer T3 Toggle Latch Output</b>
	U1C1_DOUT	O3	St/A	<b>USIC1 Channel 1 Shift Data Output</b>
	ADCx_REQTRYC	I	St/A	<b>External Request Trigger Input for ADC0/1</b>



**Table 4 Pin Definitions and Functions (cont'd)**

<b>Pin</b>	<b>Symbol</b>	<b>Ctrl.</b>	<b>Type</b>	<b>Function</b>
18	P6.2	O0 / I	St/A	<b>Bit 2 of Port 6, General Purpose Input/Output</b>
	EMUX2	O1	St/A	<b>External Analog MUX Control Output 2 (ADC0)</b>
	T6OUT	O2	St/A	<b>GPT2 Timer T6 Toggle Latch Output</b>
	U1C1_SCLKOUT	O3	St/A	<b>USIC1 Channel 1 Shift Clock Output</b>
	U1C1_DX1C	I	St/A	<b>USIC1 Channel 1 Shift Clock Input</b>
19	P6.3	O0 / I	St/A	<b>Bit 3 of Port 6, General Purpose Input/Output</b>
	T3OUT	O2	St/A	<b>GPT1 Timer T3 Toggle Latch Output</b>
	U1C1_SELO0	O3	St/A	<b>USIC1 Channel 1 Select/Control 0 Output</b>
	U1C1_DX2D	I	St/A	<b>USIC1 Channel 1 Shift Control Input</b>
	ADCx_REQTRyD	I	St/A	<b>External Request Trigger Input for ADC0/1</b>
21	P15.0	I	In/A	<b>Bit 0 of Port 15, General Purpose Input</b>
	ADC1_CH0	I	In/A	<b>Analog Input Channel 0 for ADC1</b>
22	P15.1	I	In/A	<b>Bit 1 of Port 15, General Purpose Input</b>
	ADC1_CH1	I	In/A	<b>Analog Input Channel 1 for ADC1</b>
23	P15.2	I	In/A	<b>Bit 2 of Port 15, General Purpose Input</b>
	ADC1_CH2	I	In/A	<b>Analog Input Channel 2 for ADC1</b>
	T5IN	I	In/A	<b>GPT2 Timer T5 Count/Gate Input</b>
24	P15.3	I	In/A	<b>Bit 3 of Port 15, General Purpose Input</b>
	ADC1_CH3	I	In/A	<b>Analog Input Channel 3 for ADC1</b>
	T5EUD	I	In/A	<b>GPT2 Timer T5 External Up/Down Control Input</b>
25	P15.4	I	In/A	<b>Bit 4 of Port 15, General Purpose Input</b>
	ADC1_CH4	I	In/A	<b>Analog Input Channel 4 for ADC1</b>
	T6IN	I	In/A	<b>GPT2 Timer T6 Count/Gate Input</b>
26	P15.5	I	In/A	<b>Bit 5 of Port 15, General Purpose Input</b>
	ADC1_CH5	I	In/A	<b>Analog Input Channel 5 for ADC1</b>
	T6EUD	I	In/A	<b>GPT2 Timer T6 External Up/Down Control Input</b>
27	P15.6	I	In/A	<b>Bit 6 of Port 15, General Purpose Input</b>
	ADC1_CH6	I	In/A	<b>Analog Input Channel 6 for ADC1</b>

**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
28	P15.7	I	In/A	<b>Bit 7 of Port 15, General Purpose Input</b>
	ADC1_CH7	I	In/A	<b>Analog Input Channel 7 for ADC1</b>
29	$V_{AREF1}$	-	PS/A	<b>Reference Voltage for A/D Converter ADC1</b>
30	$V_{AREF0}$	-	PS/A	<b>Reference Voltage for A/D Converter ADC0</b>
31	$V_{AGND}$	-	PS/A	<b>Reference Ground for A/D Converters ADC0/1</b>
32	P5.0	I	In/A	<b>Bit 0 of Port 5, General Purpose Input</b>
	ADC0_CH0	I	In/A	<b>Analog Input Channel 0 for ADC0</b>
33	P5.1	I	In/A	<b>Bit 1 of Port 5, General Purpose Input</b>
	ADC0_CH1	I	In/A	<b>Analog Input Channel 1 for ADC0</b>
34	P5.2	I	In/A	<b>Bit 2 of Port 5, General Purpose Input</b>
	ADC0_CH2	I	In/A	<b>Analog Input Channel 2 for ADC0</b>
	TDI_A	I	In/A	<b>JTAG Test Data Input</b>
35	P5.3	I	In/A	<b>Bit 3 of Port 5, General Purpose Input</b>
	ADC0_CH3	I	In/A	<b>Analog Input Channel 3 for ADC0</b>
	T3IN	I	In/A	<b>GPT1 Timer T3 Count/Gate Input</b>
39	P5.4	I	In/A	<b>Bit 4 of Port 5, General Purpose Input</b>
	ADC0_CH4	I	In/A	<b>Analog Input Channel 4 for ADC0</b>
	CCU63_T12HRB	I	In/A	<b>External Run Control Input for T12 of CCU63</b>
	T3EUD	I	In/A	<b>GPT1 Timer T3 External Up/Down Control Input</b>
	TMS_A	I	In/A	<b>JTAG Test Mode Selection Input</b>
40	P5.5	I	In/A	<b>Bit 5 of Port 5, General Purpose Input</b>
	ADC0_CH5	I	In/A	<b>Analog Input Channel 5 for ADC0</b>
	CCU60_T12HRB	I	In/A	<b>External Run Control Input for T12 of CCU60</b>
41	P5.6	I	In/A	<b>Bit 6 of Port 5, General Purpose Input</b>
	ADC0_CH6	I	In/A	<b>Analog Input Channel 6 for ADC0</b>
42	P5.7	I	In/A	<b>Bit 7 of Port 5, General Purpose Input</b>
	ADC0_CH7	I	In/A	<b>Analog Input Channel 7 for ADC0</b>

**Table 4 Pin Definitions and Functions (cont'd)**

<b>Pin</b>	<b>Symbol</b>	<b>Ctrl.</b>	<b>Type</b>	<b>Function</b>
43	P5.8	I	In/A	<b>Bit 8 of Port 5, General Purpose Input</b>
	ADC0_CH8	I	In/A	<b>Analog Input Channel 8 for ADC0</b>
	CCU6x_T12HRC	I	In/A	<b>External Run Control Input for T12 of CCU6x</b>
	CCU6x_T13HRC	I	In/A	<b>External Run Control Input for T13 of CCU6x</b>
44	P5.9	I	In/A	<b>Bit 9 of Port 5, General Purpose Input</b>
	ADC0_CH9	I	In/A	<b>Analog Input Channel 9 for ADC0</b>
	CC2_T7IN	I	In/A	<b>CAPCOM2 Timer T7 Count Input</b>
45	P5.10	I	In/A	<b>Bit 10 of Port 5, General Purpose Input</b>
	ADC0_CH10	I	In/A	<b>Analog Input Channel 10 for ADC0</b>
	BRKIN_A	I	In/A	<b>OCDS Break Signal Input</b>
46	P5.11	I	In/A	<b>Bit 11 of Port 5, General Purpose Input</b>
	ADC0_CH11	I	In/A	<b>Analog Input Channel 11 for ADC0</b>
47	P5.12	I	In/A	<b>Bit 12 of Port 5, General Purpose Input</b>
	ADC0_CH12	I	In/A	<b>Analog Input Channel 12 for ADC0</b>
48	P5.13	I	In/A	<b>Bit 13 of Port 5, General Purpose Input</b>
	ADC0_CH13	I	In/A	<b>Analog Input Channel 13 for ADC0</b>
	EX0BINB	I	In/A	<b>External Interrupt Trigger Input</b>
49	P5.14	I	In/A	<b>Bit 14 of Port 5, General Purpose Input</b>
	ADC0_CH14	I	In/A	<b>Analog Input Channel 14 for ADC0</b>
50	P5.15	I	In/A	<b>Bit 15 of Port 5, General Purpose Input</b>
	ADC0_CH15	I	In/A	<b>Analog Input Channel 15 for ADC0</b>
51	P2.12	O0 / I	St/B	<b>Bit 12 of Port 2, General Purpose Input/Output</b>
	U0C0_SELO4	O1	St/B	<b>USIC0 Channel 0 Select/Control 4 Output</b>
	U0C1_SELO3	O2	St/B	<b>USIC0 Channel 1 Select/Control 3 Output</b>
	READY	I	St/B	<b>External Bus Interface READY Input</b>

**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
52	P2.11	O0 / I	St/B	<b>Bit 11 of Port 2, General Purpose Input/Output</b>
	U0C0_SELO2	O1	St/B	<b>USIC0 Channel 0 Select/Control 2 Output</b>
	U0C1_SELO2	O2	St/B	<b>USIC0 Channel 1 Select/Control 2 Output</b>
	$\overline{\text{BHE}}/\overline{\text{WRH}}$	OH	St/B	<b>External Bus Interf. High-Byte Control Output</b> Can operate either as Byte High Enable ( $\overline{\text{BHE}}$ ) or as Write strobe for High Byte ( $\overline{\text{WRH}}$ ).
53	P11.5	O0 / I	St/B	<b>Bit 5 of Port 11, General Purpose Input/Output</b>
55	P2.0	O0 / I	St/B	<b>Bit 0 of Port 2, General Purpose Input/Output</b>
	CCU63_CC60	O2 / I	St/B	<b>CCU63 Channel 0 Input/Output</b>
	AD13	OH / I	St/B	<b>External Bus Interface Address/Data Line 13</b>
	RxDC0C	I	St/B	<b>CAN Node 0 Receive Data Input</b>
56	P2.1	O0 / I	St/B	<b>Bit 1 of Port 2, General Purpose Input/Output</b>
	TxDC0	O1	St/B	<b>CAN Node 0 Transmit Data Output</b>
	CCU63_CC61	O2 / I	St/B	<b>CCU63 Channel 1 Input/Output</b>
	AD14	OH / I	St/B	<b>External Bus Interface Address/Data Line 14</b>
	ESR1_5	I	St/B	<b>ESR1 Trigger Input 5</b>
	EX0AINA	I	St/B	<b>External Interrupt Trigger Input</b>
57	P11.4	O0 / I	St/B	<b>Bit 4 of Port 11, General Purpose Input/Output</b>
58	P2.2	O0 / I	St/B	<b>Bit 2 of Port 2, General Purpose Input/Output</b>
	TxDC1	O1	St/B	<b>CAN Node 1 Transmit Data Output</b>
	CCU63_CC62	O2 / I	St/B	<b>CCU63 Channel 2 Input/Output</b>
	AD15	OH / I	St/B	<b>External Bus Interface Address/Data Line 15</b>
	ESR2_5	I	St/B	<b>ESR2 Trigger Input 5</b>
	EX1AINA	I	St/B	<b>External Interrupt Trigger Input</b>
59	P11.3	O0 / I	St/B	<b>Bit 3 of Port 11, General Purpose Input/Output</b>

**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
60	P4.0	O0 / I	St/B	<b>Bit 0 of Port 4, General Purpose Input/Output</b>
	CC2_24	O3 / I	St/B	<b>CAPCOM2 CC24IO Capture Inp./ Compare Out.</b>
	$\overline{\text{CS0}}$	OH	St/B	<b>External Bus Interface Chip Select 0 Output</b>
61	P2.3	O0 / I	St/B	<b>Bit 3 of Port 2, General Purpose Input/Output</b>
	U0C0_DOUT	O1	St/B	<b>USIC0 Channel 0 Shift Data Output</b>
	CCU63_COUT63	O2	St/B	<b>CCU63 Channel 3 Output</b>
	CC2_16	O3 / I	St/B	<b>CAPCOM2 CC16IO Capture Inp./ Compare Out.</b>
	A16	OH	St/B	<b>External Bus Interface Address Line 16</b>
	ESR2_0	I	St/B	<b>ESR2 Trigger Input 0</b>
	U0C0_DX0E	I	St/B	<b>USIC0 Channel 0 Shift Data Input</b>
	U0C1_DX0D	I	St/B	<b>USIC0 Channel 1 Shift Data Input</b>
	RxDC0A	I	St/B	<b>CAN Node 0 Receive Data Input</b>
62	P11.2	O0 / I	St/B	<b>Bit 2 of Port 11, General Purpose Input/Output</b>
	CCU63_CCPOS2A	I	St/B	<b>CCU63 Position Input 2</b>
63	P4.1	O0 / I	St/B	<b>Bit 1 of Port 4, General Purpose Input/Output</b>
	TxDC2	O2	St/B	<b>CAN Node 2 Transmit Data Output</b>
	CC2_25	O3 / I	St/B	<b>CAPCOM2 CC25IO Capture Inp./ Compare Out.</b>
	$\overline{\text{CS1}}$	OH	St/B	<b>External Bus Interface Chip Select 1 Output</b>
64	P2.4	O0 / I	St/B	<b>Bit 4 of Port 2, General Purpose Input/Output</b>
	U0C1_DOUT	O1	St/B	<b>USIC0 Channel 1 Shift Data Output</b>
	TxDC0	O2	St/B	<b>CAN Node 0 Transmit Data Output</b>
	CC2_17	O3 / I	St/B	<b>CAPCOM2 CC17IO Capture Inp./ Compare Out.</b>
	A17	OH	St/B	<b>External Bus Interface Address Line 17</b>
	ESR1_0	I	St/B	<b>ESR1 Trigger Input 0</b>
	U0C0_DX0F	I	St/B	<b>USIC0 Channel 0 Shift Data Input</b>
	RxDC1A	I	St/B	<b>CAN Node 1 Receive Data Input</b>
65	P11.1	O0 / I	St/B	<b>Bit 1 of Port 11, General Purpose Input/Output</b>
	CCU63_CCPOS1A	I	St/B	<b>CCU63 Position Input 1</b>

**General Device Information**
**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
66	P11.0	O0 / I	St/B	<b>Bit 0 of Port 11, General Purpose Input/Output</b>
	CCU63_ CCPOS0A	I	St/B	<b>CCU63 Position Input 0</b>
67	P2.5	O0 / I	St/B	<b>Bit 5 of Port 2, General Purpose Input/Output</b>
	U0C0_ SCLKOUT	O1	St/B	<b>USIC0 Channel 0 Shift Clock Output</b>
	TxDC0	O2	St/B	<b>CAN Node 0 Transmit Data Output</b>
	CC2_18	O3 / I	St/B	<b>CAPCOM2 CC18IO Capture Inp./ Compare Out.</b>
	A18	OH	St/B	<b>External Bus Interface Address Line 18</b>
	U0C0_DX1D	I	St/B	<b>USIC0 Channel 0 Shift Clock Input</b>
68	P4.2	O0 / I	St/B	<b>Bit 2 of Port 4, General Purpose Input/Output</b>
	TxDC2	O2	St/B	<b>CAN Node 2 Transmit Data Output</b>
	CC2_26	O3 / I	St/B	<b>CAPCOM2 CC26IO Capture Inp./ Compare Out.</b>
	CS2	OH	St/B	<b>External Bus Interface Chip Select 2 Output</b>
	T2IN	I	St/B	<b>GPT1 Timer T2 Count/Gate Input</b>
69	P2.6	O0 / I	St/B	<b>Bit 6 of Port 2, General Purpose Input/Output</b>
	U0C0_ SELO0	O1	St/B	<b>USIC0 Channel 0 Select/Control 0 Output</b>
	U0C1_ SELO1	O2	St/B	<b>USIC0 Channel 1 Select/Control 1 Output</b>
	CC2_19	O3 / I	St/B	<b>CAPCOM2 CC19IO Capture Inp./ Compare Out.</b>
	A19	OH	St/B	<b>External Bus Interface Address Line 19</b>
	U0C0_DX2D	I	St/B	<b>USIC0 Channel 0 Shift Control Input</b>
	RxDC0D	I	St/B	<b>CAN Node 0 Receive Data Input</b>
70	P4.4	O0 / I	St/B	<b>Bit 4 of Port 4, General Purpose Input/Output</b>
	CC2_28	O3 / I	St/B	<b>CAPCOM2 CC28IO Capture Inp./ Compare Out.</b>
	CS4	OH	St/B	<b>External Bus Interface Chip Select 4 Output</b>
	CLKIN2	I	St/B	<b>RTC Count Clock Signal Input</b>

**Table 4 Pin Definitions and Functions (cont'd)**

<b>Pin</b>	<b>Symbol</b>	<b>Ctrl.</b>	<b>Type</b>	<b>Function</b>
71	P4.3	O0 / I	St/B	<b>Bit 3 of Port 4, General Purpose Input/Output</b>
	CC2_27	O3 / I	St/B	<b>CAPCOM2 CC27IO Capture Inp./ Compare Out.</b>
	CS3	OH	St/B	<b>External Bus Interface Chip Select 3 Output</b>
	RxDC2A	I	St/B	<b>CAN Node 2 Receive Data Input</b>
	T2EUD	I	St/B	<b>GPT1 Timer T2 External Up/Down Control Input</b>
75	P0.0	O0 / I	St/B	<b>Bit 0 of Port 0, General Purpose Input/Output</b>
	U1C0_DOUT	O1	St/B	<b>USIC1 Channel 0 Shift Data Output</b>
	CCU61_ CC60	O3 / I	St/B	<b>CCU61 Channel 0 Input/Output</b>
	A0	OH	St/B	<b>External Bus Interface Address Line 0</b>
	U1C0_DX0A	I	St/B	<b>USIC1 Channel 0 Shift Data Input</b>
76	P4.5	O0 / I	St/B	<b>Bit 5 of Port 4, General Purpose Input/Output</b>
	CC2_29	O3 / I	St/B	<b>CAPCOM2 CC29IO Capture Inp./Compare Out.</b>
77	P4.6	O0 / I	St/B	<b>Bit 6 of Port 4, General Purpose Input/Output</b>
	CC2_30	O3 / I	St/B	<b>CAPCOM2 CC30IO Capture Inp./ Compare Out.</b>
	T4IN	I	St/B	<b>GPT1 Timer T4 Count/Gate Input</b>
78	P2.7	O0 / I	St/B	<b>Bit 7 of Port 2, General Purpose Input/Output</b>
	U0C1_ SELO0	O1	St/B	<b>USIC0 Channel 1 Select/Control 0 Output</b>
	U0C0_ SELO1	O2	St/B	<b>USIC0 Channel 0 Select/Control 1 Output</b>
	CC2_20	O3 / I	St/B	<b>CAPCOM2 CC20IO Capture Inp./ Compare Out.</b>
	A20	OH	St/B	<b>External Bus Interface Address Line 20</b>
	U0C1_DX2C	I	St/B	<b>USIC0 Channel 1 Shift Control Input</b>
	RxDC1C	I	St/B	<b>CAN Node 1 Receive Data Input</b>

**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
79	P0.1	O0 / I	St/B	<b>Bit 1 of Port 0, General Purpose Input/Output</b>
	U1C0_DOUT	O1	St/B	<b>USIC1 Channel 0 Shift Data Output</b>
	TxDC0	O2	St/B	<b>CAN Node 0 Transmit Data Output</b>
	CCU61_ CC61	O3 / I	St/B	<b>CCU61 Channel 1 Input/Output</b>
	A1	OH	St/B	<b>External Bus Interface Address Line 1</b>
	U1C0_DX0B	I	St/B	<b>USIC1 Channel 0 Shift Data Input</b>
	U1C0_DX1A	I	St/B	<b>USIC1 Channel 0 Shift Clock Input</b>
80	P2.8	O0 / I	DP/B	<b>Bit 8 of Port 2, General Purpose Input/Output</b>
	U0C1_ SCLKOUT	O1	DP/B	<b>USIC0 Channel 1 Shift Clock Output</b>
	EXTCLK	O2	DP/B	<b>Programmable Clock Signal Output</b> 1)
	CC2_21	O3 / I	DP/B	<b>CAPCOM2 CC21IO Capture Inp./ Compare Out.</b>
	A21	OH	DP/B	<b>External Bus Interface Address Line 21</b>
	U0C1_DX1D	I	DP/B	<b>USIC0 Channel 1 Shift Clock Input</b>
81	P4.7	O0 / I	St/B	<b>Bit 7 of Port 4, General Purpose Input/Output</b>
	CC2_31	O3 / I	St/B	<b>CAPCOM2 CC31IO Capture Inp./ Compare Out.</b>
	T4EUD	I	St/B	<b>GPT1 Timer T4 External Up/Down Control Input</b>
82	P2.9	O0 / I	St/B	<b>Bit 9 of Port 2, General Purpose Input/Output</b>
	U0C1_DOUT	O1	St/B	<b>USIC0 Channel 1 Shift Data Output</b>
	TxDC1	O2	St/B	<b>CAN Node 1 Transmit Data Output</b>
	CC2_22	O3 / I	St/B	<b>CAPCOM2 CC22IO Capture Inp./ Compare Out.</b>
	A22	OH	St/B	<b>External Bus Interface Address Line 22</b>
	CLKIN1	I	St/B	<b>Clock Signal Input</b>
	TCK_A	I	St/B	<b>JTAG Clock Input</b>



**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
83	P0.2	O0 / I	St/B	<b>Bit 2 of Port 0, General Purpose Input/Output</b>
	U1C0_SCLKOUT	O1	St/B	<b>USIC1 Channel 0 Shift Clock Output</b>
	TxDC0	O2	St/B	<b>CAN Node 0 Transmit Data Output</b>
	CCU61_CC62	O3 / I	St/B	<b>CCU61 Channel 2 Input/Output</b>
	A2	OH	St/B	<b>External Bus Interface Address Line 2</b>
	U1C0_DX1B	I	St/B	<b>USIC1 Channel 0 Shift Clock Input</b>
84	P10.0	O0 / I	St/B	<b>Bit 0 of Port 10, General Purpose Input/Output</b>
	U0C1_DOUT	O1	St/B	<b>USIC0 Channel 1 Shift Data Output</b>
	CCU60_CC60	O2 / I	St/B	<b>CCU60 Channel 0 Input/Output</b>
	AD0	OH / I	St/B	<b>External Bus Interface Address/Data Line 0</b>
	ESR1_2	I	St/B	<b>ESR1 Trigger Input 2</b>
	U0C0_DX0A	I	St/B	<b>USIC0 Channel 0 Shift Data Input</b>
	U0C1_DX0A	I	St/B	<b>USIC0 Channel 1 Shift Data Input</b>
85	P3.0	O0 / I	St/B	<b>Bit 0 of Port 3, General Purpose Input/Output</b>
	U2C0_DOUT	O1	St/B	<b>USIC2 Channel 0 Shift Data Output</b>
	BREQ	OH	St/B	<b>External Bus Request Output</b>
	ESR1_1	I	St/B	<b>ESR1 Trigger Input 1</b>
	U2C0_DX0A	I	St/B	<b>USIC2 Channel 0 Shift Data Input</b>
	RxDC3B	I	St/B	<b>CAN Node 3 Receive Data Input</b>
	U2C0_DX1A	I	St/B	<b>USIC2 Channel 0 Shift Clock Input</b>
86	P10.1	O0 / I	St/B	<b>Bit 1 of Port 10, General Purpose Input/Output</b>
	U0C0_DOUT	O1	St/B	<b>USIC0 Channel 0 Shift Data Output</b>
	CCU60_CC61	O2 / I	St/B	<b>CCU60 Channel 1 Input/Output</b>
	AD1	OH / I	St/B	<b>External Bus Interface Address/Data Line 1</b>
	U0C0_DX0B	I	St/B	<b>USIC0 Channel 0 Shift Data Input</b>
	U0C0_DX1A	I	St/B	<b>USIC0 Channel 0 Shift Clock Input</b>

**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
87	P0.3	O0 / I	St/B	<b>Bit 3 of Port 0, General Purpose Input/Output</b>
	U1C0_SELO0	O1	St/B	<b>USIC1 Channel 0 Select/Control 0 Output</b>
	U1C1_SELO1	O2	St/B	<b>USIC1 Channel 1 Select/Control 1 Output</b>
	CCU61_COUT60	O3	St/B	<b>CCU61 Channel 0 Output</b>
	A3	OH	St/B	<b>External Bus Interface Address Line 3</b>
	U1C0_DX2A	I	St/B	<b>USIC1 Channel 0 Shift Control Input</b>
	RxDC0B	I	St/B	<b>CAN Node 0 Receive Data Input</b>
88	P3.1	O0 / I	St/B	<b>Bit 1 of Port 3, General Purpose Input/Output</b>
	U2C0_DOUT	O1	St/B	<b>USIC2 Channel 0 Shift Data Output</b>
	TxDC3	O2	St/B	<b>CAN Node 3 Transmit Data Output</b>
	HLDA	OH / I	St/B	<b>External Bus Hold Acknowledge Output/Input</b> Output in master mode, input in slave mode.
	U2C0_DX0B	I	St/B	<b>USIC2 Channel 0 Shift Data Input</b>
89	P10.2	O0 / I	St/B	<b>Bit 2 of Port 10, General Purpose Input/Output</b>
	U0C0_SCLKOUT	O1	St/B	<b>USIC0 Channel 0 Shift Clock Output</b>
	CCU60_CC62	O2 / I	St/B	<b>CCU60 Channel 2 Input/Output</b>
	AD2	OH / I	St/B	<b>External Bus Interface Address/Data Line 2</b>
	U0C0_DX1B	I	St/B	<b>USIC0 Channel 0 Shift Clock Input</b>
90	P0.4	O0 / I	St/B	<b>Bit 4 of Port 0, General Purpose Input/Output</b>
	U1C1_SELO0	O1	St/B	<b>USIC1 Channel 1 Select/Control 0 Output</b>
	U1C0_SELO1	O2	St/B	<b>USIC1 Channel 0 Select/Control 1 Output</b>
	CCU61_COUT61	O3	St/B	<b>CCU61 Channel 1 Output</b>
	A4	OH	St/B	<b>External Bus Interface Address Line 4</b>
	U1C1_DX2A	I	St/B	<b>USIC1 Channel 1 Shift Control Input</b>
	RxDC1B	I	St/B	<b>CAN Node 1 Receive Data Input</b>