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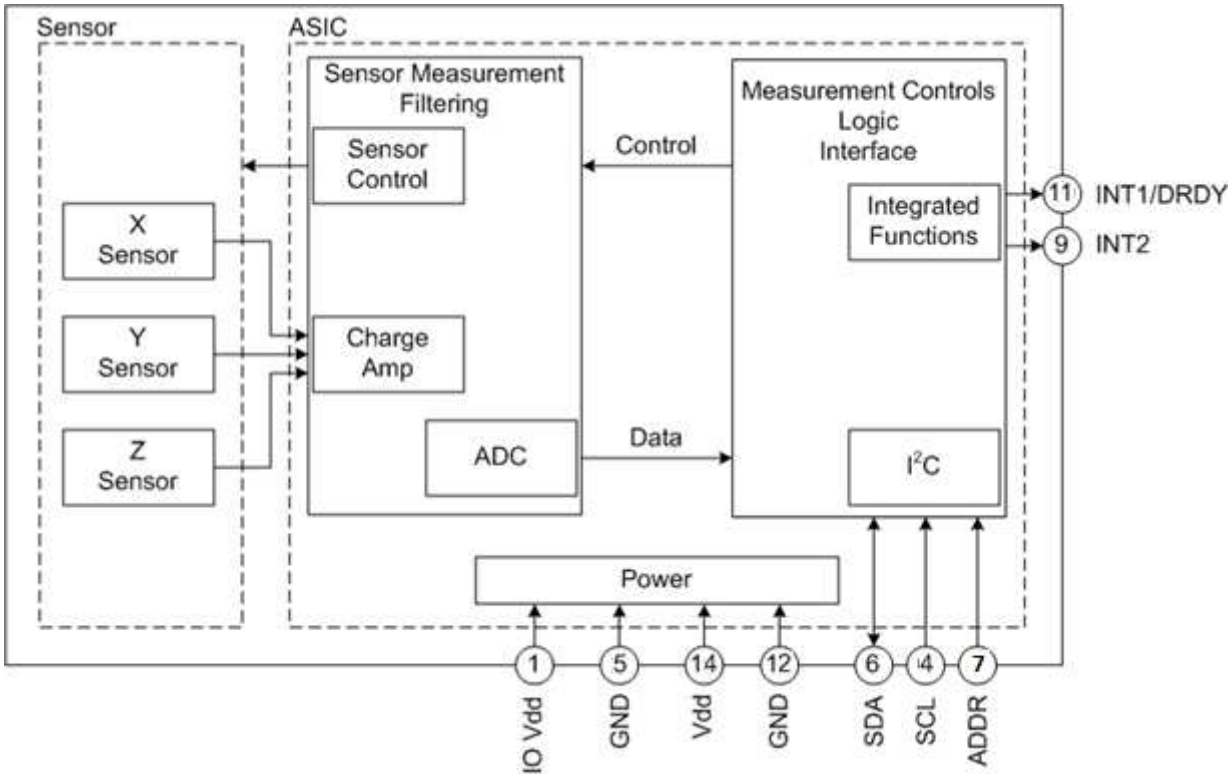
Kionix®	**± 2g / 4g / 6g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXCNL-1010** **Rev 3.0**

Product Description

The KXCNL-1010 is a tri-axis +/-2g, +/-4g, +/-6g, or +/-8g silicon micromachined accelerometer with integrated programmable state machines. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable state machines. The accelerometer is delivered in a 3 x 3 x 0.9 mm LGA plastic package operating from a 1.8 – 3.6V DC supply. I^2C interface is used to communicate to the chip to load state programs, configure settings, and check updates to the acceleration data.

Functional Diagram



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Product Specifications

Table 1. Mechanical

(specifications are for 12-bit operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Zero-g Offset		mg		±25	
Zero-g Offset Variation from RT over Temp.		mg/ºC		0.5 (xy), 0.8 (z)	
Sensitivity[1]	SC_1=0, SC_0=0 (± 2g)	counts/g		1024	
	SC_1=0, SC_0=1 (± 4g)			512	
	SC_1=1, SC_0=0 (± 6g)			341	
	SC_1=1, SC_0=1 (± 8g)			256	
Sensitivity Variation from RT over Temp.		%/ºC		0.01	
Self Test Output change on Activation		g		0.5 (x) 0.7 (y) 0.7 (z)	
Mechanical Resonance (-3dB)[2]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.5	
Cross Axis Sensitivity		%		2	
Noise[3]		µg/sqrt(Hz)		400	

Notes:

1. Acceleration ranges are user selectable via I^2C.
2. Resonance as defined by the dampened mechanical sensor.
3. Measured in ± 2g range and including variation over operating temperature range at ODR5 (100Hz).

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Table 2. Electrical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Operating	V	1.7	2.5	3.6
I/O Pads Supply Voltage (V_{IO})		V	1.12	2.5	V_{dd}
Current Consumption	Active-mode ODR7	µA		150	
	Active- mode ODR5			125	
	Active-mode ODR0			35	
	Standby-mode			0.2	
	Off-mode Leakage			0.2	
Output Low Voltage (V_{OL})[1]		V			0.2 * V_{IO}
Output High Voltage (V_{OH})		V	0.8 * V_{IO}		
Input Low Voltage (V_{IL})		V	0		0.3 * V_{IO}
Input High Voltage (V_{IH})		V	0.7 * V_{IO}		V_{IO}
Input Pull-down Current		µA		0	
Power Up Time[2]		ms		3	
Start Up Time[3]		ms		2	
Turn Off Time[4]		ms		1	
Interrupt Pulse Width (when pulse selected)		µs		100	
I^2C Communication Rate[5]		MHz			3.4
Output Data Rate (ODR)[6]		Hz	3.125	100	1600
Bandwidth (-3dB)[7]		Hz		ODR/2	

Notes:

1. Assuming I^2C communication and minimum 1.5Kohm pull-up resistor on SCL and SDA pins.
2. Power up time is from V_{IO} and Vdd valid to device boot completion. (Off-mode to Standby-mode)
3. Start up time is from Standby-mode to Active-mode.
4. Turn off time is from Active-mode to Standby-mode
5. Supports I^2C Standard speed (100kHz), Fast speed (400kHz), and High speed (3.4MHz)
6. User selectable through I^2C.
7. User selectable and dependant on ODR.

Table 3. Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Absolute Limits	V	-0.3	-	4.0
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000
	MM		-	-	200
	CDM		-	-	500

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Floor Life

Factory floor life exposure of the KXCNL reels removed from the moisture barrier bag should not exceed a maximum of 168 hours at 30C/70%RH. If this floor life is exceeded, the parts should be dried per the IPC/JEDEC J-STD-033A standard.

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Terminology

g

A unit of acceleration equal to the acceleration of gravity at the earth's surface.

$$1g = 9.8\frac{m}{s^2}$$

One thousandth of a g (0.0098 m/ s^2) is referred to as 1 milli-g (1 mg).

Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal V_{dd} and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

$$Sensitivity = \frac{(Output\ @+1g - Output\ @-1g)}{2g}$$

The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25ºC), the sensitivity will vary by the amount shown in Table 1.

Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the OUTX, OUTY, OUTZ registers = 00h, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 00h. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified in Table 1, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

Functionality

Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

ASIC interface

A separate ASIC device packaged with the sense element provides all of the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I^2C digital communications provided by the ASIC. In addition, the ASIC contains all of the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic. Plus, there are two programmable state machines which allow the user to create unique embedded functions based on changes in acceleration.

Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in non volatile memory (OTP). Additionally, all functional register default values are also programmed into the non volatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.

Application Schematic

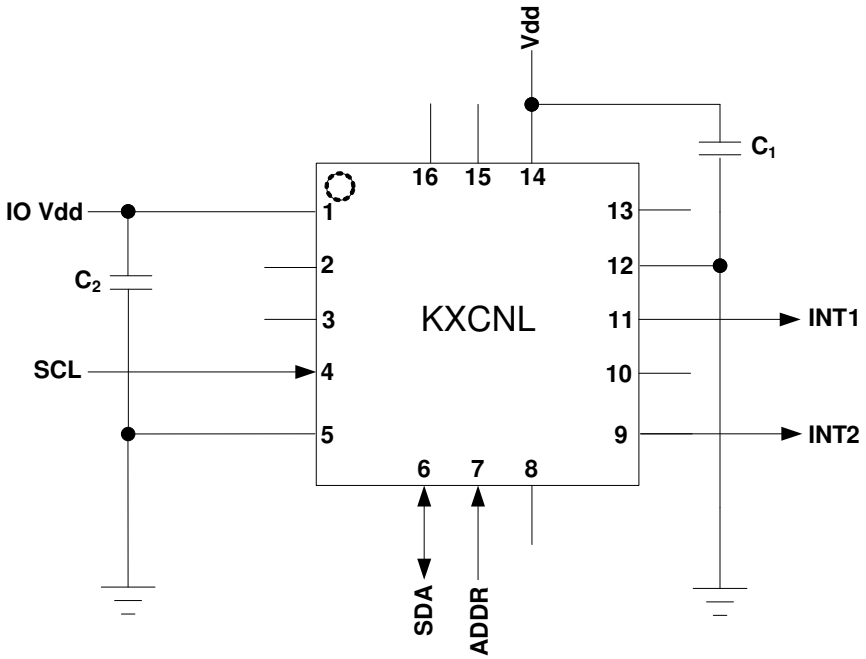

Table 4. KXCNL Pin Descriptions

Pin	Name	Description
1	V_{IO}	The power supply input for the digital logic and communication bus. Decouple this pin to ground with a 0.001 - 0.01uF ceramic capacitor.
2	NC	Not Connected Internally.
3	NC	Not Connected Internally.
4	SCL	I^2C Serial Clock
5	GND	Ground
6	SDA	I^2C Serial Data
7	ADDR	I^2C Address selection. Connect to **V_{IO}** or **GND** to select I^2C slave address.
8	NC	Not Connected Internally.
9	INT2	Physical Interrupt 2
10	NC	Not Connected Internally.
11	INT1	Physical Interrupt 1 / Data Ready
12	GND	Ground
13	NC	Not Connected Internally.
14	Vdd	The main power supply input. Decouple this pin to ground with a 0.1 - 0.47uF ceramic capacitor.
15	NC	Not Connected Internally.
16	NC	Not Connected Internally.

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Test Specifications

***Special Characteristics**:*

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

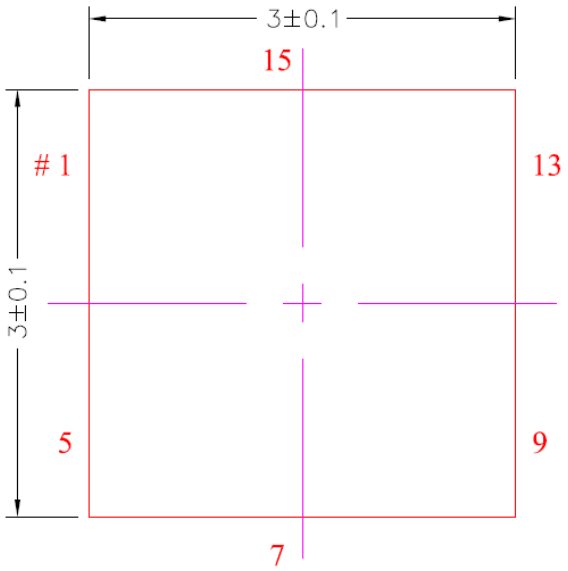
Table 5. Test Specifications

Parameter	Specification	Test Conditions
Current consumption ODR7	<250uA	25C, Vdd = 2.5 V
Offset	150mg	25C, Vdd = 2.5 V
ODR clock accuracy	10%	25C, Vdd = 2.5 V

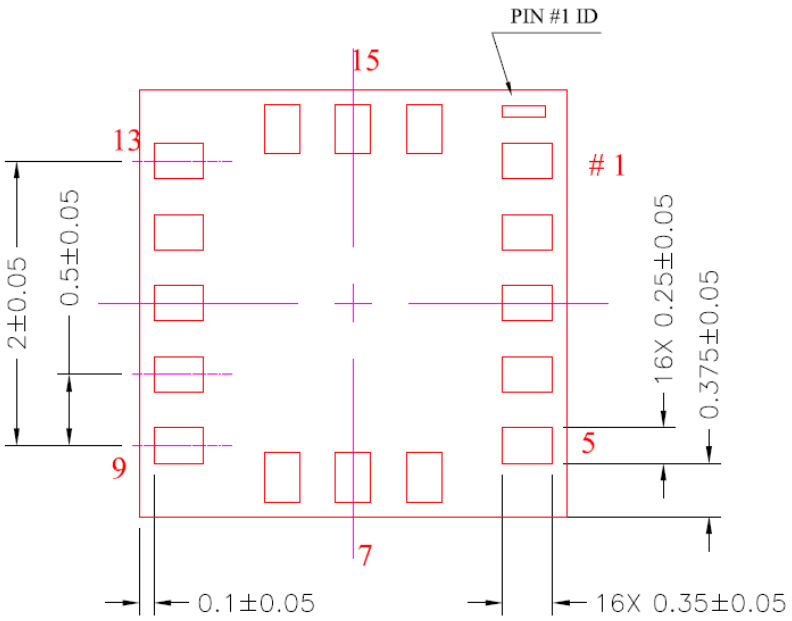
All specifications in Tables 1, 2, and 3 which are not listed in Table 5 (above) are tested on an audit or validation basis only and are not guaranteed to be within the minimum and maximum values prior to shipment.

Package Dimensions and Orientation

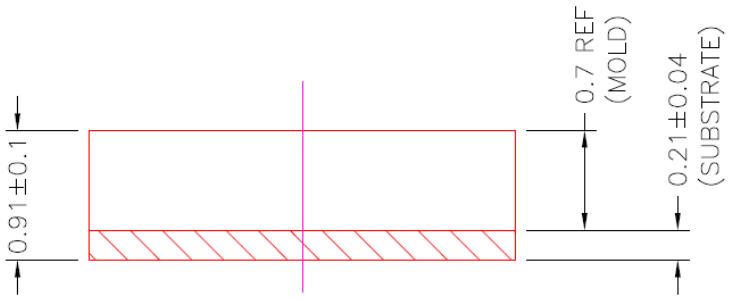
3 x 3 x 0.9 mm LGA



TOP VIEW



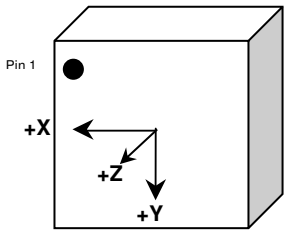
BOTTOM VIEW



SIDE VIEW

All dimensions and tolerances conform to ASME Y14.5M-1994

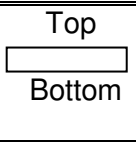
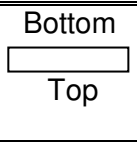
Orientation

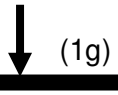


When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

SC_1=0, SC_0=0 (± 2g)

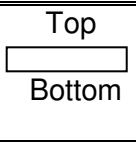
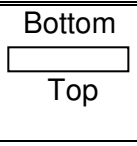
Position	1	2	3	4	5	6
Diagram						
X (counts)	0	-1024	0	1024	0	0
Y (counts)	-1024	0	1024	0	0	0
Z (counts)	0	0	0	0	1024	-1024
X-Polarity	**0**	**-**	**0**	**+**	**0**	**0**
Y-Polarity	**-**	**0**	**+**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**

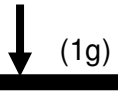


Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

SC_1=0, SC_0=1 (± 4g)

Position	1	2	3	4	5	6
Diagram						
X (counts)	0	-512	0	512	0	0
Y (counts)	-512	0	512	0	0	0
Z (counts)	0	0	0	0	512	-512
X-Polarity	**0**	**-**	**0**	**+**	**0**	**0**
Y-Polarity	**-**	**0**	**+**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**



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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

SC_1=1, SC_0=0 (± 6g)

Position	1	2	3	4	5	6
Diagram					Top Bottom	Bottom Top
X (counts)	0	-341	0	341	0	0
Y (counts)	-341	0	341	0	0	0
Z (counts)	0	0	0	0	341	-341
X-Polarity	**0**	**-**	**0**	**+**	**0**	**0**
Y-Polarity	**-**	**0**	**+**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

SC_1=1, SC_0=1 (± 8g)

Position	1	2	3	4	5	6
Diagram					Top Bottom	Bottom Top
X (counts)	0	-256	0	256	0	0
Y (counts)	-256	0	256	0	0	0
Z (counts)	0	0	0	0	256	-256
X-Polarity	**0**	**-**	**0**	**+**	**0**	**0**
Y-Polarity	**-**	**0**	**+**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**

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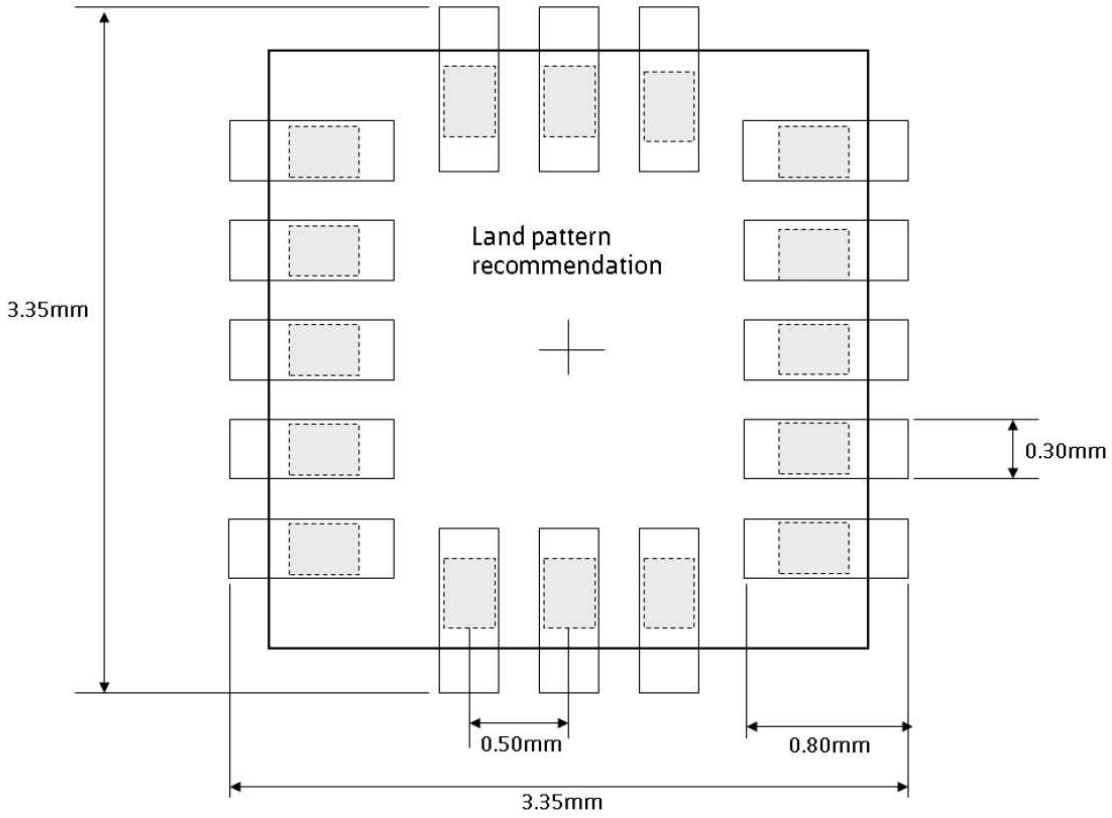
Land Pattern Recommendation



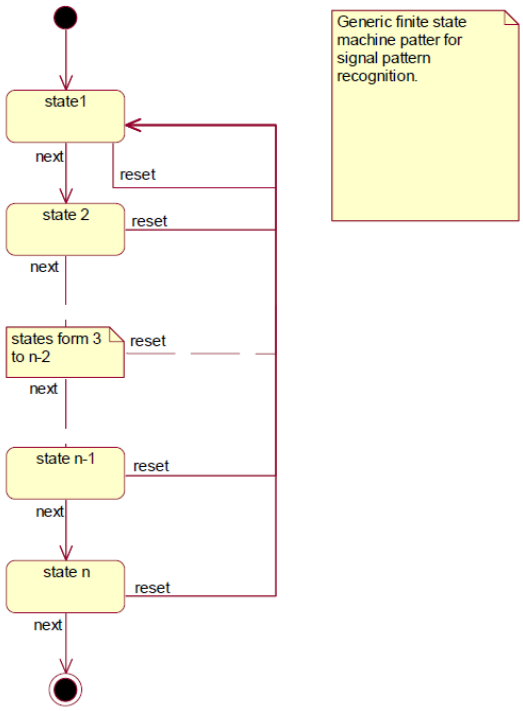
Soldering

Soldering recommendations are available upon request or from www.kionix.com.

State Programs

The most important feature of the KXCNL is that it has two independent State Programs which can be programmed by the user to produce interrupts and peak values.

A State Program follows a structure of successive states. From each state (n) it is only possible to have a transition to the next state (n+1) or to the state pointed to by the Reset Pointer (state 1). Transition to the Reset Point happens when the "RESET condition" is true. Transition to the next step happens when "NEXT condition" is true. An interrupt is sent when the Output/Stop/Continue state is reached.



In the KXCNL, a State Program is a series of states, parameters and internal memories running an algorithm in its own logic machine. Two independent State Program areas are defined (State Program 1 and State Program 2).

- Each program can be one shot run or continuously running.
- Outputs of program are internal interrupt signal and interrupt source information.
- Program code steps and parameter sets are loaded into fixed register memory space by the host.
- Input data comes from measurement/signal blocks according ODR and DES2 timing definitions.

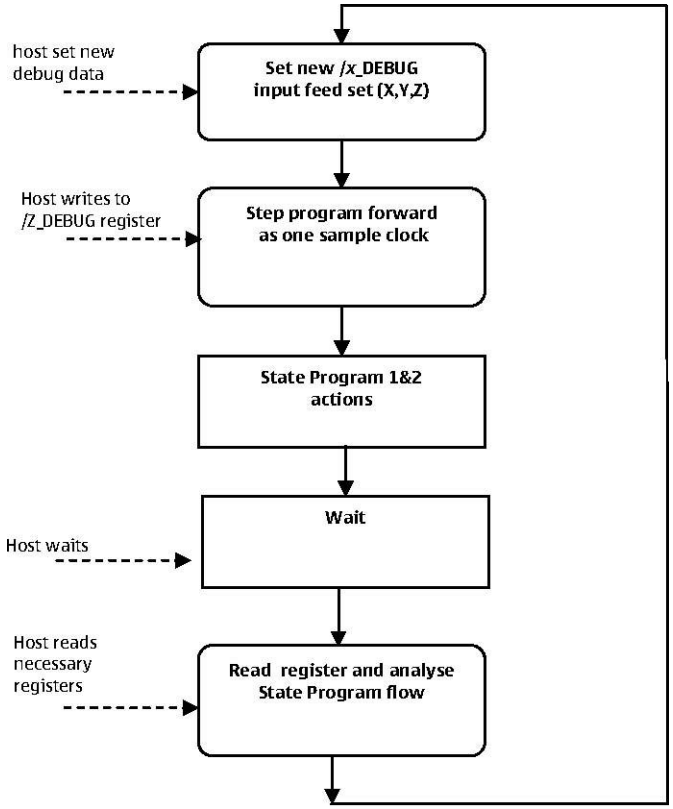
One sample is the timing base for the NEXT and RESET conditions. State Programs 1 and 2 are running independently or synchronized but with same input data.

Interrupts are the main output of the State Programs. According program flow, the channel that triggered the interrupt also memorizes its peak (highest or lowest) value.

State Program 1 and 2 are identical and exactly working same manners with some exceptions as extra sub functionalities:

- State Program 2 has decimator functionality.
- State Program 2 has a difference (DIFF) functionality/filter. The DIFF filter can be configured with two settings:
  - Difference between current and previous data values (X,Y,Z)
  - Difference between current data values and a constant
- When DIFF functionality selected in State Program 2, vector calculated value (V) is left intact.

State Programs can be debugged with simple step method and host assistance. When register /CNTL1, bit DEBUG == 1, normal measurement data is not fed to the State Programs. Instead, the host feeds manual data to the debug input registers (/*X,Y,Z*_DEBUG) to imitate measurement data. This debug data is sent to the state programs after writing the /Z_DEBUG register (stepping command like clock).

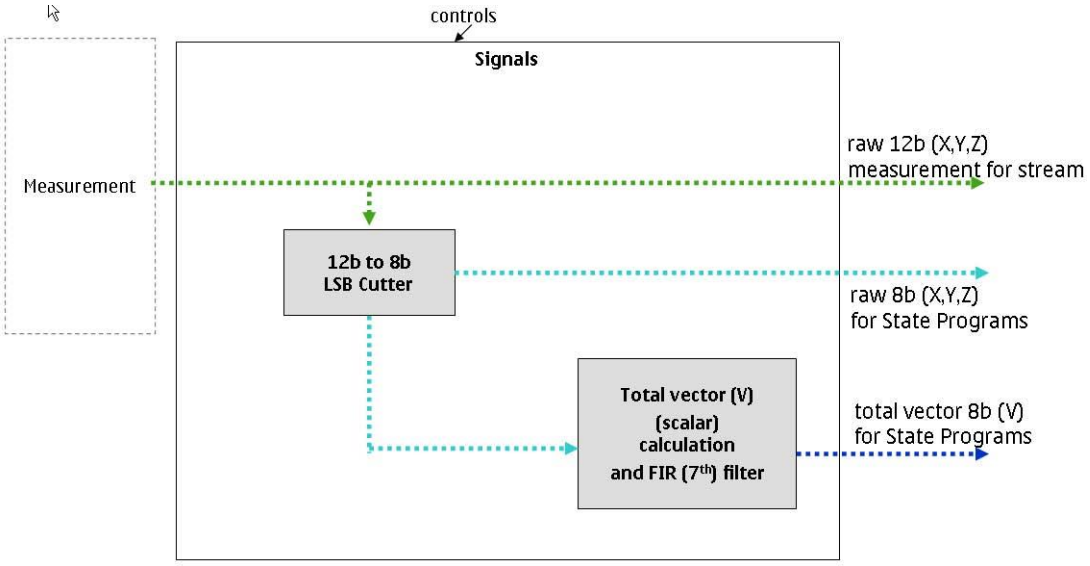


Debug (input) data is feed to State Programs via registers:

- /X_DEBUG = debug feed for x - channel
- /Y_DEBUG = debug feed for y - channel
- /Z_DEBUG = debug feed for z - channel

Signal path

The acceleration measurement data flows through several paths according customizable setup of the KXCNL.



Real acceleration measurement data is available to external applications through the 12-bit /OUT_X, /OUT_Y, and /OUT_Z registers. Data is provided at the selected ODR.

The Integrated Functions of the KXCNL are not using the raw 12-bit data. There are several other data forms available for the Integrated Interrupt Functions (State Programs). Internal data sets in 8-bit format for State Programs usage are:

- Raw (X,Y,Z) acceleration data limited in range from -127 to +127
- Vector (V), calculated and filtered (if enabled), limited to range from -127 to +127
- DIFF is data process method which calculates the difference of the current (X,Y,Z) data measurement to the previous (X,Y,Z) data measurement or the difference of the current (X,Y,Z) data measurement to set of constants. (Available only for State Program 2)

Vector calculation and filter

Total (3D) vector length is calculated with an approximation formula. The calculated vector length result is filtered with an adjustable Band Pass filter. The vector approximation formulas are the following:

$$a1 = |x| + |y| + |z|$$

$$a2 = \max(|x|, |y|, |z|)$$

$$v_{raw} = (45 * a1 + 77 * a2)/256$$

where:

- x, y, z are the 8-bit measured acceleration values limited in range from -127 to +127.
- $a1$ and $a2$ are temporary maximum 16-bit values.
- 45 and 77 are fixed 8-bit constants.
- 256 is the scale factor for the calculation.
- v_{raw} is the vector length, maximum 16-bit scalar temporary value.
- If filtering is not enabled, v_{raw} is fed to the State Programs as V after a limiter of -127 to +127.

Vector filter:

When enabled, the 16-bit vector scalar (v_{raw}) data from the vector calculation phase is passed through a band pass filter. The target corner frequency for the band pass filter is 0.5Hz to 10Hz (in ODR5, 100Hz). ODR selection affects the corner frequencies so ODR5 as 100Hz is the main time base for the vector filter. Filter coefficients are adjustable. The calculation is performed with maximum 16-bit temporary values.

FIR filter, 7 orders (8 taps)
- 4 asymmetric coefficients (8b wide constants)
- 8 tap filter as 4x2 structure
    - /VFC_1, /VFC_2, /VCF_3, /VCF_4 and
    - -/VFC_1, -/VFC_2, -/VCF_3, -/VCF_4
    - Reference construction: (53,127,127,53, -53,-127,-127,-53)

- Scale factor for filter output (temporary value) is 256 (16b to 8b) and it is limited to range from -127 to +127
- Output is 8b filtered vector scalar (V) data (/V_I internal memory)
- Last 8 input values are kept in /BUF1 to /BUF8 (8b) internal memories

Vector filter can be enabled or disable via register /CNTL4, bit VFILT setting.

Power Modes

The KXCNL has three power modes: Off, Stand-by, and Active. The part exists in one of these three modes at any given time. Off and Stand-by modes have very low current consumptions.

Power Mode	Bus State	V_{IO}	V_{dd}	Function	Outputs
Off	-	OFF	OFF	No sensor activity	Not available
Off	-	ON	OFF	No sensor activity	Not available
Off	-	OFF	ON	No sensor activity	Not available
Stand-by	Active	ON	ON	Waiting activation command	Not available
Active	Active	ON	ON	All functionalities available	Available

Off mode

One or both of the power supplies (V_{dd} or V_{IO}) are not powered. The sensor is completely inactive and not reporting or communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

Initial Startup

The preferred startup sequence is to turn on V_{IO} before V_{dd}, but if V_{dd} is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power On Reset (POR) is performed every time when:

1. V_{IO} supply is valid
2. V_{dd} power supply is going to valid level

OR

1. V_{IO} power supply is going to valid level
2. V_{dd} supply is valid

When POR occurs, the following registers and signals are set and the part is put into Stand-by mode:

- Interrupt (*INT1/DRDY* and *INT2*) signals are set to inactive (high Z)
- Registers set to default:
  - /STAT
  - /CNTL1 (14h)
  - /CNTL2
  - /CNTL3
  - /CNTL4
  - Offset registers (/OFF_X, /OFF_Y, /OFF_Z)
  - /OUTS1, OUTS2

Stand-by mode

The primary function of the stand-by mode is to ensure fast wake-up to active mode and to minimize current consumption. This mode is set as default when both power supplies are applied and the POR function occurs. A Soft Reset command also performs the POR function and puts the part into Stand-by mode.

Stand-by mode is a low power waiting state for fast turn on time. All time critical functionalities are ready to start measurement. Bus communication actions of other components are not disturbed if they are using the same bus. There is only one possible way to change to active mode – a register command via the I^2C bus.

Active mode

Stand-by-mode can be changed to Active mode by writing to register /CNTL1, bit PC = 1.

Active mode engages the full functionality of accelerometer measurements. The host also has the ability to change settings in the control registers, readback status registers, and program state machines.

Active mode to Stand-by mode transitions

Two possible methods for transition from Active mode to Stand-by mode can be used.

1. Register /CNTL1, PC =0 command:
    a. Status register /STAT1 is set to default value
    b. Interrupt (*INT1/DRDY* and *INT2*) signals are set to inactive (High Z/High impedance)
    c. Register memory is kept intact
2. Register /CNTL4, STRT=1 command:
    a. changes are performed to physical signal and register values as POR sequence

When a transition from Active mode to Stand-by mode and back to Active mode has been done by the host:

- If State Program 1 /CNTL2, SM1_EN = 1 (State Program 1 was running in earlier Active mode session), then State Program 1 is disabled during the Stand-by mode and re-enabled when the component is returned to Active mode. However, this resets State Program 1 to its Default Initial position.
- If State Program 2 /CNTL3, SM2_EN = 1 (State Program 2 was running in earlier Active mode session), then State Program 2 is disabled during the Stand-by mode and re-enabled when the component is returned to Active mode. However, this resets State Program 1 to its Default Initial position.

KXCNL Digital Interface

The Kionix KXCNL digital accelerometer has the ability to communicate on the I²C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 6. Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KXCNL has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KXCNL always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are high.

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The Slave Address associated with the KXCNL is:

ADDR pin status	SAD	SAD + Read	SAD + Write
ADDR = 0	0011110 (1Eh)	00111101 (3Dh)	00111100 (3Ch)
ADDR = 1	0011101 (1Dh)	00111011 (3Bh)	00111010 (3Ah)

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it

remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free.

Writing to a KXCNL 8-bit Register

Upon power up, the KXCNL enters into stand-by mode. The I^2C Master must write to the KXCNL's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KXCNL ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KXCNL to which 8-bit register the Master will be writing the data. The KXCNL acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KXCNL acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KXCNL is now stored in the appropriate register. The KXCNL automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Reading from a KXCNL 8-bit Register

When reading data from a KXCNL 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KXCNL acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KXCNL again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KXCNL with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KXCNL automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page.

If a receiver cannot transmit or receive another complete byte of data until it has performed some other function, it can hold SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases SCL.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I^2C bus and how the Master and Slave interact during these transfers. Table 7 defines the I^2C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 7. I^2C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5. HS-mode data transfer of the Master writing one byte to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	S	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

KXCNL Register Map

Register Name	Type Read/Write	I²C Read/Write Address	
		Hex	Binary
Reserved[1]		00h – 0Ch	0000 0000 – 0000 1100
/INFO1	R	0Dh	0000 1101
/INFO2	R	0Eh	0000 1110
/WIA	R	0Fh	0000 1111
/OUTX_L	R	10h	0001 0000
/OUTX_H	R	11h	0001 0001
/OUTY_L	R	12h	0001 0010
/OUTY_H	R	13h	0001 0011
/OUTZ_L	R	14h	0001 0100
/OUTZ_H	R	15h	0001 0101
/LC_L	R/W	16h	0001 0110
/LC_H	R/W	17h	0001 0111
/STAT	R	18h	0001 1000
/PEAK1	R	19h	0001 1001
/PEAK2	R	1Ah	0001 1010
/CNTL1	R/W	1Bh	0001 1011
/CNTL2	R/W	1Ch	0001 1100
/CNTL3	R/W	1Dh	0001 1101
/CNTL4	R/W	1Eh	0001 1110
/THRS3	R/W	1Fh	0001 1111
/OFF_X	R/W	20h	0010 0000
/OFF_Y	R/W	21h	0010 0001
/OFF_Z	R/W	22h	0010 0010
Reserved[1]		23h	0010 0011
/CS_X	R/W	24h	0010 0100
/CS_Y	R/W	25h	0010 0101
/CS_Z	R/W	26h	0010 0110
Reserved[1]		27h	0010 0111
/X_DEBUG	R/W	28h	0010 1000
/Y_DEBUG	R/W	29h	0010 1001
/Z_DEBUG	R/W	2Ah	0010 1010
Reserved[1]	R/W	2Bh	0010 1011
/VFC_1	R/W	2Ch	0010 1100
/VFC_2	R/W	2Dh	0010 1101
/VFC_3	R/W	2Eh	0010 1110
/VFC_4	R/W	2Fh	0010 1111
Reserved[1]		30h – 3Fh	0011 0000 – 0011 1111
/ST1_1	W	40h	0100 0000
/ST2_1	W	41h	0100 0001
/ST3_1	W	42h	0100 0010
/ST4_1	W	43h	0100 0011
/ST5_1	W	44h	0100 0100
/ST6_1	W	45h	0100 0101
/ST7_1	W	46h	0100 0110
/ST8_1	W	47h	0100 0111
/ST9_1	W	48h	0100 1000
/ST10_1	W	49h	0100 1001
/ST11_1	W	4Ah	0100 1010
/ST12_1	W	4Bh	0100 1011
/ST13_1	W	4Ch	0100 1100
/ST14_1	W	4Dh	0100 1101
/ST15_1	W	4Eh	0100 1110
/ST16_1	W	4Fh	0100 1111
/TIM4_1	W	50h	0101 0000
/TIM3_1	W	51h	0101 0001

Register Name	Type Read/Write	I²C Read/Write Address	
		Hex	Binary
/TIM2_1_L	W	52h	0101 0010
/TIM2_1_H	W	53h	0101 0011
/TIM1_1_L	W	54h	0101 0100
/TIM1_1_H	W	55h	0101 0101
/THRS2_1	W	56h	0101 0110
/THRS1_1	W	57h	0101 0111
Not used – fixed content	R	58h	0101 1000
/SA1	W	59h	0101 1001
/MA1	W	5Ah	0101 1010
/SETT1	W	5Bh	0101 1011
/PPRP1	R	5Ch	0101 1100
/TC1_L	R	5Dh	0101 1101
/TC1_H	R	5Eh	0101 1110
/OUTS1	R	5Fh	0101 1111
/ST1_2	W	60h	0110 0000
/ST2_2	W	61h	0110 0001
/ST3_2	W	62h	0110 0010
/ST4_2	W	63h	0110 0011
/ST5_2	W	64h	0110 0100
/ST6_2	W	65h	0110 0101
/ST7_2	W	66h	0110 0110
/ST8_2	W	67h	0110 0111
/ST9_2	W	68h	0110 1000
/ST10_2	W	69h	0110 1001
/ST11_2	W	6Ah	0110 1010
/ST12_2	W	6Bh	0110 1011
/ST13_2	W	6Ch	0110 1100
/ST14_2	W	6Dh	0110 1101
/ST15_2	W	6Eh	0110 1110
/ST16_2	W	6Fh	0110 1111
/TIM4_2	W	70h	0111 0000
/TIM3_2	W	71h	0111 0001
/TIM2_2_L	W	72h	0111 0010
/TIM2_2_H	W	73h	0111 0011
/TIM1_2_L	W	74h	0111 0100
/TIM1_2_H	W	75h	0111 0101
/THRS2_2	W	76h	0111 0110
/THRS1_2	W	77h	0111 0111
/DES2	W	78h	0111 1000
/SA2	W	79h	0111 1001
/MA2	W	7Ah	0111 1010
/SETT2	W	7Bh	0111 1011
/PPRP2	R	7Ch	0111 1100
/TC2_L	R	7Dh	0111 1101
/TC2_H	R	7Eh	0111 1110
/OUTS2	R	7Fh	0111 1111

Notes:

1. Reserved registers should not be written to.