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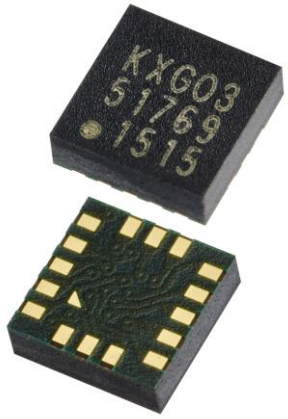
Kionix®	**Digital Tri-axis Gyroscope/ Tri-axis Accelerometer Specifications**	**PART NUMBER** **KXG03-1034** **Rev. 2.0** **14-Feb-17**

Product Description

KXG03-1034 is a 6 Degrees-of-Freedom inertial sensor system that features digital outputs accessed through I^2C or SPI communication. The KXG03 sensor consists of a tri-axial micro machined gyroscope plus a tri-axial accelerometer and an KXG03 packaged in a 3 x 3 x 0.9 mm 16-pin Land Grid Array (LGA) package. The KXG03 is realized in standard CMOS technology and features flexible user programmable gyroscope full scale ranges of ±256, ±512, ±1024, and ±2048°/sec and user-programmable ±2g/±4g/±8g/±16g full scale range for the accelerometer. An auxiliary I^2C master serial interface exists for communication with up to 2 other sensors to access data that can be accumulated in an internal 1024-byte FIFO buffer and transmitted to the application processor. In addition, the KXG03 has an embedded temperature sensor.



During operation, the gyroscope sensor elements are forced into vibration. When angular velocities are applied about the sensing axes, vibration is transferred to sensing elements, causing capacitance changes at the sensor electrodes. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. Capacitance changes are amplified and converted into digital signals which are processed by a dedicated digital signal processing unit. The digital signal processor applies filtering, bias and sensitivity adjustment, as well as temperature compensation. The DSP also feeds back the driving signal to ensure the proper sensor excitation.

The KXG03 series is designed to strike a balance between current consumption and noise performance with excellent bias stability over temperature. These sensors can accept supply and digital communication voltages between 1.8V and 3.6V.

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Kionix®	**Digital Tri-axis Gyroscope/ Tri-axis Accelerometer Specifications**	**PART NUMBER** **KXG03-1034** **Rev. 2.0** **14-Feb-17**

Features

- 3 x 3 x 0.9 mm LGA
- User-selectable low power or high resolution mode
- User selectable gyroscope full scale ranges of:
  ±256 deg/s
  ±512 deg/s
  ±1024 deg/s
  ±2048 deg/s
- User selectable accelerometer full scale rages of:
  ±2g
  ±4g
  ±8g
  ±16g
- Temperature sensor with min measurement range of -40 C to +85 C with 16-bit output
- User-selectable Output Data Rate (ODR) up to 51200Hz
- 1024 byte FIFO buffer
- Wake-up and Back-to-sleep functions
- Auxiliary I2C master interface to control up to 2 auxiliary sensors
- Independent Output Data Rate (ODR) : Over Sampling Rate (OSR) control for accelerometer
- User-configurable wake-up function
- Digital I^2C up to 3.4MHz
- Digital SPI up to 10MHz
- Lead-free Solderability
- Excellent Temperature Performance
- High Shock Survivability
- Factory Programmed Offset and Sensitivity
- Self-test Function

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Kionix®	**Digital Tri-axis Gyroscope/ Tri-axis Accelerometer Specifications**	**PART NUMBER** **KXG03-1034** **Rev. 2.0** **14-Feb-17**

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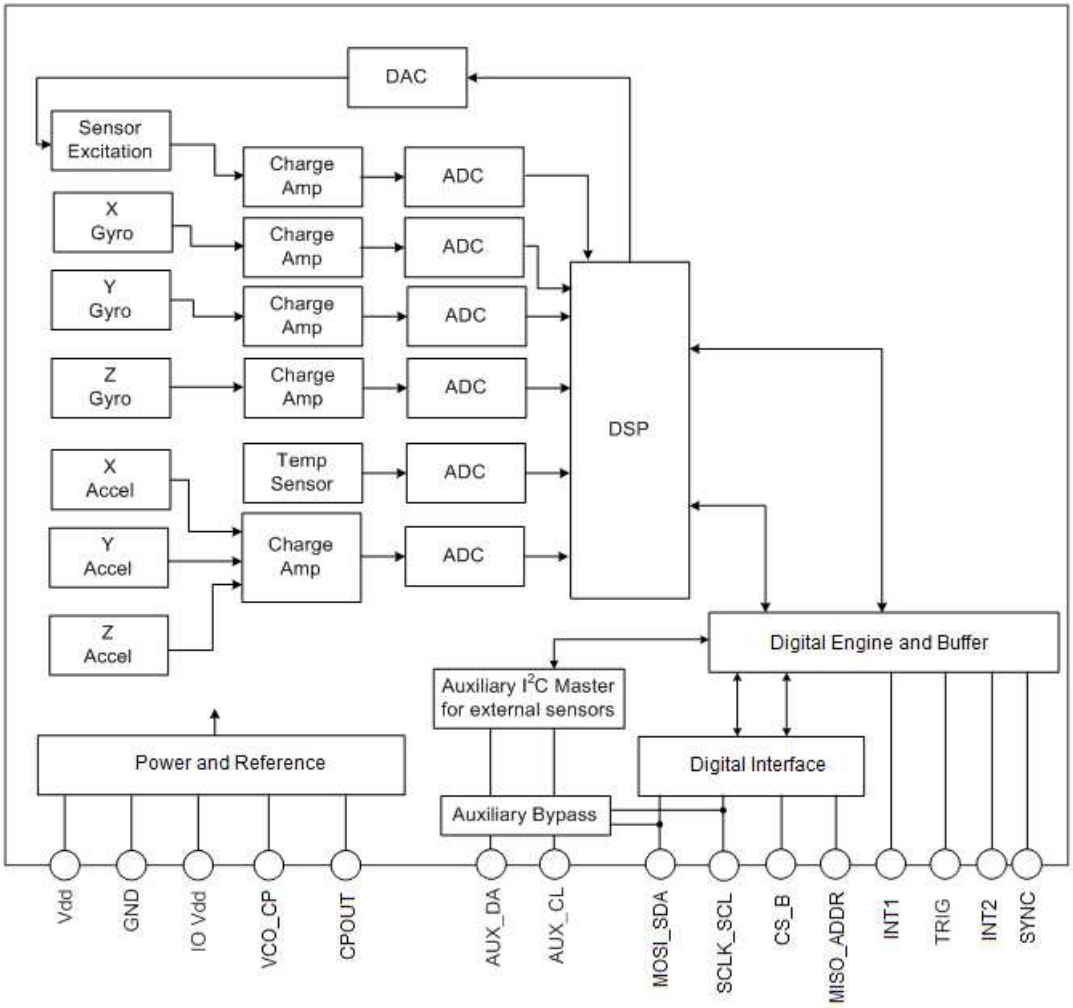
Functional Diagram



Product Specifications

Gyroscope Mechanical

(Specifications are for operation at VDD = 2.5V and T = 25°C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	85
Zero Rate Output, Digital		counts		0	
Zero Rate Output Stability		± % of FS		1	
Zero Rate Output Variation over Temperature		± dps / °C		0.4	
Sensitivity (16-bit) [1]	RSEL1 = 0, RSEL0 = 0, ±256 deg/sec	counts/deg/sec		128	
	RSEL1 = 0, RSEL0 = 1, ±512 deg/sec			64	
	RSEL1 = 1, RSEL0 = 0, ±1024 deg/sec			32	
	RSEL1 = 1, RSEL0 = 1, ±2048 deg/sec			16	
Sensitivity Variation over Temperature		± % / °C		0.04	
Noise Density		deg/sec/√Hz		0.03	
Output Noise (10 Hz BW)		dps-rms		0.096	
Non-Linearity		% of FS		0.5	
Cross Axis Sensitivity		± %		1	
Bandwidth [2]		Hz	10		160

Table 1: Gyroscope Mechanical Specifications

Notes:

1. Resolution and rotation rate ranges are user selectable.
2. User selectable via control register.

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Accelerometer Mechanical

(Specifications are for operation at VDD = 2.5V and T = 25°C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	85
Zero-g Offset		mg	-	±25	±125
Zero-g Offset Variation from RT over Temp.		± mg/ °C		0.25	
Sensitivity (16-bit)[1]	GSEL1=1, GSEL0=1 (± 2g)	counts/g	15565	16384	17203
	GSEL1=0, GSEL0=0 (± 4g)		7782	8192	8602
	GSEL1=0, GSEL0=1 (± 8g)		3891	4096	4301
	GSEL1=1, GSEL0=0 (± 16g)		1946	2048	2150
Sensitivity Variation from RT over Temp.		± % / °C		0.01 (xy) 0.03 (z)	
Self-Test Output		g		0.5	
Mechanical Resonance (-3dB)[2]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.5	
Cross Axis Sensitivity		%		2	
Noise Density		$\mu g / \sqrt{Hz}$		175	
Bandwidth (-3dB)		Hz		ODR/2	

Table 2: Accelerometer Mechanical Specifications

Notes:

1. Resolution and acceleration ranges are user selectable.
2. Resonance as defined by the dampened mechanical sensor.

Temperature Sensor

(Specifications are for operation at VDD = 2.5V and T = 25 °C unless stated otherwise)

Parameters	Units	Min	Typical	Max
Operating Temperature Range	°C	-40	-	85
Output Accuracy	± °C		3	
Sensitivity (16-bit digital)	counts/ °C		128	

Table 3: Temperature Sensor Specifications

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Electrical

(Specifications are for operation at VDD = 2.5V and T = 25 °C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.8	2.5	3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.7		VDD
Current Consumption	Operating (gyroscope + accelerometer)	mA		2.1	
	Gyroscope only	mA		1.85	
	Accelerometer only High Res Mode	µA		325	
	Accelerometer only Low Power Mode [6]	µA		5	
	Standby	µA		1.5	
Output Low Voltage[1] (V_{OL})		V	-	-	0.3 * IO_VDD
Output High Voltage (V_{OH})		V	0.9 * IO_VDD	-	-
Input Low Voltage (V_{IL})		V	-	-	0.2 * IO_VDD
Input High Voltage(V_{IH})		V	0.8 * IO_VDD	-	-
Power Up Time (Power on Reset Time)[2]		ms			50
Software Reset[7]		ms			2
Sensor Start-Up Time[3]	Gyroscope	ms		80	
	Accelerometer (100Hz)	ms		20	
I^2C Communication Rate[4,5]		MHz			3.4
I^2C Address				4E / 4F	
SPI communication Rate		MHz			10

Table 4: Electrical Specifications

Notes:

1. Assuming I^2C communication and minimum 1.5kΩ pull-up resistor on SCL and SDA.
2. From OFF to Standby mode after VDD and IO_VDD are valid
3. Time from sensor standby mode to operating mode (GYRO_RUN = 1). Accelerometer time varies with accelerometer Output Data Rate (ODR) per table below.
4. Assuming max bus capacitance load of 20pF.
5. The I^2C bus supports Standard-Mode, Fast-Mode and High Speed Mode.
6. Accelerometer only in Low Power Mode current varies with accelerometer Output Data Rate (ODR) and Output Wake-up Function (OWUF) per figure on the next page.
7. Software Reset Time is defined as the time it takes to perform a RAM reboot routine following the setting of the SRST bit to 1 in the CTL_REG_1 register. The SRST bit will remain 1 until the RAM reboot routine is completed.

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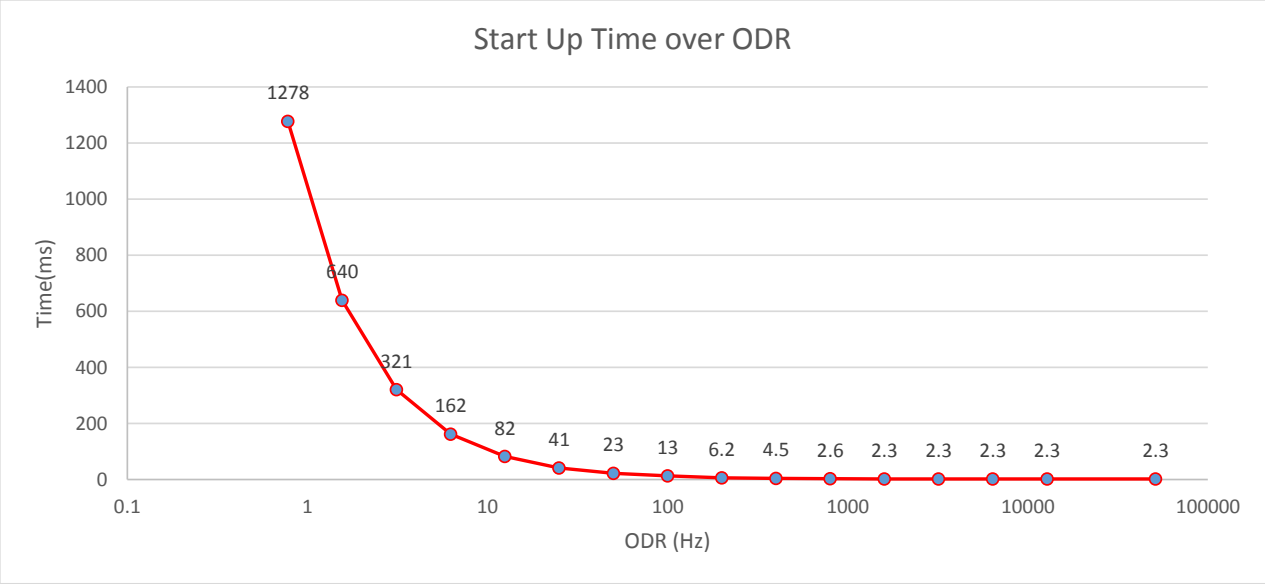
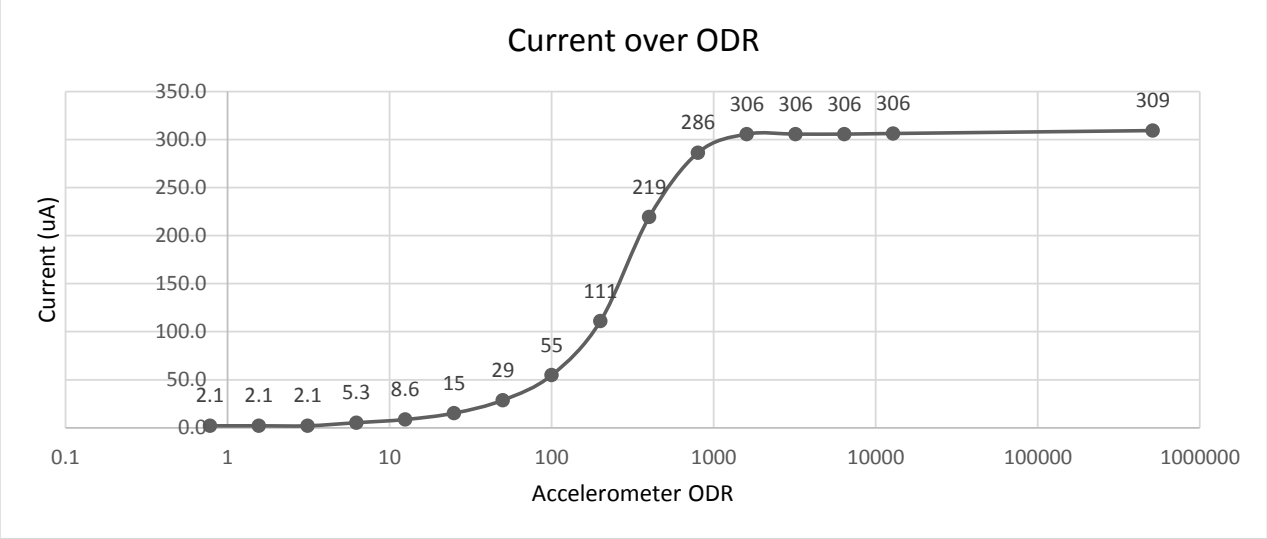
Accelerometer Start-up time versus ODR profile:



Accelerometer Low Power Mode Current versus ODR profile:



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Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD_{Low}, T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{Low}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the **VDD** ramp up time **T_{VDD}** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD_{Low}, T_{VDD}, T_{VDD_OFF} and temperature as POR performance can vary depending on these parameters.

Please refer to Technical Note ***TN022 Power-On Procedure*** for more information.

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Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.3	-	3.6
Operating Temperature Range		°C	-40	-	85
Storage Temperature Range		°C	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5 ms 10000 for 0.2 ms
ESD	HBM	V	-	-	2000

Table 5: Environmental Specifications

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

These products conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are “of uniform composition throughout”. The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.

Applicable Exemption: *7C-I - Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix compound.*

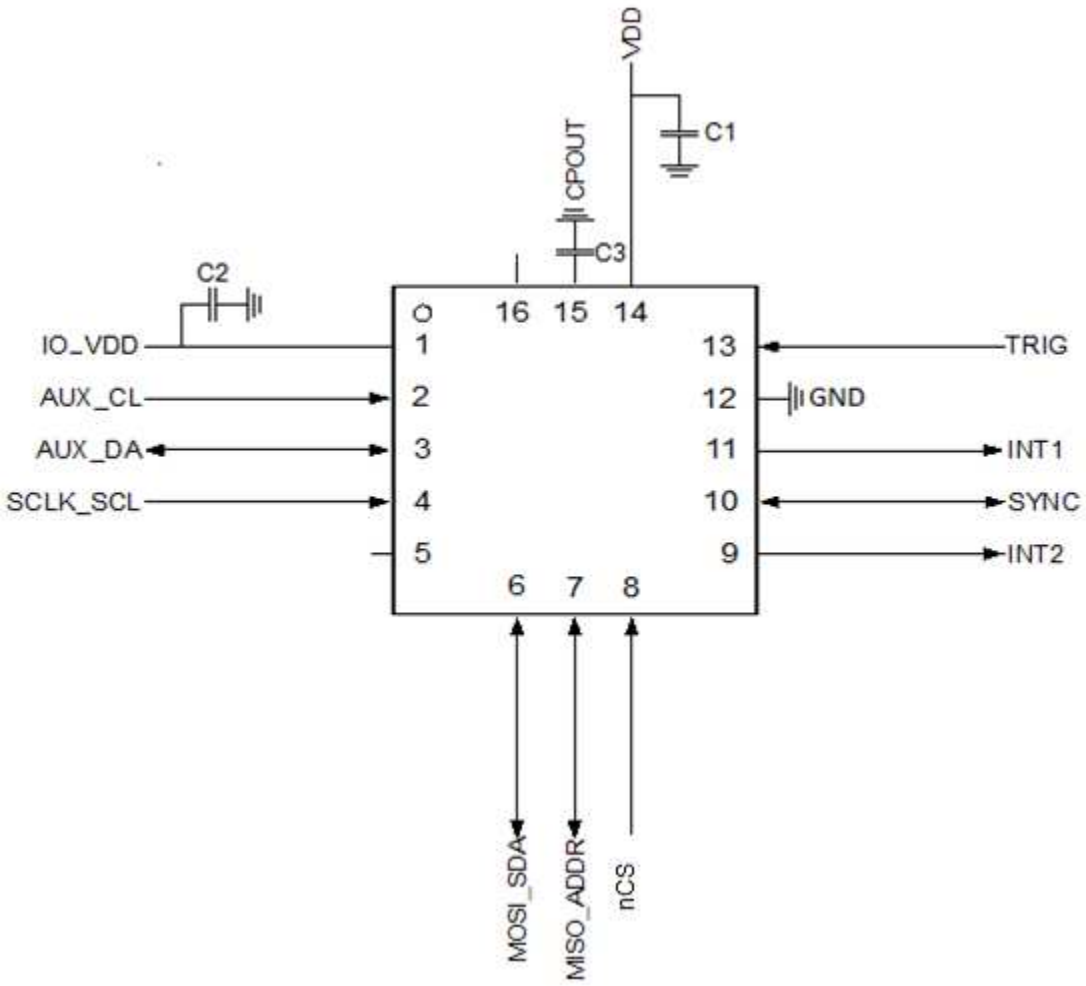
These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-161) as identified by the European Chemicals Agency as of 17 December 2014.

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Application Schematic



ID	Stress	Value	Rating	Type
C1	3 V	0.1 µF	16 V	Y5V
C2	3 V	0.1 µF	16 V	Y5V
C3	20 V	2.2 nF	50 V	Y5V

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Pin Descriptions

Pin	Name	Description
1	IO_VDD	External supply for IO ring. Connect bypass capacitor C2
2	AUX_CL[4]	Auxiliary I²C master serial clock
3	AUX_DA[4]	Auxiliary I²C master serial data
4	SCLK_SCL[1]	SPI/I²C serial clock
5	RESERVED	Connect to GND or leave floating. Do not connect to IO_VDD.
6	MOSI_SDA[2]	SPI MOSI / I²C serial data
7	MISO_ADDR	Serial data input during 4-wire SPI communication and part of the device address during I²C communication.
8	nCS	Chip Select (active LOW) for SPI communication. Connect to IO_VDD for I²C communication. Do not leave floating.
9	INT2	Programmable interrupt output. Leave floating if not used.
10	SYNC[3]	Sync input or output. If configured as input, connect to IO_VDD or GND. If configured as output, leave floating.
11	INT1	Programmable interrupt output. Leave floating if not used.
12	GND	Ground
13	TRIG	External trigger input for buffer actions. Connect to IO_VDD or GND if unused.
14	VDD	External supply with bypass capacitor C1
15	CPOUT	External charge pump reservoir cap C3
16	RESERVED	Connect to GND or leave floating

Table 6: Pin Descriptions

Notes:

1, 2 For I²C communication, connect an external IO_VDD pull-up resistors on SCL (pin 4) and SDA (pin 6). The value of the pull up resistors should be 1.5 kΩ or above to ensure a V_{OL} that is less than the maximum specified value.

3 Care must be taken with external connection of the SYNC pin. The reset state of the SYNC pin is tri-stated. If pin is not used in application, connect to IO_VDD or GND and ensure the state of the pin is never changed to output through register write to FSYNC_CTL register. If pin is configured as Output in the application, the pin must be left floating to avoid internal short circuit to IO_VDD or GND.

4 The AUX_DA and AUX_CL pins should be left floating for applications that do not use the auxiliary I²C interface. Applications interfacing to the sensor in I²C mode and not using aux I2C can keep the default aux_bypass=1 and aux_pull_up=0 settings (see AUX_I2C_CTL_REG). Applications trying to limit the main I²C bus capacitance should set aux_bypass=0 and aux_pull_up=1. Applications interfacing to the sensor in SPI mode and not using aux I2C should set bypass=0 and pull_up=1. Please note SPI applications may see increased standby current until aux_bypass and aux_pull_up have been changed from the default settings.

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Package Dimensions and Orientation:

Dimensions

3 x 3 x 0.9 mm LGA Dimensions

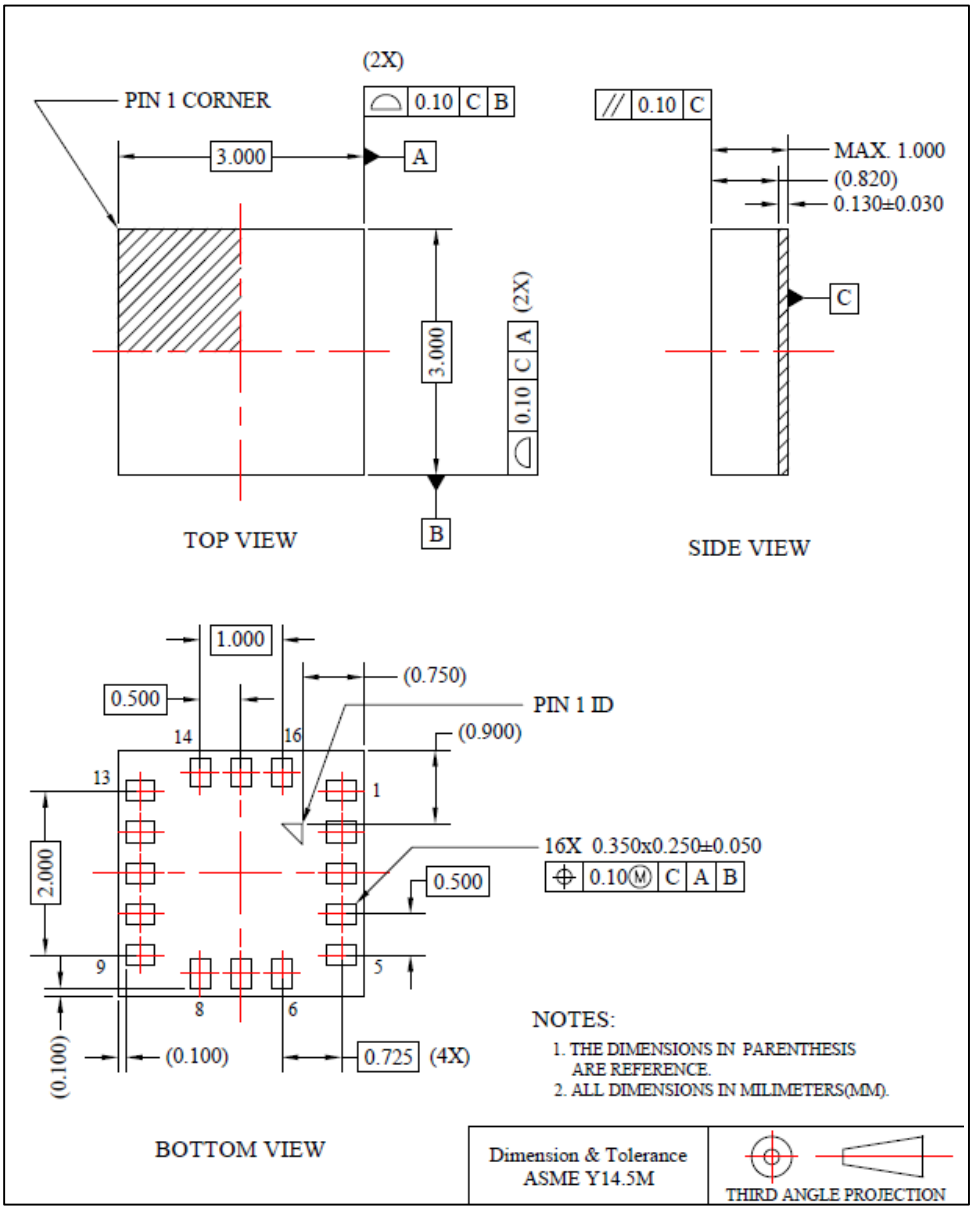

Figure 1: Package Dimensions

Orientation

When the device is accelerated or rotated in +X, +Y, or +Z direction, the corresponding output will increase.

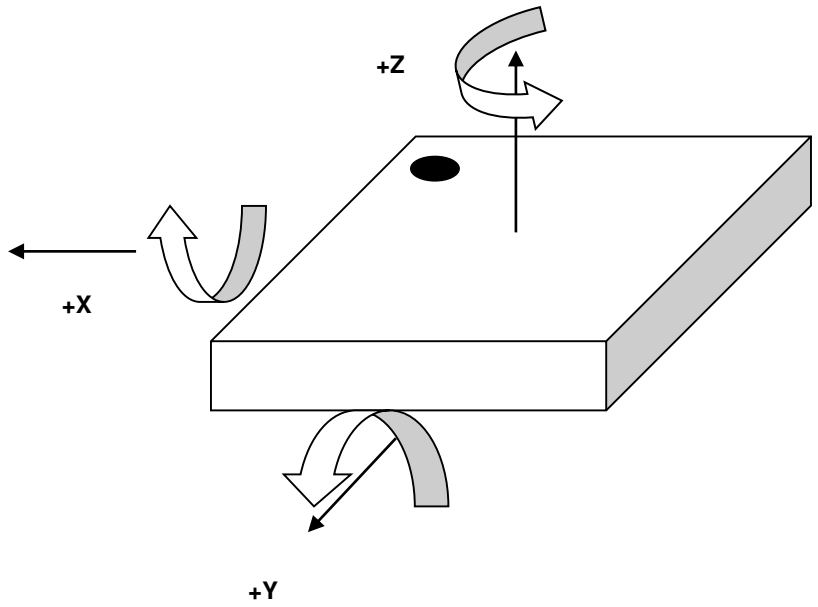

Figure 2: Device Orientation

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Digital Interface

The Kionix KXG03 digital sensor has the ability to communicate via the I²C and SPI digital serial interface protocols. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in the table below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 7: Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KXG03 has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KXG03 always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are high.

The I²C interface is compliant with high-speed mode, fast mode and standard mode I²C protocols.

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I²C Operation

Transactions on the I2C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The KXG03 Slave Address is comprised of a user programmable part, a factory programmable part, and a fixed part, which allows for connection of multiple sensors to the same I²C bus. The Slave Address associated with the KXG03 is 10011YX, where the user programmable bit X, is determined by the assignment of MISO_ADDR (pin 7) to GND or IO_VDD. Also, the factory programmable bit Y is set at the factory. For KXG03-1034, the factory programmable bit Y is fixed to 1 (contact your Kionix sales representative for list of available devices). Table 8 lists possible I2C addresses for KXG03-1034.

									Y	**X**	
Description	**Address Pad**	**7-bit Address**	**Address**	**<7>**	**<6>**	**<5>**	**<4>**	**<3>**	**<2>**	**<1>**	**<0>**
I2C Wr	GND	0x4E	0x9C	1	0	0	1	1	**1**	0	0
I2C Rd	GND	0x4E	0x9D	1	0	0	1	1	**1**	0	1
I2C Wr	IO_VDD	0x4F	0x9E	1	0	0	1	1	**1**	1	0
I2C Rd	IO_VDD	0x4F	0x9F	1	0	0	1	1	**1**	1	1

Table 8: I²C Slave Addresses for KXG03-1034

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I²C bus is now free. Note that if the KXG03 is accessed through I²C protocol before the startup is finished a NACK signal is sent.

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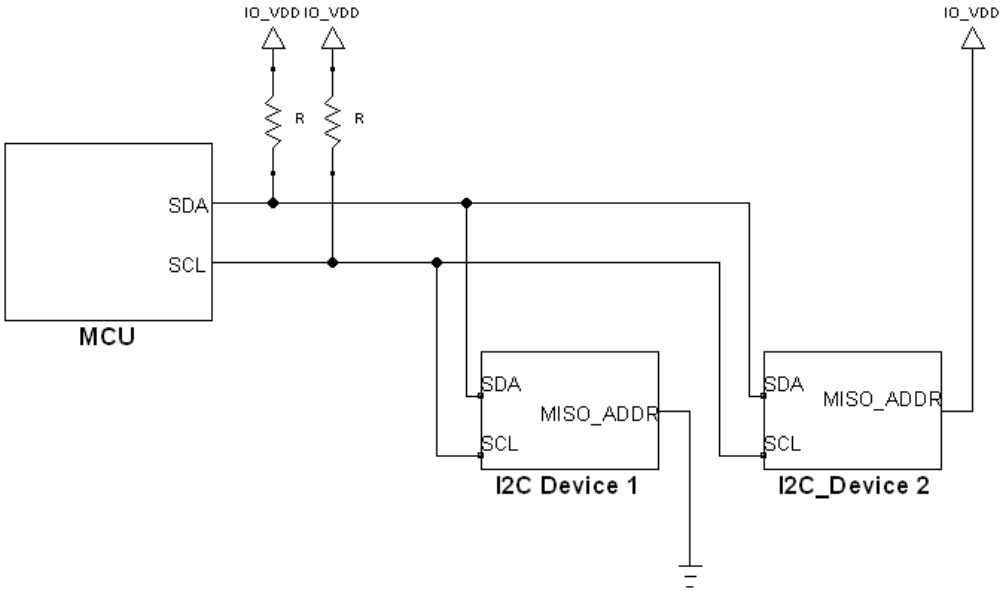

I2C Device	Part Number	ADDR Pin	Slave Address	Bit Y (Bit 1 in 7-bit address)
1	KXG03-1034	GND	0x4E	Factory Set to 1
2	KXG03-1034	IO_VDD	0x4F	Factory Set to 1

Figure 3: Multiple KXG03 Sensors on a Shared I²C Bus

Writing to 8-bit Register

Upon power up, the Master must write to the KXG03's control registers to set its operational mode. Therefore, when writing to a control register on the I²C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KXG03 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KXG03 to which 8-bit register the Master will be writing the data. Since this is I²C mode, the MSB of the RA command should always be zero (0). The KXG03 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KXG03 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KXG03 is now stored in the appropriate register. The KXG03 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.
Note** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it may alter the content of the affected registers.

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Reading from 8-bit Register

When reading data from a KXG03 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KXG03 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KXG03 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KXG03 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KXG03 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 below. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command. Note, accelerometer's and/or gyroscope's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.

****Note**** KXG03's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.

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Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I²C bus and how the Master and Slave interact during these transfers. The table below defines the I²C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 9: I²C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

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HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5: HS-mode data transfer of the Master writing multiple bytes to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	Sr	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

n bytes + ack.

Sequence 6: HS-mode data transfer of the Master receiving multiple bytes of data from the Slave.

Speed	FS-mode			HS-mode				
Master	S	M-code	NACK	Sr	SAD + W		RA	
Slave						ACK		ACK

Speed	HS-mode								FS-mode
Master	Sr	SAD + R					NACK	P	
Slave			ACK	DATA	ACK	DATA			

(n-1) bytes + ack.

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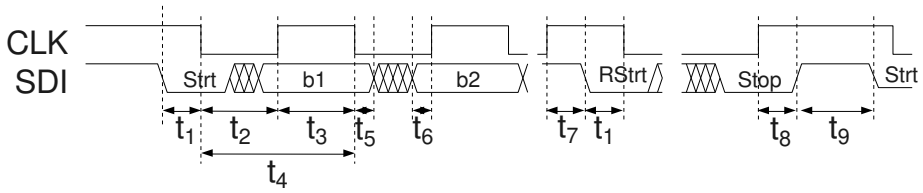
I²C Timing Diagram



I²C Timing Specifications

		Standard and Fast Mode		High Speed Mode		
Number	**Description**	**MIN**	**MAX**	**MIN**	**MAX**	**Units**
t_1	Hold time START condition	600		160		ns
t_2	SCL low	1300		320		ns
t_3	SCL high	600		120		ns
t_4	SCL Period	25000		588		ns
t_5	SDI to SCL rise setup time	100		10		ns
t_6	SCL fall to SDI hold time	0	900	0	150	ns
t_7	Setup time for repeated START condition	600		160		ns
t_8	Setup time SCL rise to SDI rise for STOP condition	600		600		ns
t_9	Bus free time between STOP and START conditions	1300		1300		ns
	SCL rise transition time (30-70%)		300		160	ns
	SCL fall transition time (30-70%)		300		80	ns
	SDI rise transition time (30-70%)		300		80	ns
	SDI fall transition time (30-70%)		300		160	ns

Table 10: I²C Timing Specifications (Standard, Fast and High Speed Mode)

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Auxiliary I²C Operation

The KXG03 has an auxiliary I²C bus for communicating to external I²C-supported sensors. This bus has an I²C Host Mode where the KXG03 acts as a host to external sensors, and a Bypass Mode where the KXG03 directly connects the primary and auxiliary I²C buses together. This allows the system processor to directly communicate with the external sensors. Maximum data rate for this bus is 400KHz Fast Mode. With the auxiliary I²C enabled the AUX_CL pin operates as an output-only pin. The auxiliary I2C hence does not support clock stretching and KXG03 should not be mated with external devices using clock stretching

Auxiliary I²C Host Mode

This mode allows the KXG03 to directly access the data registers of any external sensors connected to the auxiliary I²C bus. In this mode, the KXG03 directly obtains data from the auxiliary sensors and packages them with its own sensor data inside the internal FIFO buffer.

In Host Mode the KXG03 is easily configured to read up to six successive registers from up to two different auxiliary devices. The user simply configures KXG03 control registers with up to two different I²C SAD's, starting register addresses and the number of bytes to be read back via auto-increment.

Auxiliary I²C Bypass Mode

This mode allows an external processor to act as host and directly communicate to the auxiliary devices. This allows the host to initialize the auxiliary sensors for operation, or to access them directly while the KXG03 is disabled. The AUX_CL and AUX_DA pins can be operated in bypass mode shorted to SCLK_SCL and the MOSI_SDA pins, respectively. When operated in bypass mode the connection to the main I2C pins is broken while nCS is low (i.e. while the main interface is operating in SPI mode).

Internal Pull-up Resistor

The auxiliary I²C interface can be operated with external or internal pull up devices. Internal pull up devices are automatically disabled in bypass mode to prevent pulling up the main I²C /SPI interface. The KXG03 AUX_CL pin is driven by as a rail-to-rail (push-pull) CMOS output. The AUX_CL pin hence does not require external (or internal) pull ups.

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