Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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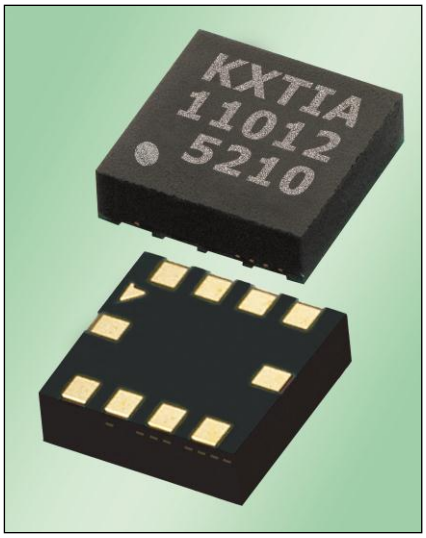
Kionix®	**± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXTIA-1006** **Rev. 4** **Dec-2012**

Product Description



The KXTIA is a tri-axis +/-2g, +/-4g or +/-8g silicon micromachined accelerometer with integrated orientation, tap/double tap, and activity detecting algorithms. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable application algorithms. The accelerometer is delivered in a 3 x 3 x 0.9 mm LGA plastic package operating from a 1.8 – 3.6V DC supply. Voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics over the range of input supply voltages and virtually undetectable ratiometric error. The SPI digital protocol is used to communicate with the chip to configure and check for updates to the orientation, Directional Tap™ detection and activity monitoring algorithms.

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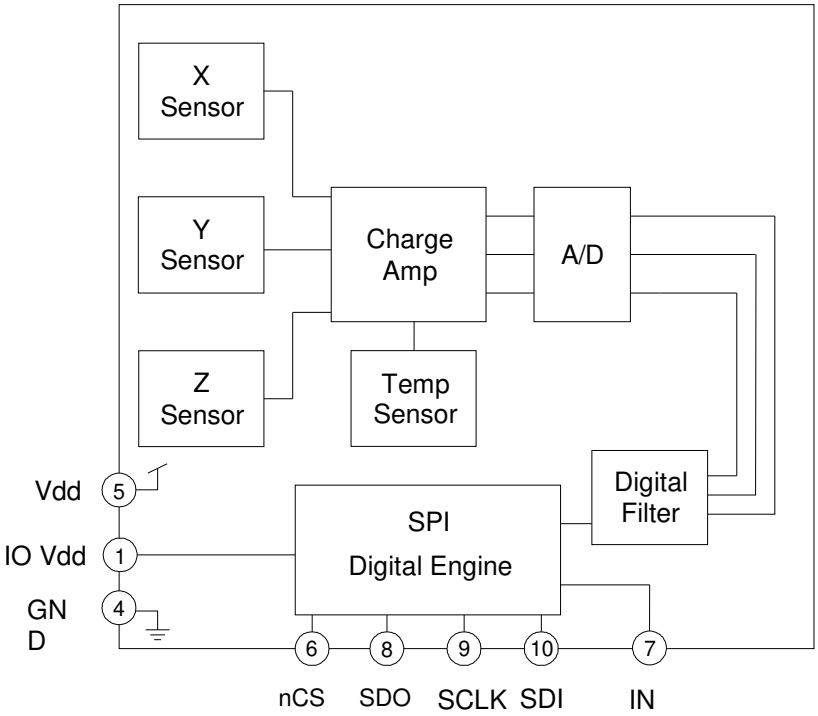
Functional Diagram



Kionix®	**± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXTIA-1006** **Rev. 4** **Dec-2012**

Product Specifications

Table 1. Mechanical

(specifications are for operation at 2.6V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Zero-g Offset		mg	-	±25	±125
Zero-g Offset Variation from RT over Temp.		mg/ºC		0.7 (xy) 0.4 (z)	
Sensitivity (12-bit)[1]	GSEL1=0, GSEL0=0 (± 2g)	counts/g	988	1024	1060
	GSEL1=0, GSEL0=1 (± 4g)		494	512	530
	GSEL1=1, GSEL0=0 (± 8g)		247	256	265
Sensitivity (8-bit)[1]	GSEL1=0, GSEL0=0 (± 2g)	counts/g	61	64	67
	GSEL1=0, GSEL0=1 (± 4g)		30	32	34
	GSEL1=1, GSEL0=0 (± 8g)		15	16	17
Sensitivity Variation from RT over Temp.		%/ºC		0.01 (xy) 0.03 (z)	
Self Test Output change on Activation		g		0.7 (xy) 0.5 (z)	
Mechanical Resonance (-3dB)[2]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.6	
Cross Axis Sensitivity		%		2	

Notes:

1. Resolution and acceleration ranges are user selectable via SPI.
2. Resonance as defined by the dampened mechanical sensor.

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Table 2. Electrical

(specifications are for operation at 2.6V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Operating	V	1.71	2.6	3.6
I/O Pads Supply Voltage (V_{IO})		V	1.7		V_{dd}
Current Consumption	All On (RES = 1)	µA		325	
	Directional Tap™ (RES = 0, ODR = 400Hz)			165	
	Low Power (RES = 0, ODR ≤ 25Hz)			100	
	Standby			10	
Output Low Voltage		V	-	-	0.2 * V_{io}
Output High Voltage		V	0.8 * V_{io}	-	-
Input Low Voltage		V	-	-	0.2 * V_{io}
Input High Voltage		V	0.8 * V_{io}	-	-
Input Pull-down Current		µA		0	
Start Up Time[1]	RES = 0	ms		0.050	
	RES = 1, ODR = 12.5Hz			81	
	RES = 1, ODR = 25 Hz			41	
	RES = 1, ODR = 50Hz			21	
	RES = 1, ODR = 100Hz			11	
	RES = 1, ODR = 200Hz			6	
	RES = 1, ODR = 400Hz			4	
	RES = 1, ODR = 800Hz			2.5	
Power Up Time[2]		ms		10	
SPI Communication Rate		MHz			20
Output Data Rate (ODR)[3]		Hz	12.5	50	800
Bandwidth (-3dB)[4]	RES = 0	KHz		1.59	
	RES = 1	Hz		ODR/2	

Notes:

1. Start up time is from PC1 set to valid outputs.
2. Power up time is from Vdd valid to device boot completion.
3. User selectable through SPI.
4. User selectable and dependant on ODR and RES.

Table 3. Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Absolute Limits	V	-0.5	-	3.63
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Application Schematic

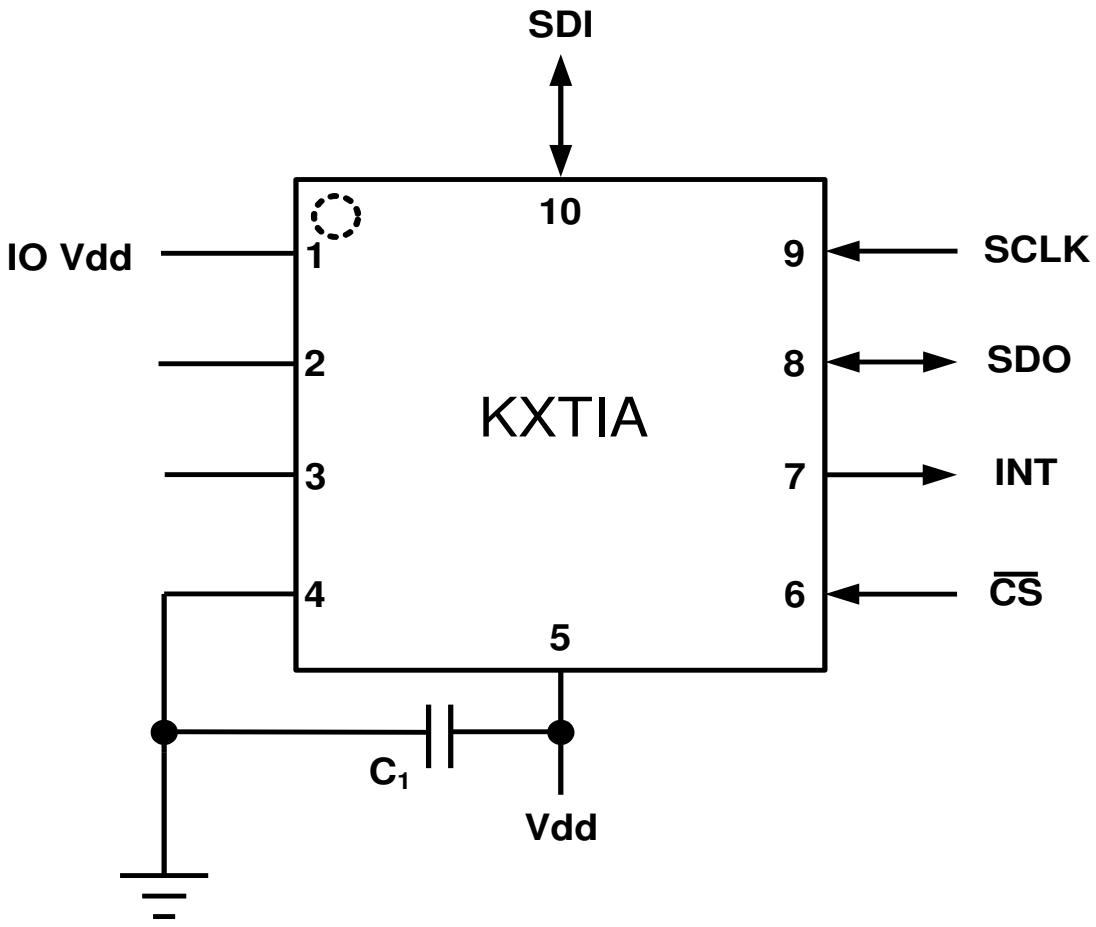

Table 4. KXTIA Pin Descriptions

Pin	Name	Description
1	IO Vdd	The power supply input for the digital communication bus
2	DNC	Reserved – Do Not Connect
3	DNC	Reserved – Do Not Connect
4	GND	Ground
5	Vdd	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
6	nCS	SPI Enable
7	INT	Interrupt
8	SDO	SPI Serial Data Output
9	SCLK	SPI Serial Clock
10	SDI	SPI Serial Data Input

Test Specifications

! ***Special Characteristics**:*

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

Table 5. Test Specifications

Parameter	Specification	Test Conditions
Zero-g Offset @ RT	0 +/- 128 counts	25C, Vdd = 2.6 V
Sensitivity @ RT	1024 +/- 35.8 counts/g	25C, Vdd = 2.6 V

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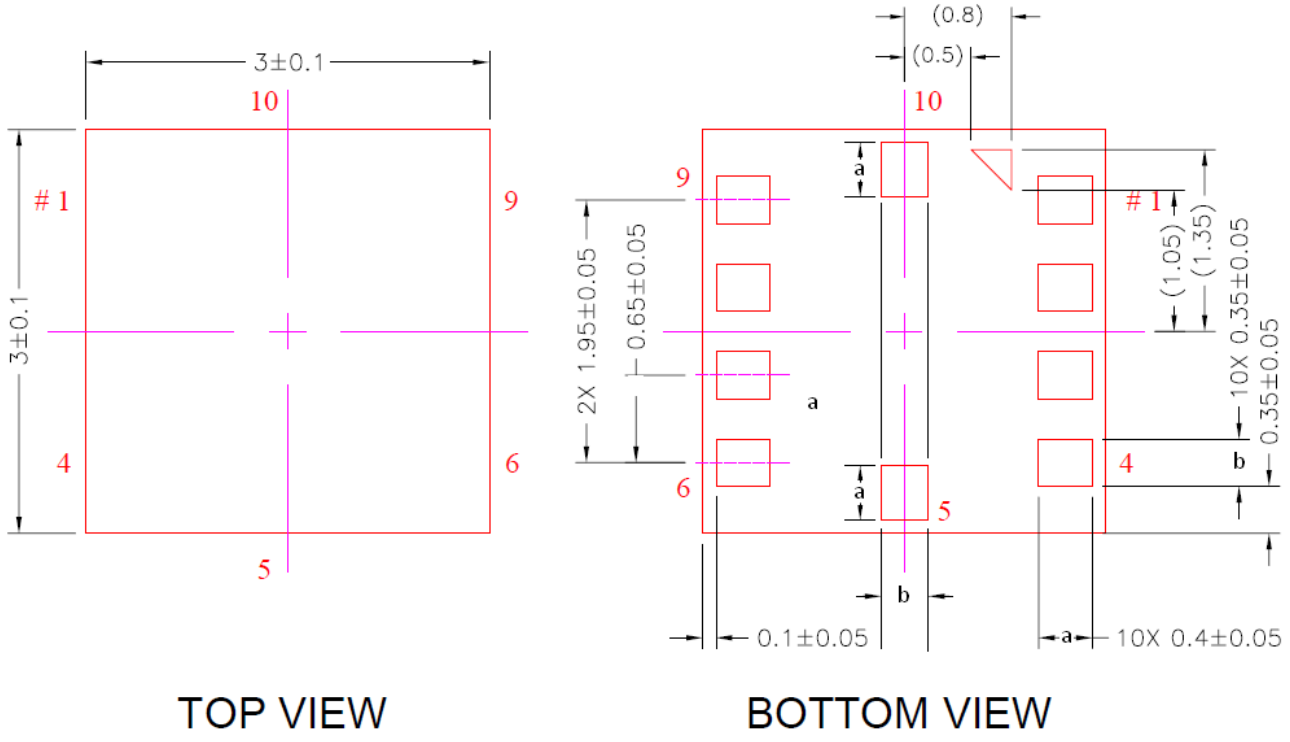
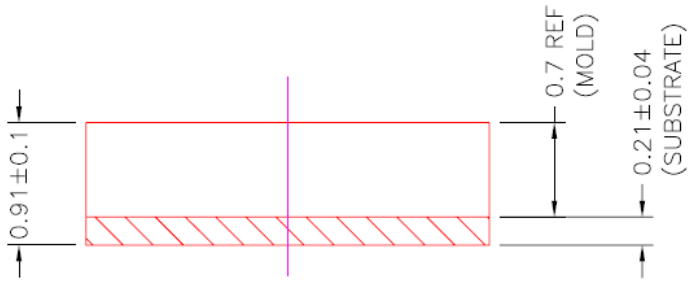
Package Dimensions and Orientation

3 x 3 x 0.9 mm LGA



TOP VIEW

BOTTOM VIEW



SIDE VIEW

All dimensions and tolerances conform to ASME Y14.5M-1994

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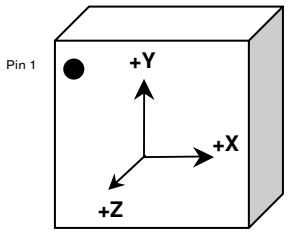
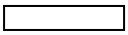
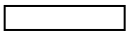
Orientation



When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0 (± 2g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	1024	64	0	0	-1024	-64	0	0	0	0
Y (counts)	1024	64	0	0	-1024	-64	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	1024	64	-1024	-64
X-Polarity	**0**		**+**		**0**		**-**		**0**		**0**	
Y-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

Earth's Surface

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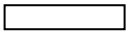
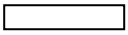
Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1 (± 4g)

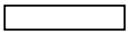
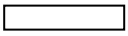
Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	512	32	0	0	-512	-32	0	0	0	0
Y (counts)	512	32	0	0	-512	-32	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	512	32	-512	-32
X-Polarity	**0**		**+**		**0**		**-**		**0**		**0**	
Y-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

 (1g)

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0 (± 8g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	256	16	0	0	-256	-16	0	0	0	0
Y (counts)	256	16	0	0	-256	-16	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	256	16	-256	-16
X-Polarity	**0**		**+**		**0**		**-**		**0**		**0**	
Y-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

 (1g)

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KXTIA Digital Interface

The Kionix KXTIA digital accelerometer has the ability to communicate on the SPI digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 6. Serial Interface Terminologies

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4-Wire SPI Communications

KXTIA 4-Wire SPI Timing Diagram

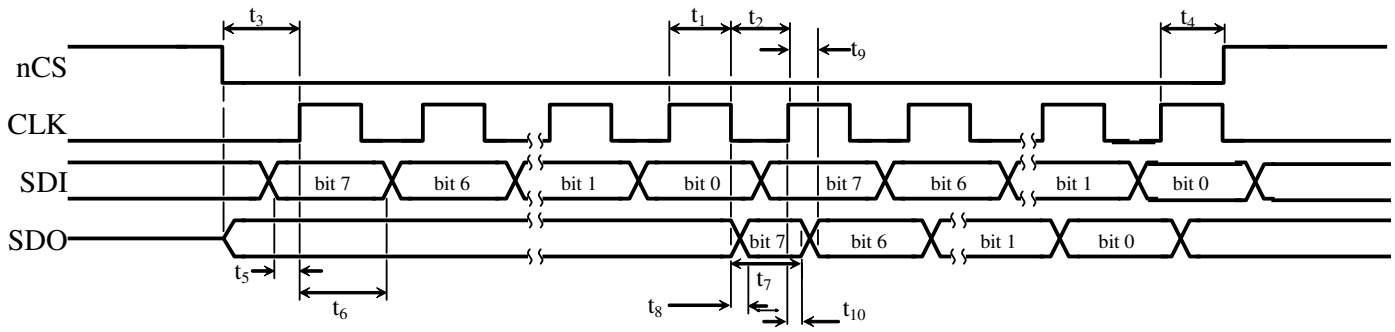

Table 7. 4-Wire SPI Timing

Number	Description	MIN	MAX	Units
t_1	CLK pulse width: high	24		ns
t_2	CLK pulse width: low	26		ns
t_3	nCS low to first CLK rising edge	13		ns
t_4	nCS low after the final CLK rising edge	20		ns
t_5	SDI valid to CLK rising edge	13		ns
t_6	CLK rising edge to SDI invalid	11		ns
t_7	CLK falling edge to SDO valid		t_2	ns
t_8	CLK falling edge to SDO valid bit<7>	19	25	ns
t_9	CLK rising edge to SDO valid bit<6:0>	19	23	ns
t_{10}	CLK rising edge to SDO invalid	15		ns

Notes

1. t_7 is only present during reads.
2. Timings are for Vdd of 1.8V to 3.6V with 1KΩ pull-up resistor and maximum 20pF load capacitor on SDO.
3. Falling Edge timing of Bit 7 applies only to first byte in auto-increment read and not subsequent bytes. For Bit 7 Max is t2/2.

KXTIA 3-Wire SPI Timing Diagram

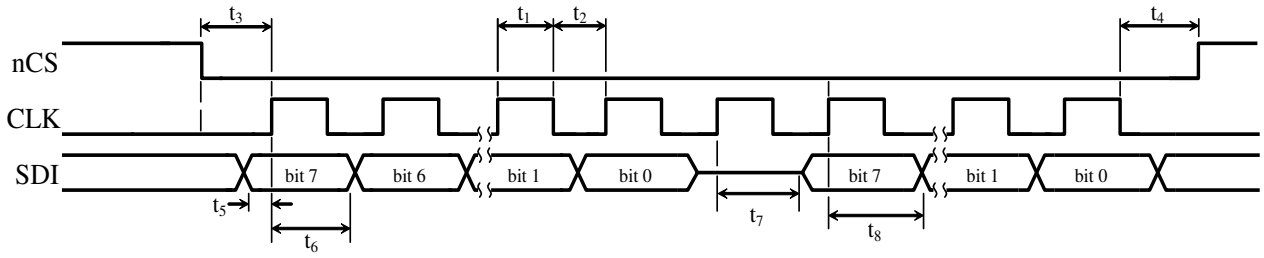

Table 8. 3-Wire SPI Timing

Number	Description	MIN	MAX	Units
t_1	CLK pulse width: high	15	-	ns
t_2	CLK pulse width: low	15	-	ns
t_3	nCS low to first CLK rising edge	8	-	ns
t_4	nCS low after the final CLK falling edge	12	-	ns
t_5	SDI valid to CLK rising edge	8	-	ns
t_6	CLK rising edge to SDI input invalid	14	-	ns
t_7	CLK extra clock cycle rising edge to SDI output becomes valid	15	-	ns
t_8	CLK rising edge to SDI output becomes valid	-	18	ns

Notes
1. t_7 and t_8 are only present during reads.
2. Timings are for Vdd of 1.8V to 3.6V with 1KΩ pull-up resistor and maximum 20pF load capacitor on SDI.

4-Wire SPI Interface

The KXTIA also utilizes an integrated 4-Wire Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The KXTIA always operates as a Slave device during standard Master-Slave SPI operation.

4-wire SPI is a synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDI or MOSI) and the Data Input (SDO or MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in Figure 2 below.

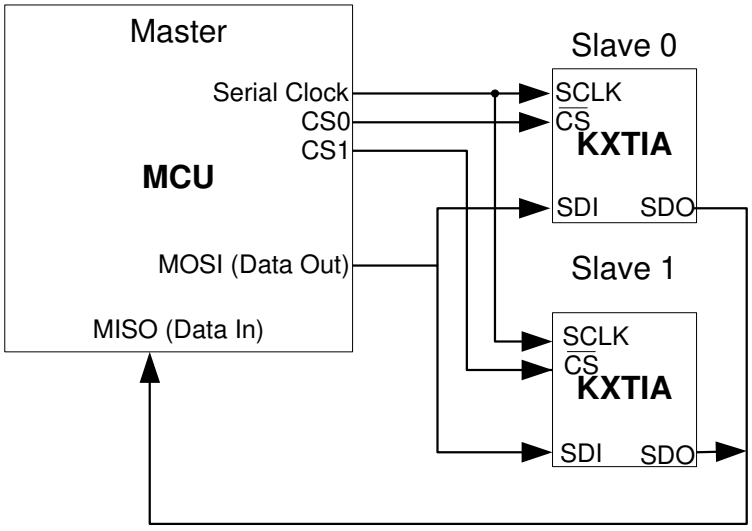

Figure 2 KXTIA 4-wire SPI Connections

Read and Write Registers

The registers embedded in the KXTIA have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. This operation occurs over 16 clock cycles. All commands are sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. Figure 3 below shows the timing diagram for carrying out an 8-bit register write operation.

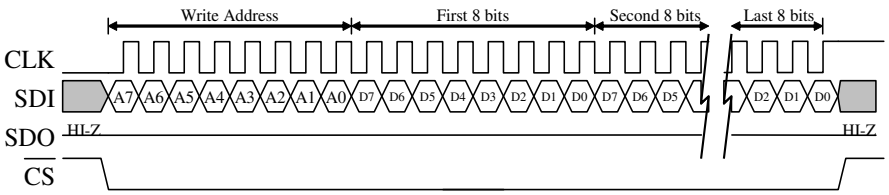

Figure 3 Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. This operation also occurs over 16 clock cycles. All returned data is sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. Figure 4 shows the timing diagram for an 8-bit register read operation.

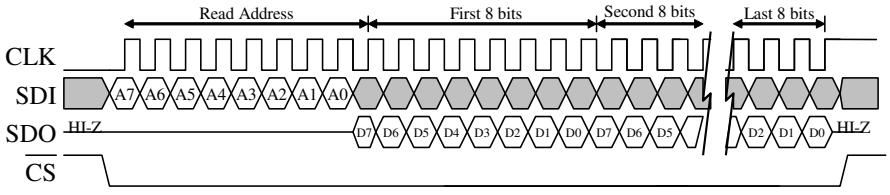

Figure 4 Timing Diagram for 8-Bit Register Read Operation

3-Wire SPI Interface

The KXTIA also utilizes an integrated 3-Wire Serial Peripheral Interface (SPI) for digital communication. 3-wire SPI is a synchronous serial interface that uses two control lines and one data line. With respect to the Master, the Serial Clock output (SCLK), the Data Output/Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. This allows multiple Slave devices to share a master SPI port as shown in Figure 6 below.

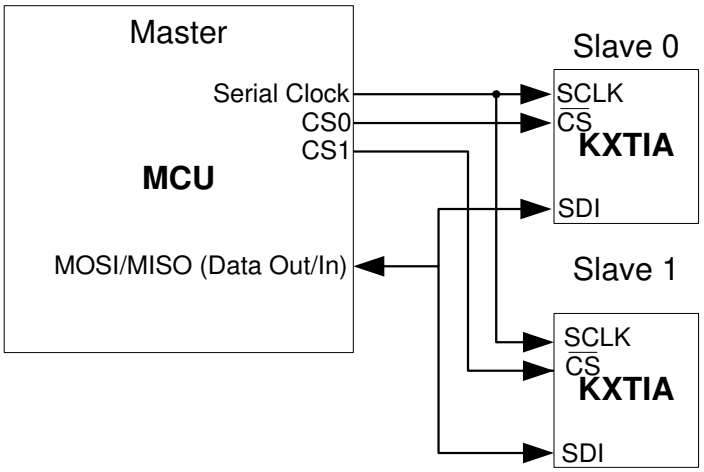

Figure 5 KXTIA 3-wire SPI Connections

Read and Write Registers

The registers embedded in the KXTIA have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. A read operation occurs over 17 clock cycles and a write operation occurs over 16 clock cycles. All commands are sent MSB first, and the host must return nCS high for at least one clock cycle before the next address transmission. Figure 6 below shows the timing diagram for carrying out an 8-bit register write operation.

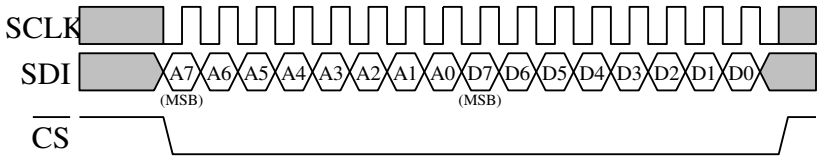

Figure 6 Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. For 3-wire read operations, one extra clock cycle between the address byte and the data output byte is required. Therefore, this operation occurs over 17 clock cycles. All returned data is sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. Figure 7 shows the timing diagram for an 8-bit register read operation.

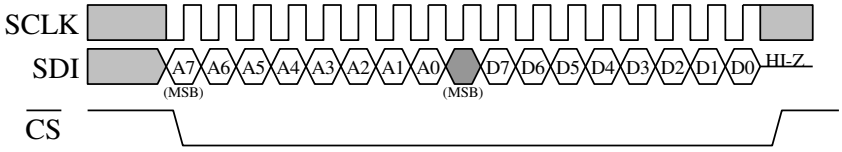

Figure 7 Timing Diagram for 8-Bit Register Read Operation

KXTIA Embedded Registers

The KXTIA has 44 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 9 below provides a listing of the accessible 8-bit registers and their addresses.

Register Name	Type Read/Write	SPI Write Address Hex	SPI Write Address Binary	SPI Read Address Hex	SPI Read Address Binary
XOUT_HPF_L	R	0x00	0000 0000	0x80	1000 0000
XOUT_HPF_H	R	0x01	0000 0001	0x81	1000 0001
YOUT_HPF_L	R	0x02	0000 0010	0x82	1000 0010
YOUT_HPF_H	R	0x03	0000 0011	0x83	1000 0011
ZOUT_HPF_L	R	0x04	0000 0100	0x84	1000 0100
ZOUT_HPF_H	R	0x05	0000 0101	0x85	1000 0101
XOUT_L	R	0x06	0000 0110	0x86	1000 0110
XOUT_H	R	0x07	0000 0111	0x87	1000 0111
YOUT_L	R	0x08	0000 1000	0x88	1000 1000
YOUT_H	R	0x09	0000 1001	0x89	1000 1001
ZOUT_L	R	0x0A	0000 1010	0x8A	1000 1010
ZOUT_H	R	0x0B	0000 1011	0x8B	1000 1011
DCST_RESP	R	0x0C	0000 1100	0x8C	1000 1100
Not Used	-	0x0D	0000 1101	0x8D	1000 1101
Not Used	-	0x0E	0000 1110	0x8E	1000 1110
WHO_AM_I	R	0x0F	0000 1111	0x8F	1000 1111
TILT_POS_CUR	R	0x10	0001 0000	0x90	1001 0000
TILT_POS_PRE	R	0x11	0001 0001	0x91	1001 0001
Kionix Reserved	-	0x12	0001 0010	0x92	1001 0010
Kionix Reserved	-	0x13	0001 0011	0x93	1001 0011
Kionix Reserved	-	0x14	0001 0100	0x94	1001 0100
INT_SRC_REG1	R	0x15	0001 0101	0x95	1001 0101
INT_SRC_REG2	R	0x16	0001 0110	0x96	1001 0110
Not Used	-	0x17	0001 0111	0x97	1001 0111
STATUS_REG	R	0x18	0001 1000	0x98	1001 1000
Not Used	-	0x19	0001 1001	0x99	1001 1001
INT_REL	R	0x1A	0001 1010	0x9A	1001 1010
CTRL_REG1*	R/W	0x1B	0001 1011	0x9B	1001 1011
CTRL_REG2*	R/W	0x1C	0001 1100	0x9C	1001 1100

CTRL_REG3*	R/W	0x1D	0001 1101	0x9D	1001 1101
INT_CTRL_REG1*	R/W	0x1E	0001 1110	0x9E	1001 1110
INT_CTRL_REG2*	R/W	0x1F	0001 1111	0x9F	1001 1111
INT_CTRL_REG3*	R/W	0x20	0010 0000	0xA0	1010 0000
DATA_CTRL_REG*	R/W	0x21	0010 0001	0xA1	1010 0001
Not Used	-	0x22 – 0x27	-	0xA2 – 0xA7	-
TILT_TIMER*	R/W	0x28	0010 1000	0xA8	1010 1000
WUF_TIMER*	R/W	0x29	0010 1001	0xA9	1010 1001
Not Used	-	0x2A	0010 1010	0xAA	1010 1010
TDT_TIMER*	R/W	0x2B	0010 1011	0xAB	1010 1011
TDT_H_THRESH*	R/W	0x2C	0010 1100	0xAC	1010 1100
TDT_L_THRESH*	R/W	0x2D	0010 1101	0xAD	1010 1101
TDT_TAP_TIMER*	R/W	0x2E	0010 1110	0xAE	1010 1110
TDT_TOTAL_TIMER*	R/W	0x2F	0010 1111	0xAF	1010 1111
TDT_LATENCY_TIMER*	R/W	0x30	0011 0000	0xB0	1011 0000
TDT_WINDOW_TIMER*	R/W	0x31	0011 0001	0xB1	1011 0001
BUF_CTRL1*	R/W	0x32	0011 0010	0xB2	1011 0010
BUF_CTRL2*	R/W	0x33	0011 0011	0xB3	1011 0011
BUF_STATUS_REG1	R	0x34	0011 0100	0xB4	1011 0100
BUF_STATUS_REG2	R	0x35	0011 0101	0xB5	1011 0101
BUF_CLEAR	W	0x36	0011 0110	0xB6	1011 0110
Reserved	-	0x37 – 0x39	-	0xB7 - 0xB9	-
SELF_TEST	R/W	0x3A	0011 1010	0xBA	1011 1010
Reserved	-	0x3B – 0x59	-	0xBB – 0xD9	-
WUF_THRESH*	R/W	0x5A	0101 1010	0xDA	1101 1010
Reserved	-	0x5B	0101 1011	0xDB	1101 1011
TILT_ANGLE*	R/W	0x5C	0101 1100	0xDC	1101 1100
Reserved	-	0x5D – 0x5E	-	0xDD – 0xDE	-
HYST_SET*	R/W	0x6F	0110 1111	0xEF	1110 1111
BUF_READ	R	0x7F	0111 1111	0xFF	1111 1111

* Note: When changing the contents of these registers, the PC1 bit in CTRL_REG1 must first be set to “0”.

Table 9. KXTIA Register Map

KXTIA Register Descriptions

Accelerometer Outputs

These registers contain up to 12-bits of valid acceleration data for each axis depending on the setting of the RES bit in CTRL_REG1, where the acceleration outputs are represented in 12-bit valid data when RES = '1' and 8-bit valid data when RES = '0'. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Figure 1 below. The register acceleration output binary data is represented in N-bit 2's complement format. For example, if N = 12 bits, then the Counts range is from -2048 to 2047, and if N = 8 bits, then the Counts range is from -128 to 127.

12-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111 1111	2047	+1.999g	+3.998g	+7.996g
0111 1111 1110	2046	+1.998g	+3.996g	+7.992g
…	…	…	…	…
0000 0000 0001	1	+0.001g	+0.002g	+0.004g
0000 0000 0000	0	0.000g	0.000g	0.000g
1111 1111 1111	-1	-0.001g	-0.002g	-0.004g
…	…	…	…	…
1000 0000 0001	-2047	-1.999g	-3.998g	-7.996g
1000 0000 0000	-2048	-2.000g	-4.000g	-8.000g

8-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111	127	+1.984g	+3.968g	+7.936g
0111 1110	126	+1.968g	+3.936g	+7.872g
…	…	…	…	…
0000 0001	1	+0.016g	+0.032g	+0.064g
0000 0000	0	0.000g	0.000g	0.000g
1111 1111	-1	-0.016g	-0.032g	-0.064g
…	…	…	…	…
1000 0001	-127	-1.984g	-3.968g	-7.936g
1000 0000	-128	-2.000g	-4.000g	-8.000g

Figure 1. Acceleration (g) Calculation

Note: *The High Pass Filter outputs are only available if the Wake Up Function is enabled.*

XOUT_HPF_L

X-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
XOUTD3	XOUTD2	XOUTD1	XOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x00h		
					SPI Read Address: 0x80h		

XOUT_HPF_H

X-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
XOUTD11	XOUTD10	XOUTD9	XOUTD8	XOUTD7	XOUTD6	XOUTD5	XOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x01h		
					SPI Read Address: 0x81h		

YOUT_HPF_L

Y-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
YOUTD3	YOUTD2	YOUTD1	YOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x02h		
					SPI Read Address: 0x82h		

YOUT_HPF_H

Y-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
YOUTD11	YOUTD10	YOUTD9	YOUTD8	YOUTD7	YOUTD6	YOUTD5	YOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x03h		
					SPI Read Address: 0x83h		

ZOUT_HPF_L

Z-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x04h		
					SPI Read Address: 0x84h		

ZOUT_HPF_H

Z-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
ZOUTD11	ZOUTD10	ZOUTD9	ZOUTD8	ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x05h		
					SPI Read Address: 0x85h		

XOUT_L

X-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
XOUTD3	XOUTD2	XOUTD1	XOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x06h		
					SPI Read Address: 0x86h		

XOUT_H

X-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
XOUTD11	XOUTD10	XOUTD9	XOUTD8	XOUTD7	XOUTD6	XOUTD5	XOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x07h		
					SPI Read Address: 0x87h		

YOUT_L

Y-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
YOUTD3	YOUTD2	YOUTD1	YOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x08h		
					SPI Read Address: 0x88h		

YOUT_H

Y-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
YOUTD11	YOUTD10	YOUTD9	YOUTD8	YOUTD7	YOUTD6	YOUTD5	YOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x09h		
					SPI Read Address: 0x89h		

ZOUT_L

Z-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x0Ah		
					SPI Read Address: 0x8Ah		

ZOUT_H

Z-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
ZOUTD11	ZOUTD10	ZOUTD9	ZOUTD8	ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					SPI Write Address: 0x0Bh		
					SPI Read Address: 0x8Bh		

DCST_RESP

This register can be used to verify proper integrated circuit functionality. It always has a byte value of 0x55h unless the DCST bit in CTRL_REG3 is set. At that point this value is set to 0xAAh. The byte value is returned to 0x55h after reading this register.

R	R	R	R	R	R	R	R	
DCSTR7	DCSTR6	DCSTR5	DCSTR4	DCSTR3	DCSTR2	DCSTR1	DCSTR0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01010101
					SPI Write Address: 0x0Ch			
					SPI Read Address: 0x8Ch			

WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x06h.

R	R	R	R	R	R	R	R	
WIA7	WIA6	WIA5	WIA4	WIA3	WIA2	WIA1	WIA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000110
					SPI Write Address: 0x0Fh			
					SPI Read Address: 0x8Fh			