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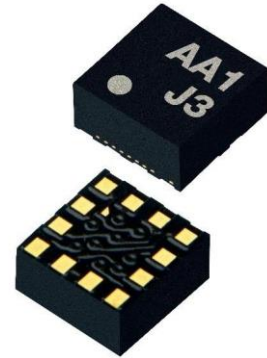
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	± 2g / 4g / 8g / 16g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KXTJ3-1057 Rev. 3.0 27-Sep-2017
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Product Description

The KXTJ3-1057 is a tri-axis $\pm 2g$, $\pm 4g$, $\pm 8g$, or $\pm 16g$ silicon micromachined accelerometer. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning and digital communications. The accelerometer is delivered in a 2 x 2 x 0.9 mm LGA plastic package operating from a 1.71V – 3.6V DC supply. Voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics over the range of input supply voltages and virtually undetectable ratiometric error. The I²C digital protocol is used to communicate with the chip to configure the part and monitor outputs.



Features

- Small footprint: 2 x 2 x 0.9 mm LGA 12-pin package (pin-to-pin compatible with KXTJ2)
- Low current consumption: 0.9 μ A in standby, 10 μ A in Low Power, and 155 μ A in High Resolution modes
- Extended user-configurable g-ranges: $\pm 2g$, $\pm 4g$, $\pm 8g$, $\pm 16g$
- 8-bit, 12-bit, and 14-bit resolution modes
- Wide supply voltage range: 1.71V – 3.6V with internal voltage regulator
- High resolution Wake-Up function with threshold configurable down to 3.9 mg
- User-configurable Output Data Rates from 0.781Hz to 1600Hz
- I²C digital communication interface up to 3.4MHz
- Highly configurable interrupt control
- Embedded Low Pass filter
- Improved design to virtually eliminate post reflow offset and sensitivity shifts
- Improved noise performance
- Stable performance over temperature
- High shock survivability
- Self-test function
- RoHS / REACH compliant



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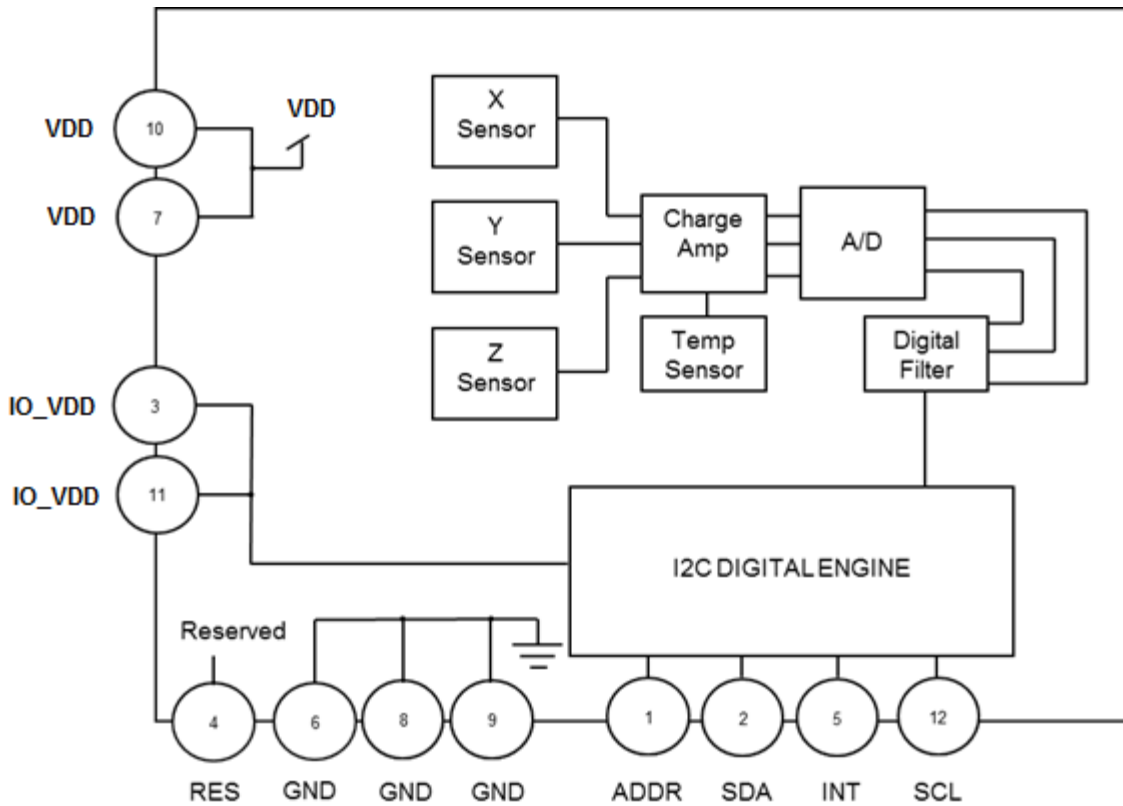
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Functional Diagram



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Product Specifications

Mechanical


(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	+85
Zero-g Offset		mg		±25	
Zero-g Offset Variation from RT over Temp.		mg/°C		0.2	
Sensitivity (14-bit) ^{1,2}	± 8g	counts/g		1024	
	± 16g			512	
Sensitivity (12-bit) ¹	± 2g	counts/g		1024	
	± 4g			512	
	± 8g			256	
	± 16g			128	
Sensitivity (8-bit) ¹	± 2g	counts/g		64	
	± 4g			32	
	± 8g			16	
	± 16g			8	
Sensitivity Variation from RT over Temp.		%/°C		0.01	
Positive Self-test Output change on Activation ³		g		0.5	
Signal Bandwidth (-3dB)		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.6	
Cross Axis Sensitivity		%		2	
Noise ⁴	RMS Noise	mg		0.7	
	Noise Density	µg / √Hz		150	

Table 1: Mechanical Specifications

Notes:

- Resolution and acceleration ranges are user selectable via I²C and via CTRL_REG1 register.
- 14-bit Resolution is only available for registers 0x06 – 0x0B in the 8g or 16g High Resolution mode
- Self-test can be exercised by setting STPOL bit = 1 in INT_CTRL_REG1, then writing 0xCA to the SELF_TEST register.
- Noise measured in High Resolution Mode (RES = 1) at 50Hz ODR.

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Electrical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.71	2.5	3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.7		3.6
Current Consumption	High Resolution Mode (RES=1)	µA		155	
	Low Power Mode ¹ (RES=0)			10	
	Disabled			0.9	
Output Low Voltage (IO_VDD < 2V) ²		V	-	-	0.2 * IO_VDD
Output Low Voltage (IO_VDD ≥ 2V) ²		V	-	-	0.4
Output High Voltage		V	0.8 * IO_VDD	-	-
Input Low Voltage		V	-	-	0.2 * IO_VDD
Input High Voltage		V	0.8 * IO_VDD	-	-
Start Up Time ³		ms		~1/ODR	
Power Up Time ⁴		ms		12	30
I ² C Communication Rate		MHz			3.4
I ² C Slave Address (7-bit)				0x0E / 0x0F	
Output Data Rate (ODR) ⁵		Hz	0.781	50	1600
Bandwidth (-3dB) ⁶	RES = 0			800	
	RES = 1			ODR/2	

Table 2: Electrical Specifications

Notes:

1. Current varies with Output Data Rate (ODR). See Current Profile section for details.
2. For I²C communication, this assumes a minimum 1.5kΩ pull-up resistor on SCL and SDA pins.
3. Start up time is from PC1 set to valid outputs. Time varies with Output Data Rate (ODR). See Table 3: *Start Up Time* for details.
4. Power up time is from VDD and IO_VDD valid to device boot completion.
5. User selectable through I²C
6. User selectable and dependent on ODR and RES



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Start Up Time Profile

RES	Mode	ODR (Hz)	Start up time (ms)
0	Low-power	0.781	2
0	Low-power	1.563	2
0	Low-power	3.125	2
0	Low-power	6.25	2
0	Low-power	12.5	2
0	Low-power	25	2
0	Low-power	50	2
0	Low-power	100	2
0	Low-power	200	2
0	Full-power	400	4
0	Full-power	800	3
0	Full-power	1600	2
1	Full-power	0.781	1281
1	Full-power	1.563	641
1	Full-power	3.125	321
1	Full-power	6.25	161
1	Full-power	12.5	81
1	Full-power	25	41
1	Full-power	50	21
1	Full-power	100	11
1	Full-power	200	6
1	Full-power	400	4
1	Full-power	800	3
1	Full-power	1600	2

Table 3: Start Up Time



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Current Profile

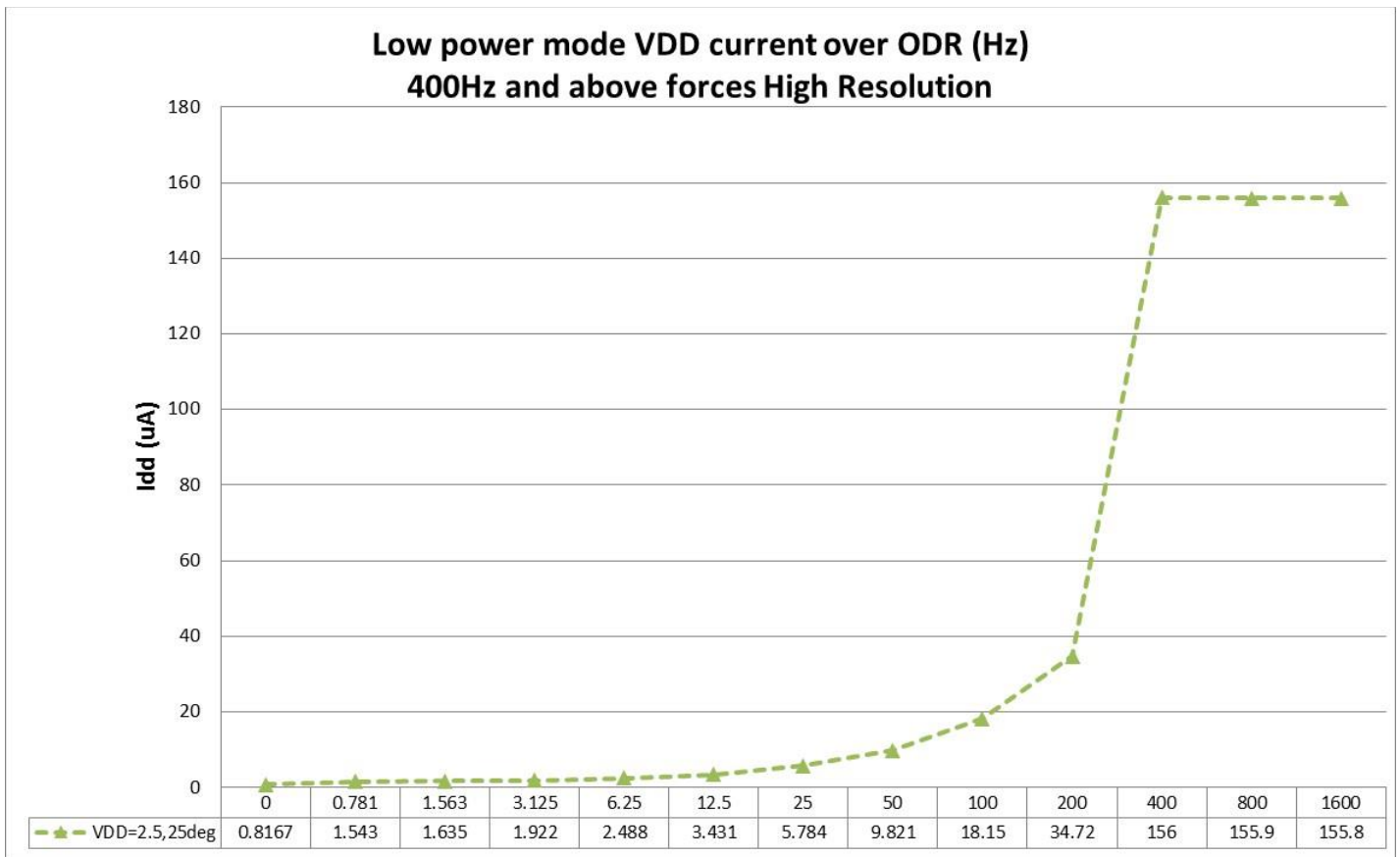



Figure 1: Current Profile

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Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD**, **VDD_{LOW}**, **T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{LOW}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the **VDD** ramp up time **T_{VDD}** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

- ! *To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD_{LOW}, T_{VDD}, T_{VDD_OFF} and temperature as POR performance can vary depending on these parameters.*

Please refer to Technical Note [TN017 KXTJ3 Accelerometer Power-On Procedure](#) for more information.

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Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.5	-	3.63
Operating Temperature Range		°C	-40	-	85
Storage Temperature Range		°C	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Table 4: Environmental Specifications



Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.



These products conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are “of uniform composition throughout”. The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.


Applicable Exemption: *7C-1 - Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix compound.*



These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-174) as identified by the European Chemicals Agency as of 12 July 2017.



This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.


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Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Floor Life

Factory floor life exposure of the KXTJ3 reels removed from the moisture barrier bag should not exceed a maximum of 168 hours at 30C/60%RH. If this floor life is exceeded, the parts should be dried per the IPC/JEDEC J-STD-033A standard.

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Terminology

g

A unit of acceleration equal to the acceleration of gravity at the earth's surface.

$$1g = 9.8 \frac{m}{s^2}$$

One thousandth of a g (0.0098 m/ s²) is referred to as 1 milli-g (1 mg).

Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal VDD and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

$$Sensitivity = \frac{(Output @ +1g - Output @ -1g)}{2g}$$


The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25°C), the sensitivity will vary by the amount shown in Table 1.

Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the OUTX, OUTY, OUTZ registers = 00h, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 00h. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified in Table 1, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

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Functionality

Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

ASIC interface

A separate ASIC device packaged with the sense element provides all of the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I²C digital communications provided by the ASIC. In addition, the ASIC contains all of the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic. Plus, there are two programmable state machines which allow the user to create unique embedded functions based on changes in acceleration.

Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in non-volatile memory (OTP). Additionally, all functional register default values are also programmed into the nonvolatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.



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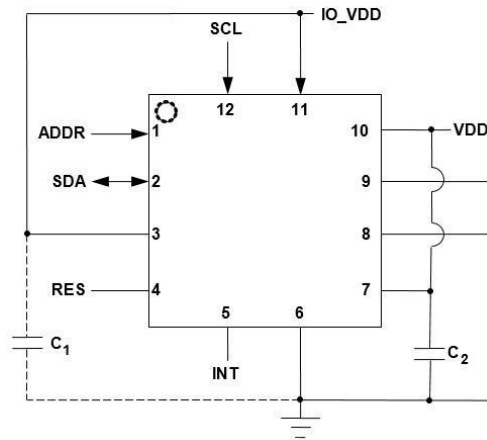
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Application Schematic



Pin Description

Pin	Name	Description
1	ADDR	I2C programmable address bit. Must be connected to IO_VDD or GND. (see Note 5)
2	SDA	I2C Serial Data
3	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor. (see Note 1)
4	RES	Reserved. Connect to GND. Do not leave floating if not used. (see Note 4)
5	INT	Physical Interrupt pin (Push-Pull). Leave floating if not used.
6	GND	Ground (see Note 2)
7	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor. (see Note 3)
8	GND	Ground (see Note 2)
9	GND	Ground (see Note 2)
10	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor. (see Note 3)
11	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor. (see Note 1)
12	SCL	I2C Serial Clock

Table 5: Pin Description

Notes:

1. IO_VDD Pins 3, and 11 are internally tied together. For backwards compatibility with other parts, one of the two pins may be left floating.
2. GND Pins 6, 8, and 9 are internally tied together. For backwards compatibility with other parts, any two of the three pins may be left floating.
3. VDD Pins 7, and 10 are internally tied together. For backwards compatibility with other parts, one of the two pins may be left floating.
4. RES Pin 4 can be optionally tied to IO_VDD or VDD instead.
5. See Digital Interface section for connection details.



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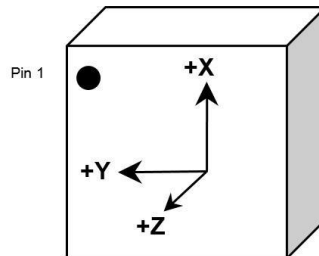
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Orientation



When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.


Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0, EN16G=0 (± 2g)

Position	1		2		3		4		5		6	
Diagram									Top Bottom		Bottom Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	1024	64	0	0	-1024	-64	0	0	0	0	0	0
Y (counts)	0	0	-1024	-64	0	0	1024	64	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	1024	64	-1024	-64
X-Polarity	+		0		-		0		0		0	
Y-Polarity	0		-		0		+		0		0	
Z-Polarity	0		0		0		0		+		-	





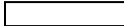
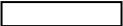


Earth's Surface

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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1, EN16G =0 (± 4g)

Position	1		2		3		4		5		6	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	512	32	0	0	-512	-32	0	0	0	0	0	0
Y (counts)	0	0	-512	-32	0	0	512	32	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	512	32	-512	-32
X-Polarity	+		0		-		0		0		0	
Y-Polarity	0		-		0		+		0		0	
Z-Polarity	0		0		0		0		+		-	







Earth's Surface

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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0, EN16G =0 (± 8g)
GSEL1=1, GSEL0=1, EN16G=0 (± 8g)¹

Position	1			2			3			4			5			6		
Diagram													<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; width: 20px; height: 10px; margin: 0 auto;"></div> <div style="text-align: center;">Top</div> </div> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; width: 20px; height: 10px; margin: 0 auto;"></div> <div style="text-align: center;">Bottom</div> </div>			<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; width: 20px; height: 10px; margin: 0 auto;"></div> <div style="text-align: center;">Top</div> </div> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; width: 20px; height: 10px; margin: 0 auto;"></div> <div style="text-align: center;">Bottom</div> </div>		
Resolution (bits)	14	12	8	14	12	8	14	12	8	14	12	8	14	12	8	14	12	8
X(counts)	1024	256	16	0	0	0	-1024	-256	-16	0	0	0	0	0	0	0	0	0
Y (counts)	0	0	0	-1024	-256	-16	0	0	0	1024	256	16	0	0	0	0	0	0
Z(counts)	0	0	0	0	0	0	0	0	0	0	0	0	1024	256	16	-1024	-256	-16
X-Polarity	+			0			-			0			0			0		
Y-Polarity	0			-			0			+			0			0		
Z-Polarity	0			0			0			0			+			-		





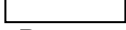
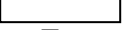
↓ (1g)

Earth's Surface

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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0, EN16G =1 (± 16g)
 GSEL1=0, GSEL0=1, EN16G =1 (± 16g)
 GSEL1=1, GSEL0=0, EN16G =1 (± 16g)
 GSEL1=1, GSEL0=1, EN16G =1 (± 16g)¹

Position	1			2			3			4			5			6		
Diagram													<div style="text-align: center;">Top</div>  <div style="text-align: center;">Bottom</div>			<div style="text-align: center;">Bottom</div>  <div style="text-align: center;">Top</div>		
Resolution (bits)	14	12	8	14	12	8	14	12	8	14	12	8	14	12	8	14	12	8
X(counts)	512	128	8	0	0	0	-512	-128	-8	0	0	0	0	0	0	0	0	0
Y (counts)	0	0	0	-512	-128	-8	0	0	0	512	128	8	0	0	0	0	0	0
Z(counts)	0	0	0	0	0	0	0	0	0	0	0	0	512	128	8	-512	-128	-8
X-Polarity	+			0			-			0			0			0		
Y-Polarity	0			-			0			+			0			0		
Z-Polarity	0			0			0			0			+			-		

↓ (1g)

Earth's Surface

Notes:

1. This is applicable for 14-bit mode only in High Resolution mode

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Digital Interface

The Kionix KXTJ3 digital accelerometer has the ability to communicate on the I²C digital serial interface bus. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 6: Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KXTJ3 has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KXTJ3 always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are high. The I²C interface is compliant with high-speed mode, fast mode and standard mode I²C standards.

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The KXTJ3's Slave Address is comprised of a programmable part and a fixed part, which allows for connection of multiple KXTJ3's to



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the same I²C bus. The Slave Address associated with the KXTJ3 is 000111X, where the programmable bit X is determined by the assignment of ADDR (pin 1) to GND or IO_VDD (Table 7). Also, Figure 2 shows how two KXTJ3's would be implemented on the same I²C bus.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I²C bus is now free. Note that if the KXTJ3 is accessed through I²C protocol before the startup is finished a NACK signal is sent.

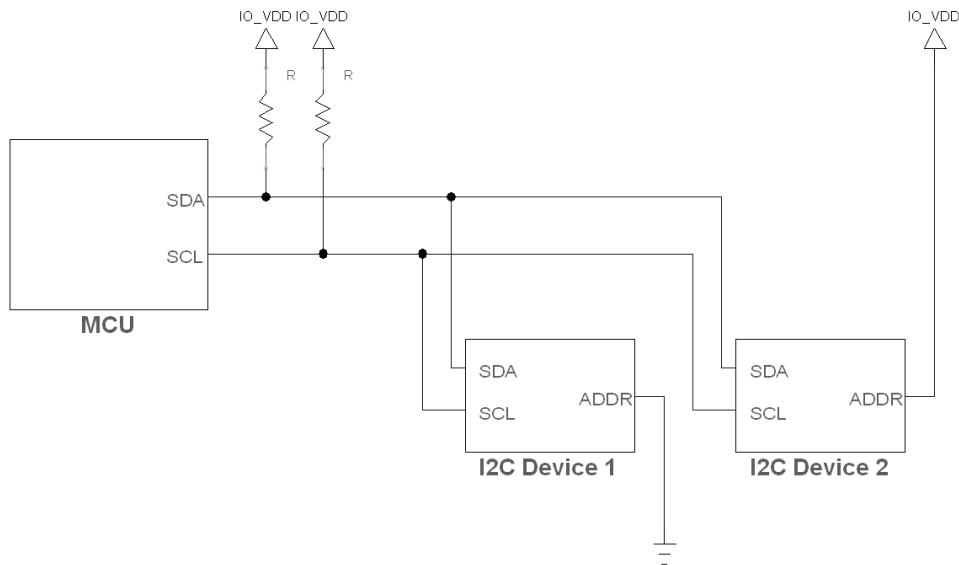



Figure 2: Multiple KXTJ3 I²C Connection

Description	Address Pad	7-bit Address	Address	<7>	<6>	<5>	<4>	<3>	Y		X	
									<2>	<1>	<0>	<0>
I2C Wr	GND	0x0E	0x1C	0	0	0	1	1	1	0	0	0
I2C Rd	GND	0x0E	0x1D	0	0	0	1	1	1	0	1	1
I2C Wr	IO_VDD	0x0F	0x1E	0	0	0	1	1	1	1	1	0
I2C Rd	IO_VDD	0x0F	0x1F	0	0	0	1	1	1	1	1	1

Table 7: I²C Slave Addresses for KXTJ3-1057

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Writing to an 8-bit Register

Upon power up, the Master must write to the KXTJ3's control registers to set its operational mode. Therefore, when writing to a control register on the I²C bus, as shown Sequence 1 below, the following protocol must be observed: After a start condition, SAD+W transmission, and the KXTJ3 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KXTJ3 to which 8-bit register the Master will be writing the data. Since this is I²C mode, the MSB of the RA command should always be zero (0). The KXTJ3 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KXTJ3 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KXTJ3 is now stored in the appropriate register. The KXTJ3 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Note** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it may alter the content of the affected registers.

Reading from an 8-bit Register

When reading data from a KXTJ3 8-bit register on the I²C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KXTJ3 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KXTJ3 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KXTJ3 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KXTJ3 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4. The 8-bit register data is transmitted using a left-most format, first bit shifted/clocked out being the MSB bit. If a receiver cannot transmit or receive another complete byte of data until it has performed some other function, it can hold SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases SCL.

Note** Accelerometer's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.

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Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I²C bus and how the Master and Slave interact during these transfers. Table 8 defines the I²C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 8: I²C Terms

Sequence 1: The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2: The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3: The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4: The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

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HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5: HS-mode data transfer of the Master writing multiple bytes to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	Sr	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

n bytes + ack.

Sequence 6: HS-mode data transfer of the Master receiving multiple bytes of data from the Slave.

Speed	FS-mode			HS-mode				
Master	S	M-code	NACK	Sr	SAD + W		RA	
Slave						ACK		ACK

Speed	HS-mode								FS-mode
Master	Sr	SAD + R					NACK	P	
Slave			ACK	DATA	ACK	DATA			

(n-1) bytes +
ack.



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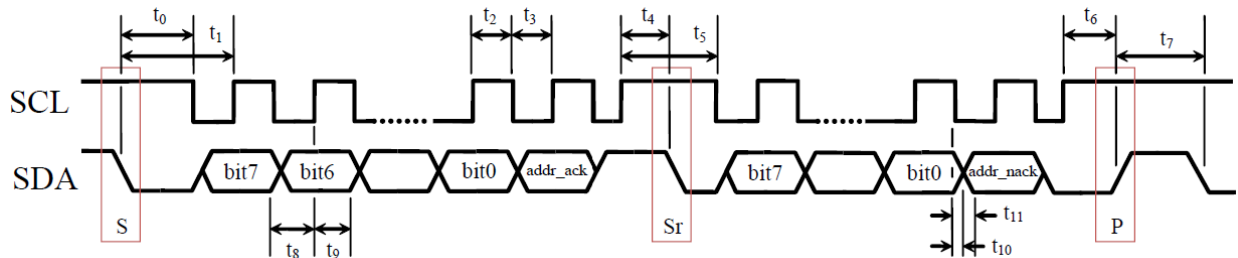
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I²C Timing Diagram



Number	Description	MIN	MAX	Units
t ₀	SDA low to SCL low transition (Start event)	50	-	ns
t ₁	SDA low to first SCL rising edge	100	-	ns
t ₂	SCL pulse width: high	100	-	ns
t ₃	SCL pulse width: low	100	-	ns
t ₄	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t ₅	SCL pulse width: high during a S/Sr/P event	100	-	ns
t ₆	SCL high before SDA rising edge (Stop)	50	-	ns
t ₇	SDA pulse width: high	25	-	ns
t ₈	SDA valid to SCL rising edge	50	-	ns
t ₉	SCL rising edge to SDA invalid	50	-	ns
t ₁₀	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t ₁₁	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I ² C CLK	2.5	-	us

Table 9: I²C Timing (Fast Mode)