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L-ASC10

In-System Programmable
Hardware Management Expander

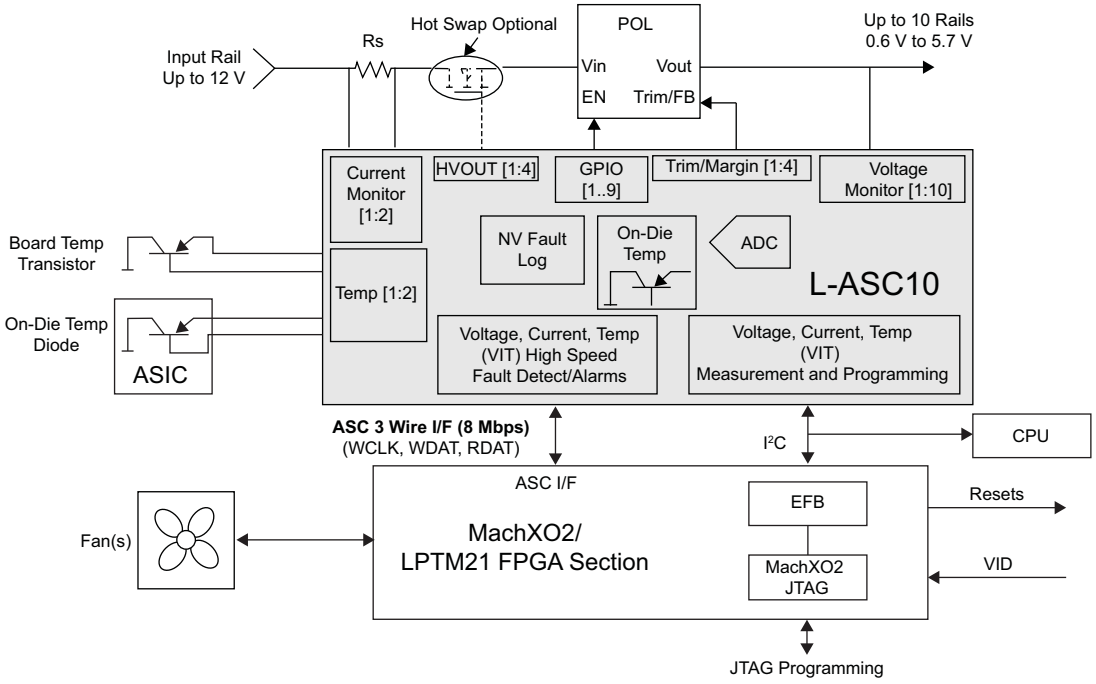
May 2016 **Data Sheet DS1042**

Features

- **Ten Rail Voltage Monitoring and Measurement**
  - UV/OV Fault Detection Accuracy - 0.2% Typ.
  - Fault Detection Speed <100 µs
  - High Voltage, Single Ended and Differential Sensing
- **Two Channel Wide-Range Current Monitoring and Measurement**
  - High-side current Measurement up to 12 V
  - Programmable OC/UC Fault Detect
  - Detects Current faults in < 1 µs
- **Three Temperature Monitoring and Measurement Channels**
  - Programmable OT/UT Faults Threshold
  - Two channels of Temperature Monitoring using external diodes
  - One On-Chip Temperature Monitor
- **Four High-Side MOSFET Drivers**
  - Programmable Charge Pump
- **Four Precision Trim and Margin Channels**
  - Closed Loop Operation
  - Voltage Scaling and VID Support
- **Nine General Purpose Input / Output**
  - 5 V tolerant I/O
- **Non-Volatile Fault Logging**
- **In-system Programmable Through I²C**
  - Non-Volatile Configuration
  - Background Programming Support
- **System Level Support**
  - 3.3 V Operation, wide input supply range 2.8 V to 3.6 V
  - Industrial temperature range
  - 48-pin QFN
  - RoHS compliant and halogen-free
- **Applications**
  - Telecommunication and Networking
  - Industrial, Test & Measurement
  - Medical Systems
  - Servers and Storage Systems
  - High Reliability Systems

Application Diagram

Figure 1. Hardware Management Application Block Diagram



Description

The L-ASC10 (Analog Sense and Control - 10 rail) is a Hardware Management (Power, Thermal, and Control Plane Management) Expander designed to be used with Platform Manager 2 or MachXO2 FPGAs to implement the Hardware Management Control function in a circuit board. The L-ASC10 (referred to as ASC) enables seamless scaling of power supply voltage and current monitoring, temperature monitoring, sequence and margin control channels. The ASC includes dedicated interfaces supporting the exchange of monitor signal status and output control signals with these centralized hardware management controllers. Up to eight ASC devices can be used to implement a hardware management system.

The ASC provides three types of analog sense channels: voltage (nine standard channels and one high voltage channel), current (one standard voltage and one high voltage), and temperature (two external and one internal) as shown in Figure 2.

Each of the analog sense channels is monitored through two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. The current sense channels feature a programmable gain amplifier and a fast fault detect (<1 µs response time) for detecting short circuit events. The temperature sense channels can be configured to work with different external transistor or diode configurations.

Nine general purpose 5 V tolerant open-drain digital input/output pins are provided that can be used in a system for controlling DC-DC converters, low-drop-out regulators (LDOs) and optocouplers, as well as for supervisory and general purpose logic interface functions. Four high-voltage charge pumped outputs (HVOUT1-HVOUT4) may be configured as high-voltage MOSFET drivers to control high-side MOSFET switches. These HVOUT outputs can also be programmed as static output signals or as switched outputs (to support external charge pump implementation) operating at a dedicated duty cycle and frequency.

The ASC device incorporates four TRIM outputs for controlling the output voltages of DC-DC converters. Each power supply output voltage can be maintained typically within 0.5% tolerance across various load conditions using the Digital Closed Loop Control mode.

The internal 10-bit A/D converter can be used to monitor the voltage and current through the I^2C bus. The ADC is also used in the digital closed loop control mode of the trimming block.

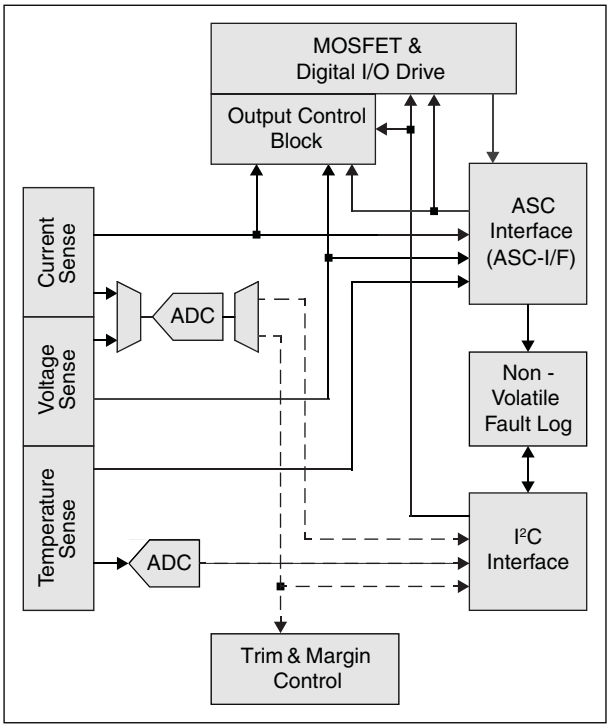
The ASC also provides the capability of logging up to 16 status records into the on-chip nonvolatile EEPROM memory. Each record includes voltage, current and temperature monitor signals along with digital input and output levels.

The dedicated ASC Interface (ASC-I/F) is a reliable serial channel used to communicate with a Platform Manager 2 or a MachXO2 FPGA in a scalable star topology. The centralized control algorithm in the FPGA monitors signal status and controls output behavior via this ASC-I/F. The ASC I^2C interface is used by the FPGA or an external microcontroller for ASC background programming, interface configuration, and additional data transfer such as parameter measurement or I/O control or status. For example, voltage trim targets can be set over the I^2C bus and measured voltage, current, or temperature values can be read over the I^2C bus.

The ASC also includes an on-chip output control block (OCB) which allows certain alarms and control signals a direct connection to the GPIOs or HVOUTs, bypassing the ASC-I/F for a faster response. The OCB is used to connect the fast current fault detect signal to an FPGA input directly. It also supports functions like Hot Swap with a programmable hysteretic controller.

ASC Block Diagram

Figure 2. ASC Block Diagram



DC and Switching Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max.	Units
V_{CCA}	Main Power Supply		–0.5	4.5	V
V_{IN_VMON}	VMON input voltage		–0.5	6	V
V_{IN_VMONGS}	VMON input voltage ground sense		–0.5	6	V
V_{IN_HIMONP}	High voltage IMON input voltage		–0.5	13.3	V
V_{IN_HIMONN}	High voltage IMON return/ VMON input voltage		–0.5	13.3	V
V_{DIFF_HIMON}	High voltage IMON differential voltage		–2.0	2.0	V
V_{IN_IMONP}	Low voltage IMON1 input voltage		–0.5	6.0	V
V_{IN_IMONN}	Low voltage IMON1 return voltage		–0.5	6.0	V
V_{DIFF_IMON}	Low voltage IMON1 differential voltage		–2.0	2.0	V
V_{IN_TMONP}	TMON input voltage		–0.5	V_{CCA}	V
V_{IN_TMONN}	TMON return voltage		–0.5	V_{CCA}	V
V_{IN_GPIO}	Digital input voltage		–0.5	6	V
V_{OUT}	Open-drain output voltage	HVOUT [1:4]	–0.5	13.3	V
		GPIO[1:6], GPIO[8:10]	–0.5	6	V
V_{TRIM}	TRIM output voltage		–0.5	V_{CCA}	V
$I_{SINKMAX}$	Maximum Sink Current on any output			23	mA
T_S	Device Storage Temperature		–65	+125	°C
T_A	Ambient Temperature		–40	+125	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max.	Units
V_{CCA}	Main Power Supply[1]		2.8	3.6	V
V_{IN_VMON}	VMON input voltage		–0.3	5.9	V
V_{IN_VMONGS}	VMON input voltage ground sense		–0.2	0.3	V
V_{IN_HIMONP}	High voltage IMON input voltage[2]		4.5	13.2	V
V_{IN_HIMONN}	High voltage IMON return/ VMON input voltage[2]		4.5	13.2	V
V_{DIFF_HIMON}	High voltage IMON differential voltage		0	500	mV
V_{IN_IMONP}	Low voltage IMON1 input voltage	Low Side Sense Disabled	0.6	5.9	V
		Low Side Sense Enabled	–0.3	1.0	V
V_{IN_IMONN}	Low voltage IMON1 return voltage	Low Side Sense Disabled	0.6	5.9	V
		Low Side Sense Enabled	–0.3	1.0	V
V_{DIFF_IMON}	Low voltage IMON1 differential voltage		0	500	mV
V_{IN_GPIO}	Digital input voltage		–0.3	5.5	V
V_{OUT}	Open-drain output voltage	HVOUT [1:4]	–0.3	13.2	V
		GPIO[1:6], GPIO[8:10]	–0.3	5.5	V
T_A	Ambient Temperature		–40	+85	°C

1. VCCA of ASC0 must be connected with VCC of MachXO2 or LPTM21 and VCCIO of bank used for ASC-I/F of ASC0. See System Connections section for more details
2. HIMON circuits are operational down to 3 V. Accuracy is guaranteed within Recommended Operating Conditions

Analog Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{CCA}	Supply Current	V_{CCA} = 3.3 V, Ta 25 °C		25	35	mA
$I_{CC\text{-}HVOUT}$	Supply Current Adder per HVOUT	V_{HVOUT} = 12 V, I_{SRC} = 100 uA, V_{CCA} = 3.3 V, Ta 25 °C			2	mA
I_{CCPROG}	Supply Current during Programming	V_{CCA} = 3.3 V, Ta 25 °C			40	mA

ESD Performance

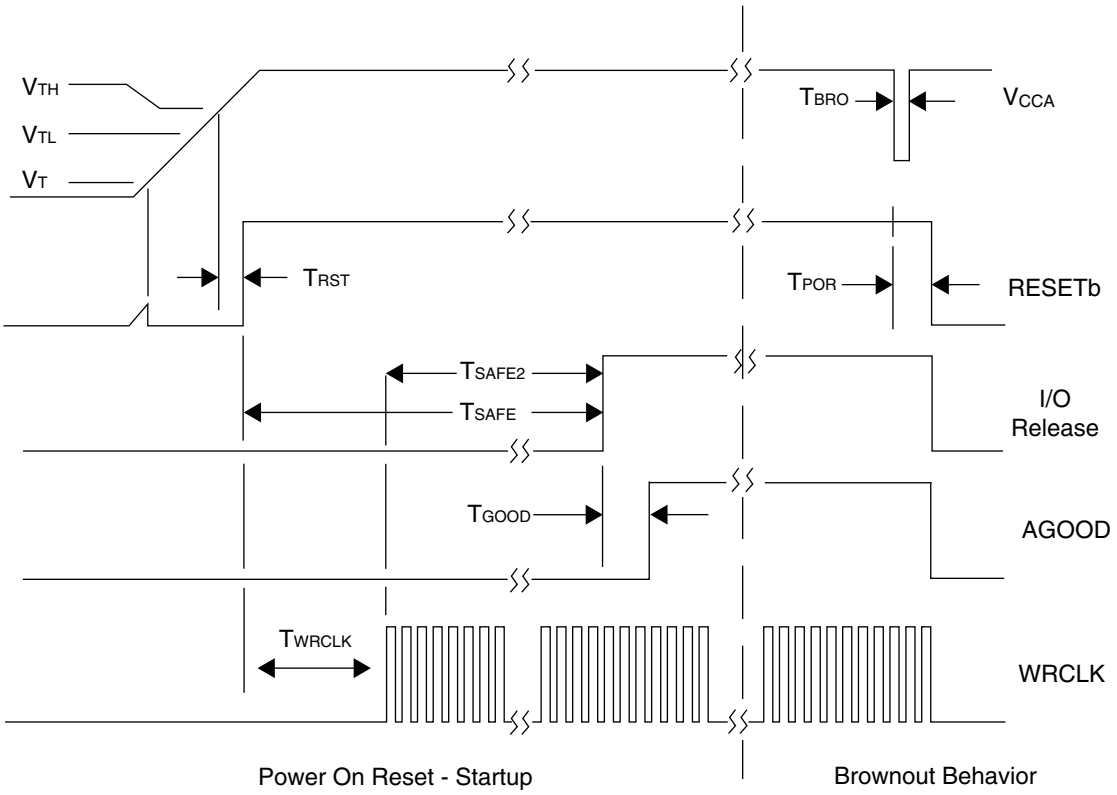
Please refer to the Platform Manager 2 Product Family Qualification Summary for complete qualification data, including ESD performance.

Power-On Reset

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
T_{RST}	Delay from VTH to start-up state				100	µs
T_{SAFE}	Delay from RESETb release to ASC Safe State Exit and I/O Release[1, 2]			1.8		ms
T_{SAFE2}	Delay from WRCLK start to ASC Safe State Exit and I/O Release[1, 2, 3]		56			µs
T_{GOOD}	Delay from I/O release to AGOOD asserted high in FPGA section[4]			16		µs
T_{WRCLK}	Delay from RESETb release to WRCLK start[5]			1.4		ms
T_{BRO}	Minimum duration brown out required to trigger RESETb		1		5	µs
T_{POR}	Delay from Brown out to reset state				13	µs
V_{TL}	Threshold below which RESETb is LOW				2.3	V
V_{TH}	Threshold above which RESETb is Hi-Z		2.7			V
V_T	Threshold above which RESETb is valid		0.8			V
C_L	Capacitive load on RESETb				200	pF

1. Both T_{SAFE} and T_{SAFE2} must complete before I/O are released from Safe State.
2. During the calibration period before T_{SAFE} and T_{SAFE2}, the ASC may ignore RESETb being driven low. After T_{SAFE} and T_{SAFE2}, the ASC can be reset by another device by driving RESETb low.
3. Safe State is released at ASC after a fixed number (64) of WRCLK cycles (typ. 8 MHz frequency) and three ASC-I/F data packets are properly detected.
4. AGOOD asserted in the FPGA on the next ASC-I/F packet after I/O exits Safe State as ASC.
5. Parameter is dependent on the FPGA configuration refresh time during POR. See Platform Manager 2 or MachXO2 datasheet for details.

Figure 3. ASC Power-On Reset



Voltage Monitors[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{VMON_in}	Input Resistance		55	65	75	kΩ
C_{VMON_in}	Input Capacitance			8		pF
V_{MON} Range	Programmable trip-point Range		0.075		5.734	Volts
V_{MON} Accuracy	Absolute accuracy of any trip-point – Differential VMON pins	VMON voltage > 0.650 V		0.2	0.7	%
	Single-ended VMON pins	VMON voltage > 0.650 V		0.3	0.9	%
V_{MON} HYST	Hysteresis of any trip-point (relative to setting)			1		%
V_{MON} CMR	Differential VMON Common mode rejection ratio			60		dB
V_Z Sense	Low Voltage Sense Trip Point Error – Differential VMON1-4	Trip Point = 0.075 V	–5		+5	mV
		Trip Point = 0.150 V	–5		+5	mV
		Trip Point = 0.300 V	–10		+10	mV
		Trip Point = 0.545 V	–15		+15	mV
	Low Voltage Sense Trip Point Error – Single-Ended VMON5-9	Trip Point = 0.080 V	–10		+10	mV
		Trip Point = 0.155 V	–15		+15	mV
		Trip Point = 0.310 V	–25		+25	mV
		Trip Point = 0.565 V	–55		+55	mV
High Voltage Monitor						
HV_{MON} Range	High Voltage VMON programmable trip-point range		0.3		13.2	Volts
HV_{MON} Accuracy	HVMON Absolute accuracy of any trip-point	HVMON voltage > 1.8 V		0.4	1.0	%
V_Z Sense	Low Voltage Sense Trip Point Error - HVMON pin	Trip Point = 0.220 V	–20		+20	mV
		Trip Point = 0.425 V	–35		+35	mV
		Trip Point = 0.810 V	–75		+75	mV
		Trip Point = 1.280 V	–130		+130	mV

1. VMON accuracy may degrade based on SSO conditions of hardware management controller ASC-I/F. See the System Connections section for more details.

Current Monitors

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IMONPleak}$	IMON1P input leakage	Low Side Sense Disabled Fast Trip Point V_{sns} = 500 mV	–2		250	µA
		Low Side Sense Enabled Fast Trip Point V_{sns} = 500 mV	–2		40	µA
$I_{IMONNleak}$	IMON1N input leakage	Low Side Sense Disabled Fast Trip Point V_{sns} = 500 mV	–2		2	µA
		Low Side Sense Enabled Fast Trip Point V_{sns} = 500 mV	–200		2	µA
$I_{HIMONPleak}$	HIMONP input leakage	Fast Trip Point V_{sns} = 500 mV			550	µA
$I_{HIMONNleak}$	HIMONN_HVMON input leakage				350	µA
$I_{MONA/B}$ Accuracy[2]	HIMON, IMON1A/B Comparator Trip Point accuracy	Gain = 100x		8		%
		Gain = 50x		5		%
		Gain = 25x		3		%
		Gain = 10x		2		%
$I_{MONA/B}$ Gain	Programmable Gain Setting	Four settings in software		10		V/V
				25		V/V
				50		V/V
				100		V/V
I_{MONF} Accuracy[2]	Fast comparator trip-point accuracy	V_{sns}[1] = 50 mV, 100 mV, or 150 mV		8		%
		V_{sns} = 200 mV, 250 mV, or 300 mV		5		%
		V_{sns} = 400 mV or 500 mV		3		%
t_{IMONF}	Fast comparator response time				1	µs

1. V_{sns} is the differential voltage between IMON1P and IMON1N (or HIMONP and HIMONN).
2. IMON accuracy may degrade based on SSO conditions of hardware management controller ASC-I/F. See the System Connections section for more details.

ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution			10		Bits
$t_{CONVERT}$	Conversion Time from I^2C Request				200	µs
Voltage Monitors						
$V_{VMON-IN}$	Input Range Full scale	Programmable Attenuator = 1	0		2.048	V
		Programmable Attenuator = 3	0		5.91	
LSB	ADC Step Size	Programmable Attenuator = 1		2		mV
		Programmable Attenuator = 3		6		
$E_{VMON-attenuator}$	Error due to attenuator	Programmable Attenuator = 3		+/– 0.1		%
High Voltage Monitor						
$V_{HVMON-IN}$	Input Range Full scale	Programmable Attenuator = 4	0		8.192	V
		Programmable Attenuator = 8	0		13.21	
LSB	ADC Step Size	Programmable Attenuator = 4		8		mV
		Programmable Attenuator = 8		16		
$E_{HVMON-attenuator}$	Error due to attenuator	Programmable Attenuator = 4		+/–0.2		%
		Programmable Attenuator = 8		+/–0.4		%
Current Monitors						
$t_{IMON-sample}$	Sample period of HIMON and IMON1 conversions for averaged value	4 Settings via I^2C command		1		ms
				2		
				4		
				8		
$V_{IMON-IN}$	Input Range Full scale[1]	Programmable Gain 10x	0		200	mV
		Programmable Gain 25x	0		80	
		Programmable Gain 50x	0		40	
		Programmable Gain 100x	0		20	
LSB	ADC Step Size	Programmable Gain 10x		0.2		mV
		Programmable Gain 25x		0.08		
		Programmable Gain 50x		0.04		
		Programmable Gain 100x		0.02		

1. Differential voltage applied across HIMONP/IMON1P and HIMONN/IMON1N before programmable gain amplification.

ADC Error Budget Across Entire Operating Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TADC Error	Total ADC Measurement Error at Any Voltage (Differential Analog Inputs)[1, 3]	Measurement Range 600 mV - 2.048 V, VMONxGS > –100 mV, Attenuator =1	8	+/– 4	8	mV
		Measurement Range 600 mV - 2.048 V, VMONxGS > –200 mV, Attenuator =1		+/– 6		mV
		Measurement Range 0 - 2.048 V, VMONxGS > –200 mV, Attenuator =1		+/– 10		mV
	Total Measurement Error at Any Voltage (Single-Ended Analog Inputs including IMON)[1, 2, 3]	Measurement Range 600 mV - 2.048 V, Attenuator =1	–8	+/– 4	8	mV

1. Total error, guaranteed by characterization, includes INL, DNL, Gain, Offset, and PSR specs of the ADC.
2. Programmable gain error on IMON not included.
3. ADC accuracy may degrade based on SSO conditions of hardware management controller ASC-I/F. See the System Connections section for more details

Temperature Monitors

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{MON_REMOTE} Accuracy[1, 7]	Temp Error – Remote Sensor	Ta=–40 to +85 °C Td=–64 to 150 °C		1		°C
T_{MON_INT} Accuracy[7]	Internal Sensor – Relative to ambient[6]	Ta=–40 to +85 °C		1		°C
T_{MON} Resolution	Measurement Resolution			0.25		°C
T_{MON} Range	Programmable threshold range		–64		155	°C
T_{MON} Offset	Temperature offset	Programmable in software	–64		63.75	°C
T_{MON} Hysteresis	Hysteresis of trip points	Programmable in software	0		63	°C
t_{TMON_settle}[2]	Temperature measurement settling time[3]	Measurement Averaging Coefficient = 1		15		ms
		Measurement Averaging Coefficient = 8		120		ms
		Measurement Averaging Coefficient = 16		240		ms
T_n	Ideality Factor ***n***	Programmable in software	0.9		2	
T_{limit}	Temperature measurement limit[4]				160	°C
C_{TMON}	Maximum capacitance between T_{MONP} and T_{MONN} pins				200	pF
$R_{TMONSeries}$	Equivalent external resistance to sensor[5]				200	ohms

1. Accuracy number is valid for the use of a grounded collector pnp configuration, programmed with proper ideality factor, and 16x measurement filter enabled. Any other device or configuration can have additional errors, including beta, series resistance and ideality factor accuracy. See the Temperature Monitors section for more details.
2. Settling time based on one TMON enabled. For multiple TMONs, settling time can be multiplied by the number of enabled TMON channels.
3. Settling time is defined as the time it takes a step change to settle to 1% of the measured value.
4. All values above T_{limit} read as 0x3FF over I^2C. There is no cold temperature limiting reading, although performance is not specified below –64 °C.
5. This is the maximum series resistance which the TMON circuit can compensate out. Equivalent series resistance includes all board trace wiring (TMONP and TMONN) as well as parasitic base and emitter resistances. Re=1/gm should not be included as part of series resistance.
6. Internal sensor is subject to self-heating, dependent on PCB design and device configuration. Self-heating not included in published accuracy.
7. TMON accuracy may degrade based on SSO conditions of hardware management controller ASC-I/F. See the System Connections section for more details.

Digital Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IL},I_{IH}	Input Leakage, no pull-up, pull-down[2]				+/– 10	µA
I_{PD}	Active Pull-Down Current[2]	GPIO[1:10] configured as Inputs, Internal Pull-Down enabled		200		µA
$I_{PD-ASCIF}$	Input Leakage (WDAT and WRCLK)[3]	Internal Pull-Down		175		µA
$I_{OH-HVOUT}$	Output Leakage Current	HVOUT[1:4] in open drain mode and pulled up to 12 V		35	100	µA
$I_{PU-RESETb}$	Input Pull-Up Current (RESETb)			–50		µA
V_{IL}	Voltage input, logic low	GPIO[1:10]			0.8	V
		SCL, SDA			30% VCCA	
V_{IH}	Voltage input, logic high	GPIO[1:10]	2.0			V
		SCL, SDA	70% VCCA			
V_{OL}	HVOUT[1:4] (open drain mode)	I_{SINK} = 10 mA			0.8	V
	GPIO[1:6], GPIO[8:10]	I_{SINK} = 20 mA				
$I_{SINKTOTAL}$[1]	All digital outputs				130	mA

1. Sum of maximum current sink from all digital outputs combined. Reliable operation is not guaranteed if this value is exceeded.
2. During safe-state, all GPIO default to output, see the Safe State of Digital Outputs for more details. GPIO[1:6] and GPIO[10] default to active low output. This will result in a leakage current dependent on the input voltage which can exceed the specified input leakage
3. WRCLK and WDAT pins may see transients above 1 mA in hot socket conditions. DC levels will remain below 1 mA.

High Voltage FET Drivers

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PP}	Gate driver output voltage	Four settings in software		12		Volts
				10		
				8		
				6		
I_{OUTSRC}	Gate driver source current (HIGH state)	Four settings in software		12.5		µA
				25		
				50		
				100		
$I_{OUTSINK}$	Gate driver sink current (LOW state)	Four settings in software		100		µA
				250		
				500		
				3000		
Frequency	Switched Mode Frequency	Two settings in software		15.625		kHz
				31.25		
Duty Cycle	Switched Mode Programmable Duty Cycle Range	Programmable in software	6.25		93.75	%
	Duty Cycle step size			6.25		%

Margin/Trim DAC Output Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
	Resolution			8 (7 + sign)		Bits
FSR	Full scale range			+/– 320		mV
LSB	LSB step size			2.5		mV
I_{OUT}	Output source/sink current		–200		200	µA
I_{TRIM_Hi-Z}	Tri-state mode leakage			0.1		µA
BPZ	Bipolar zero output voltage (code=80h)	Four settings in software		0.6		V
				0.8		
				1.0		
				1.25		
t_S	TrimCell output voltage settling time[1]	DAC code changed from 80H to FFH or 80H to 00H			2.5	ms
		Single DAC code change		256		µs
C_LOAD	Maximum load capacitance				50	pF
TOSE	Total open loop supply voltage error[2]	Full scale DAC corresponds to +/– 5% supply voltage variation	–1%		+1%	V/V

1. To 1% of set value with 50 pF load connected to trim pins.
2. Total resultant error in the trimmed power supply output voltage referred to any DAC code due to DAC's INL, DNL, gain, output impedance, offset error and bipolar offset error across the temperature, and V_{CCA} ranges of the device.

Fault Log

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Records	Number of available fault log records in EEPROM			16		Records
$t_{faultTrigger}$	Minimum active time of trigger signal to start fault recording		64			µs
$t_{faultRecord}$	Time to copy fault record to EEPROM				5	ms

Oscillator

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
CLK_{ASC}	Internal ASC0 Clock		7.6	8	8.4	MHz
CLK_{ext}	Externally Applied Clock		7.6	8	8.4	MHz

Propagation Delays

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Voltage Monitors						
$t_{VMONtoFPGA}$	Propagation delay VMON input to signal update at FPGA	Glitch Filter Off		48		µs
		Glitch Filter ON		96		µs
$t_{VMONtoOCB}$[2]	Propagation delay VMON input to output update at OCB	Glitch Filter Off			16	µs
		Glitch Filter ON			64	µs
Current Monitors						
$t_{IMONtoFPGA}$	Propagation delay IMON input to signal update at FPGA	Glitch Filter Off		48		µs
		Glitch Filter ON		96		µs
$t_{IMONtoOCB}$[2]	Propagation delay IMON input to output update at OCB	Glitch Filter Off			16	µs
		Glitch Filter ON			64	µs
$t_{IMONFtoOCB}$[2]	Propagation delay IMONF input to output update at OCB				1	µs
Temperature Monitors						
$t_{TMONtoFPGA}$	Propagation delay TMON input to signal update at FPGA[1]	Monitor Alarm Filter Depth = 1		15		ms
		Monitor Alarm Filter Depth = 16		240		ms
GPIO – Inputs						
$t_{GPIOtoFPGA}$	Propagation delay GPIO input to signal update at FPGA			32		µs
$t_{GPIOtoOCB}$[2]	Propagation delay GPIO input to output update at OCB				50	ns
GPIO – Outputs						
$t_{FPGAtoGPIO}$	Propagation delay FPGA signal update to GPIO output			32		µs
$t_{OCBtoGPIO}$[3]	Propagation delay OCB input to output update at GPIO				50	ns
HVOUT						
$t_{FPGAtoHVOUT}$	Propagation delay FPGA signal update to HVOUT output			32		µs
$t_{OCBtoHVOUT}$[3, 4]	Propagation delay OCB input to output update at HVOUT				110	ns
TRIM DAC						
$t_{FPGAtoTrimOE}$	Propagation delay FPGA signal update to TRIM_OE update			32		µs

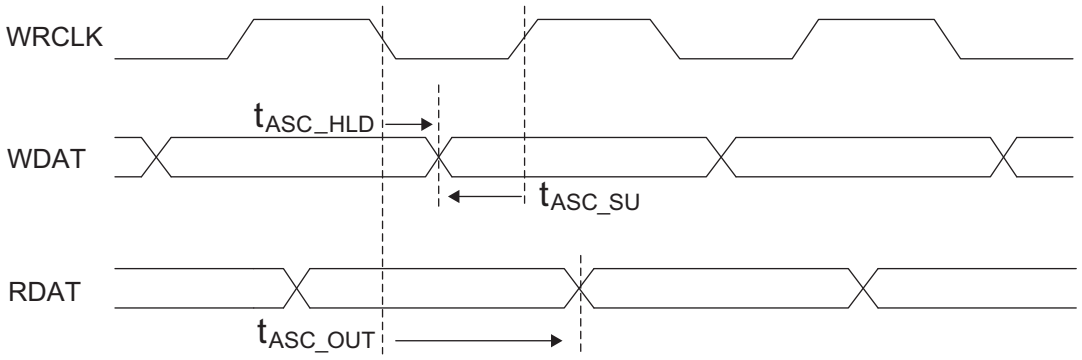
1. Propagation delay based on one TMON enabled. For multiple TMONs, propagation delay can be multiplied by the number of enabled TMON channels.
2. OCB output propagation delays measured using time delay to GPIO output from OCB. Propagation delay is measured on falling GPIO outputs. Rising output propagation time will be dependent on external pull-up resistor.
3. OCB input propagation delays measured using time delay from GPIO input to OCB. Propagation delay is measured on falling GPIO outputs. Rising output propagation time will be dependent on external pull-up resistor.
4. HVOUT propagation delay measured with HVOUT in open-drain mode, with switched mode disabled. Propagation delay in charge pump mode is dependent on external load and HVOUT settings.

ASC Interface (ASC-I/F) Timing Specifications[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{wrclk}	WRCLK frequency			8		MHz
t_{ASC_HLD}	Hold time between WRCLK falling edge and WDAT transition		0			ns
t_{ASC_SU}	Setup time between WDAT transition and WRCLK rising edge		25			ns
t_{ASC_OUT}	Delay from WRCLK falling edge to RDAT transition				50	ns

1. All timing conditions valid for VCCIO = 3.3 V at FPGA ASC-I/F and ASC VCCA range of 2.8 V to 3.6 V.

Figure 4. ASC Interface (ASC-I/F) Timing Diagram



I²C Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency		400	kHz

1. ASC supports the following modes:
   a. Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   b. Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

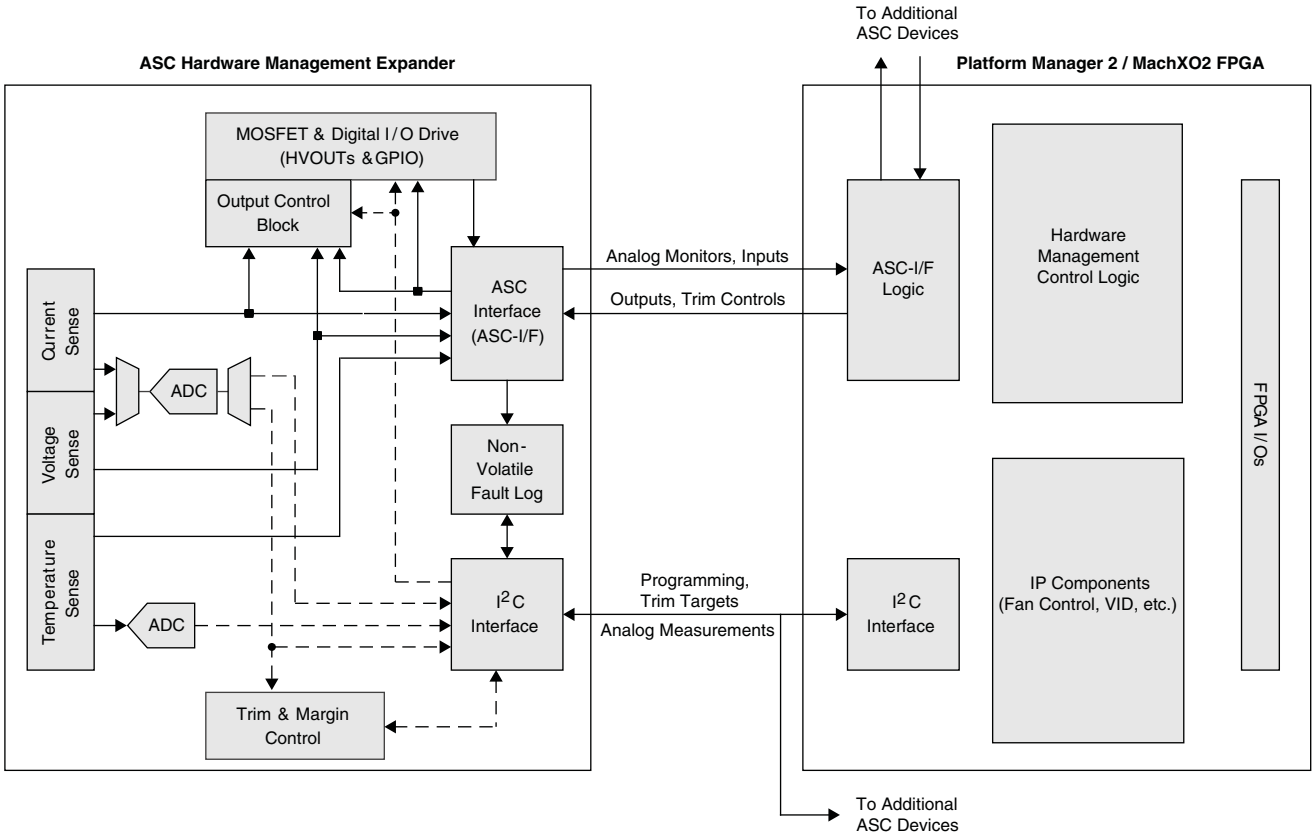
Theory of Operation

Hardware Management System

The ASC Hardware Management Expander is designed to seamlessly increase the number of analog sense and control channels in the hardware management section of a circuit board. The device functions as a hardware management expander in systems with the Lattice Platform Manager 2 or MachXO2 FPGAs. The functional blocks for analog voltage, current and temperature monitoring, measurement, and control are built into the ASC. The ASC depends on the Platform Manager 2 or MachXO2 FPGA to interpret the analog monitor status signals and provide control commands.

The Platform Manager 2 or MachXO2 FPGA includes the hardware management control logic and other plug-in IP components to support functions like Fan Control, or Voltage by Identification (VID). ASC devices can be added to the hardware management system to scale with application requirements and are connected to the same Platform Manager 2 or MachXO2 FPGA. This architecture supports a single centralized hardware management logic design, with up to eight distributed ASC devices. The basic system concept is shown in Figure 5. The connections are described in detail in the System Connections section.

Figure 5. Hardware Management System with ASC Hardware Management Expander

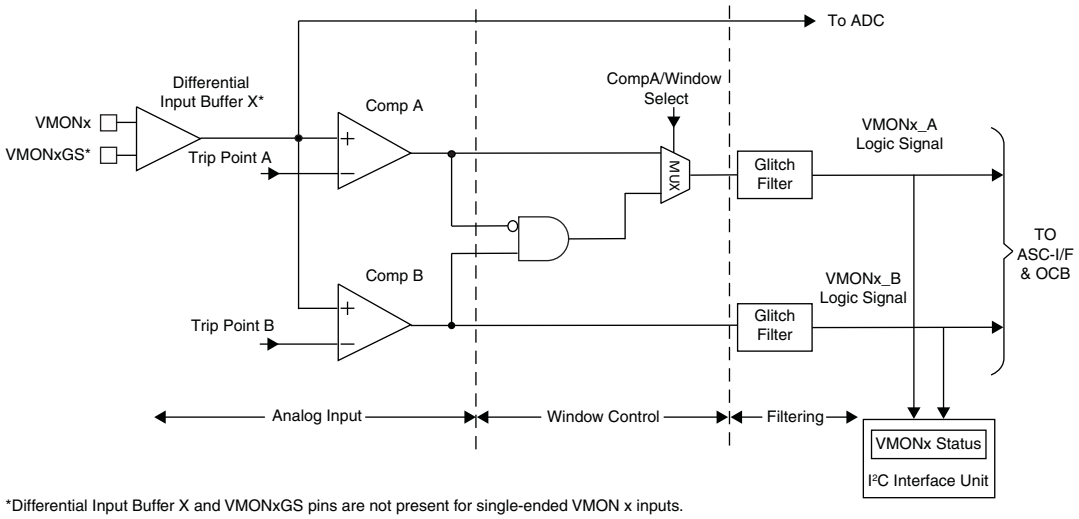


The Hardware Management System is configured using Platform Designer, a part of Lattice Diamond software. Platform Designer provides an easy to use graphical and spreadsheet based interface. Platform Designer automatically generates the device memory configuration based on the options selected in the software. See the For Further Information section for more details.

Voltage Monitor Inputs

The ASC provides ten independently programmable voltage monitor input circuits. There are nine standard voltage channels and one high voltage channel. The standard voltage channels are shown in Figure 6, while the high voltage channel is described in the High Voltage Current Monitor section. Two individually programmable trip-point comparators are connected to each voltage monitoring input. Each comparator reference has programmable trip points over the range of 0.075 V to 5.734 V. The 75 mV 'zero-detect' threshold allows the voltage monitors to determine if a monitored signal has dropped to ground level. This feature is especially useful for determining if a power supply's output has decayed to a substantially inactive condition after it has been switched off.

Figure 6. ASC Voltage Monitors



*Differential Input Buffer X and VMONxGS pins are not present for single-ended VMON x inputs.

Figure 6 shows the functional block diagram of one of the nine voltage monitor inputs - 'x' (where x = 1...9). Each voltage monitor can be divided into three sections: Analog Input, Window Control, and Filtering. The first section provides a differential input buffer to monitor the power supply voltage through VMONx (to sense the positive terminal of the supply) and VMONxGS (to sense the power supply ground). Differential voltage sensing minimizes inaccuracies in voltage measurement with ADC and monitor thresholds due to the potential difference between the ASC device ground and the ground potential at the sensed node on the circuit board.

The voltage output of the differential input buffer is monitored by two individually programmable trip-point comparators, shown as Comp A and Comp B. The differential input buffer shown above is not present for any of the single-ended VMON inputs. VMON1-4 are differential inputs, while VMON5-10 are single-ended.

Each comparator outputs a HIGH signal to the ASC-I/F if the voltage at its positive terminal is greater than its programmed trip point setting; otherwise it outputs a LOW signal. The VMON4A and VMON9A comparators also output their status signals to the OCB.

Hysteresis is provided by the comparators to reduce false triggering as a result of input noise. The hysteresis provided by the voltage monitor is a function of the input divider setting. Table 1 lists the typical hysteresis versus voltage monitor trip-point.

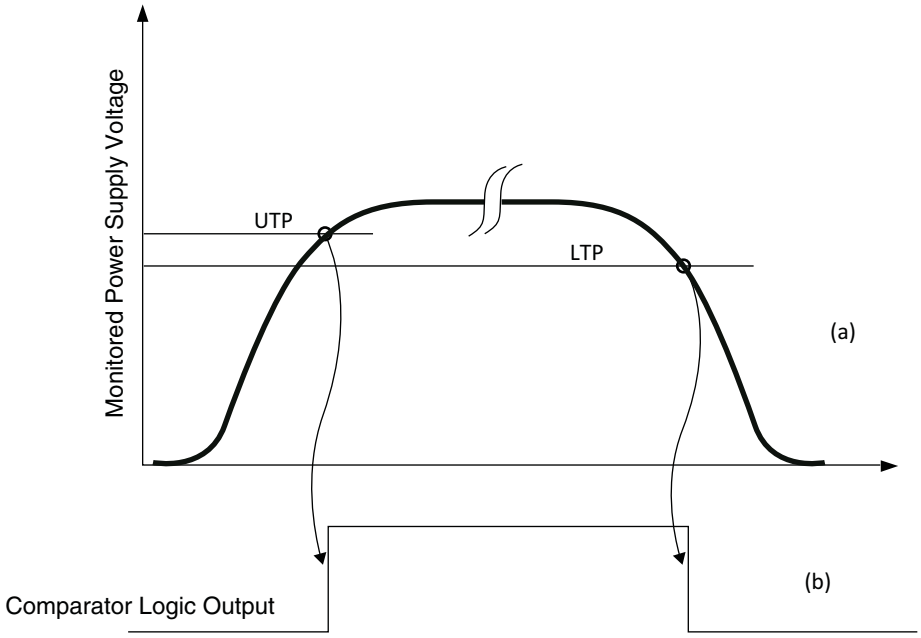
AGOOD Logic Signal

All the VMON, IMON and TMON comparators auto-calibrate following a power-on reset event. During this time, the digital glitch filters are also initialized. This process completion is signaled by an internally generated logic signal: AGOOD. The ASC-I/F will not begin communicating valid VMON status bits or receiving GPIO control signals until the AGOOD signal is initialized.

Programmable Over-Voltage and Under-Voltage Thresholds

Figure 7 shows the power supply ramp-up and ramp-down voltage waveforms. Because of hysteresis, the comparator outputs change state at different thresholds depending on the direction of excursion of the monitored power supply.

Figure 7. Power Supply Voltage Ramp-up and Ramp-down Waveform and the Resulting Comparator Output (a) and Corresponding to Upper and Lower Trip Points (b)



During power supply ramp-up the comparator output changes from logic zero to one when the power supply voltage crosses the upper trip point (UTP). During ramp down the comparator output changes from logic state one to zero when the power supply voltage crosses the lower trip point (LTP). To monitor for over voltage fault conditions, the UTP should be used. To monitor under-voltage fault conditions, the LTP should be used. The upper and lower trip points are automatically selected in software depending on whether the user is monitoring for an over-voltage condition or an under-voltage condition. Table 1 shows the comparator hysteresis versus the trip-point range.

Table 1. Voltage Monitor Comparator Hysteresis vs. Trip-Point

Trip-point Range (V)		Hysteresis (mV)
Low Limit	**High Limit**	
0.66	0.79	8
0.79	0.9	10
0.94	1.12	12
1.12	1.33	14
1.33	1.58	17
1.58	1.88	20
1.88	2.24	24
2.24	2.66	28
2.66	3.16	34
3.16	3.76	40
4.05	4.82	51
4.82	5.73	61
0.075	0.57	0 (Disabled)

The window control section of the voltage monitor circuit is an AND gate (with inputs: an inverted COMPA “ANDed” with COMPB signal) and a multiplexer that supports the ability to develop a ‘window’ function in hardware. Through the use of the multiplexer, voltage monitor’s ‘A’ output may be set to report either the status of the ‘A’ comparator, or the window function of both comparator outputs. The voltage monitor’s ‘A’ output indicates whether the input signal is between or outside the two comparator thresholds. **Important:** This windowing function is only valid in cases where the threshold of the ‘A’ comparator is set to a value higher than that of the ‘B’ comparator. Table 2 shows the operation of window function logic.

Table 2. Voltage Monitoring Window Logic

Input Voltage	Comp A	Comp B	Window (B and Not A)	Comment
V_{IN} < Trip-Point B < Trip-Point A	0	0	0	Outside window, low
Trip-Point B <V_{IN} < Trip-Point A	0	1	1	Inside window
Trip-Point B < Trip-Point A < V_{IN}	1	1	0	Outside window, high

Note that when the ‘A’ output of the voltage monitor circuit is set to windowing mode, the ‘B’ output continues to monitor the output of the ‘B’ comparator. This can be useful in that the ‘B’ output can be used to augment the windowing function by determining if the input is above or below the windowing range.

The third section in the voltage monitor circuit is a glitch filter. When enabled, glitches of less than 64 µs will not result in the comparator output changing. This results in a comparator output delay of 64 µs (typical) for all comparator transitions. This is especially useful for reducing the possibility of false triggering from noise that may be present on the voltages being monitored. When the filter is disabled, the comparator output will be delayed by 16 µs (typical). See the Propagation Delays section for more details.

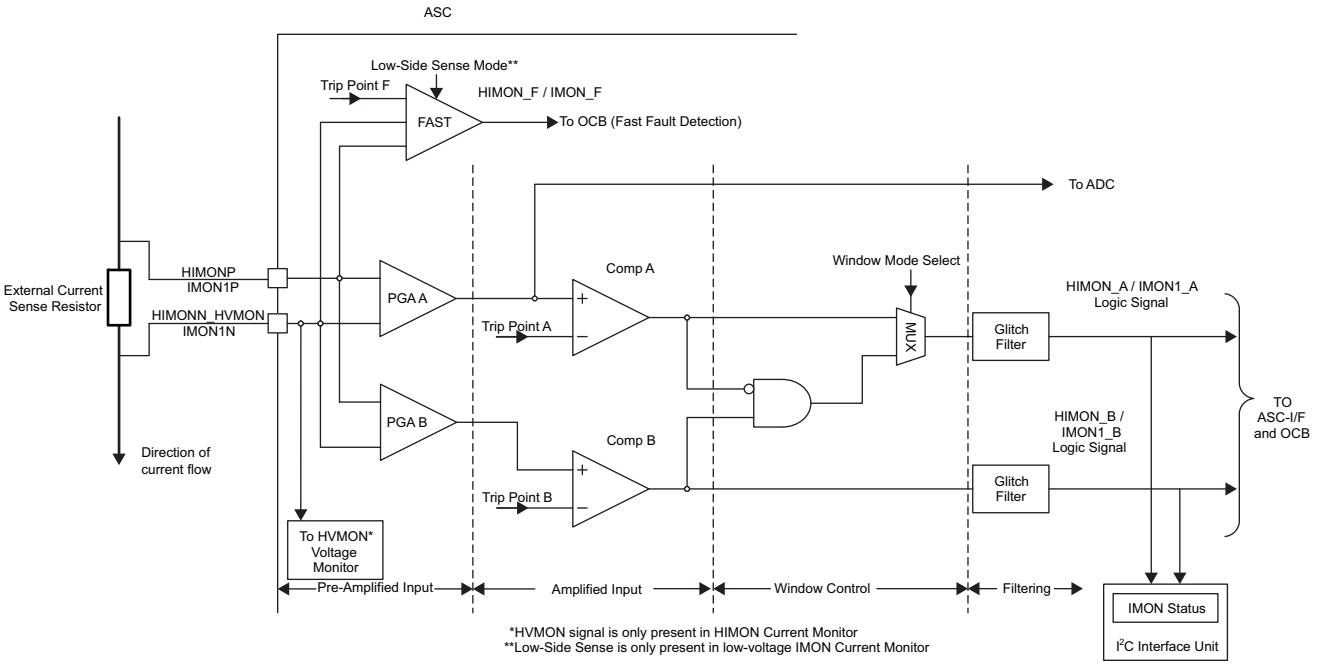
The comparator status can be read from the I^2C interface. For details on the I^2C interface, please refer to the I^2C Interface section of this data sheet.

Current Monitor Inputs

The ASC provides two current monitor circuits as shown in Figure 8. This includes a low-voltage current monitor (with a common mode voltage up to around 6V, see V_{IN_IMONP} in Recommended Operating Conditions section) and a high-voltage current monitor (with a common mode voltage range of up to around 13 V, see V_{IN_HIMONP} in Recommended Operating Conditions section). The low-voltage and high-voltage current monitors share the same basic functional blocks, which are described in this section. Only the low-voltage current monitor supports the low-side sensing mode (shown in Figure 8). The high-voltage current monitor shares input pins with the high-voltage monitor described in the next section.

The current monitor circuits have a differential input that is connected to an external shunt resistor. The differential input goes to a pair of programmable gain amplifiers (PGA) and a fast comparator. The output of PGA A is connected to the ADC and the programmable trip point comparator A. The output of PGA B is connected to the programmable trip point comparator B. The output of the fast comparator is routed to the on-chip Output Control Block (OCB). This signal is useful for fast overcurrent or short circuit shutdown scenarios.

Figure 8. ASC Current Monitor



The Current Monitors can be divided into four sections: Pre-Amplified Input, Amplified Input, Window Control, and Filtering. The first section includes the differential input pins IMON1P and IMON1N (low-voltage current monitor) or HIMONP and HIMONN_HVMON (high-voltage current monitor). These pins are connected to the PGA circuits as well as the direct differential connection to the Fast Fault Detector.

The differential input is monitored by the fast fault detector. The fast fault detector has coarse accuracy and eight programmable trip points. The key feature of the fast fault detector is its response time. The fast fault detector outputs a HIGH signal to the OCB if the differential voltage across the current sensing shunt exceeds the programmed trip point setting. The current shunt is normally connected on the high-side of the input voltage. However, the low-voltage current monitor also supports low-side sensing. The low-side sensing mode should be enabled when sensing negative voltage supplies (such as –48 V) or if the current sense resistor is placed in the return line between the load and ground. This insures proper operation of the fast comparator in a low-side sensing circuit.

Table 3 shows the available trip points for the fast fault detector vs. three frequently used sense resistor values.

Table 3. Fast Fault Detector Current Trip Points vs. Frequently Used Sense Resistor Values

Trip Point Setting	Frequently Used Sense Resistor Value		
	1 Milliohm	5 Milliohm	10 Milliohm
50 mV	50 A	10 A	5 A
100 mV	100 A	20 A	10 A
150 mV	150 A	30 A	15 A
200 mV	200 A	40 A	20 A
250 mV	250 A	50 A	25 A
300 mV	300 A	60 A	30 A
400 mV	400 A	80 A	40 A
500 mV	500 A	100 A	50 A

The Programmable Gain Amplifiers have gain settings of 10x, 25x, 50x, and 100x. The PGA circuits amplify the voltage differential across the current shunt and pass the results to the amplified input section of the current monitor.

The Amplified Input section provides two individually programmable trip-point comparators, shown as Comp A and Comp B above. Each comparator supports four different trip points. Combining these trip points with the respective PGA settings, 16 unique threshold levels are selected for each current monitor.

Table 4 shows the available voltage differential trip points.

Table 4. Comparator Trip Points

Trip Point Setting	Programmable Gain Amplifier Setting (V/V)			
	10 x	**25 x**	**50 x**	**100 x**
1	75 mV	30.5 mV	15.5 mV	8 mV
2	100 mV	40.5 mV	20.5 mV	10.5 mV
3	140 mV	56.5 mV	28.5 mV	14.5 mV
4	190 mV	77 mV	39 mV	20 mV

The output of PGA A is also passed to the on-chip ADC. The current is measured and averaged by the ADC at regular intervals, as described in the Current Measurement with ADC section of the datasheet.

The window control section of the current monitor circuit is an AND gate (with inputs: an inverted COMPA “ANDed” with COMPB signal) and a multiplexer that supports the ability to develop a ‘window’ function in hardware, similar to the voltage monitor window function. Through the use of the multiplexer, the current monitor’s ‘A’ output may be set to report either the status of the ‘A’ comparator, or the window function of both comparator outputs. The current monitor’s ‘A’ output indicates whether the input signal is between or outside the two comparator thresholds. Important: This windowing function is only valid in cases where the threshold of the ‘A’ comparator is set to a value higher than that of the ‘B’ comparator. Table 5 shows the operation of window function logic.

Table 5. IMON Window Mode Behavior

Input Voltage	Comp A	Comp B	Window (B and Not A)	Comment
IIN < Trip-Point B < Trip-Point A	0	0	0	Outside window, low
Trip-Point B <IIN < Trip-Point A	0	1	1	Inside window
Trip-Point B < Trip-Point A < IIN	1	1	0	Outside window, high

Note that when the ‘A’ output of the current monitor circuit is set to windowing mode, the ‘B’ output continues to monitor the output of the ‘B’ comparator. This can be useful in that the ‘B’ output can be used to augment the windowing function by determining if the input is above or below the windowing range.

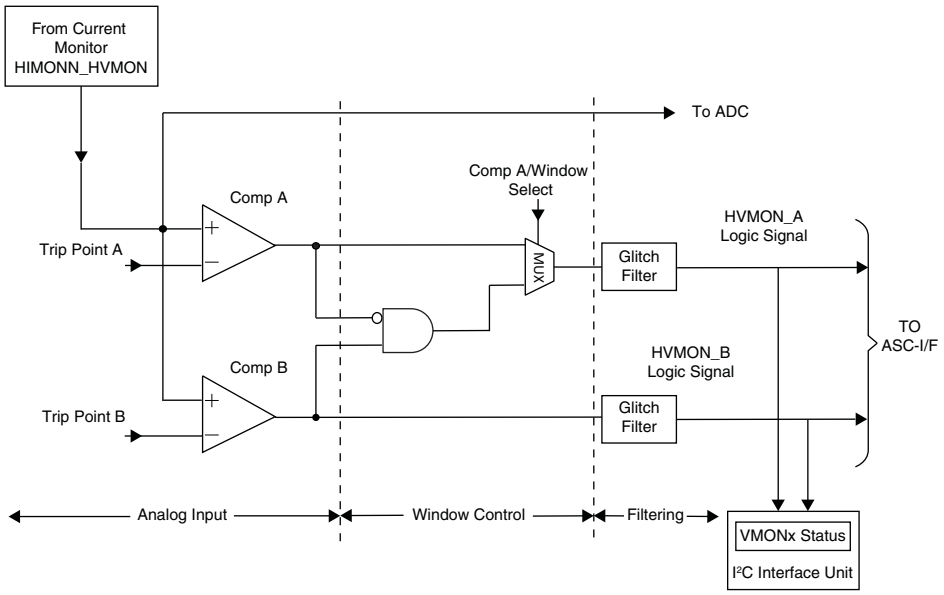
The fourth section in the current monitor circuit is a glitch filter. When enabled, glitches of less than 64 µs will not result in the comparator output changing. This results in a comparator output delay of 64 µs (typical) for all comparator transitions. This is especially useful for reducing the possibility of false triggering from noise that may be present on the currents being monitored. When the filter is disabled, the comparator output will be delayed by 16 µs (typical). See the Propagation Delays section for more details.

The comparator status can be read from the I^2C interface. For details on the I^2C interface, please refer to the I^2C Interface section of this data sheet.

High Voltage Monitor

The High Voltage Monitor circuit is a single-ended high voltage monitor (HVMON) which is connected to the same input pin as the High Voltage Current Monitor (HIMONN_HVMON). Figure 9 shows the single-ended monitor circuit, which monitors the voltage on the HIMON pin.

Figure 9. HVMON Monitor Circuit



The HVMON follows the same structure as the Voltage Monitor circuits. Two individually programmable trip-point comparators are connected to the HIMONN_HVMON pin voltage. Each of the comparator references has 408 programmable trip points, over a range of 0.227 V to 13.226 V.

The functional block diagram, shown in Figure 9, is a similar structure to the other single-ended Voltage Monitor circuits. Each comparator outputs a HIGH signal to the ASC-I/F if the voltage at its positive terminal is greater than its programmable trip point setting. A hysteresis of approximately 1% of the setpoint is provided by the comparators to reduce false triggering. Table 6 shows a typical hysteresis versus voltage monitor trip point.

Table 6. HVMON Hysteresis vs Trip Point Range

Trip-point Range (V)		Hysteresis (mV)
Low Limit	High Limit	
1.91	2.27	22
2.27	2.7	28
2.69	3.2	30
3.16	3.76	38
3.72	4.43	44
4.40	5.24	52
5.18	6.17	61
6.04	7.20	72
7.08	8.43	84
8.29	9.87	99
9.68	11.52	115
11.17	13.2	133
0.23	1.28	0 (Disabled)

The Over-Voltage and Under-Voltage thresholds, along with the window mode and glitch filter, are identical to the features described in the voltage monitor section.

VMON and IMON Measurement with the On-Chip Analog to Digital Converter (ADC)

The ASC has an on-chip analog to digital converter that can be used for measuring the voltages at the VMON inputs or the currents at the IMON inputs. This ADC is also used in closed loop trimming of DC-DC converters. Closed loop trimming is covered later in this document.

Figure 10. ADC Monitoring VMON and IMON

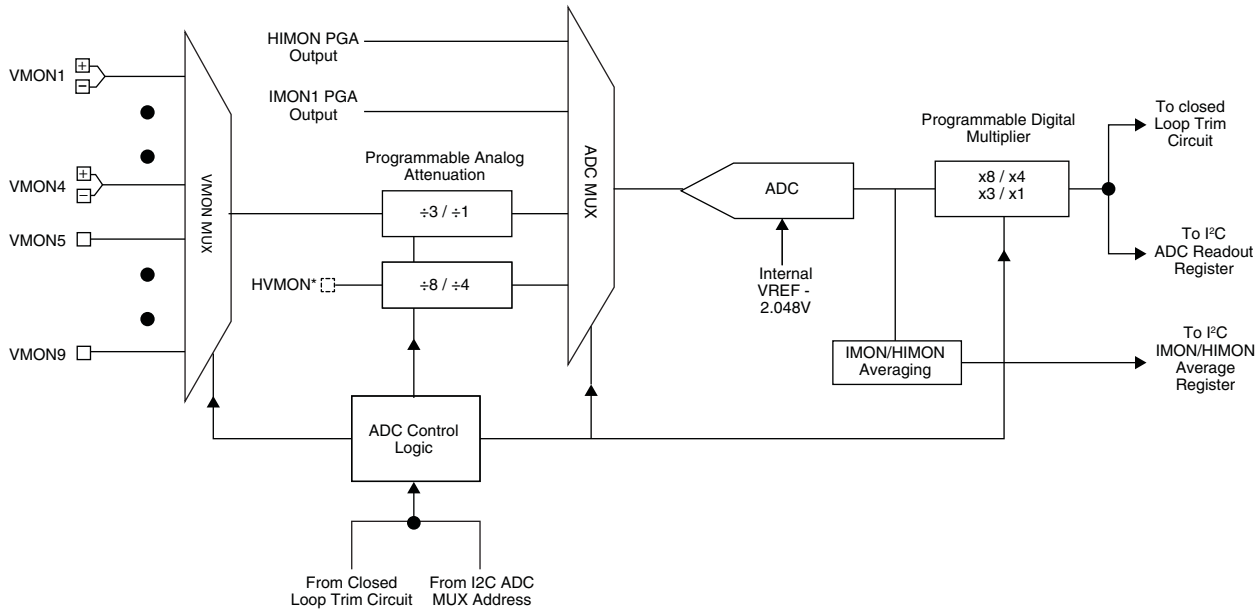


Figure 10 shows the ADC circuit arrangement within the ASC device. The ADC can measure all analog input voltages up to 2.048V through the multiplexer, ADC MUX. The ADC MUX receives inputs from the High Voltage IMON Programmable Amplifier (PGA), the IMON1 PGA, the High Voltage Monitor (HVMON) at the HIMONN_HVMON pin, and the VMON MUX. The VMON voltages can be attenuated (divided by three) or unattenuated (divided by one). The divided-by-three setting is used to measure voltages from 0 V to 6 V range and divided-by-one setting is used to measure the voltages from 0 V to 2 V range. The HVMON voltage requires attenuation, with settings for divided by eight (voltages between 8 V and 13.2 V) or divided by four (voltages between 8 V and 0 V). The HIMON and IMON1 PGA output voltages must be kept below 2.0 V for proper ADC operation since they are not attenuated.

The ADC control logic manages the MUX and attenuation settings. The control logic manages conversion requests from I^2C and the Closed Loop Trim Circuit. The control logic also schedules regular IMON1 and HIMON conversions, which are subsequently averaged and stored for user access. These IMON conversions are configured through the I^2C bus and filtered using an eight sample, weighted averaging scheme.

The control logic also sets the digital multiplication factor. This results in VMON and HVMON voltages, regardless of attenuation setting, maintaining a 2 mV per LSB scale. (See calculation section for more details). The IMON1/HIMON voltages are not multiplied.

A microcontroller or FPGA IP can place a request for any VMON or IMON voltage measurement at any time through the I^2C bus. After the receipt of an I^2C command, the control logic will connect the ADC to the I^2C selected VMON or IMON through the ADC MUX. The ADC output is then latched into the I^2C readout registers.

Calculation

The algorithm to convert the ADC code to the corresponding VMON / HVMON voltage takes into consideration the relevant attenuation setting. In other words, if the attenuation is set to divide-by-eight, then the 10-bit ADC result is automatically multiplied by eight to calculate the actual voltage at that VMON input. Thus, the I^2C readout register is 13 bits instead of 10 bits. The other attenuator settings are also automatically compensated using the digital multiplier. The following formula can always be used to calculate the actual voltage from the ADC code.

Voltage at the VMONx Pins

VMON= ADC code (13 bits, converted to decimal) * 2 mV

The ADC code includes the ADC_VALUE_HIGH (8 bits) and ADC_VALUE_LOW (5 bits) read from I^2C interface

Calculating the HIMON or IMON1 current is slightly more complex, and requires knowledge about the current PGA setting and the resistance value of the current sense shunt resistor. The PGA has four settings (x10, x25, x50, and x100), while the current sensing resistance is chosen by the customer.

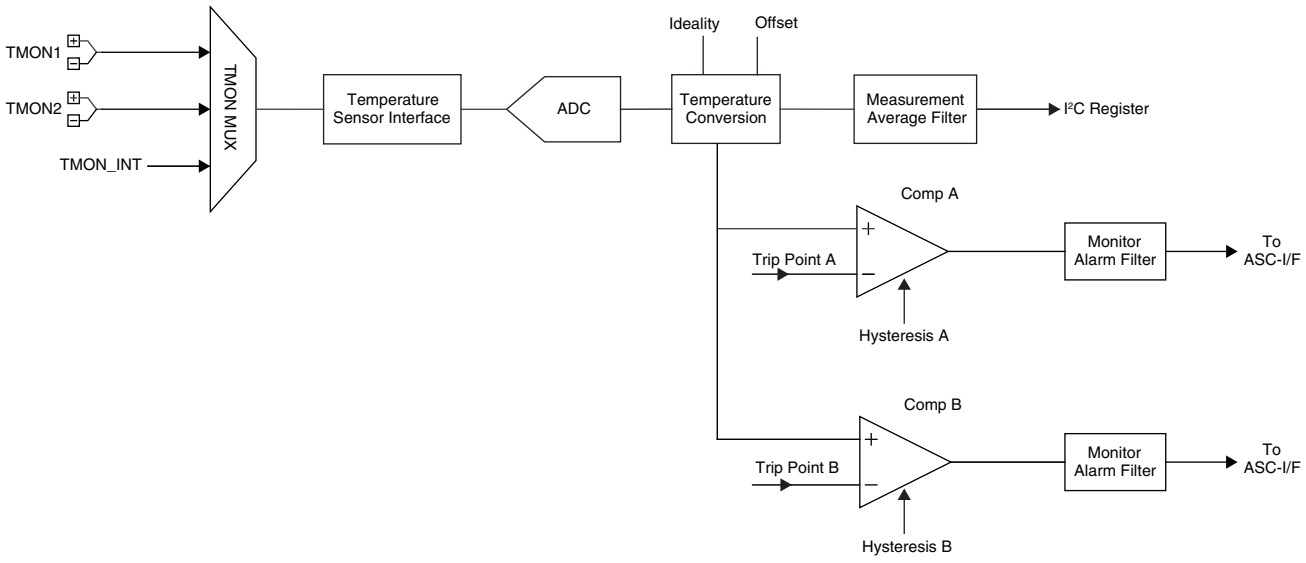
Current at the HIMON / IMON1 Pins

IMON current = ADC code (13 bits, converted to decimal) * 2 mV / (PGAsetting x Rsense)

Temperature Monitor Inputs

The ASC provides two external temperature monitor inputs and one internal temperature monitor as shown in Figure 11.

Figure 11. Temperature Monitor



The independently programmable temperature monitor inputs can be used with internal substrate diodes on microprocessors, FPGAs, ASICs, or with low cost external NPN or PNP transistors. The temperature sensor interface block includes programmable support for a variety of sensor configurations as shown in Figure 12. The sensor configuration settings available in the design software are described in Table 7.

Figure 12. Remote TMON Diode Configurations

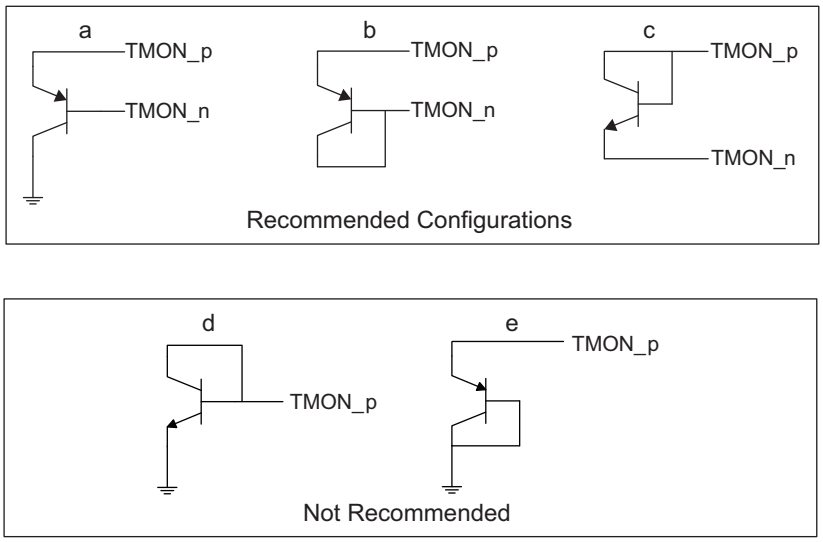


Table 7. Remote TMON Diode Configurations

Sensor Configuration	Figure Number	Auto-β Compensation	Series Resistance Compensation	Accuracy
Beta Compensated PNP	11-a	Effective	Effective	Specified in recommended operating conditions
Differential PNP or NPN or Diode	11-b / 11-c	Not effective	Effective	Dependent on β variance
Single Ended	11-d / 11-e	Not effective	Not Effective	Not specified

The temperature sensor interface block also has built-in circuits to automatically compensate for the series resistance of the PCB traces to the sensor as well as the intrinsic device resistance. In addition, the interface block has circuits to compensate for the variable Beta (β) of the transistor sensor when it is connected in the configuration shown in Figure 12-a. (In order for the variable β compensation circuit to be effective it must be able to measure the base current separately from the collector current.) For a discrete PNP or NPN transistor with high β (approximately 100 or greater) the effect of variable beta is typically negligible. However, most substrate diode temperature sensors will have a low β value which can vary considerably over temperature and current density making this a very useful feature.

The temperature signal information is converted to digital data by the dedicated TMON ADC. The digital data is scaled and converted to a two's complement, 11-bit temperature reading by the Temperature Conversion block. The measurement resolution is 0.25 ºC per bit. The temperature conversion block takes into account the user entered ideality factor and offset value.

The ideality factor (also known as the emission coefficient or the N-factor) is a measure of how closely a real diode follows the ideal diode equation. In a real diode imperfections allow some recombination to occur in the junctions or by other methods which are not accounted for in the ideal equation. The ASC temperature conversion block is optimized for an ideality factor of 1 so any errors in the actual ideality factor of the sensor will produce a proportional error in the temperature value (in Kelvins). The diode ideality factor can be programmed in the range from 0.9 to 2.0 to match the actual ideality factor of the sensor.

An approximate value for the ideality factor for a 2N3904 NPN transistor is 1.004 and for a 2N3906 PNP transistor is 1.008. A substrate diode temperature sensor will typically have an ideality factor published in its data sheet.

Uncertainty can be introduced in temperature measurement by using an approximate value rather than the actual value for a 2N3904 or a 2N3906 transistor. This can lead to an error of around 0.4 °C. If the ideality factor for the transistor being used is not published it can be determined by the ASC using the following procedure.

1. Force the system temperature to a known value (Tref).
2. With the ASC ideality factor set to 1.000, record the temperature value calculated (Tnocal).
3. Convert the Tref and Tnocal to Kelvin.
4. Divide the Tnocal (K) by Tref (K).

The result will be the actual ideality factor to be entered for the given TMON channel in the design software.

Note: The calibration is only as accurate as the Tref value. Any errors in the test equipment used will be transferred to the ASC readings.

The temperature conversion block also provides user programmable temperature offset from –64 °C to 63.75 °C for each channel's digital data to mitigate errors due to self-heating of the sensor, systematic offset and other unforeseen errors.

The conversion block also includes programmable output values for detected short or open conditions at the monitor input. The output levels are shown in Table 8.

Table 8. Temperature Measurement Fault Readings

Fault	Short	Open
0	–255.75 °C	255.75 °C
1	255.75 °C	–255.75 °C

The converted temperature data for each channel is stored in two registers and can be read out via I^2C, after the programmable Measurement Averaging filter. For more details about the data register format, please refer to Measurement and Control Register Access in the I^2C Interface section of this data sheet.

The programmable measurement filter performs exponential averaging. Data is available immediately after one update cycle and is continually averaged using the programmable filter coefficients of 1, 8, or 16 per channel. The filtering equation is shown below:

$$TempAve[x] = \frac{TempMeas[x]}{FiltCo} + TempAve[x-1] \times \frac{FiltCo-1}{FiltCo}$$

When the temperature input changes it will require some settling time for the new value to be fully reflected in the results register due to the averaging filter. The settling time will vary depending upon how many channels are enabled and the programmed averaging coefficient. The settling time for various averaging coefficients and number of channels is shown in Table 9.

Table 9. Temperature Measurement Settling Time[1]

Measurement Averaging Coefficient	Number of Channels Enabled	Average Settling Time (ms)
1	1	14.2
8	1	114
16	1	228
1	2	28.4
8	2	227
16	2	454
1	3	42.6
8	3	341
16	3	682

1. Values are approximate and are not guaranteed by characterization.

In addition to the direct temperature measurement the ASC has a temperature comparison function. The digital data of each channel is monitored by two trip-point comparators, shown as Comp A and Comp B in Figure 11. The digital temperature data monitored at the comparators is not processed by the measurement averaging filters. Each comparator reference has programmable trip points over the range of –64 ºC to 155 ºC with resolution of 1ºC. Whenever the monitored temperature is above the trip point, the comparator output is set to one. The comparator outputs are transmitted over the ASC-I/F to the FPGA, depending on the setting of the Alarm Filter.

The two comparators each support programmable Hysteresis of 0 ºC to 63 ºC. When a comparator is used for over-temperature monitoring the programmed hysteresis value is subtracted from the trip point and when the comparator is used for under-temperature monitoring the programmed hysteresis value is added to the trip point. The hysteresis behavior is displayed in Figure 13 and Figure 14.

Figure 13. Monitor Alarm Signal Behavior - Overtemperature (OT) Setting