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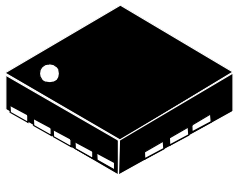
L3GD20H

MEMS motion sensor: three-axis digital output gyroscope

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- Wide supply voltage, 2.2 V to 3.6 V
- Wide extended operating temperature range (from -40 °C to 85 °C)
- Low voltage compatible IOs, 1.8 V
- Low power consumption
- Embedded power-down
- Sleep mode
- Fast turn-on and wake-up
- Three selectable full scales up to 2000 dps
- 16 bit rate value data output
- 8 bit temperature data output
- I^2C/SPI digital output interface
- 2 dedicated lines (1 interrupt, 1 data ready)
- User enable integrated high-pass filters
- Embedded temperature sensor
- Embedded 32 levels of 16 bit data output FIFO
- High shock survivability
- ECOPACK® RoHS and “Green” compliant

Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics

Description

The L3GD20H is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface able to provide the measured angular rate to the external world through digital interface (I^2C/SPI).

The sensing element is manufactured using a dedicated micromachining process developed by ST to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The L3GD20H has a full scale of ±245/±500/±2000 dps and is capable of measuring rates with a user selectable bandwidth.

The L3GD20H is available in a plastic land grid array (LGA) package and can operate within a temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order code	Temperature range (°C)	Package	Packing
L3GD20H	-40 to +85	LGA-16 (3x3x1)	Tray
L3GD20HTR	-40 to +85	LGA-16 (3x3x1)	Tape and reel

This is information on a product in full production. www.st.com

Contents

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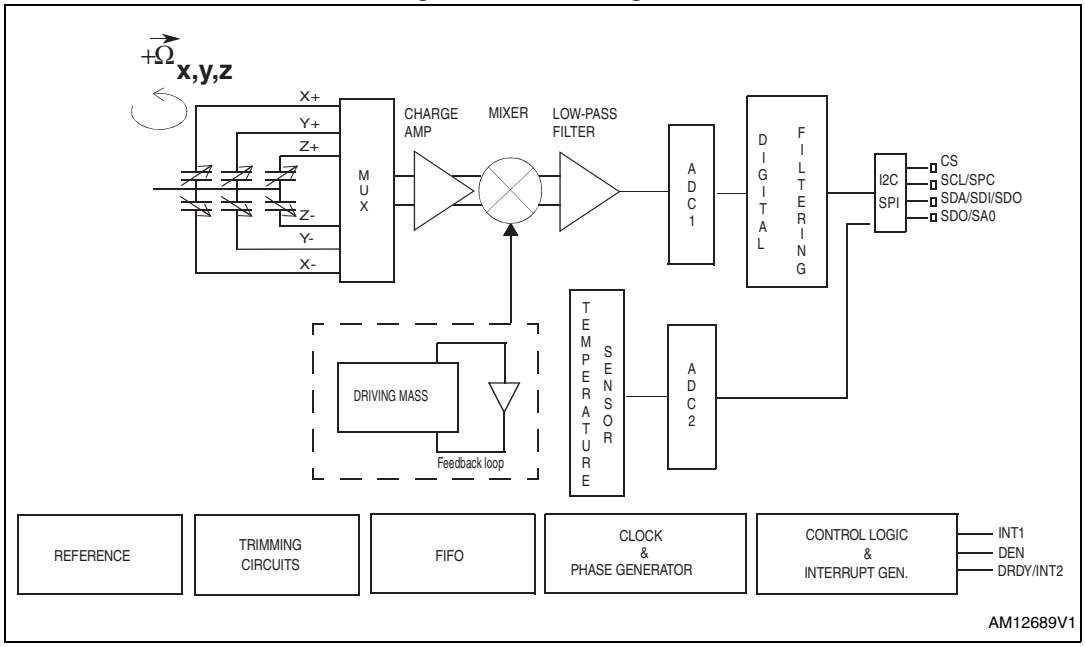
1 Block diagram and pin description

Figure 1. Block diagram



The vibration of the structure is maintained by a drive circuitry in a feedback loop. The sensing signal is filtered and appears as digital signal at the output.

1.1 Pin description

Figure 2. Pin connection

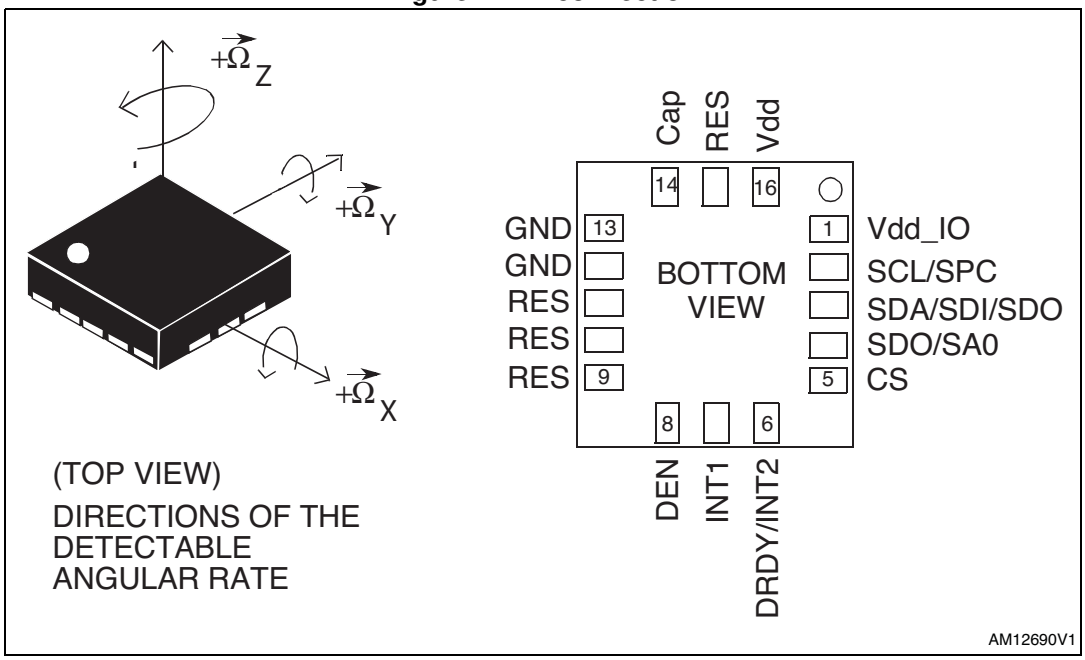


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO(1)	Power supply for I/O pins
2	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)
5	CS	I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I2C disabled)
6	DRDY/INT2	Data ready/fifo interrupt (FIFO threshold/overrun/empty)
7	INT1	Programmable interrupt
8	DEN(2)	Gyroscope data enable
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND or VDD
12	GND	0 V supply
13	GND	0 V supply
14	Cap	Connect to GND with ceramic capacitor(3)
15	Reserved	Connect to GND or VDD
16	Vdd(4)	Power supply

1. Recommended 100 nF filter capacitor.
2. Connected to GND if DEN is not used.
3. 10 nF (+/-10%), 25 V. 1 nF minimum value has to be guaranteed under 12 V bias condition.
4. Recommended 100 nF plus 10 µF capacitors.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
FS	Measurement range	User selectable		±245 ±500 ±2000		dps
So	Sensitivity			8.75 17.50 70.00		mdps/digit
SoDr	Sensitivity change vs. temperature[2]	From -40 °C to +85 °C Delta from T = 25 °C		±2		%
DVoff	Digital Zero-rate level	FS = 2000 dps		±25		dps
OffDr	Zero-rate level change vs temperature[3]	FS = 2000 dps		±0.04		dps/°C
NL	Non linearity[3]	Best fit straight line		0.2		% FS
Rn	Rate noise density[3]	BW = 50 Hz		0.011		dps/($\sqrt{Hz}$)
ODR	Digital output data rate[3]			11.9/23.7/ 47.3/94.7/ 189.4/ 378.8/ 757.6		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Guaranteed by design.
3. The period (1/ODR), length of time between two consecutive sampling, must be derived by the reciprocal of the maximum. and minimum ODR limits: for example for ODR = 189.4 Hz, sampling period range will be within [4591 µs, 6211 µs] (where ODR minimum and maximum have been approximated at 162 Hz, 219 Hz respectively).

a. The product is factory calibrated at 3.0 V. The operational power supply range is specified in *Table 4*.

2.2 Electrical characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted[b].

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		2.2	3.0	3.6	V
Vdd_IO	I/O pins supply voltage[2]		1.71		Vdd+0.1	V
Idd	Supply current			5.0		mA
IddSL	Supply current in sleep mode[3]	Selectable by digital interface		2.5		mA
IddPdn	Supply current in power-down mode	Selectable by digital interface		1		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
Ton	Turn-on time[4]	LPF2 disabled ODR = 190 Hz		50		ms
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
3. Sleep mode introduces a faster turn-on time related to power down mode.
4. Time to obtain stable sensitivity (within ±5% of final value) after exiting power-down mode. It is guaranteed by design.

b. The product is factory calibrated at 3.0 V.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted[c].

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
TSDr	Temperature sensor output change vs temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

c. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

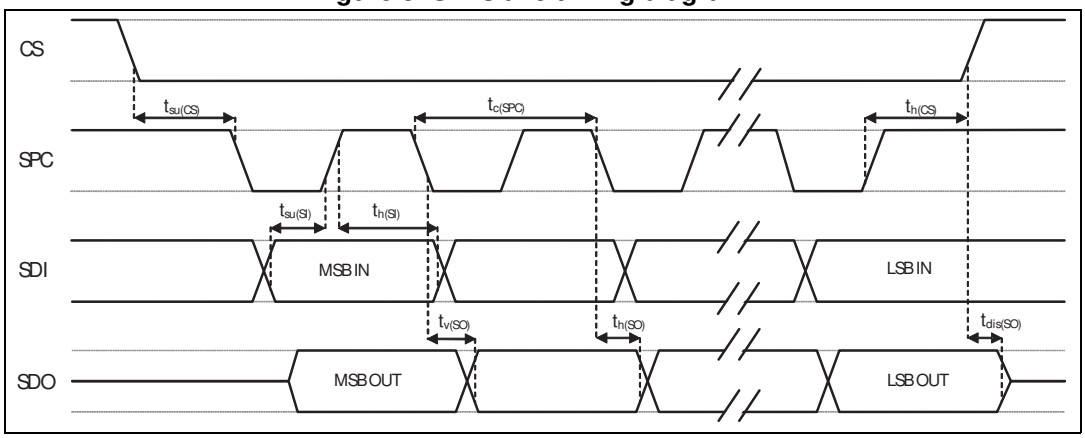
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	20		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	5		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram(d)



d. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both Input and Output port.

2.4.2 I²C - Inter IC control interface

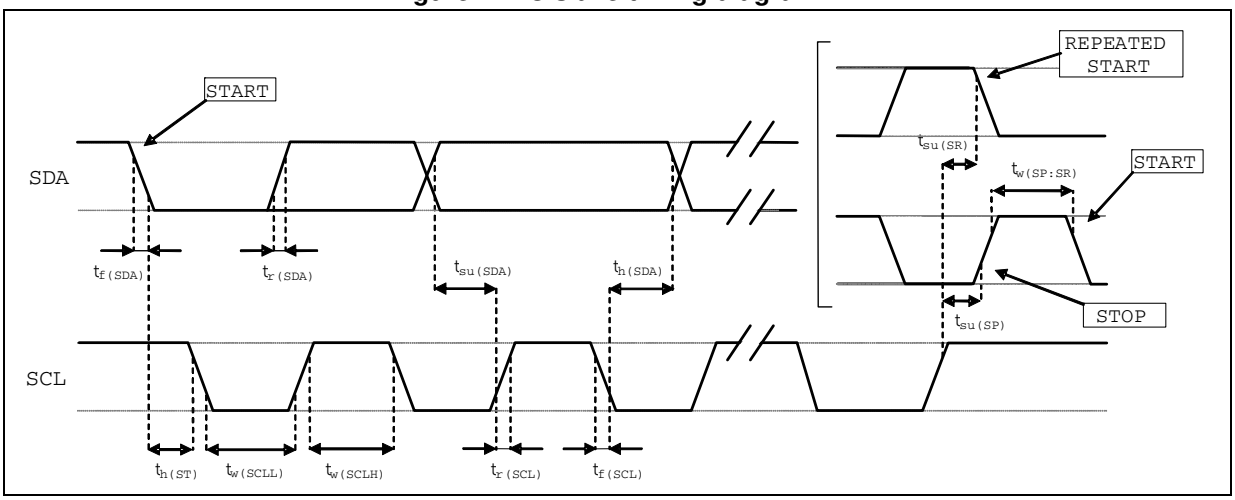
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	μs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		μs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. Cb = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram(e)



e. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	g
ESD	Electrostatic discharge protection	2 (HBM)	kV
Vin	Input voltage on any control pin (including CS,SCL/SPC,SDA/SDI/SDO,SDO/SA0,DEN)	0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going analog output for counterclockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress.

2.7 Soldering information

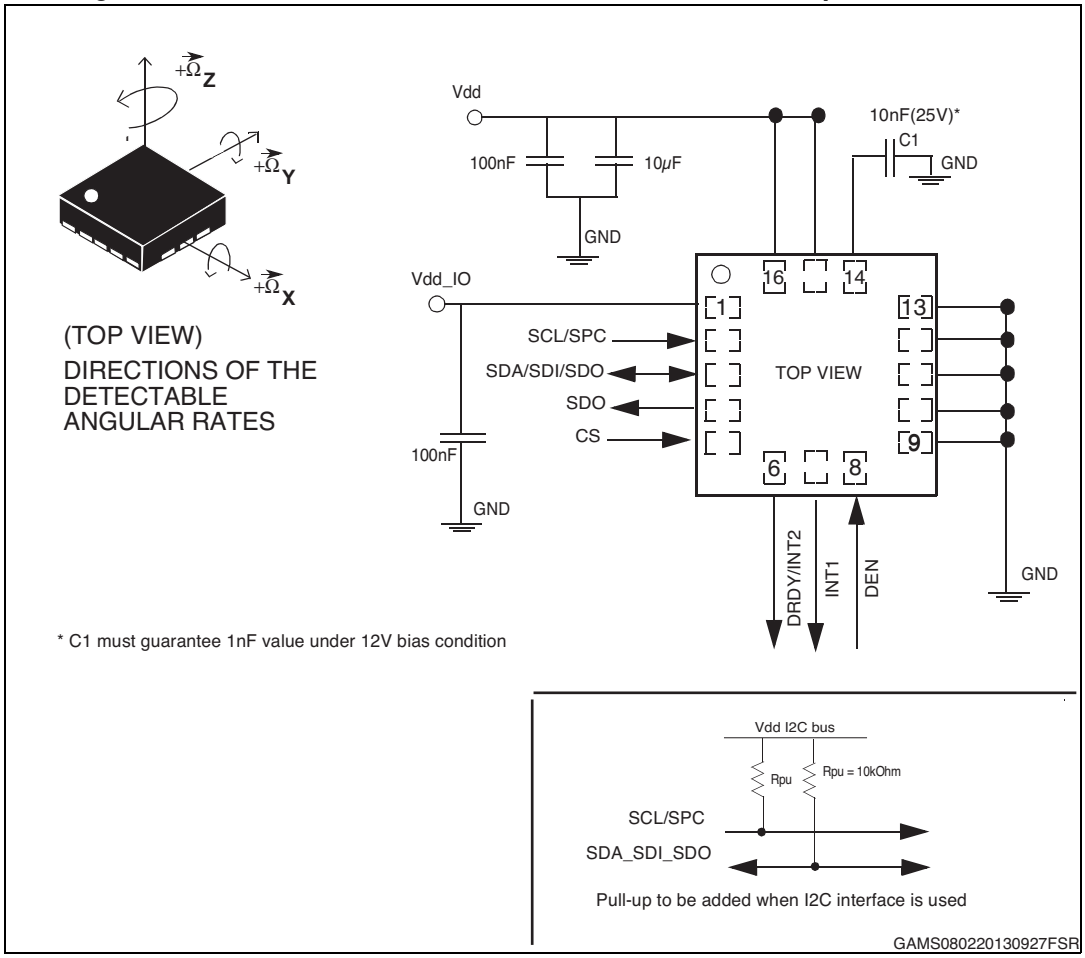
The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

3 Application hints

Figure 5. L3GD20H electrical connections and external components values



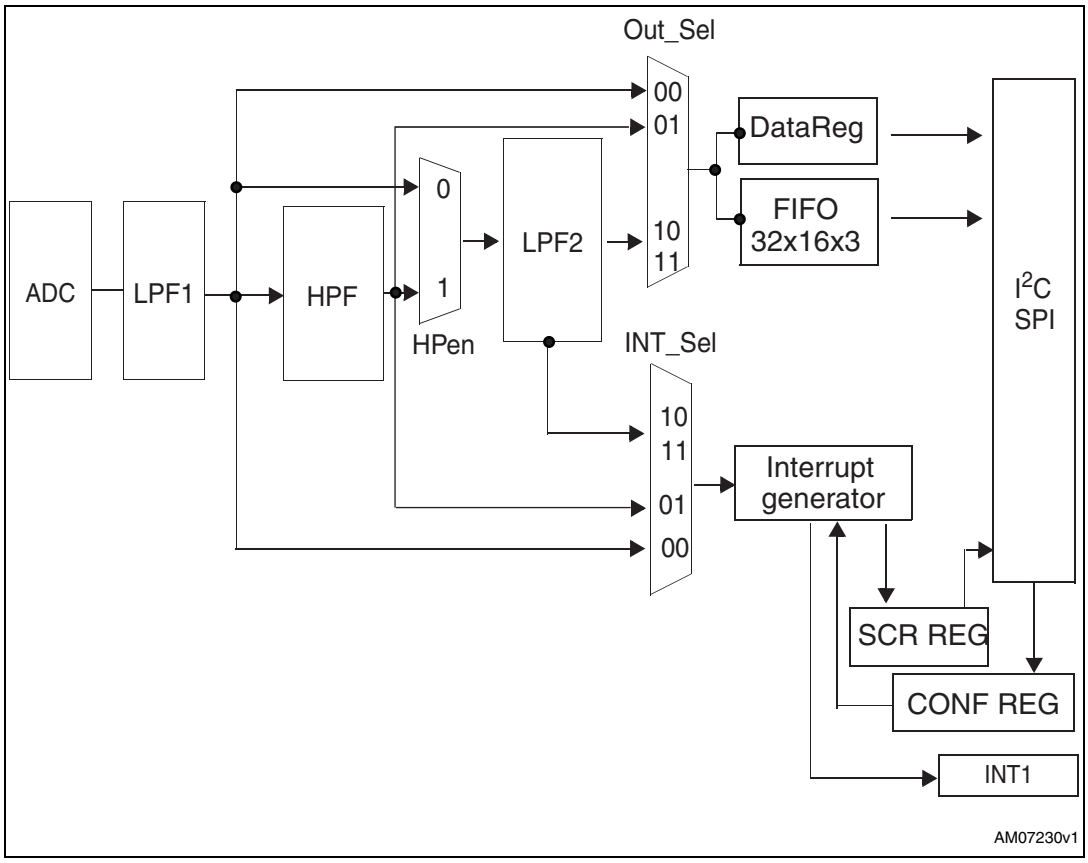
Power supply decoupling capacitors (100 nF + 10 μF) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd_IO are not connected together, 100 nF and 10 μF decoupling capacitors must be placed between Vdd and common ground while 100 nF between Vdd_IO and common ground. Capacitors should be placed as near as possible to the device (common design practice).

4 Digital main blocks

4.1 Block diagram

Figure 6. Block diagram



4.2 FIFO

L3GD20H embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wakeup only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to seven different modes: Bypass mode, FIFO-mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream, Dynamic-Stream, Bypass-to-FIFO. Each mode is selected by the FM2:0 bits in FIFO_CTRL register. Programmable FIFO threshold level, FIFO empty or FIFO overrun events are available on FIFO_SRC register and can be set to generate dedicated interrupts on DRDY/INT2 pin.

FIFO_SRC(EMPTY) is equal to '1' when no samples are available.

FIFO_SRC(FTH) goes to '1' if a new data arrives and FIFO_SRC(FSS4:0) is greater than or equal to FIFO Threshold configured to FTH4:0 into FIFO_CTRL (2Eh). FIFO_SRC(FTH) goes to '0' if reading Yaw, Pitch and Roll data slot from FIFO and FIFO_SRC(FSS4:0) is minor than or equal to FIFO_CTRL(FTH4:0).

FIFO_SRC(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO feature is enabled writing to '1' CTRL5(FIFO_EN).

To guarantee the switching into and out of FIFO mode discard the first sample aquired.

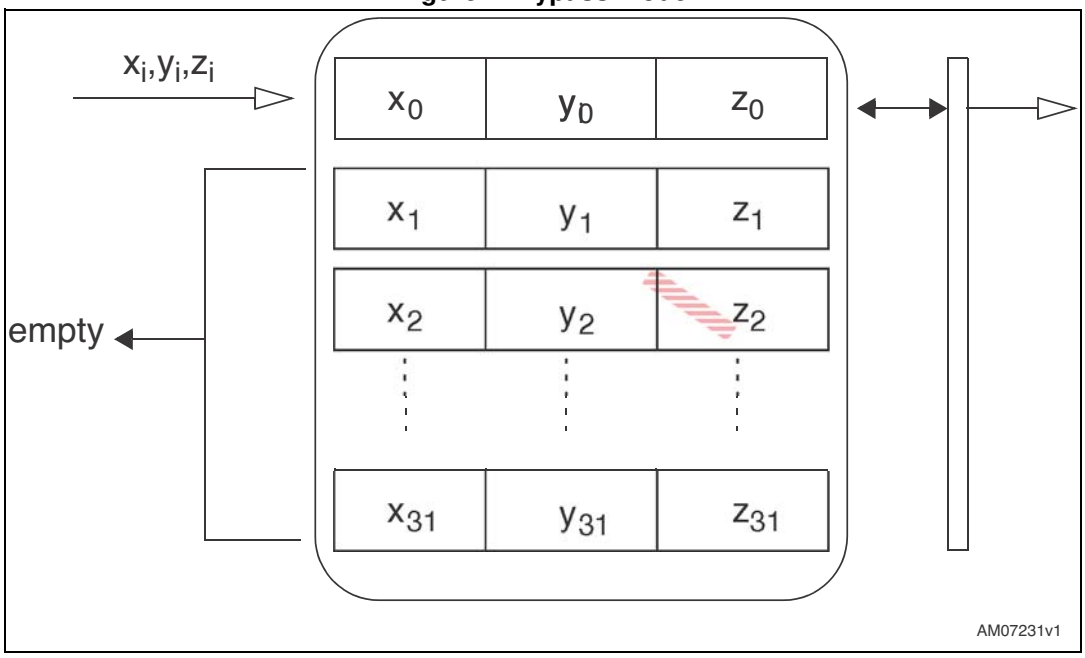
4.2.1 Bypass mode

In bypass mode (FIFO_CTRL(FM2:0) = 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO-mode.

As described in the next figure, for each channel only the first address is used. When a new data is available the old one is overwritten.

Figure 7. Bypass mode



4.2.2 FIFO mode

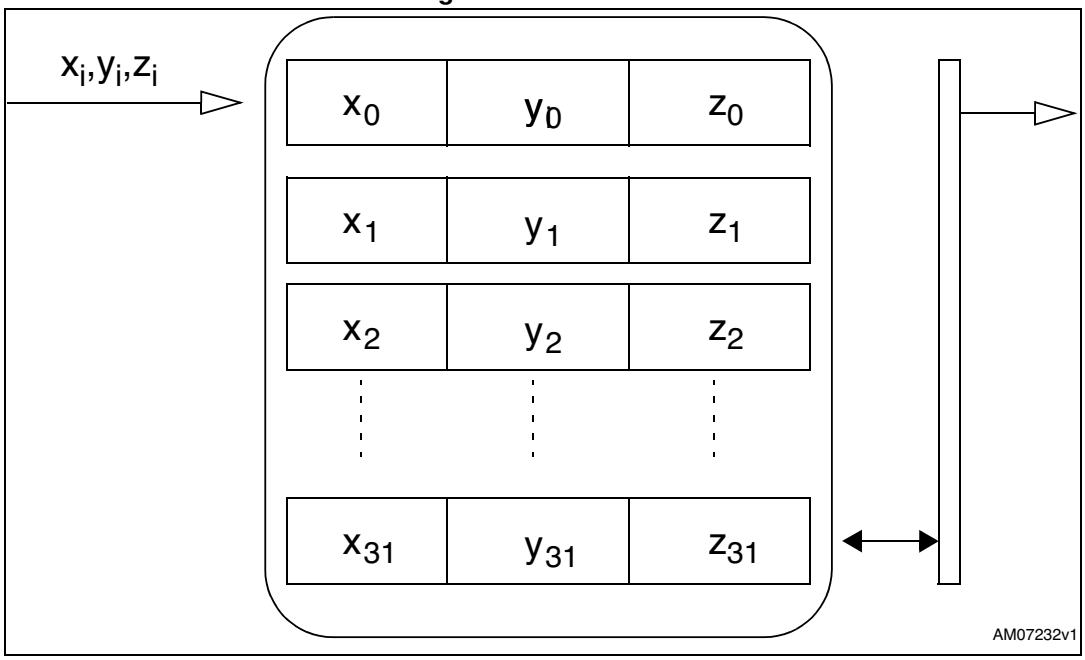
In FIFO mode (FIFO_CTRL(FM2:0) = 001) data from Yaw, Pitch and Roll channels are stored into the FIFO until it is full.

To reset FIFO content Bypass mode should be written in FIFO_CTRL(FM2:0) '000' value. After this reset command it is possible to restart FIFO mode writing FIFO_CTRL(FM2:0) the value '001'.

FIFO buffer can memorize 32 Yaw, Pitch and Roll data, but the depth of the FIFO can be reduced by means of CTRL5(StopOnFTH) bit setting to '1' StopOnFTH bit, FIFO depth is limited to FIFO_CTRL(FTH4:0) - 1.

A FIFO Threshold interrupt can be enabled (INT2_ORun bit into CTRL3 (22h)) in order to be raised when the FIFO is filled to the level specified into the FTH4:0 bits of FIFO_CTRL (2Eh). When FIFO Threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 8. FIFO mode

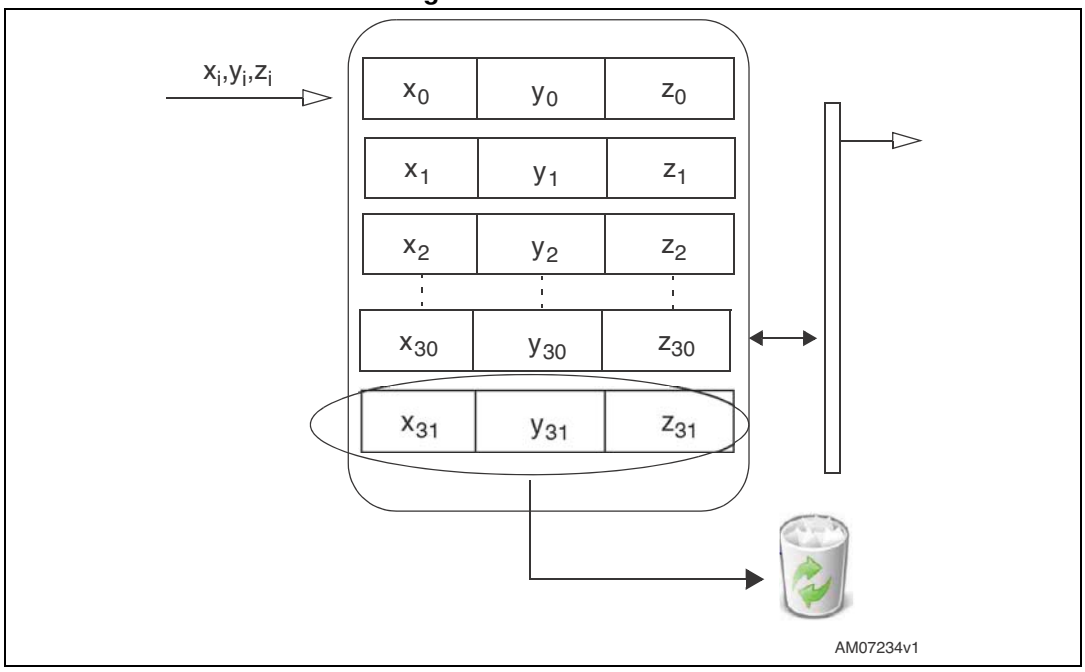


4.2.3 Stream mode - dynamic stream

Stream mode (FIFO_CTRL(FM2:0) = 010) provides continuous FIFO update: as new data arrives the older is discarded.

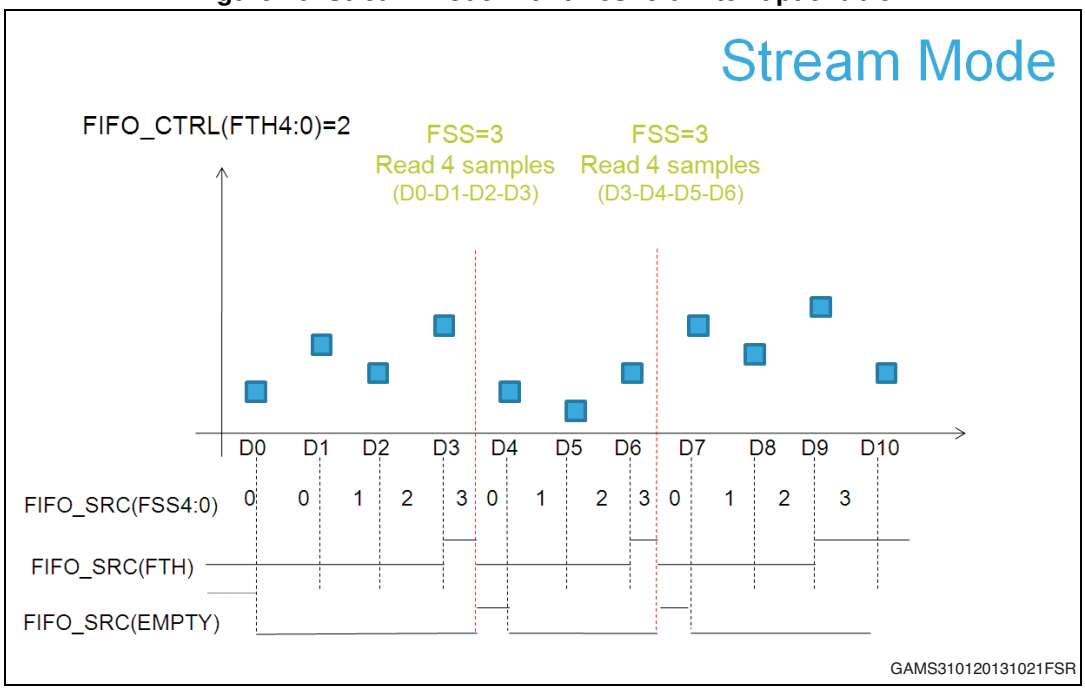
An overrun interrupt can be enabled, CTRL3(INT2_ORun)= '1', in order to read the whole FIFO content at once. If in the application no data can be lost and it is not possible to read at least one sample for each axis within one ODR period, a FIFO Threshold interrupt can be enabled in order to read partially the FIFO and let free memory slots for data incoming. Setting the FIFO_CTRL(FTH4:0) to N value, the number of Yaw, Pitch and Roll data samples that should be read at FIFO Threshold interrupt rising is up to (N+1).

Figure 9. Stream mode



In the latter case reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in previous burst, so the number of new data available in FIFO depends on previous reading (see FIFO_SRC behavior depicted in next figures).

Figure 10. Stream mode with threshold interrupt enable



In dynamic-stream mode (FIFO_CTRL(FM2:0) = 110) after emptying the FIFO the first new sample that arrives becomes the first to be read in subsequent read burst. In this way in

dynamic-stream mode (FIFO_CTRL(FM2:0) = 110) the number of new data available in FIFO does not depend on previous reading.

In dynamic-stream mode FIFO_SRC(FSS4:0) + 1 is the number of new X, Y and Z samples available in the FIFO buffer.

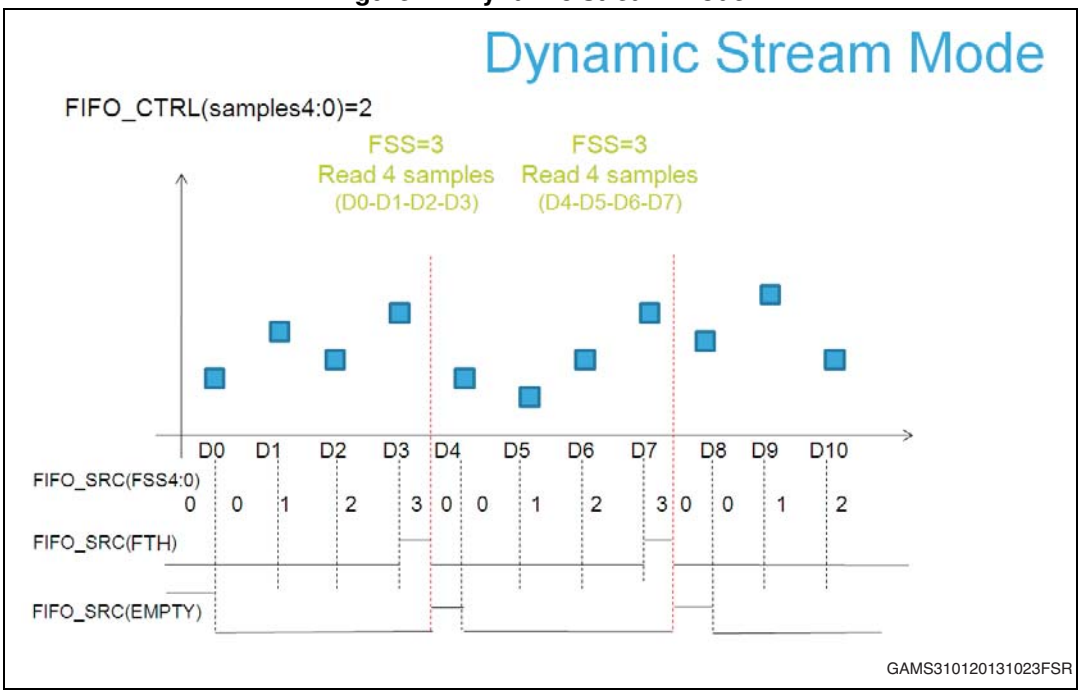
Stream mode is intended to be used reading all 32 samples of FIFO within an ODR after receiving an overrun signal.

Dynamic-stream is intended to be used to read FIFO_SRC(FSS4:0) + 1 samples when it is not possible to guarantee data reading within an ODR.

In dynamic-stream mode FIFO_CTRL(FTH4:0) setting should be between 1 and 30.

Also a FIFO Threshold interrupt CTRL3(INT2_FTH) can be enabled in order to read data from the FIFO and let free memory slot for data incoming. Setting the FIFO_CTRL(FTH4:0) to N value, the number of X, Y and Z data samples that should be read at FIFO Threshold interrupt rising, in order to read the whole FIFO content, is N + 2.

Figure 11. Dynamic stream mode



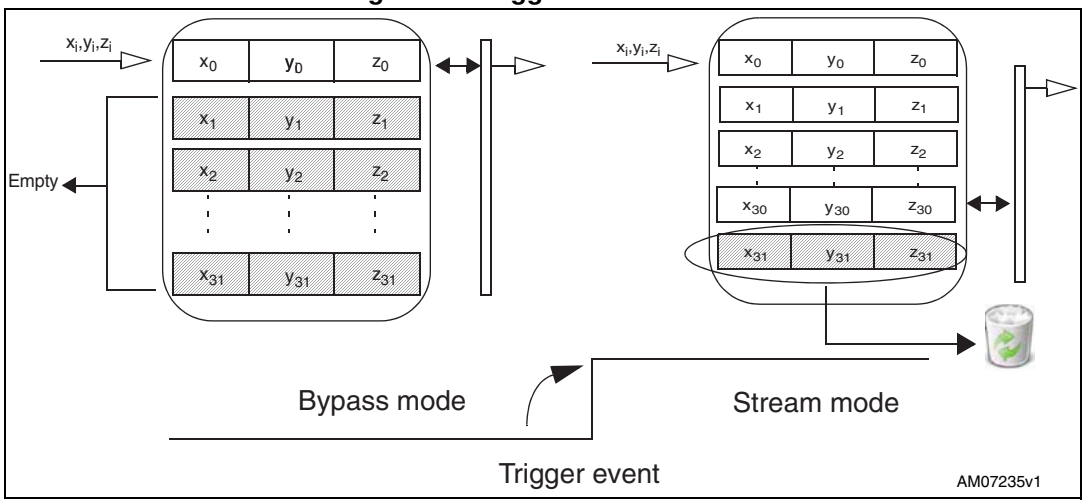
4.2.4 Stream-to-FIFO mode

In stream-to-FIFO mode (FIFO_CTRL(FM2:0) = 011), FIFO behavior changes according to IG_SRC(IA) bit. When IG_SRC(IA) bit is equal to '1' FIFO operates in FIFO-mode, when IG_SRC(IA) bit is equal to '0' FIFO operates in Stream mode.

Interrupt generator should be set to the desired configuration by means of IG_CFG, IG_THS_XH, IG_THS_XL, IG_THS_YH, IG_THS_YL, IG_THS_ZH and IG_THS_ZL.

IG_CFG(LIR) bit should be put to '1' in order to have latched interrupt.

Figure 12. Trigger stream mode



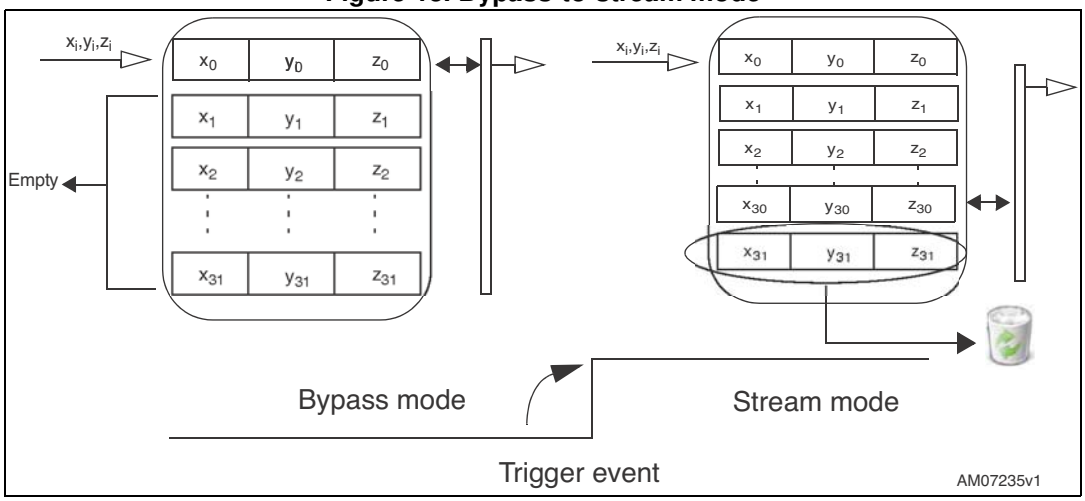
4.2.5 Bypass-to-stream mode

In bypass-to-stream mode (FIFO_CTRL(FM2:0) = '100'), Yaw, Pitch and Roll measurement storage inside FIFO operates in Stream mode when IG_SRC (IA) is equal to '1', otherwise FIFO content is reset (bypass mode) .

Interrupt generator should be set to the desired configuration by means of IG_CFG, IG_THS_XH, IG_THS_XL, IG_THS_YH, IG_THS_YL, IG_THS_ZH and IG_THS_ZL.

IG_CFG(LIR) bit should be put to '1' in order to have latched interrupt.

Figure 13. Bypass-to-stream mode



4.2.6 Bypass-to-FIFO mode

In bypass-to-FIFO mode (FIFO_CTRL(FM2:0) = '111', FIFO behavior changes according to IG_SRC(IA) bit. When IG_SRC(IA) bit is equal to '1' FIFO operates in FIFO-mode, when IG_SRC(IA) bit is equal to '0' FIFO operates in bypass mode (FIFO content reset). If a latched interrupt is generated FIFO starts collecting data until the first data into the FIFO-buffer is overwritten. Interrupt generator should be set to the desired configuration by means of IG_CFG, IG_THS_XH, IG_THS_XL, IG_THS_YH, IG_THS_YL, IG_THS_ZH and IG_THS_ZL.

IG_CFG (LIR) bit should be put to '1' in order to have latched interrupt.

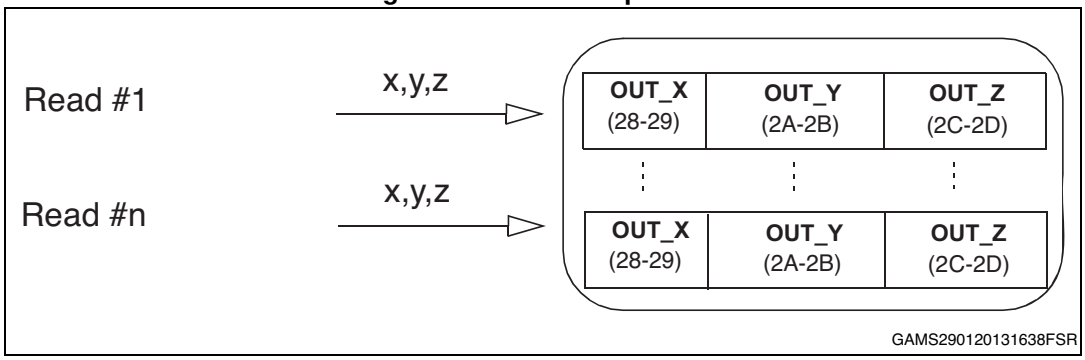
4.2.7 Retrieve data from FIFO

FIFO data is read through OUT_X_L and OUT_X_H (Addr reg 28h and 29h), OUT_Y_L OUT_Y_H (Addr reg 2Ah and 2Bh) and OUT_Z_L and OUT_Z_H (Addr reg 2Ch and 2Dh) registers. A read operation by means of serial interface of OUT_X, OUT_Y or OUT_Z output registers provides the data stored into the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed into the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst operations can be used.

4.2.8 FIFO multiple read (burst)

Starting from the Addr 28h multiple read can be performed. Once the reading reaches the Addr 2Dh the system automatically restarts from the Addr. 28h.

Figure 14. FIFO multiple read



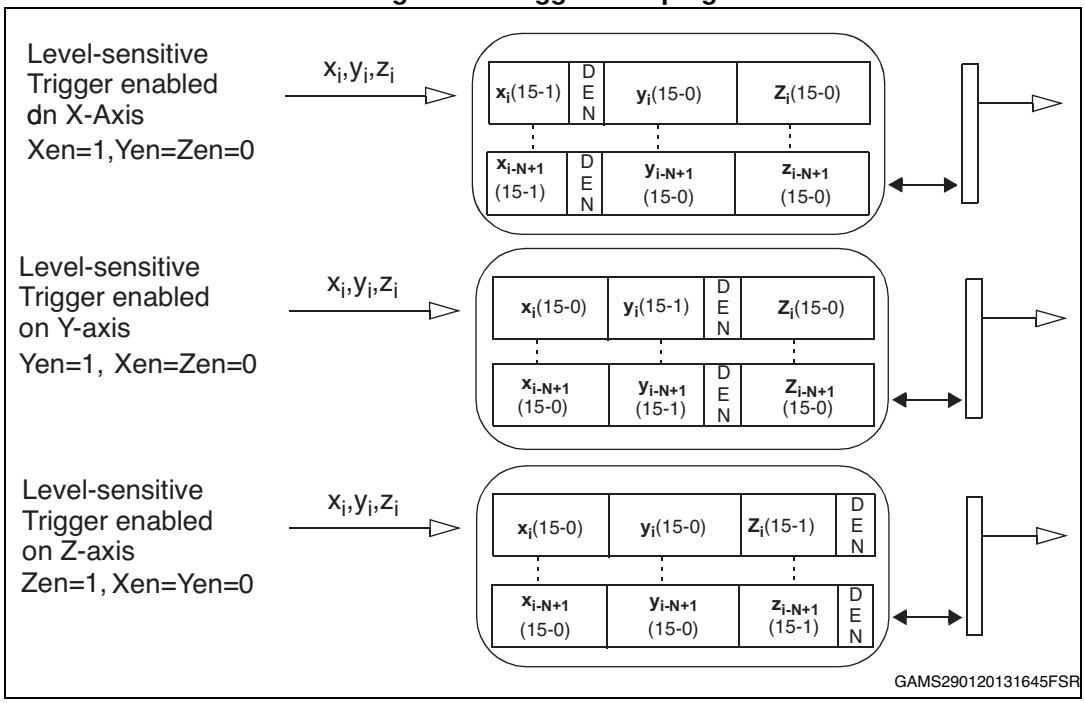
4.3 Level-sensitive/edge sensitive/impulse sensitive data enable

L3GD20H allows external trigger level recognition through enabling EXTRen and LVLen bits into CTRL2 (21h) and IMPen bit into CTRL4 (23h). Three different modes can be used: level, edge or impulse sensitive trigger.

Table 9. Trigger stamping mode

LVLen	EXTRen	IMPen	Trigger stamping mode
1	0	0	Level sensitive trigger
0	1	0	Edge sensitive trigger
1	0	1	Impulse sensitive trigger

Figure 15. Trigger stamping



4.3.1 Level sensitive trigger stamping

Level sensitive trigger can be enabled by setting to ‘1’ the LVLen bit into CTRL2 (21h) while EXTRen bit into CTRL2 (21h) and IMPen bit into CTRL4 (23h) have to be set to ‘0’.

Once enabled, DEN level replaces the LSB of X, Y or Z axes configurable through Xen, Yen, Zen bits into CTRL1 (20h). Data is stored inside the FIFO with the internal selected ODR.

4.3.2 Edge sensitive trigger

Edge sensitive trigger can be enabled by setting to ‘1’ the EXTRen bit into CTRL2 (21h) while LVLen bit into CTRL2 (21h) and IMPen bit into CTRL4 (23h) have to be set to ‘0’.