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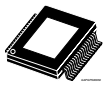
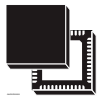
L5963

Automotive dual monolithic switching regulator with LDO and HSD

Datasheet - production data


PowerSSO-36 (exposed pad)


PowerSSO-36 (slug-up)


VQFPN-48

Featuress

- AEC-Q100 qualified
- Two step-down synchronous switching voltage regulators with internal power switches:
  - Wide input voltage range (from 3.5 V to 26 V)
  - Internal high-side/ low-side NDMOS
  - 1 V minimum output
  - 3.0 A load current
  - 250 kHz free-run frequency
  - 250 kHz < f < 2 MHz synchronization range
  - Integrated soft-start
  - Independent hardware enable pins
  - Independent power supply
  - 180° PWM output phase shift
  - Programmable switching frequency divider by 1, 2, 4 or 8 between the two DC/DC regulators
  - Power good function
- One standby / linear regulator
  - Output voltage programmable with external resistor divider
  - 250 mA maximum current capability
  - Backup function
  - Power good function
- One high side driver
  - 0.5 V max drop @ 0.5 A
  - Protected against short to ground and battery, loss of ground and battery, unsupplied short to battery
- Programmable under voltage battery detector
  - Under voltage threshold adjustable through dedicated pin (VDIN)
- Load dump protection
- Independent thermal protection on all regulators
- Independent current limit on all regulators
- Extremely low quiescent current in standby conditions
- Power good / adjustable voltage detector outputs to realize customized power up/down sequences

Description

L5963 is a dual step-down switching regulator with internal power switches, high side driver and a low drop-out linear regulator that can operate as standby regulator or normal LDO.

All the regulators can be connected directly to the vehicle battery. In addition to an adjustable voltage detector, voltage supervisors are available.

The two DC-DC converters can work in free-run condition or synchronize themselves to an external clock. DC/DCs' PWM outputs have a 180° phase shift.

The high operating frequency allowed by the synchronization input helps to reduce AM and FM interferences and grants the use of small and low cost inductors and capacitors.

This IC finds application in the automotive segment, where load dump protection and wide input voltage range are mandatory.

A slug-up package option is available for applications which require heatsink use.

In standby condition the device guarantees extremely low quiescent current (25 µA typical @ -40 °C < T < 85 °C)

Table 1. Device summary

Order code	Package	Packing
L5963D-EHX	PowerSSO36 (exposed pad)	Tube
L5963D-EHT		Tape & Reel
L5963U-KBX	PowerSSO36 (slug-up)	Tube
L5963U-KBT		Tape & Reel
L5963Q-V0Y	VQFPN-48	Tray
L5963Q-V0T		Tape & Reel

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1 Overview

The L5963 integrates two switching mode synchronous step down converters, a linearly regulated power supply, a protected high side driver and voltage detectors. To guarantee a robust operation, all the outputs have independent thermal protection and current limitation.

The two switching mode synchronous step-down converters employ voltage mode control and feed forward functions to provide good load regulation and line regulation. Each converter has its own enable. The users can adjust the output voltage of the two converters by an external resistor divider. If the converters need to work with a frequency different from the free running frequency, in order to consider EMC performance in system level, they can be synchronized to an external clock by applying it on the SYNCIN pin. The frequency should be higher than half of the free running frequency. If there are more than one L5963 in the system they can work in Master-Slave configuration, to make sure all L5963 have the same operating frequency of the Master device. This Master-Slave function is implemented by a dedicated pin SYNCOUT which always gives the operating frequency of DC/DC1.

A dedicated voltage detector is integrated in the first switching converter to monitor DC/DC1 output. When the output voltage of DC/DC1 goes above the threshold, SW1OK is released and goes back to high with configurable delay set by a capacitor on the SW1OKDLY pin.

The linear regulator can work as standby regulator with low I_q or as a non-standby regulator. Connecting its enable ENLDO to its supply VINLDO the regulator works as a standby regulator, while connecting ENLDO to a voltage lower than 5 V the regulator works as non-standby regulator, with higher load capability but also higher quiescent current.

In standby state, i.e. only the linear regulator is powered and works as a standby regulator, with a load below 100 µA the device has a quiescent current of just 25 µA.

The small drop-out voltage of the linear regulator allows its use with low operating supply voltage.

In many cases, the linear regulator has to provide voltages to devices which need the reset function, like a MCU: this is provided by the LDOOK output, that is pulled low when VOUTLDO goes below a threshold. Once VOUTLDO returns above that threshold, with a specified hysteresis, LDOOK goes back to high with a configurable delay set by a capacitor on pin LDOOKDLY.

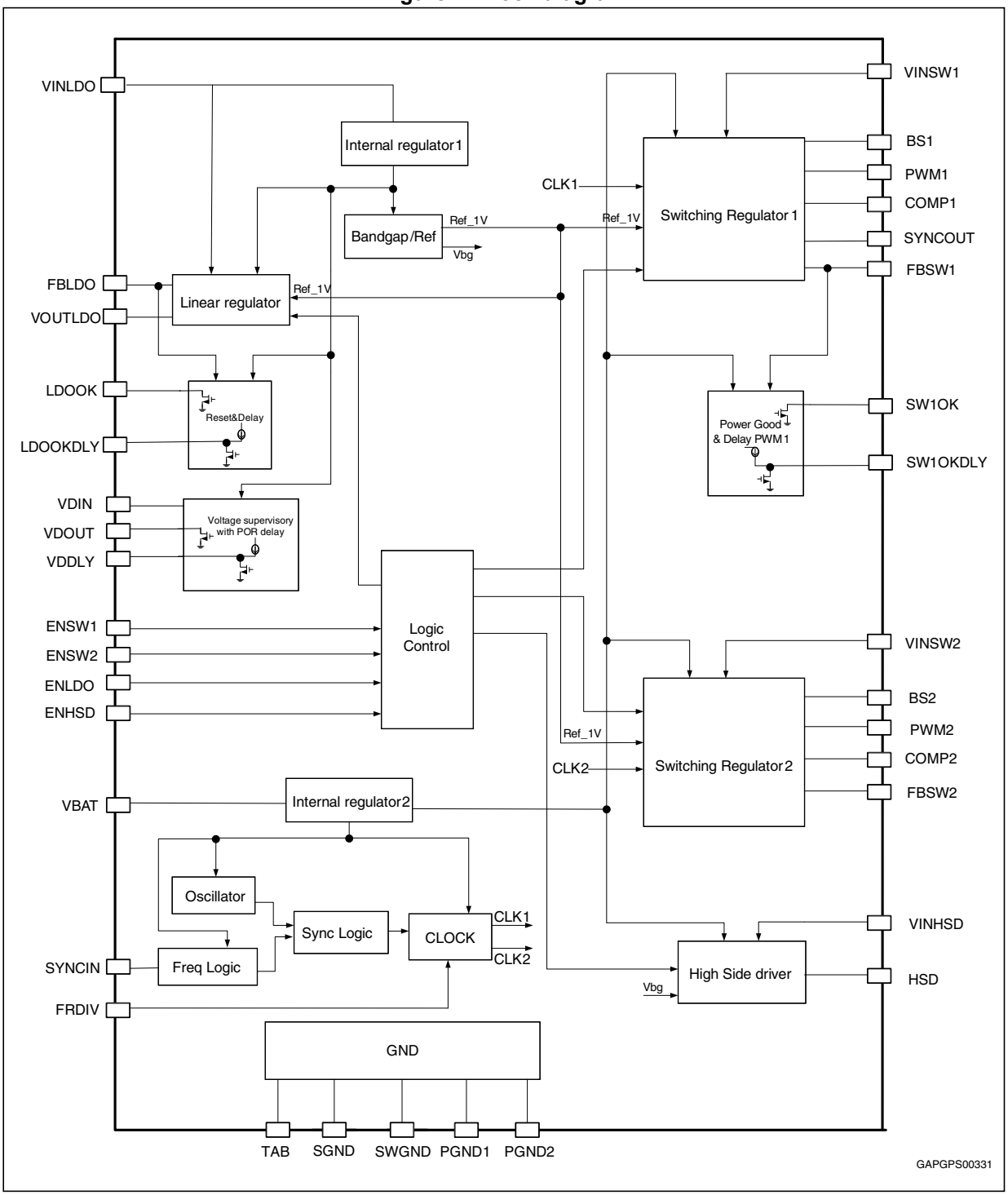
The high side driver is enabled by a dedicated pin and has a very low drop-out voltage. Protection circuits, like independent thermal protection, OCP, OVP and some special protections (loss of GND, SPU, short to supply and so on), are implemented to make it very robust.

L5963 also embeds a voltage monitor (VDOUT), adjustable by means of an external resistor divider, that can be used to sense the battery or other voltages in the system. Sensing voltage is fed to pin VDIN. For instance, VDOUT might be used to monitor the output of DC/DC2, realizing in this way the Power Good function for that block. VDOUT is pulled low when voltage on VDIN goes below the specified threshold. Once VDIN returns above that threshold, with a specified hysteresis, VDOUT goes back to high with a configurable delay set by a capacitor on pin LDOOKDLY

Two different packages are available. The PowerSSO-36 slug-down allows to dissipate the heat on the board and reduce the application size. The slug has to be connected to the ground plane. This is the package suggested for standard applications. When this is not enough, because the L5963 is used as pre-regulator for high consuming applications and both the 2 DC-DC are working at high currents, the PSSO36 slug-up allows the use of a heat-sink to make easier power dissipation.

2 Block diagram

Figure 1. Block diagram



3 Application diagrams

Figure 2. Example of a typical application diagram

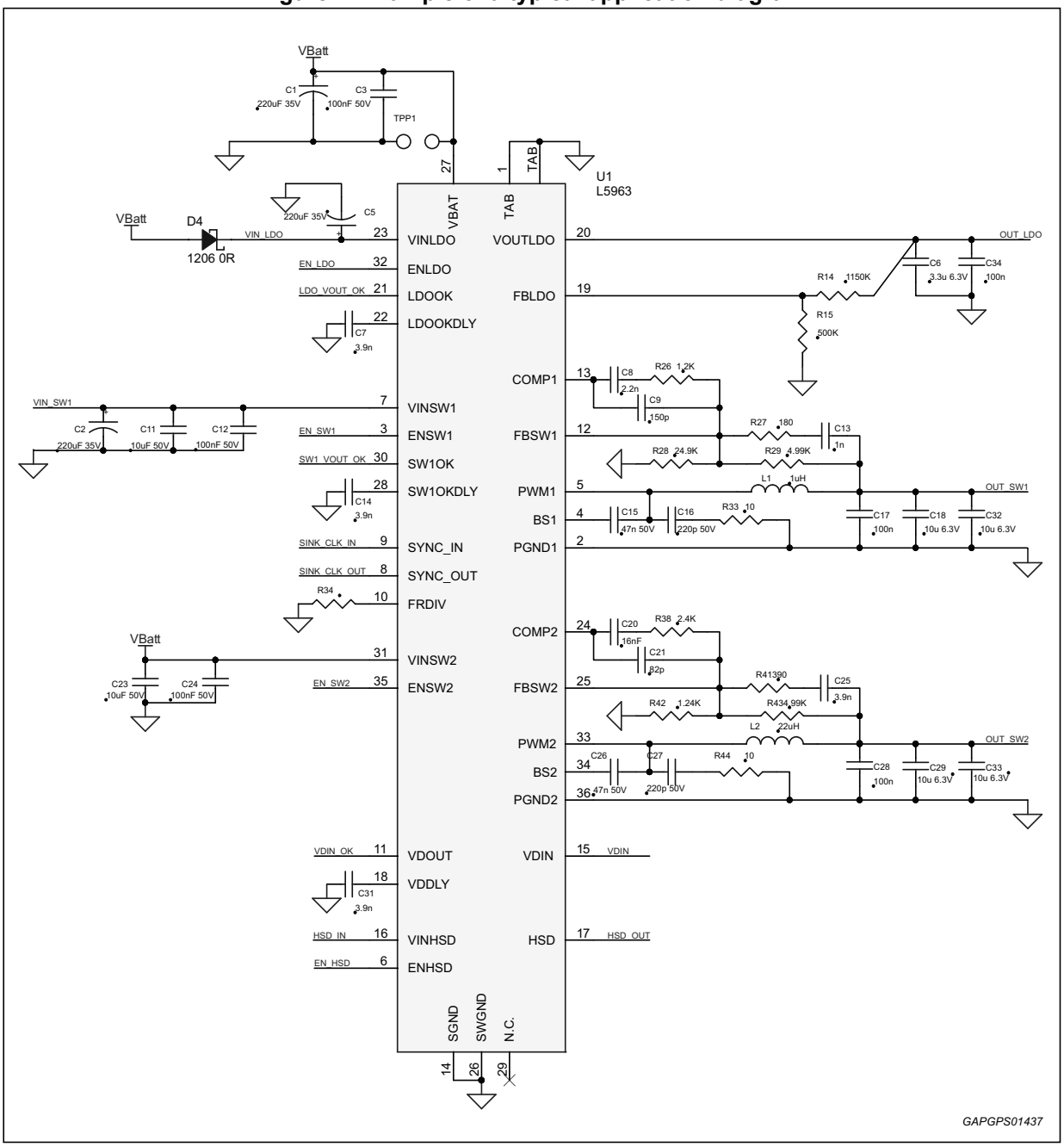
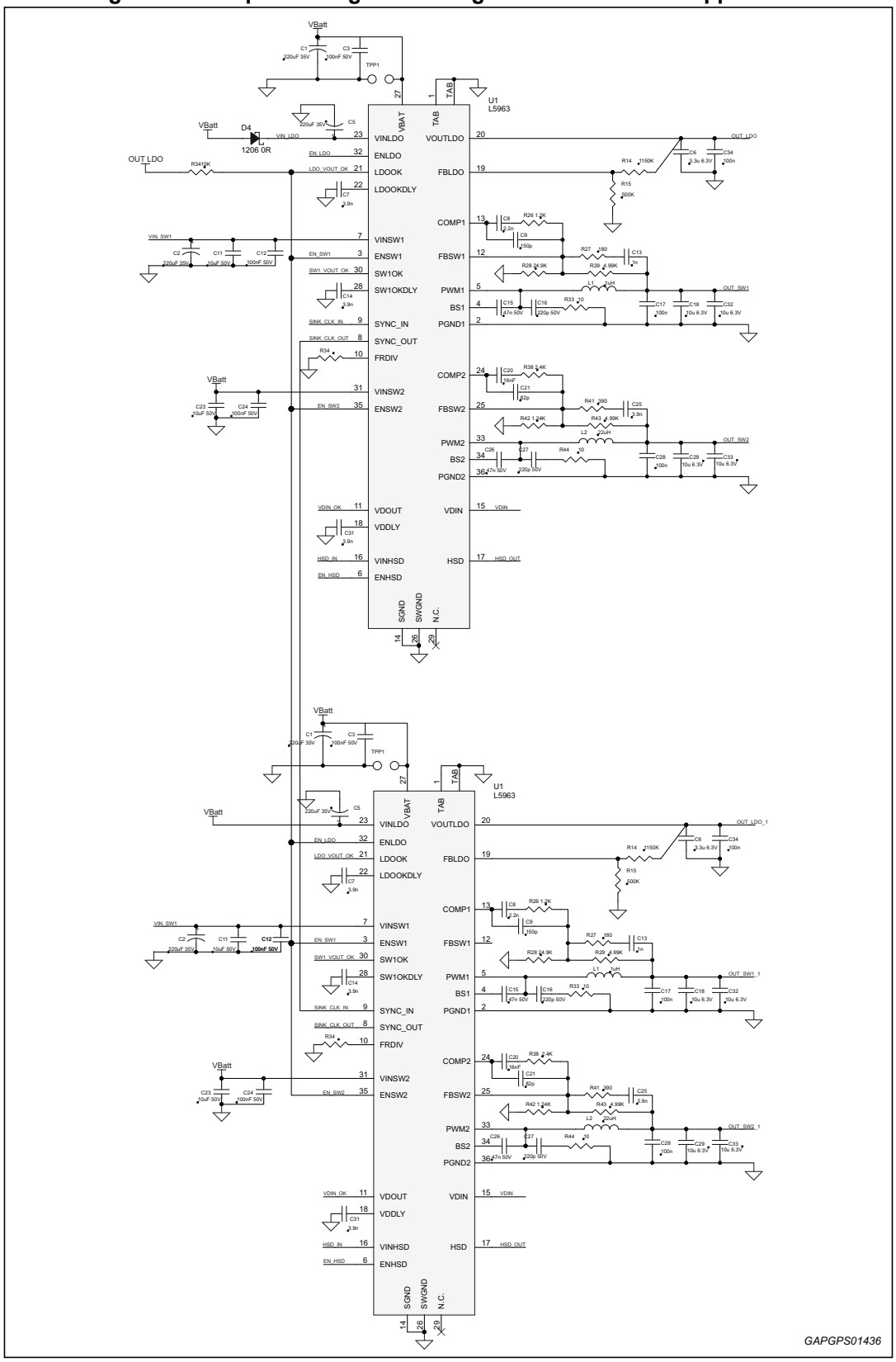


Figure 3. Example of usage of two regulators in the same application



4 Pins description

Figure 4. PowerSSO-36 pinout configuration

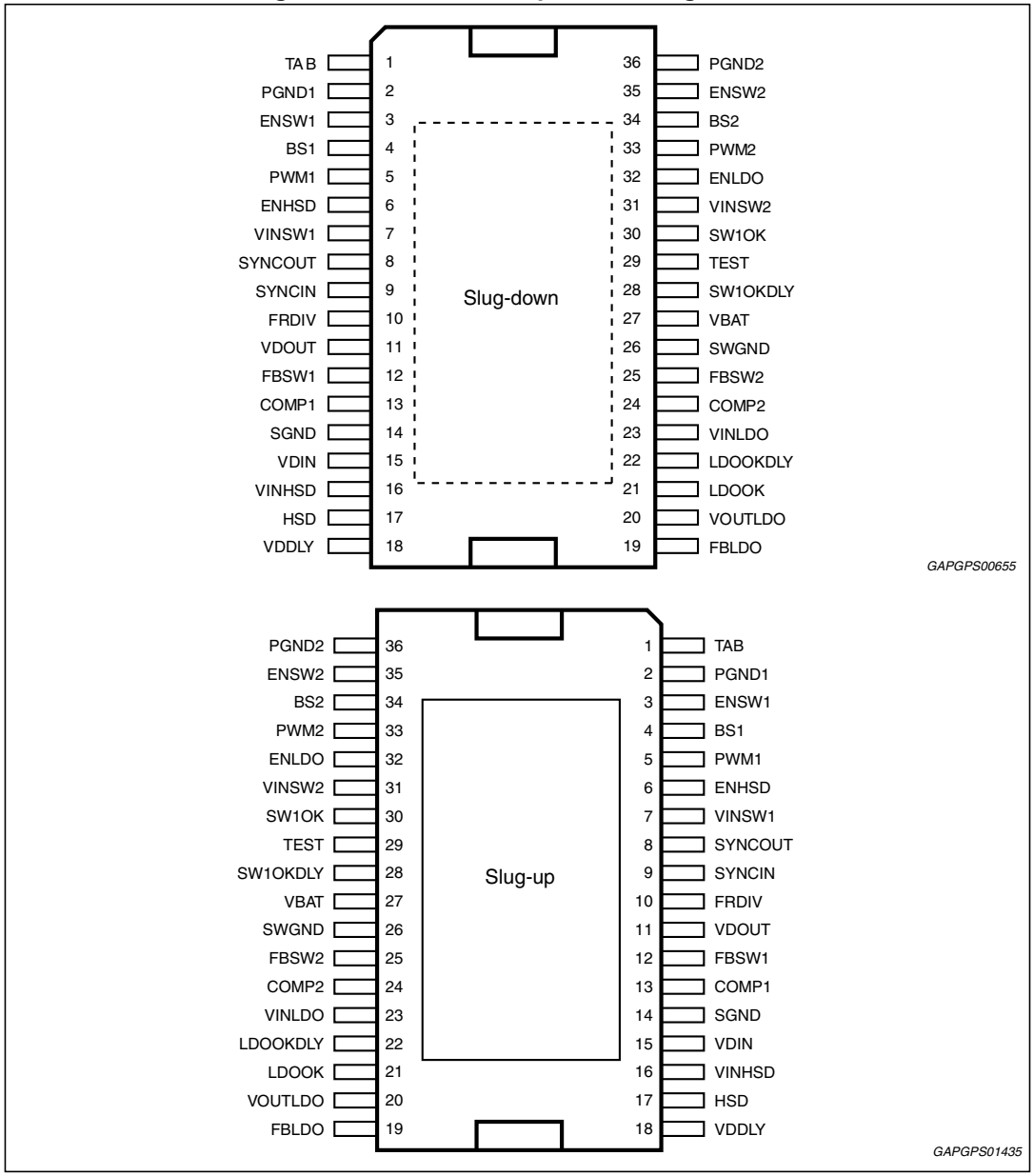


Table 2. PowerSSO-36 pins description

Pin #	Name	Type	Function
1	TAB	n.a.	Device slug terminal. To be connected to ground
2	PGND1	Ground	Switching regulator 1 power ground
3	ENSW1	Input	Switching regulator 1 enable. 1.8/3.3 V compatible
4	BS1	Supply	Switching regulator 1 boosted supply

Table 2. PowerSSO-36 pins description (continued)

Pin #	Name	Type	Function
5	PWM1	Output	Switching regulator 1 switching output
6	ENHSD	Input	Enable for High Side Driver. 1.8/3.3 V compatible
7	VINSW1	Supply	Switching regulator 1 supply voltage
8	SYNCOUT	Output	External synchronization output (push-pull)
9	SYNCIN	Input	External synchronization input
10	FRDIV	Input/output	Switching frequency divider setting
11	VDOUT	Output	Voltage detector output (open drain)
12	FBSW1	Input/output	Switching regulator 1 feedback voltage
13	COMP1	Input/output	Switching regulator 1 compensation
14	SGND	Ground	Ground for linear blocks
15	VDIN	Input	Voltage detector threshold setting
16	VINHSD	Supply	High Side Driver supply
17	HSD	Output	High Side Driver output
18	VDDLY	Input/output	Voltage Detector delay setting
19	FBLDO	Input/output	LDO feedback voltage
20	VOUTLDO	Output	LDO output
21	LDOOK	Output	LDO voltage detector output (open drain)
22	LDOOKDLY	Input/output	LDOOK delay setting
23	VINLDO	Supply	LDO supply
24	COMP2	Input/output	Switching regulator 2 compensation
25	FBSW2	Input/output	Switching regulator 2 feedback voltage
26	SWGND	Ground	Low-power switching ground
27	VBAT	Supply	Common linear blocks supply voltage
28	SW1OKDLY	Input/output	SW1OK delay setting
29	TEST	n.a.	Pin for testing purposes. To be left unconnected
30	SW1OK	Output	Switching regulator 1 voltage detector output (open drain)
31	VINSW2	Supply	Switching regulator 2 supply voltage
32	ENLDO	Input	LDO enable. 1.8/3.3 V compatible
33	PWM2	Output	Switching regulator 2 switching output
34	BS2	Supply	Switching regulator 2 boosted supply
35	ENSW2	Input	Switching regulator 2 enable. 1.8/3.3 V compatible
36	PGND2	Ground	Switching regulator 2 power ground

Figure 5. VQFPN-48 pinout configuration

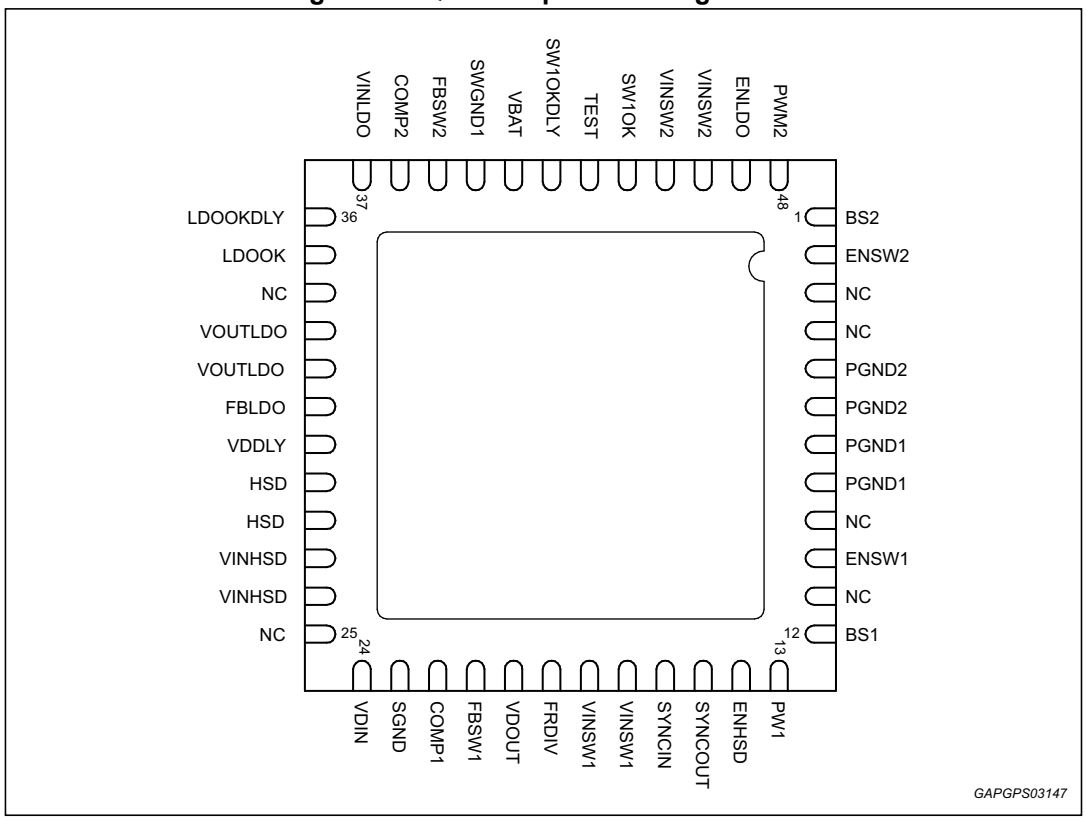


Table 3. VQFPN-48 pins description

Pin #	Name	Type	Function
1	BS2	Supply	Switching regulator 2 boosted supply
2	ENSW2	Input	Switching regulator 2 enable. 1.8/3.3 V compatible
3	NC	N.C.	Not connected
4	NC	N.C.	Not connected
5	PGND2	Ground	Switching regulator 2 power ground
6	PGND2	Ground	Switching regulator 2 power ground
7	PGND1	Ground	Switching regulator 1 power ground
8	PGND1	Ground	Switching regulator 1 power ground
9	NC	N.C.	Not connected
10	ENSW1	Input	Switching regulator 1 enable. 1.8/3.3 V compatible
11	NC	N.C.	Not connected
12	BS1	Supply	Switching regulator 1 boosted supply
13	PWM1	Output	Switching regulator 1 switching output
14	ENHSD	Input	Enable for High Side Driver. 1.8/3.3 V compatible
15	SYNCOUT	Output	External synchronization output (push-pull)

Table 3. VQFPN-48 pins description (continued)

Pin #	Name	Type	Function
16	SYNCIN	Input	External synchronization input
17	VINSW1	Supply	Switching regulator 1 supply voltage
18	VINSW1	Supply	Switching regulator 1 supply voltage
19	FRDIV	Input/output	Switching frequency divider setting
20	VDOUT	Output	Voltage detector output (open drain)
21	FBSW1	Input/output	Switching regulator 1 feedback voltage
22	COMP1	Input/output	Switching regulator 1 compensation
23	SGND	Ground	Ground for linear blocks
24	VDIN	Input	Voltage detector threshold setting
25	NC	N.C.	Not connected
26	VINHSD	Supply	High Side Driver supply
27	VINHSD	Supply	High Side Driver supply
28	HSD	Output	High Side Driver output
29	HSD	Output	High Side Driver output
30	VDDLY	Input/output	Voltage Detector delay setting
31	FBLDO	Input/output	LDO feedback voltage
32	VOUTLDO	Output	LDO output
33	VOUTLDO	Output	LDO output
34	NC	N.C.	Not connected
35	LDOOK	Output	LDO voltage detector output (open drain)
36	LDOOKDLY	Input/output	LDOOK delay setting
37	VINLDO	Supply	LDO supply
38	COMP2	Input/output	Switching regulator 2 compensation
39	FBSW2	Input/output	Switching regulator 2 feedback voltage
40	SWGND1	Ground	Low-power switching ground
41	VBAT	Supply	Common linear blocks supply voltage
42	SW1OKDLY	Input/output	SW1OK delay setting
43	TEST	n.a.	Pin for testing purposes. To be left unconnected
44	SW1OK	Output	Switching regulator 1 voltage detector output (open drain)
45	VINSW2	Supply	Switching regulator 2 supply voltage
46	VINSW2	Supply	Switching regulator 2 supply voltage
47	ENLDO	Input	LDO enable. 1.8/3.3 V compatible
48	PWM2	Output	Switching regulator 2 switching output

5 Electrical specifications

5.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Pin name / symbol	Parameter	Value	Unit
$VBAT_{OP}$ VIN_{OP}	Operating input voltage	-0.3 to +26	V
$VBAT_{MAX}$ VIN_{MAX}	Maximum transient supply voltage	-0.3 to +40	V
PGND1/2, SGND, SWGND, TAB	Ground pins voltage	-0.3 to +0.3	V
ENLDO	LDO enable pin voltage	-0.3 to +40	V
V_{pinop}	Other pins operating voltage	-0.3 to +3.6	V
V_{pinmax}	Other pins voltage	-0.3 to +4.6	V
T_{op}	Operating ambient temperature range	-40 to +105	°C
T_{stg}	Storage temperature range	-55 to +150	°C
T_j	Junction temperature	150	°C

5.2 Thermal data

Table 5. Thermal data (PowerSSO-36)

Symbol	Parameter	Board	Value	Unit
$R_{th\ j\text{-}a\text{-}2s}$	Thermal resistance junction-to-ambient (Max) (slug down configuration)	2s	53	°C/W
$R_{th\ j\text{-}a\text{-}2s2p}$		2s2p	27	°C/W
$R_{th\ j\text{-}a\text{-}2s2pv}$		2s2p+vias	22	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case (Max)		1.5	°C/W

Table 6. Thermal data (VQFPN-48)

Symbol	Parameter	Board	Value	Unit
$R_{th\ j\text{-}a\text{-}2s}$	Thermal resistance junction-to-ambient (Max)	2s	66	°C/W
$R_{th\ j\text{-}a\text{-}2s2p}$		2s2p	32	°C/W
$R_{th\ j\text{-}a\text{-}2s2pv}$		2s2p+vias	26	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case (Max)		2.2	°C/W

5.3 Electrical characteristics

VBAT = VIN = 14.4 V, T_{amb} = 25 °C unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Inputs and controls						
$VBAT_{OP}$	VBAT operating range	Standby mode VOUTLDO = 1.2 V/100 mA VOUTLDO = 3.3 V/100 mA	 3.5 4	 - -	 26 26	 V V
I_q	Total quiescent current	Shutdown mode	-	1.5	2	µA
		Standby mode; $Iload_{LDO}$ = 100 µA	-	23	28	
OV_{VBAT}	Overvoltage shut-down threshold on VBAT	VBAT rising	27	29	31	V
UV_{VBAT}	Undervoltage shut-down threshold on VBAT	VBAT falling VDOUT forced to 0 V	2.7	3	3.3	V
Hys_{UV}	Hysteresis on UV_{VBAT}	-	-	0.1	0.5	V
ENmin	Min voltage for enable pins high level	-	1.6	-	-	V
ENmax	Max voltage for enable pins low level	-	-	-	1	V
R_{FRDIV}	Thresholds of value of resistor connected between FRDIV pin and ground	fsw_{SW2} = fsw_{SW1}	0	-	30	kΩ
		fsw_{SW2} = $fsw_{SW1/2}$	60	-	70	
		fsw_{SW2} = $fsw_{SW1/4}$	110	-	115	
		fsw_{SW2} = $fsw_{SW1/8}$	180	-	∞	
Voltage detector						
THR_{VDIN}	Voltage Detector input voltage threshold	-	0.9	0.94	0.98	V
Hys_{VDIN}	Voltage Detector input voltage hysteresis	-	-	30	40	mV
$Vmax_{VDOUT}$	VDOUT saturation voltage	I = 1 mA in VDOUT pin	-	-	0.1	V
I_{VDDLY}	VDDLY output current	-	6	9	12	µA
THR_{VDDLY}	VDDLY threshold	-	2.1	2.3	2.5	V
Linear regulator						
V_{FBLDO}	Feedback voltage	I_{load} = 100 mA	990	1000	1010	mV
UV_{LDO}	Undervoltage shut-down threshold on LDO	VINLDO decreasing	-	2.2	2.4	V
Hys_{LDO}	Hysteresis on UVLDO	-	-	-	100	mV
LdR_{LDO}	FBLDO load regulation	10 mA < I_{load} < 250 mA	-	5	-	mV
LnR_{LDO}	FBLDO line regulation	3.5 < VINLDO < 26 V Iload = 100 mA	-	1	-	mV

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ΔV_{FBLDO} / V_{FBLDO}	FBLDO Undershoot/overshoot(1)	5 mA ↔ 250 mA Iload transition	-5	-	5	%
		8 ↔ 18 V VINLDO transition	-5	-	5	
Vdo_{LDO}	Drop-out voltage	VOUTLDO = 3.3 V Iload = 250 mA VOUTLDO decreasing of 100 mV	-	270	320	mV
$Ishort_{LDO}$	Short circuit current limit	VOUTLDO shorted to ground	-	350	420	mA
$Ishort_{ST-BY}$		VOUTLDO (st-by) shorted to ground	-	65	80	mA
$PSRR_{LDO}$	Power supply rejection ratio	Iload = 50 mA, 10 Hz < f < 10 kHz 1 Vac_{pp} on VINLDO	-	70	-	dB
n_{LDO}	Output noise	20 Hz < f < 20 kHz Iload = 5 mA	-	100	-	µV
TSD_{LDO}	Thermal shut-down temperature	Temperature rising	150	160	-	°C
Hys_{TSDLDO}	Hysteresis on thermal shutdown temperature	-	5	-	15	°C
Co	Output capacitance(1)	-	3	-	-	µF
ESR	Output capacitor ESR(1)	-	-	-	0.2	Ω
Voltage detector on LDO						
THR_{LDOOK} / V_{FBLDO}	LDOOK threshold as percentage of FBLDO voltage	-	91	94	97	%
Hys_{LDOOK}	Hysteresis on LDOOK	-	-	90	-	mV
$Vmax_{LDOOK}$	LDOOK saturation voltage	I = 1 mA in LDOOK pin	-	-	0.2	V
$Tglitch_{LDOOK}$	Glitch filter time for LDO-OK	-	5	12	20	µs
$I_{LDOOKDLY}$	LDOOKDLY output current	-	7	10	13	µA
$THR_{LDOOKDLY}$	LDOOKDLY threshold	-	2	2.2	2.4	V
Switching regulators(2)						
V_{FBSWx}	Feedback voltage	I_{load} = 100 mA	980	1000	1020	mV
LdR_{SWx}	FBSWx load regulation(3)	50 mA < I_{load} < 1 A	-	1	-	mV
LnR_{SWx}	FBSWx line regulation(3)	3.5 V < VINSWx < 26 V	-	1	-	mV
UV_{SW1}	Undervoltage shut-down threshold on SW1	VINSWx decreasing	-	2.8	3	V
Hys_{SW1}	Hysteresis on UV_{SW1} (3)	-	-	0.15	-	V
UV_{SW2}	Undervoltage shut-down threshold on SW2	VINSWx decreasing	-	2.8	3	V
Hys_{SW2}	Hysteresis on UV_{SW2} (3)	-	-	0.15	-	V
ΔV_{FBSWx} / V_{FBSWx}	FBSWx pin undershoot/overshoot(3)	500 mA ↔ 1.5 A Iload transition	-5	-	5	%
		8 ↔ 18 V VINSWx transition	-5	-	5	%

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$Ilim_{SW1}$	Peak current limitation on sw1	-	2.5	3	3.5	A
$Ilim_{SW2}$	Peak current limitation on sw2	-	3	3.5	4	A
fsw	Free-run switching frequency	-	225	250	275	kHz
fsync	Switching frequency range(3)	50% duty-cycle wave on SYNC pin	250	-	2000	kHz
Ron_{HS}	High side MOS on resistance(3)	VINSWx > 3.5 V; including bonding wires	-	85	-	mΩ
Ron_{LS}	Low side MOS on resistance(3)	Including bonding wires	-	105	-	mΩ
η	Efficiency(3)	Free run frequency VOUTSW1/2 = 5 V; Iload = 2.5 A VOUTSW1/2 = 5 V; Iload = 1 A	-	 90 93	-	%
$\Delta V_{FBSWx} / \Delta t$	FB pin slope at turn-on(3)	Including bonding wires	-	0.95	-	V/ms
TSD_{SWx}	Thermal shutdown temperature	Temperature rising	150	160	-	°C
Hys_{TSDSWx}	Hysteresis on thermal shutdown temperature	-	5	-	15	°C
THR_{SW1OK} / V_{FBSW1}	SW1OK threshold as percentage of FBSW1 voltage	-	91	94	97	%
Hys_{SW1OK}	Hysteresis on SW1OK	-	-	35	50	mV
$Vmax_{SW1OK}$	SW1OK saturation voltage	I = 1 mA in SW1OK pin	-	-	0.2	V
$Tglitch_{SW1OK}$	Glitch filter time for SW1-OK	-	9	13	17	µs
$I_{SW1OKDLY}$	SW1OKDLY output current	-	6	10	13	µA
$THR_{SW1OKDLY}$	SW1OKDLY threshold	-	2	2.2	2.4	V
t_{on-min}	Minimum on time(3)	-	-	20	-	ns
High side driver						
$Vdrop_{HSD}$	Output saturation	I_{load} = 0.5 A	-	140	170	mV
$Ishort_{HSD}$	Short circuit current limit	-	0.7	1	1.3	A
TSD_{HSD}	Thermal shut-down temperature	Temperature rising	150	160	-	°C
Hys_{TSDHSD}	Hysteresis on thermal shutdown temperature	-	5	-	15	°C

1. Not tested at ATE.
2. Tests involving switching frequencies higher than 1 MHz are guaranteed by design.
3. Test guaranteed by application measurements.

Figure 6. PSRR LDO 50 mA load vs. frequency

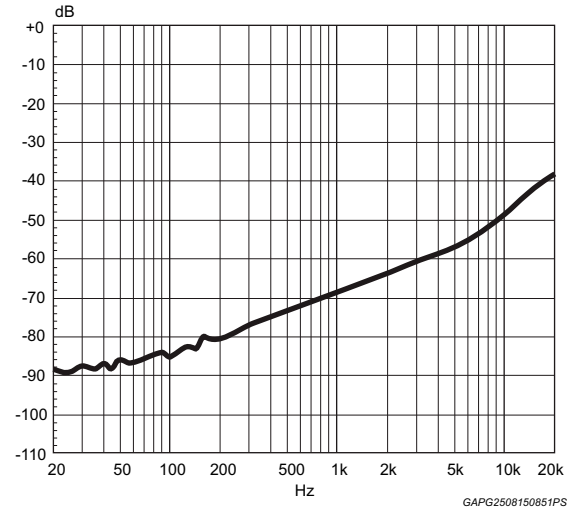


Figure 7. Efficiency vs. output current (VIN = 14 V, fsw = 2 MHz)

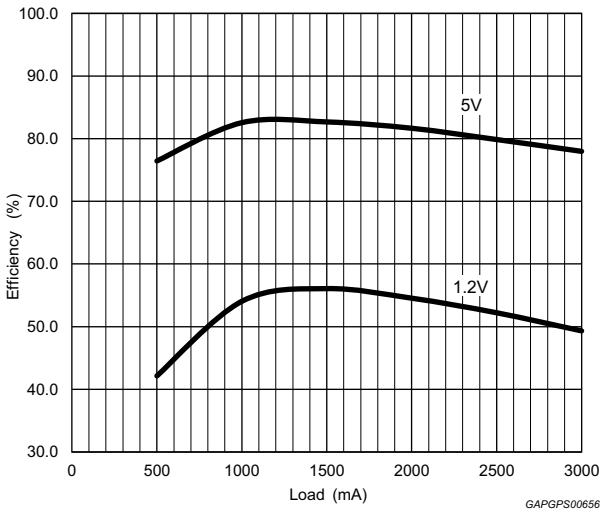
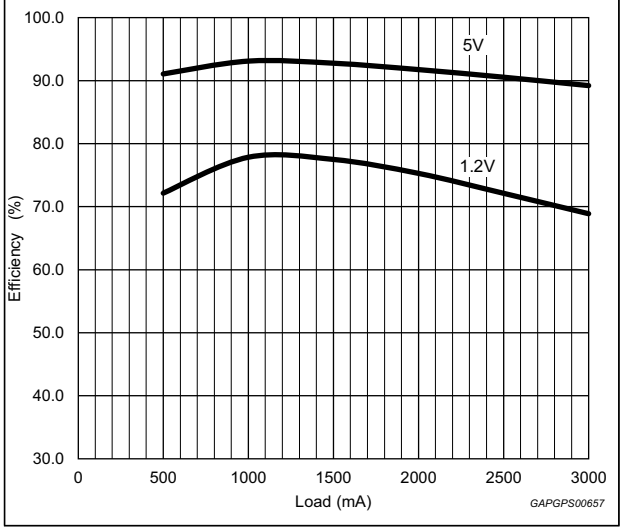


Figure 8. Efficiency vs. output current (VIN = 14 V, fsw = 250 kHz)



6 Functional Description

6.1 Operative modes

L5963 has three main operative modes:

- Shutdown mode: all enable pins are low and the device is completely off. In this condition the quiescent current is typically 1.5 µA.
- Standby mode: the linear regulator is configured as stand-by regulator by connecting ENLDO directly to VINLDO. In this condition the quiescent current is typically 25 µA.
- Normal mode: the linear regulator works as LDO and/or other blocks (DC/DC or HSD) are turned on.

6.2 Blocks functional description

6.2.1 Unregulated supply input voltage (VINLDO)

This terminal provides the power for internal circuitry to bias band-gap reference, standby regulator and other circuitry in the device.

If backup function is needed, an external capacitor connected to this pin shall be charged through an external diode which is used to block reverse discharging. With backup function, when the system battery is removed or drops too low suddenly, the internal bias and regulator can operate correctly for a certain time, which avoids MCU to work abnormally and allows MCU to have enough time to turn-off.

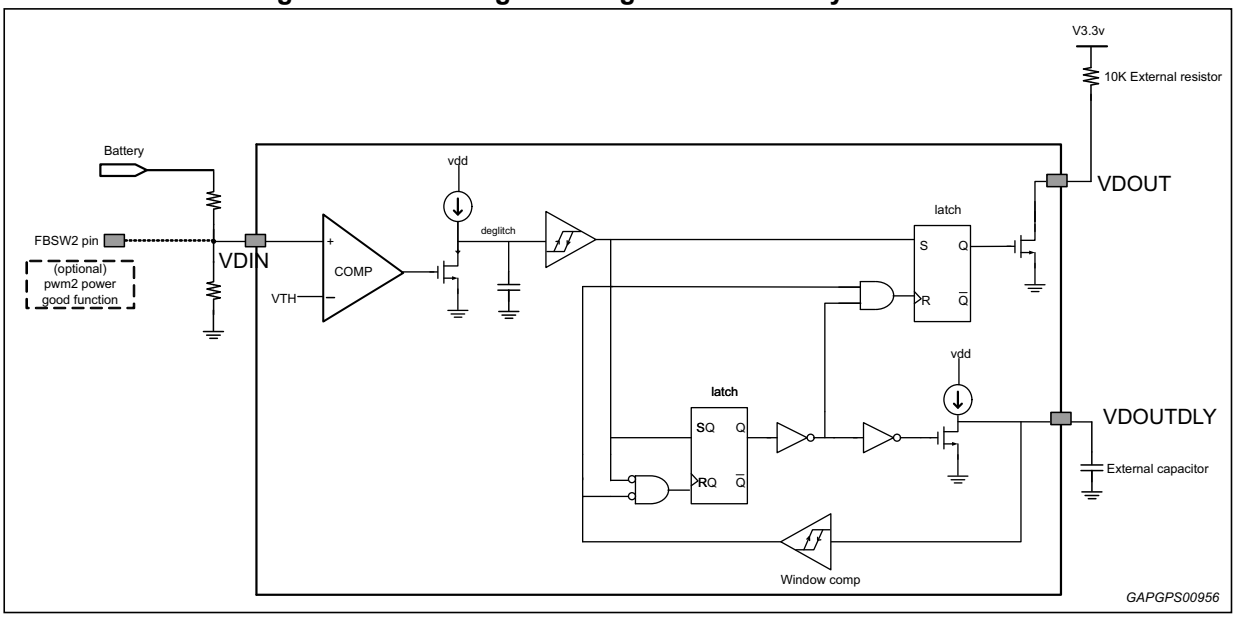
6.2.2 Low voltage warning monitor (related pins: VDIN, VDOUT, VDDLY)

An external voltage can be sensed through the VDIN pin. This voltage is scaled using an external resistor network and compared with an internal threshold to detect a low voltage condition (*Figure 9.*). Once the input voltage is below the threshold, the low voltage warning output terminal (VDOUT) is pulled low after the designed glitch-filtering (~12 µs). VDOUT is an open drain output. If the input returns above the threshold with the specified hysteresis, VDOUT is released after a defined delay, determined by the capacitor on pin VDDLY. The threshold is fixed to 0.95 V typ.

The capacitor on VDDLY pin sets VDOUT delay. A current source (~9 µA) on this pin charges the external capacitor to generate the required delay, programmable by adjusting the value of the capacitor.

This voltage monitor can also be used to monitor DC/DC2 output. Changing the ratio of the external resistor divider the low voltage warning threshold can be adjusted.

Figure 9. Low voltage warning monitor & delay schematic



6.2.3 Power-good reset (related pins: LDOOK, LDOOKDLY)

LDOOK monitors the regulator output VOUTLDO. Its circuit topology is the same as the voltage detector one (*Figure 9*). Its threshold is fixed to 95% typ of the feedback voltage, and the hysteresis is always ~2% typ. Pin LDOOK is an open drain output, and pin LDOOKDLY is used to adjust the delay in the release of LDOOK output.

6.2.4 Power-good function of DC/DC1 (related pins: SW1OK, SW1OKDLY)

SW1OK monitors DC/DC1 output. Its circuit topology is the same as the voltage detector one (*Figure 9*). Its threshold can't be adjusted, it is always 95% typ of the feedback voltage, and the hysteresis is ~35mV typ. Pin SW1OK is an open drain output, and pin SW1OKDLY is used to adjust its delay.

6.2.5 Over voltage shutdown

Two internal over voltage shutdown (OV) blocks are included in L5963. One (OV1) senses VBAT pin, the other (OV2) detects VINLDO pin.

If VBAT gets too high, to prevent any damage, DC/DC1, DC/DC2 and the high-side driver are disabled by OV1. They will be turned on once VBAT returns below the detection threshold with the specified hysteresis.

If the linear regulator works as a non-standby regulator and VINLDO gets too high, to prevent any damage the LDO is disabled by OV2. It is turned on once VINLDO returns below the detection threshold with the specified hysteresis.

On the contrary, the linear regulator works as a standby regulator, OV2 doesn't intervene and the regulator continues to work even if VINLDO increases.

6.2.6 Power ground (PGND1 and PGND2)

PGND1 pin and PGND2 pin are power ground references for the DC/DC1 and DC/DC2 respectively. All switching nodes are referred to these two pins.

6.2.7 Signal ground (SGND)

This pin is the ground reference for standby regulator, HSD and internal bias.

6.2.8 PWM signal ground (SWGND)

This pin is the ground reference for signal part of DC/DC1 and DC/DC2.

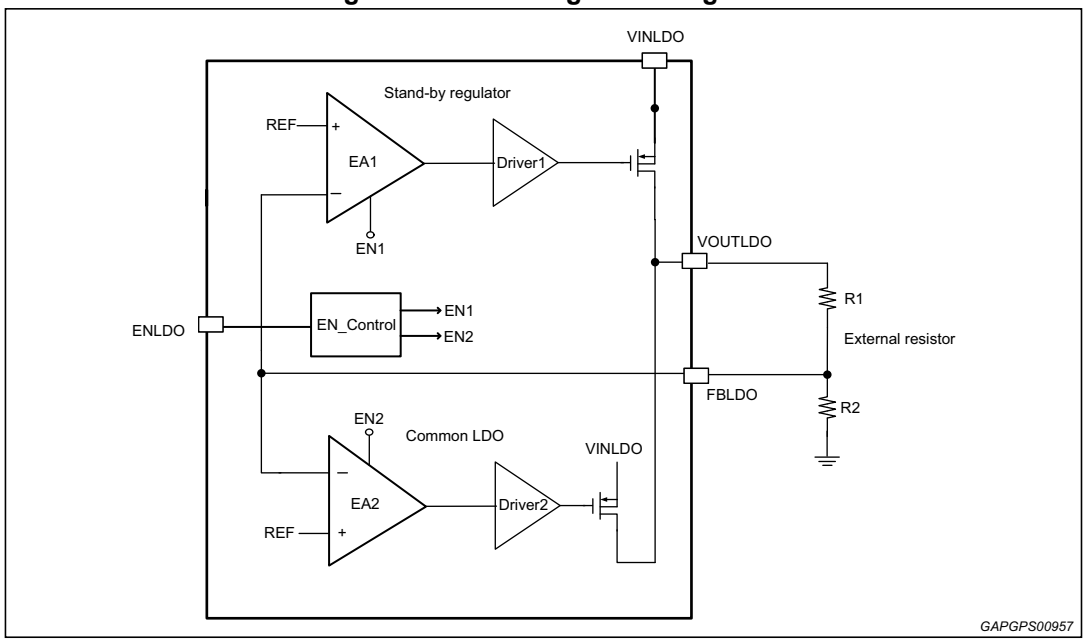
6.2.9 TAB

TAB is connected to the device substrate.

This pin must be connected to GND to guarantee the substrate is always at the lowest potential to avoid parasitic activation.

6.2.10 Linear regulator

Figure 10. Linear regulator diagram



The linear regulator has two operative modes: standby mode and non-standby mode. Its output voltage is set by an external resistor divider through the feedback pin FBLDO.

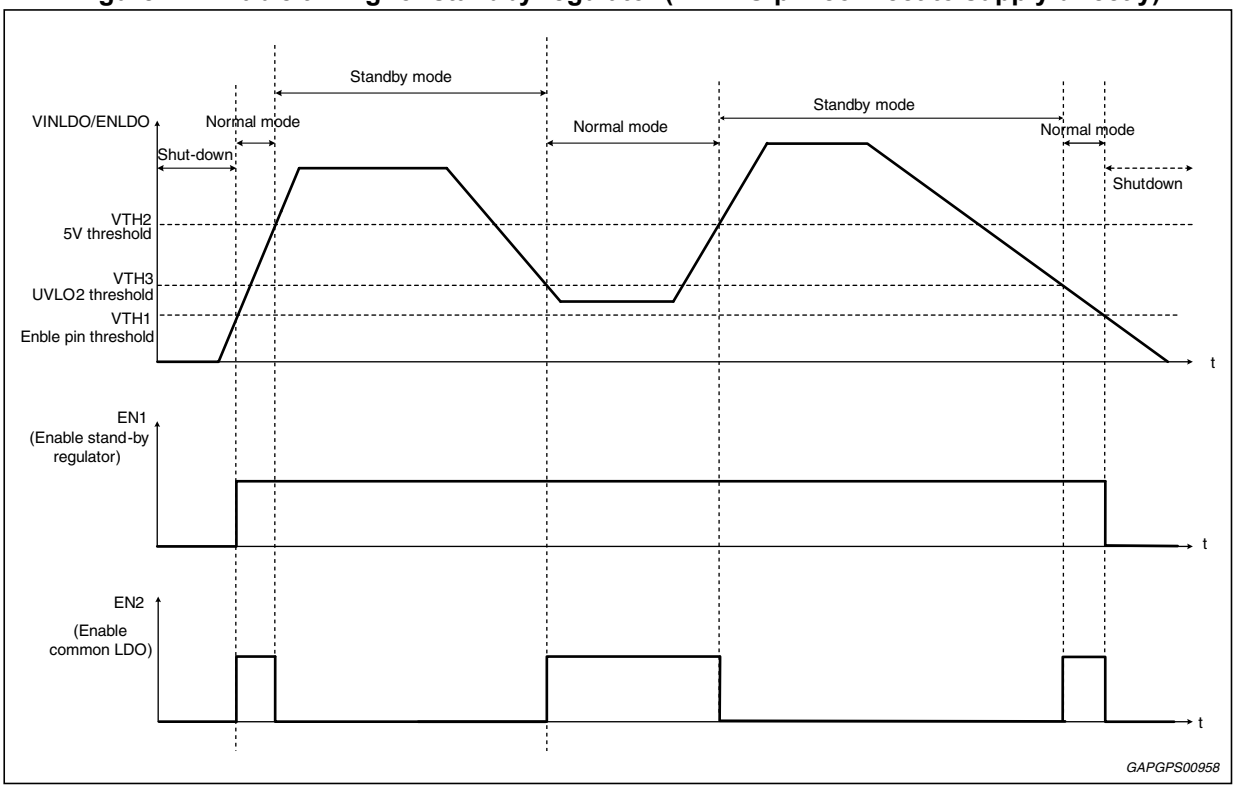
As a standby regulator, the current capability is reduced to 50 mA and the quiescent current minimized.

In this case, the external resistor divider should be in the Mega ohm order to reduce total quiescent current.

As a non standby regulator, it has higher load capability (up to 250 mA).

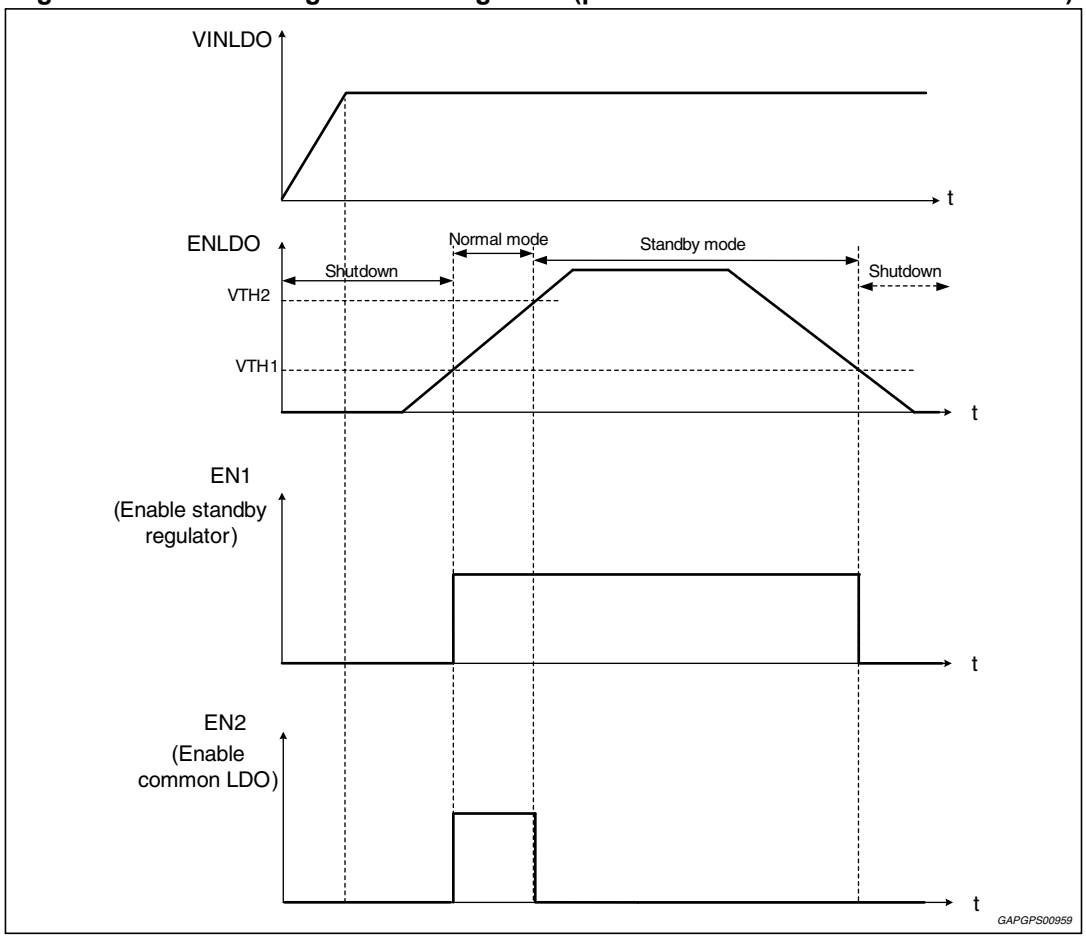
Connecting ENLDO pin directly to its supply VINLDO (it should be higher than 5 V), the regulator works as a standby regulator. Once ENLDO is ever higher than 5 V, the regulator works as a standby regulator till VINLDO is powered down, to reset a flag stored in an internal register.

Figure 11. Enable timing for standby regulator (ENLDO pin connect to supply directly)



The linear regulator works as a non-standby regulator if ENLDO is <5 V.

Figure 12. Enable timing for linear regulator (pin ENLDO isn't connected to VINLDO)



The linear regulator operates with output voltages down to 1.2 V, and offers a maximum dropout voltage of 500 mV at rated load current.

This regulator has an independent thermal protection and a current-limiting circuit.

It should be always supplied (by VINLDO) with a voltage not lower than 3.5 V because, even if not used, it gives the common supply to all internal blocks which have to stay alive when the battery drops too low (backup functionality).

6.2.11 High-side driver (HSD)

The HSD pin is the output of the high side driver. It has a dedicated enable pin ENHSD. Following protections are implemented:

- Over-current protection
- Short to supply
- Short to ground
- Short through the load to -1 V
- Unpowered short to supply
- Loss of ground
- Over voltage protection

Thermal protection

The HSD has an independent thermal shutdown protection.

If the local die temperature exceeds the thermal shutdown detection threshold, the HSD is disabled. It is enabled once the local die temperature falls below the detection threshold with the specified hysteresis. The invoking of thermal shut down on HSD does not directly affect any other outputs or circuitry in the IC.

Short to ground

The high side driver output is protected against shorts to ground. The faulted output returns to its pre-fault operating condition once the fault is removed.

Short to supply

The high-side driver is protected against shorts to battery. In such an event, the IC is not damaged. External components connected directly to the IC are not damaged by such exposure.

Loss of ground protection

The high side driver is protected against excessive leakage current to an external ground during a loss of supply ground (i.e. ground is open). During this event, the HSD is disabled and the IC is not damaged.

Loss of battery protection (Unpowered shorts to battery, SPU)

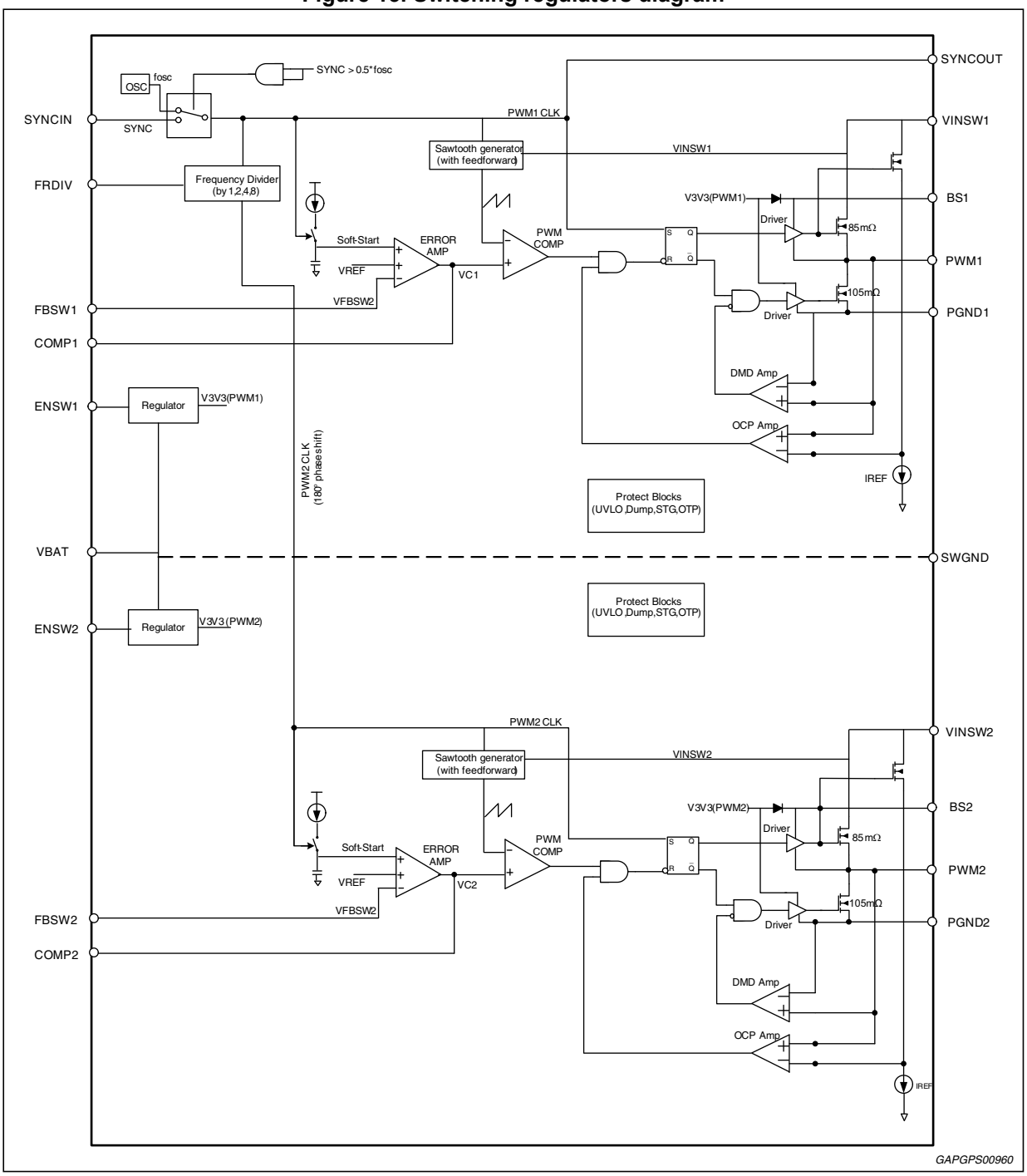
The high-side driver is protected against unpowered shorts to battery. In such an event, in typical applicative conditions, the IC will not suffer any damage.

Below-ground protection

The HSD output can be brought below ground by the inductive load. In this case, Power PMOS is turned on to charge the output, protecting itself.

6.2.12 Switching regulators

Figure 13. Switching regulators diagram



L5963 embeds two synchronous DC/DC converters that incorporate all the control and necessary protection circuitries to satisfy a wide range of applications. DC/DC1 and DC/DC2 are enabled by pin ENSW1 and pin ENSW2 respectively. The two switching converters employ voltage mode control and feed forward function to provide good load regulation and line regulation.