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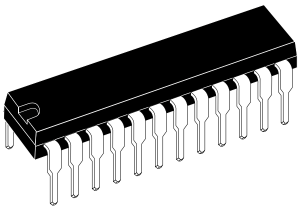
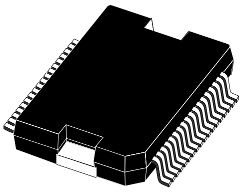
DMOS dual full bridge driver

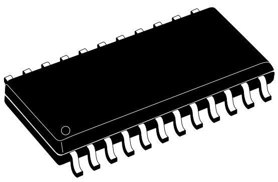
Datasheet - production data



PowerDIP24 (20 + 2 + 2)



PowerSO36



SO24 (20 + 2 + 2)

Ordering numbers:
L6206N (PowerDIP24)
L6206PD (PowerSO36)
L6206D (SO24)

Features

- Operating supply voltage from 8 to 52 V
- 5.6 A output peak current (2.8 A DC)
- $R_{DS(ON)}$ 0.3 Ω typ. value at T_j = 25 °C
- Operating frequency up to 100 KHz
- Programmable high-side overcurrent detection and protection
- Diagnostic output
- Paralleled operation
- Cross conduction protection
- Thermal shutdown
- Undervoltage lockout
- Integrated fast freewheeling diodes

Applications

- Bipolar stepper motor
- Dual or quad DC motor

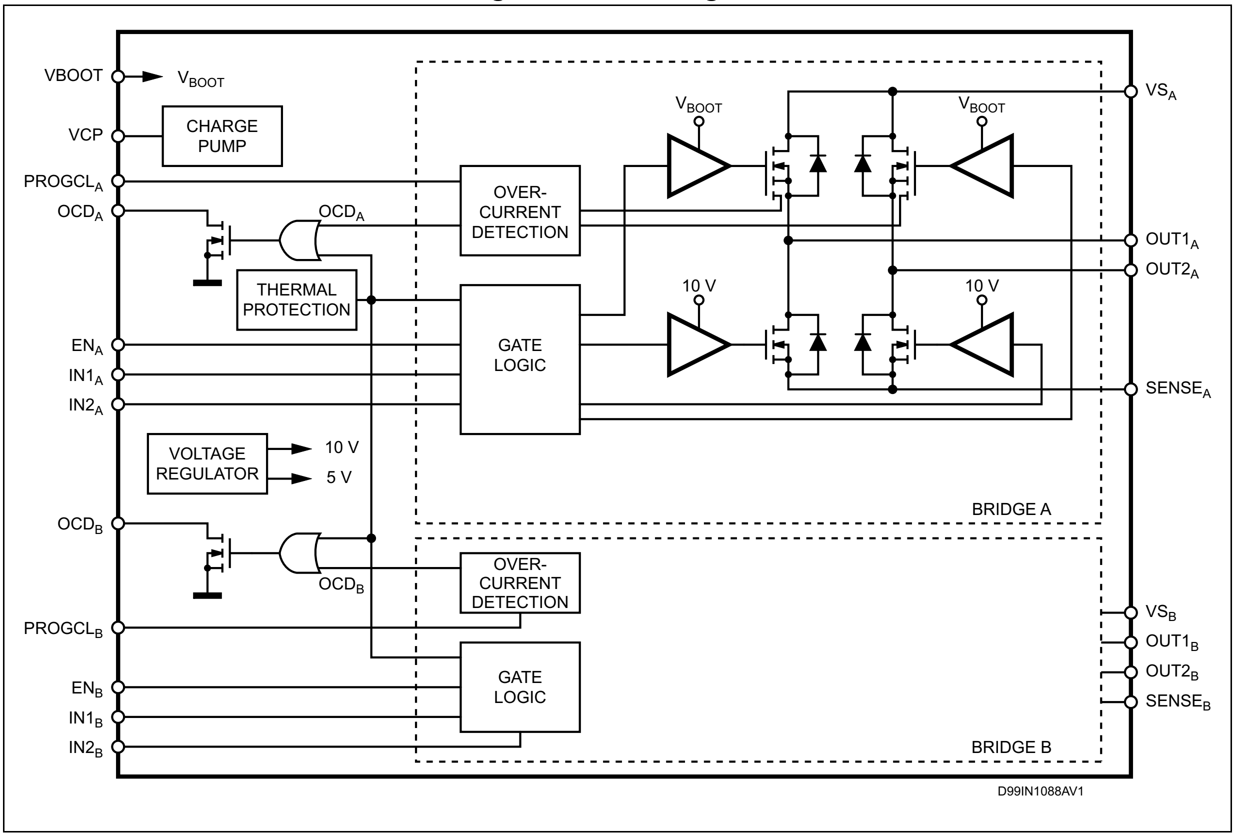
Description

The L6206 device is a DMOS dual full bridge designed for motor control applications, realized in BCD technology, which combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip. Available in the PowerDIP24 (20 + 2 + 2), PowerSO36 and SO24 (20 + 2 + 2) packages, the L6206 device features thermal shutdown and a non-dissipative overcurrent detection on the high-side Power MOSFETs plus a diagnostic output that can be easily used to implement the overcurrent protection.

Contents

1 Block diagram

Figure 1. Block diagram



2 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60$ V; $V_{SENSEA} = V_{SENSEB} =$ GND	60	V
OCD_A,OCD_B	OCD pins voltage range	-	-0.3 to +10	V
$PROGCL_A$, $PROGCL_B$	PROGCL pins voltage range	-	-0.3 to +7	V
V_{BOOT}	Bootstrap peak voltage	$V_{SA} = V_{SB} = V_S$	V_S + 10	V
V_{IN}, V_{EN}	Input and enable voltage range	-	-0.3 to +7	V
V_{SENSEA}, V_{SENSEB}	Voltage range at pins $SENSE_A$ and $SENSE_B$	-	-1 to +4	V
$I_{S(peak)}$	Pulsed supply current (for each V_S pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$; $t_{PULSE} < 1$ ms	7.1	A
I_S	RMS supply current (for each V_S pin)	$V_{SA} = V_{SB} = V_S$	2.8	A
T_{stg}, T_{OP}	Storage and operating temperature range	-	-40 to 150	°C

Table 2. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$	-	52	V
V_{SENSEA}, V_{SENSEB}	Voltage range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$) (DC)	-6 -1	6 1	V V
I_{OUT}	RMS output current	-		2.8	A
T_j	Operating junction temperature	-	-25	+125	°C
f_{sw}	Switching frequency	-		100	KHz

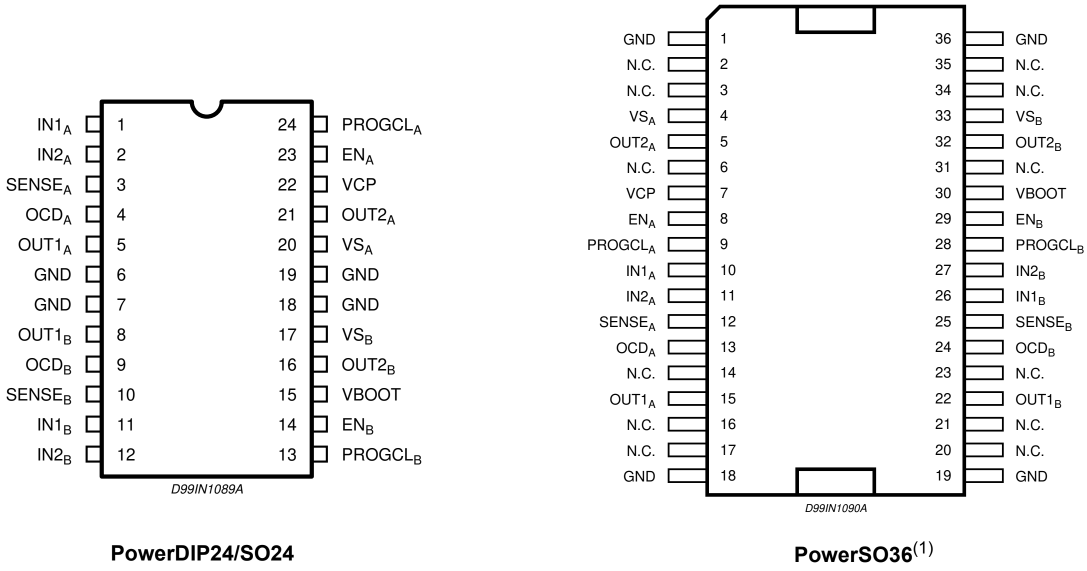
Table 3. Thermal data

Symbol	Description	PowerDIP24	SO24	PowerSO36	Unit
$R_{th\text{-}j\text{-}pins}$	Maximum thermal resistance junction pins	18	14	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum thermal resistance junction case	-	-	1	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum thermal resistance junction ambient(1)	43	51	-	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum thermal resistance junction ambient(2)	-	-	35	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum thermal resistance junction ambient(3)	-	-	15	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum thermal resistance junction ambient(4)	58	77	62	°C/W

1. Mounted on a multilayer FR4 PCB with a dissipating copper surface on the bottom side of 6 cm^2 (with a thickness of 35 µm).
2. Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm).
3. Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer.
4. Mounted on a multilayer FR4 PCB without any heatsinking surface on the board.

3 Pin connections

Figure 2. Pin connections (top view)



1. The slug is internally connected to pins 1, 18, 19 and 36 (GND pins).

Table 4. Pin description

Package		Name	Type	Function
SO24/PowerDIP24	PowerSO36			
Pin no.	Pin no.			
1	10	$IN1_A$	Logic input	Bridge A logic input 1.
2	11	$IN2_A$	Logic input	Bridge A logic input 2.
3	12	$SENSE_A$	Power supply	Bridge A source pin. This pin must be connected to power ground directly or through a sensing power resistor.
4	13	OCD_A	Open drain output	Bridge A overcurrent detection and thermal protection pin. An internal open drain transistor pulls to GND when overcurrent on bridge A is detected or in case of thermal protection.
5	15	$OUT1_A$	Power output	Bridge A output 1.
6, 7, 18, 19	1, 18, 19, 36	GND	GND	Signal ground terminals. In PowerDIP and SO packages, these pins are also used for heat dissipation toward the PCB.
8	22	$OUT1_B$	Power output	Bridge B output 1.

Table 4. Pin description (continued)

Package		Name	Type	Function
SO24/PowerDIP24	PowerSO36			
Pin no.	Pin no.			
9	24	OCD_B	Open drain output	Bridge B overcurrent detection and thermal protection pin. An internal open drain transistor pulls to GND when overcurrent on bridge B is detected or in case of thermal protection.
10	25	$SENSE_B$	Power supply	Bridge B source pin. This pin must be connected to power ground directly or through a sensing power resistor.
11	26	$IN1_B$	Logic input	Bridge B input 1
12	27	$IN2_B$	Logic input	Bridge B input 2
13	28	$PROGCL_B$	R pin	Bridge B overcurrent level programming. A resistor connected between this pin and ground sets the programmable current limiting value for the bridge B. By connecting this pin to ground the maximum current is set. This pin cannot be left non-connected.
14	29	EN_B	Logic input	Bridge B Enable. LOW logic level switches OFF all Power MOSFETs of Bridge B. If not used, it has to be connected to +5 V.
15	30	VBOOT	Supply voltage	Bootstrap voltage needed for driving the upper Power MOSFETs of both bridge A and bridge B.
16	32	$OUT2_B$	Power output	Bridge B output 2.
17	33	VS_B	Power supply	Bridge B power supply voltage. It must be connected to the supply voltage together with pin VS_A.
20	4	VS_A	Power supply	Bridge A power supply voltage. It must be connected to the supply voltage together with pin VS_B.
21	5	$OUT2_A$	Power output	Bridge A output 2.
22	7	VCP	Output	Charge pump oscillator output.
23	8	EN_A	Logic input	Bridge A enable. LOW logic level switches OFF all Power MOSFETs of bridge A. If not used, it has to be connected to +5 V.
24	9	$PROGCL_A$	R pin	Bridge A overcurrent level programming. A resistor connected between this pin and ground sets the programmable current limiting value for the bridge A. By connecting this pin to ground the maximum current is set. This pin cannot be left non-connected.

4 Electrical characteristics

Table 5. Electrical characteristics (T_{amb} = 25 °C, V_s = 48 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{Sth(ON)}$	Turn-on threshold	-	6.6	7	7.4	V
$V_{Sth(OFF)}$	Turn-off threshold	-	5.6	6	6.4	V
I_S	Quiescent supply current	All bridges OFF; T_j = -25 °C to 125 °C(1)	-	5	10	mA
$T_{j(OFF)}$	Thermal shutdown temperature	-	-	165	-	°C
Output DMOS transistors						
$R_{DS(ON)}$	High-side switch ON resistance	T_j = 25 °C	-	0.34	0.4	Ω
		T_j = 125 °C(1)	-	0.53	0.59	Ω
	Low-side switch ON resistance	T_j = 25 °C	-	0.28	0.34	Ω
		T_j = 125 °C(1)	-	0.47	0.53	Ω
I_{DSS}	Leakage current	EN = low; OUT = V_S	-	-	2	mA
		EN = low; OUT = GND	-0.15	-	-	mA
Source drain diodes						
V_{SD}	Forward ON voltage	I_{SD} = 2.8 A, EN = low	-	1.15	1.3	V
t_{rr}	Reverse recovery time	I_f = 2.8 A	-	300	-	ns
t_{fr}	Forward recovery time	-	-	200	-	ns
Logic input						
V_{IL}	Low level logic input voltage	-	-0.3	-	0.8	V
V_{IH}	High level logic input voltage	-	2	-	7	V
I_{IL}	Low level logic input current	GND logic input voltage	-10	-	-	µA
I_{IH}	High level logic input current	7 V logic input voltage	-	-	10	µA
$V_{th(ON)}$	Turn-on input threshold	-	-	1.8	2.0	V
$V_{th(OFF)}$	Turn-off input threshold	-	0.8	1.3	-	V
$V_{th(HYS)}$	Input threshold hysteresis	-	0.25	0.5	-	V
Switching characteristics						
$t_{D(on)EN}$	Enable to out turn ON delay time(2)	I_{LOAD} = 2.8 A, resistive load	100	250	400	ns
$t_{D(on)IN}$	Input to out turn ON delay time	I_{LOAD} = 2.8 A, resistive load (deadtime included)	-	1.6	-	µs
t_{RISE}	Output rise time(2)	I_{LOAD} = 2.8 A, resistive load	40	-	250	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time(2)	I_{LOAD} = 2.8 A, resistive load	300	550	800	ns
$t_{D(off)IN}$	Input to out turn OFF delay time	I_{LOAD} = 2.8 A, resistive load	-	600	-	ns
t_{FALL}	Output fall time(2)	I_{LOAD} = 2.8 A, resistive load	40	-	250	ns

Table 5. Electrical characteristics (T_{amb} = 25 °C, V_s = 48 V, unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{dt}	Deadtime protection	-	0.5	1	-	µs
f_{CP}	Charge pump frequency	-25 °C < T_j < 125 °C	-	0.6	1	MHz
Overcurrent detection						
$I_{s\ over}$	Input supply overcurrent detection threshold	-25 °C < T_j < 125 °C; R_{CL} = 39 kΩ -25 °C < T_j < 125 °C; R_{CL} = 5 kΩ -25 °C < T_j < 125 °C; R_{CL} = GND	-10% -10% -30%	0.57 4.42 5.6	+10% +10% +30%	A A A
R_{OPDR}	Open drain ON resistance	I = 4 mA	-	40	60	Ω
$t_{OCD(ON)}$	OCD turn-on delay time(3)	I = 4 mA; C_{EN} < 100 pF	-	200	-	ns
$t_{OCD(OFF)}$	OCD turn-off delay time(3)	I = 4 mA; C_{EN} < 100 pF	-	100	-	ns

1. Tested at 25 °C in a restricted range and guaranteed by characterization.
2. See *Figure 3: Switching characteristic definition*.
3. See *Figure 4: Overcurrent detection timing definition*.

Figure 3. Switching characteristic definition

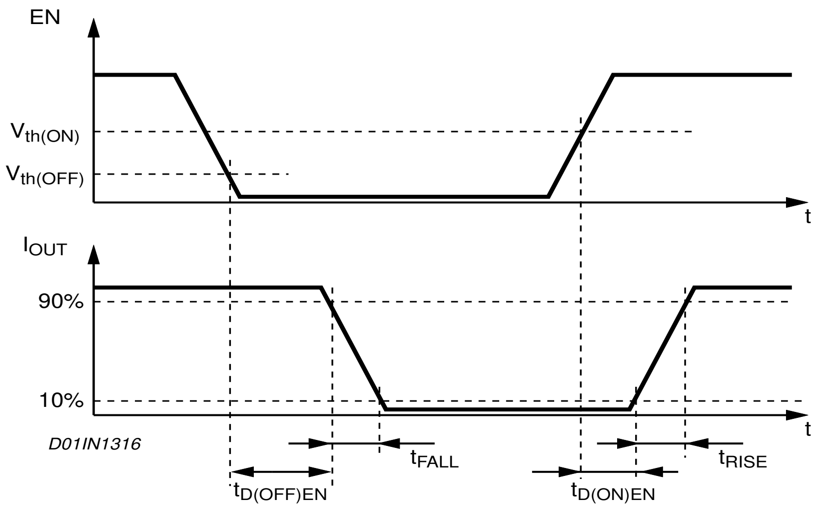
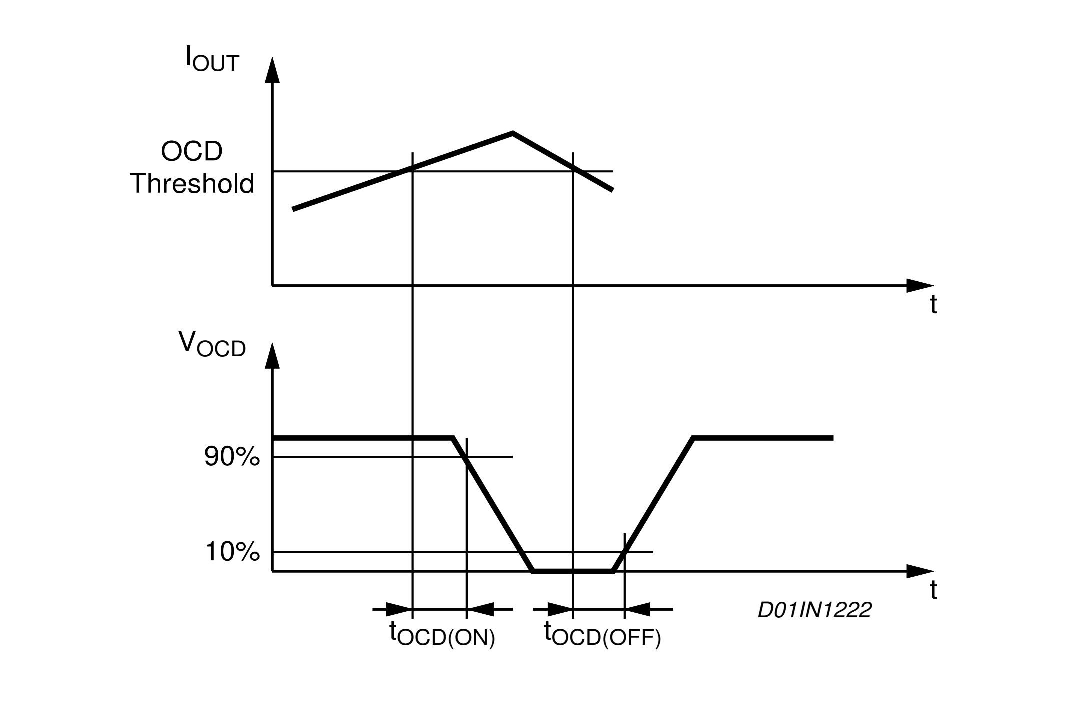


Figure 4. Overcurrent detection timing definition



5 Circuit description

5.1 Power stages and charge pump

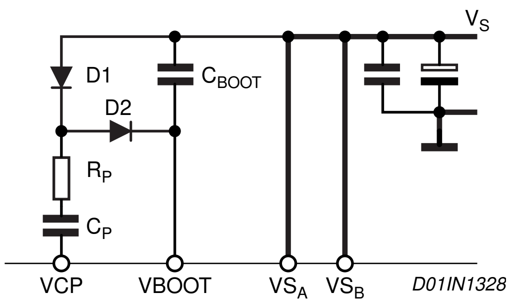
The L6206 device integrates two independent power MOS full bridges. Each power MOS has an $R_{ds(ON)}$ = 0.3 Ω (typical value at 25 °C), with intrinsic fast freewheeling diode. Cross conduction protection is achieved using a deadtime (t_d = 1µs typical) between the switch off and switch on of two power MOS in one leg of a bridge.

Using N-channel power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped (V_{BOOT}) supply is obtained through an internal oscillator and few external components to realize a charge pump circuit as shown in *Figure 5*. The oscillator output (VCP) is a square wave at 600 kHz (typical) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in *Table 6*.

Table 6. Charge pump external components values

Component	Value
C_{BOOT}	220 nF
C_P	10 nF
R_P	100 Ω
D1	1N4148
D2	1N4148

Figure 5. Charge pump circuit



5.2 Logic inputs

Pins $IN1_A$, $IN2_A$, $IN1_B$, $IN2_B$, EN_A and EN_B are TTL/CMOS compatible logic inputs. The internal structure is shown in *Figure 6*. Typical value for turn-on and turn-off thresholds are respectively $V_{th(ON)}$ = 1.8 V and $V_{th(OFF)}$ = 1.3 V.

Pins EN_A and EN_B are commonly used to implement overcurrent and thermal protection by connecting them respectively to the outputs OCD_A and OCD_B, which are open drain outputs. If that type of connection is chosen, some care needs to be taken in driving these pins. Two configurations are shown in *Figure 7* and *Figure 8*. If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in *Figure 7*. If the driver is a standard push-pull structure, the resistor R_{EN} and the capacitor C_{EN} are connected as shown in *Figure 8*. The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 KΩ and 5.6 nF. More information on selecting the values is found in *Section 5.3: Non-dissipative overcurrent detection and protection*.

Figure 6. Logic inputs internal structure

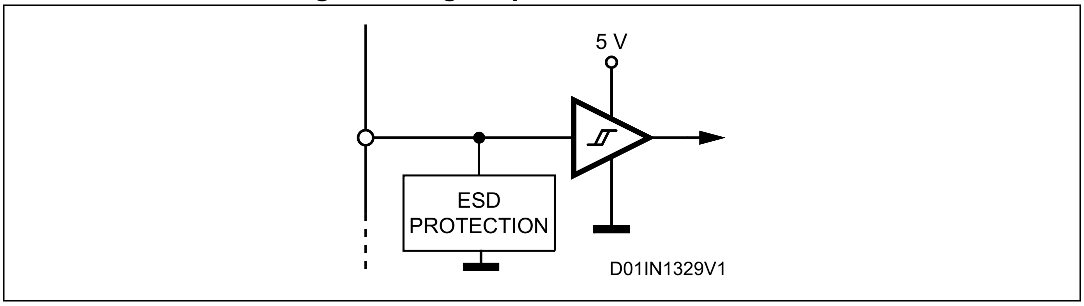


Figure 7. EN_A and EN_B pins open collector driving

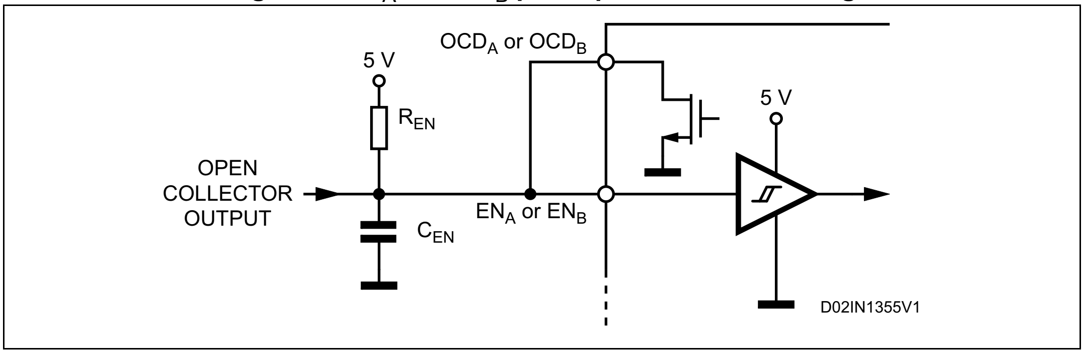


Figure 8. EN_A and EN_B pins push-pull driving

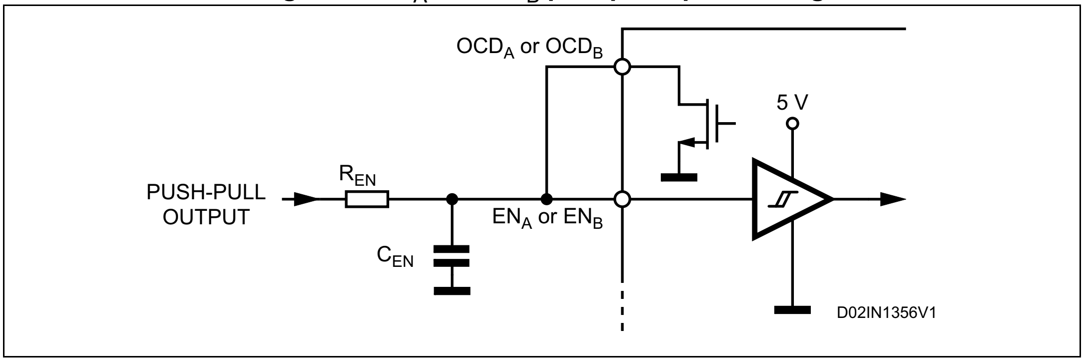


Table 7. Truth table

Inputs			Outputs	
EN	IN1	IN2	OUT1	OUT2
L	X(1)	X(1)	High Z(2)	High Z(2)
H	L	L	GND	GND
H	H	L	Vs	GND
H	L	H	GND	Vs
H	H	H	Vs	Vs

1. X = don't care.
2. High Z = high impedance output.

5.3 Non-dissipative overcurrent detection and protection

In addition to the PWM current control, an overcurrent detection circuit (OCD) is integrated. This circuit can be used to provide protection against a short-circuit to ground or between two phases of the bridge as well as a roughly regulation of the load current. With this internal overcurrent detection, the external current sense resistor normally used and its associated power dissipation are eliminated. *Figure 9* shows a simplified schematic of the overcurrent detection circuit for the bridge A. Bridge B is provided of an analogous circuit.

To implement the overcurrent detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high-side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold I_{SOVER} the OCD comparator signals a fault condition. When a fault condition is detected, an internal open drain MOS with a pull down capability of 4 mA connected to OCD pin is turned on. *Figure 10* shows the OCD operation.

This signal can be used to regulate the output current simply by connecting the OCD pin to EN pin and adding an external R-C as shown in *Figure 9*. The off time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

I_{REF} and, therefore, the output current detection threshold are selectable by R_{CL} value, following the equations:

–I_{SOVER} = 5.6 A ± 30% at -25 °C < T_j < 125 °C if R_{CL} = 0 Ω (PROGCL connected to GND)

$$-I_{SOVER} = \frac{22100}{R_{CL}} \pm 10\% \quad \text{at } -25\ °C < T_j < 125\ °C \quad \text{if } 5\ K\Omega < R_{CL} < 40\ k\Omega$$

Figure 11 shows the output current protection threshold versus R_{CL} value in the range 5 kΩ to 40 kΩ.

The disable time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in *Figure 12*. The delay time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in *Figure 13*.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 KΩ to 180 KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 KΩ and 5.6 nF that allow obtaining 200 µs disable time.

Figure 9. Overcurrent protection simplified schematic

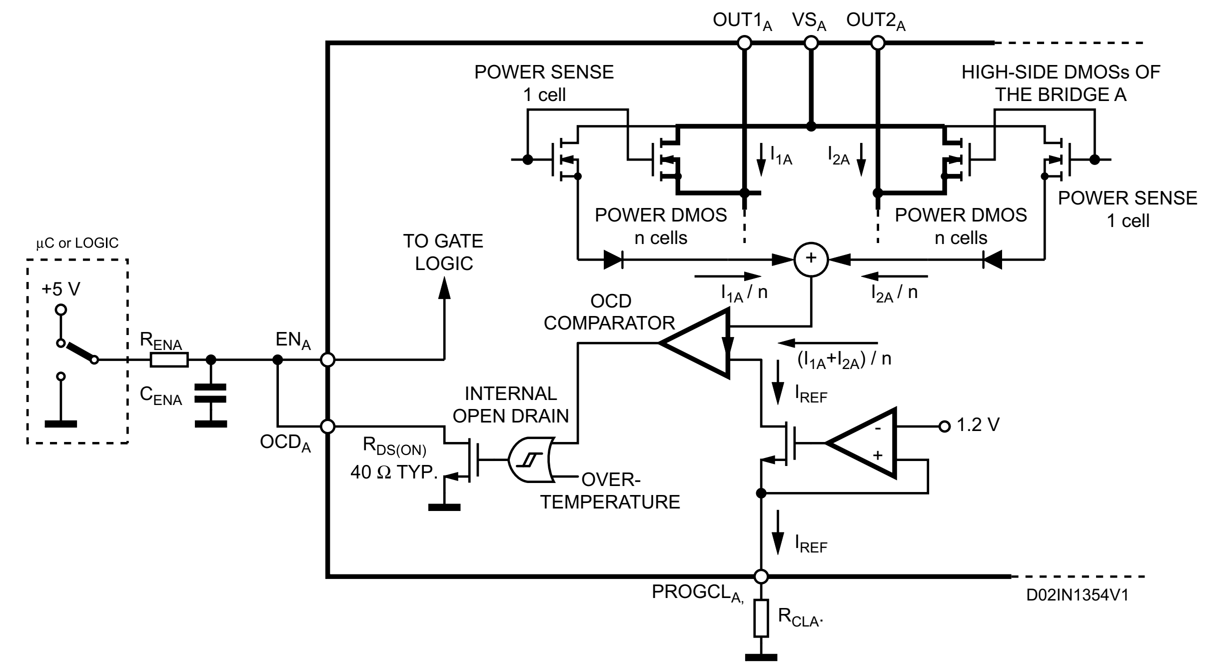


Figure 10. Overcurrent protection waveforms

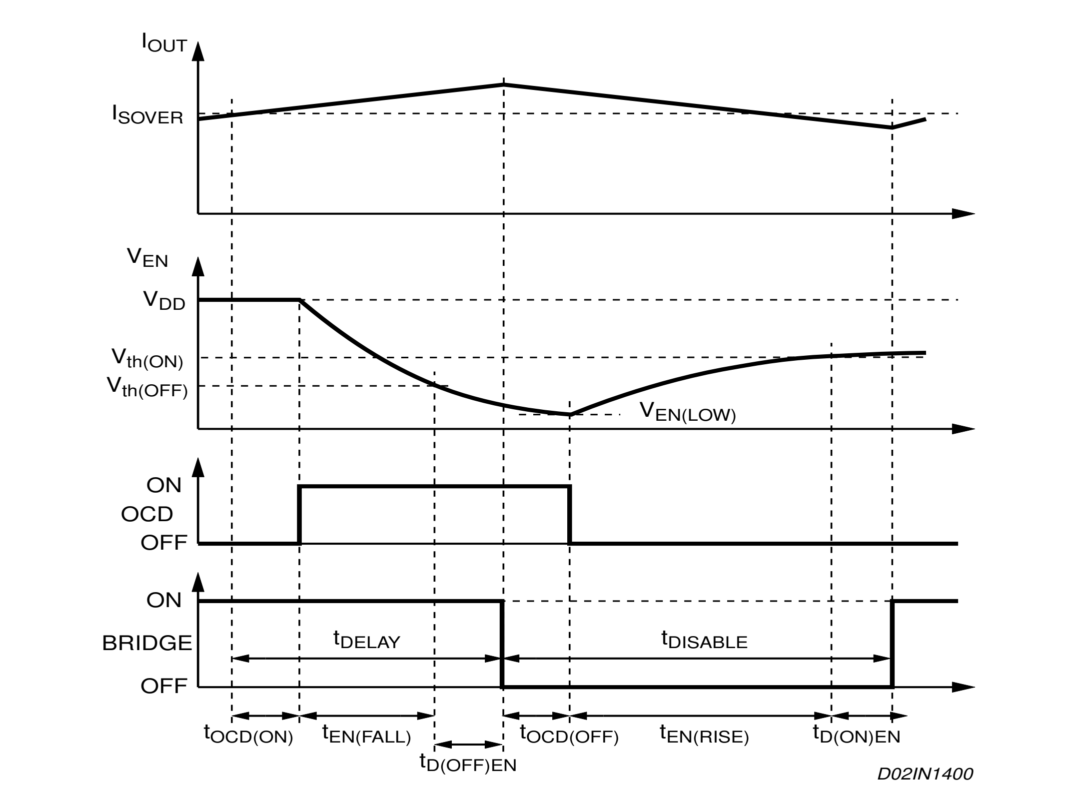


Figure 11. Output current protection threshold versus R_{CL} value

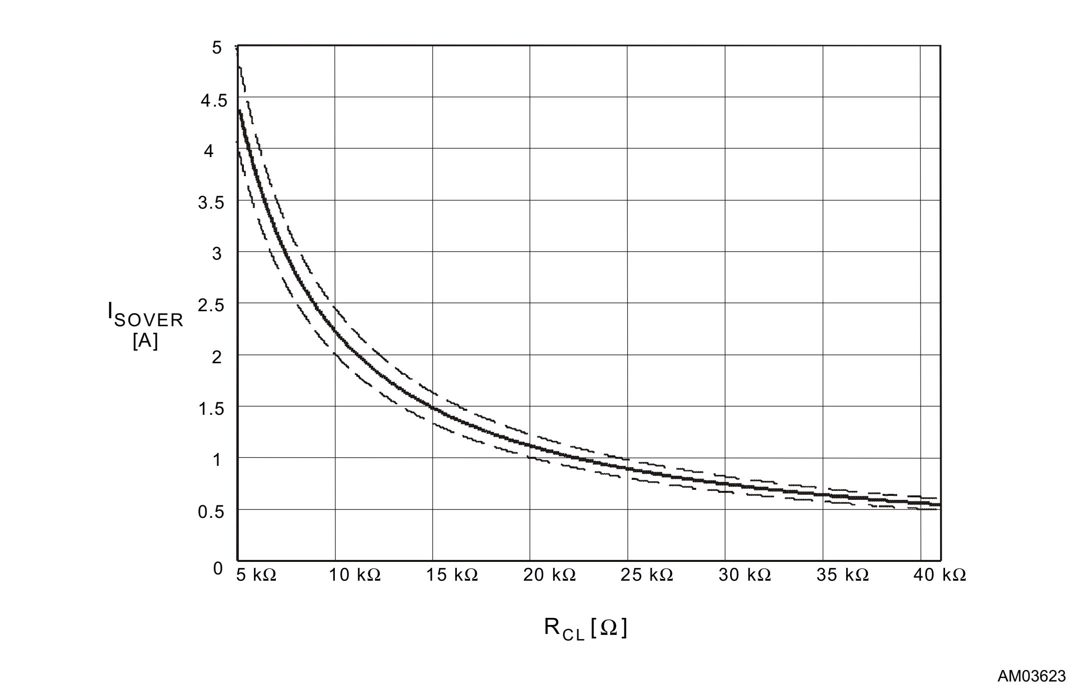


Figure 12. $t_{DISABLE}$ versus C_{EN} and R_{EN} (V_{DD} = 5 V)

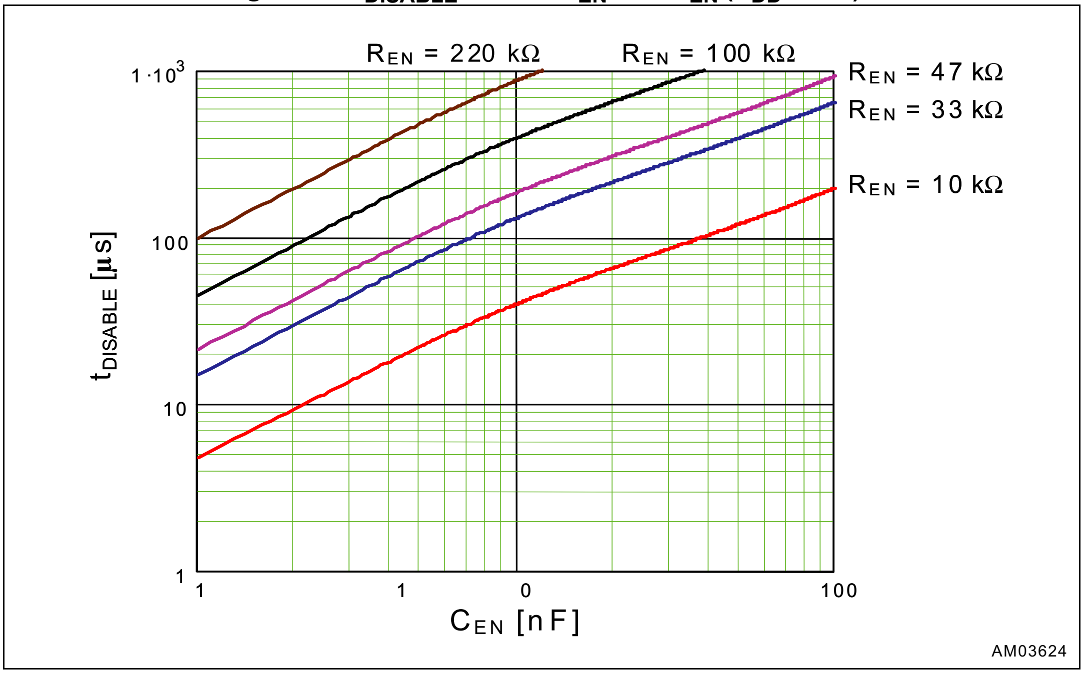
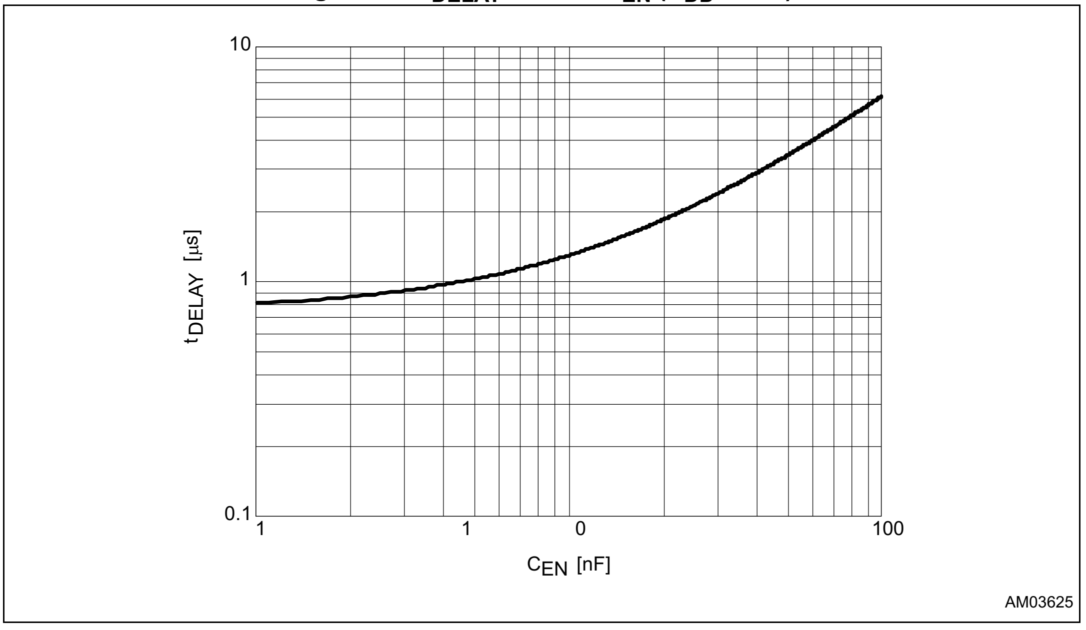


Figure 13. t_{DELAY} versus C_{EN} (V_{DD} = 5 V)



5.4 Thermal protection

In addition to the overcurrent detection, the L6206 device integrates a thermal protection for preventing the device destruction in case of junction overtemperature. It works sensing the die temperature by means of a sensible element integrated in the die. The device switches-off when the junction temperature reaches 165 °C (typ. value) with 15 °C hysteresis (typ. value).

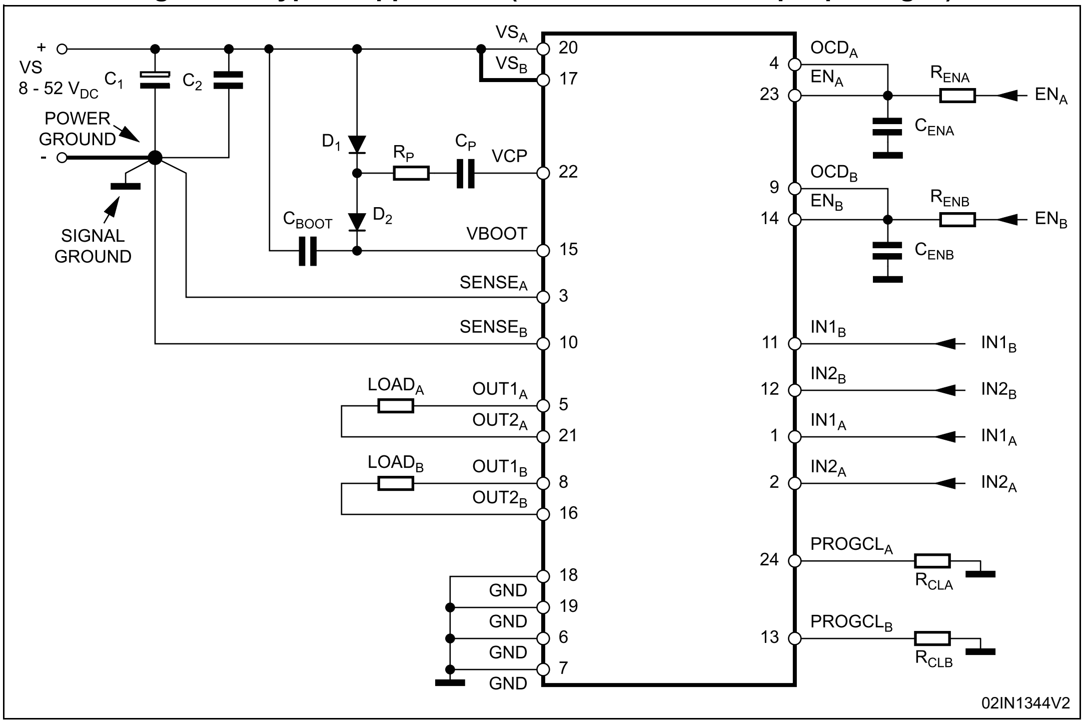
6 Application information

A typical application using the L6206 device is shown in *Figure 14*. Typical component values for the application are shown in *Table 8*. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6206 device to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the EN_A/OCD_A and EN_B/OCD_B nodes to ground set the shutdown time for the bridge A and bridge B respectively when an overcurrent is detected (see *Section 5.3: Non-dissipative overcurrent detection and protection on page 13*). The two current sources ($SENSE_A$ and $SENSE_B$) should be connected to power ground with a trace length as short as possible in the layout. To increase noise immunity, unused logic pins are best connected to 5 V (high logic level) or GND (low logic level) (see *Table 4: Pin description on page 6*). It is recommended to keep power ground and signal ground separated on the PCB.

Table 8. Component values for typical application

Component	Value	Component	Value
C_1	100 µF	D_1	1N4148
C_2	100 nF	D_2	1N4148
C_{BOOT}	220 nF	R_{CLA}	5 KΩ
C_P	10 nF	R_{CLB}	5 KΩ
C_{ENA}	5.6 nF	R_{ENA}	100 kΩ
C_{ENB}	5.6 nF	R_{ENB}	100 kΩ

Figure 14. Typical application (with reference to 24-pin packages)



6.1 Paralleled operation

The outputs of the L6206 device can be paralleled to increase the output current capability or reduce the power dissipation in the device at a given current level. It must be noted, however, that the internal wire bond connections from the die to the power or sense pins of the package must carry current in both of the associated half-bridges. When the two halves of one full bridge (for example $OUT1_A$ and $OUT2_A$) are connected in parallel, the peak current rating is not increased since the total current must still flow through one bond wire on the power supply or sense pin. In addition the overcurrent detection senses the sum of the current in the upper devices of each bridge (A or B) so connecting the two halves of one bridge in parallel does not increase the overcurrent detection threshold.

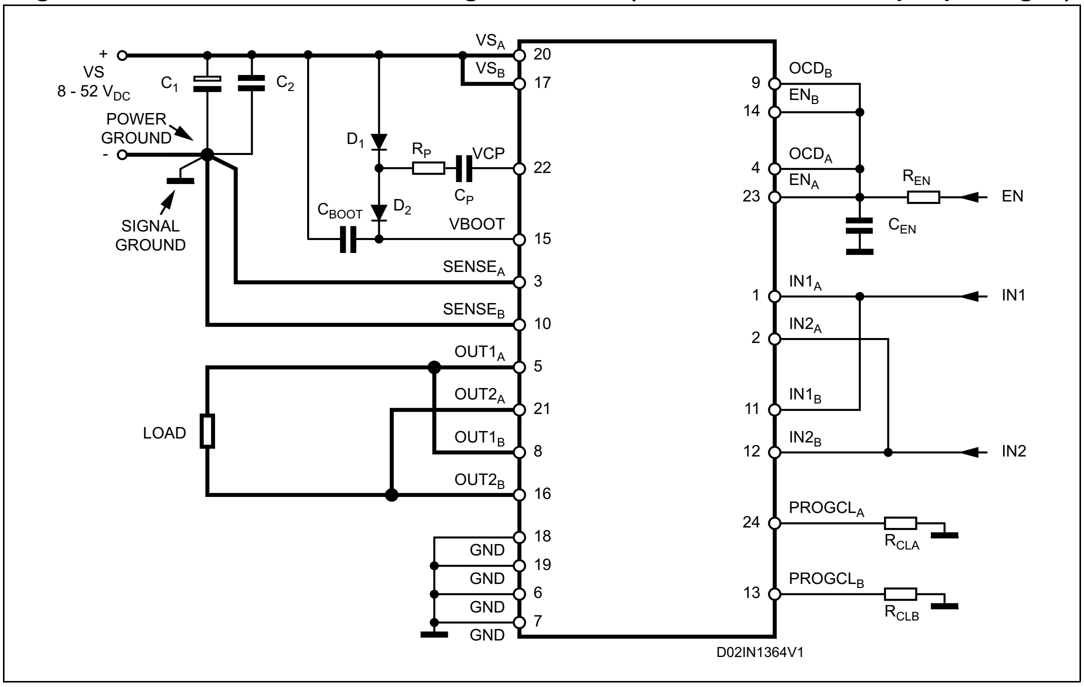
For most applications the recommended configuration is half-bridge 1 of bridge A paralleled with the half-bridge 1 of the bridge B, and the same for the half-bridges 2 as shown in *Figure 15*. The current in the two devices connected in parallel will share very well since the $R_{DS(ON)}$ of the devices on the same die is well matched.

When connected in this configuration the overcurrent detection circuit, which senses the current in each bridge (A and B), will sense the current in upper devices connected in parallel independently and the sense circuit with the lowest threshold will trip first. With the enables connected in parallel, the first detection of an overcurrent in either upper DMOS device will turn of both bridges. Assuming that the two DMOS devices share the current equally, the resulting overcurrent detection threshold will be twice the minimum threshold set by the resistors R_{CLA} or R_{CLB} in *Figure 15*. It is recommended to use $R_{CLA} = R_{CLB}$.

In this configuration the resulting bridge has the following characteristics:

- Equivalent device: full bridge
- $R_{DS(ON)}$ 0.15 Ω typ. value at T_J = 25 °C
- 5.6 A max. RMS load current
- 11.2 A max. OCD threshold

Figure 15. Parallel connection for higher current (with reference to 24-pin packages)



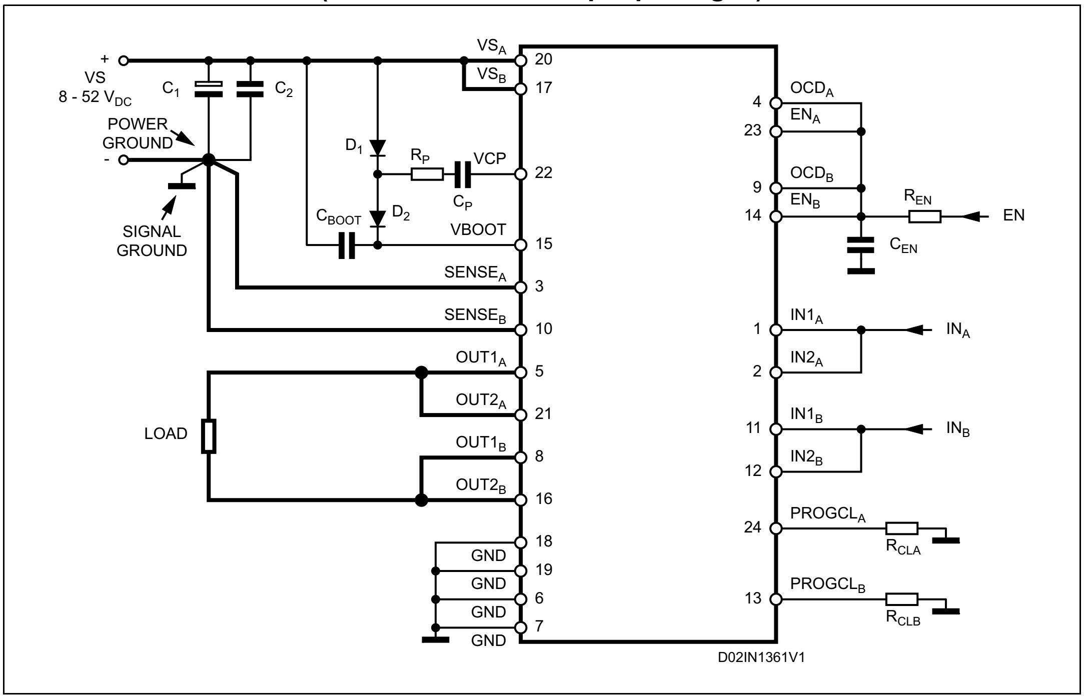
To operate the device in parallel and maintain a lower overcurrent threshold, half-bridge 1 and the half-bridge 2 of the bridge A can be connected in parallel and the same done for the bridge B as shown in *Figure 16*. In this configuration, the peak current for each half-bridge is still limited by the bond wires for the supply and sense pins so the dissipation in the device will be reduced, but the peak current rating is not increased.

When connected in this configuration the overcurrent detection circuit, senses the sum of the current in upper devices connected in parallel. With the enables connected in parallel, an overcurrent will turn of both bridges. Since the circuit senses the total current in the upper devices, the overcurrent threshold is equal to the threshold set the resistor R_{CLA} or R_{CLB} in *Figure 16*. R_{CLA} sets the threshold when outputs $OUT1_A$ and $OUT2_A$ are high and resistor R_{CLB} sets the threshold when outputs $OUT1_B$ and $OUT2_B$ are high.
It is recommended to use $R_{CLA} = R_{CLB}$.

In this configuration, the resulting bridge has the following characteristics:

- Equivalent device: full bridge
- $R_{DS(ON)}$ 0.15 Ω typ. value at T_J = 25 °C
- 2.8 A max. RMS load current
- 5.6 A max. OCD threshold

Figure 16. Parallel connection with lower overcurrent threshold (with reference to 24-pin packages)

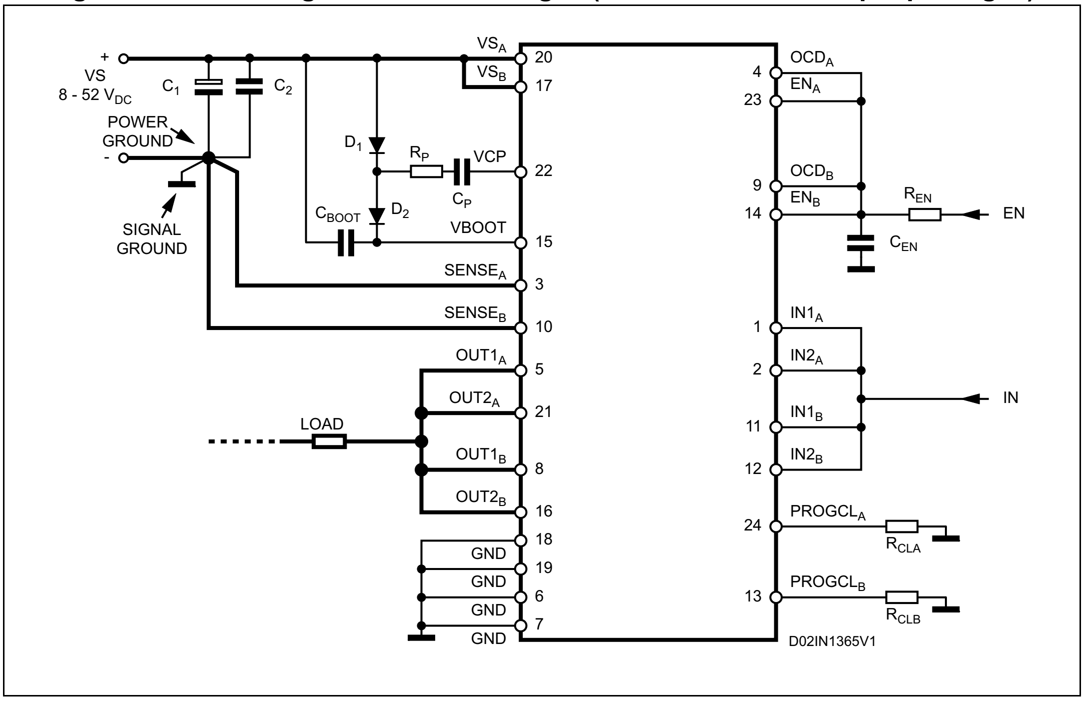


It is also possible to parallel the four half-bridges to obtain a simple half-bridge as shown in *Figure 17*. In this configuration the overcurrent threshold is equal to twice the minimum threshold set by the resistors R_{CLA} or R_{CLB} in *Figure 17*. It is recommended to use $R_{CLA} = R_{CLB}$.

The resulting half-bridge has the following characteristics:

- Equivalent device: half-bridge
- $R_{DS(ON)}$ 0.075.Ω typ. value at T_J = 25 °C
- 5.6 A max. RMS load current
- 11.2 A max. OCD threshold

Figure 17. Paralleling the four half-bridges (with reference to 24-pin packages)



6.2 Output current capability and IC power dissipation

In *Figure 18* and *Figure 19* are shown the approximate relation between the output current and the IC power dissipation using PWM current control driving two loads, for two different driving types:

- One full bridge ON at a time (*Figure 18*) in which only one load at a time is energized.
- Two full bridges ON at the same time (*Figure 19*) in which two loads at the same time are energized.

For a given output current and driving type the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125 °C maximum).

Figure 18. IC power dissipation versus output current with one full bridge ON at a time

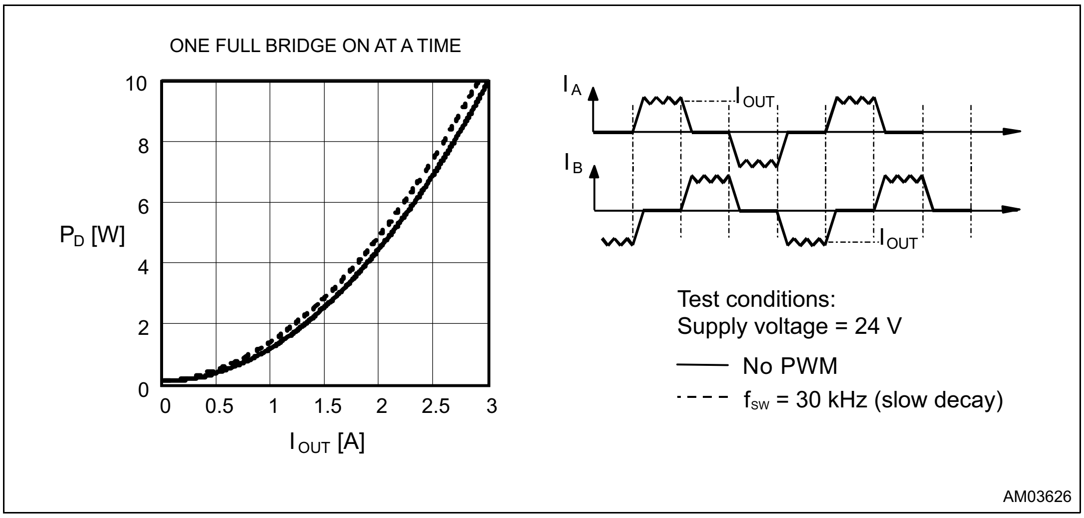
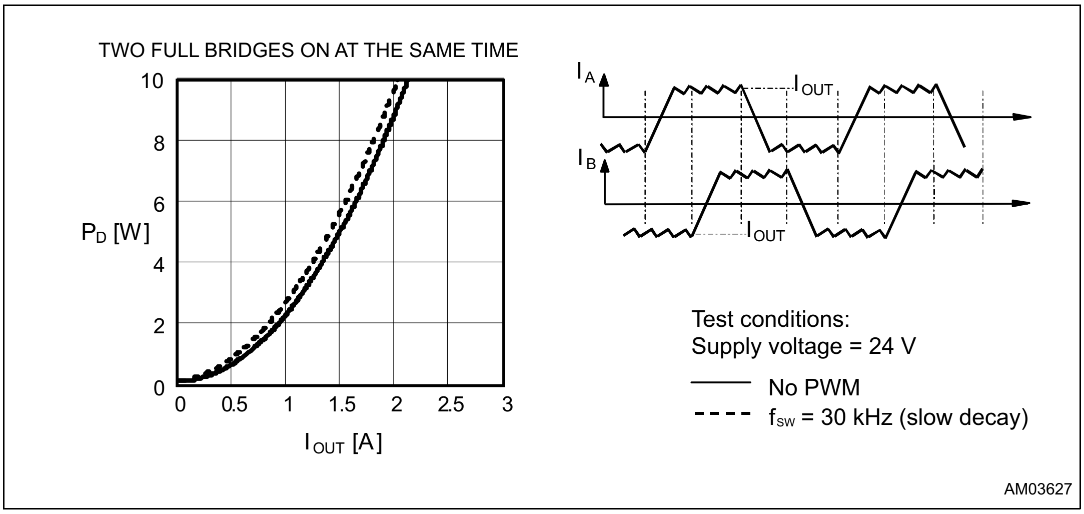


Figure 19. IC power dissipation versus output current with two full bridges ON at the same time



6.3 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heatsinking can be achieved using copper on the PCB with proper area and thickness. *Figure 21*, *22* and *23* show the junction to ambient thermal resistance values for the PowerSO36, PowerDIP24 and SO24 packages.

For instance, using a PowerSO package with a copper slug soldered on a 1.5 mm copper thickness FR4 board with a 6 cm^2 dissipating footprint (copper thickness of 35 µm), the $R_{th\ j\text{-}amb}$ is about 35 °C/W. *Figure 20* shows mounting methods for this package. Using a multilayer board with vias to a ground plane, thermal impedance can be reduced down to 15 °C/W.

Figure 20. Mounting the PowerSO package

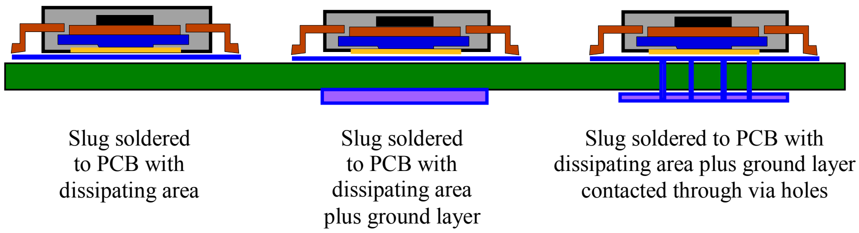


Figure 21. PowerSO36 junction ambient thermal resistance versus on-board copper area

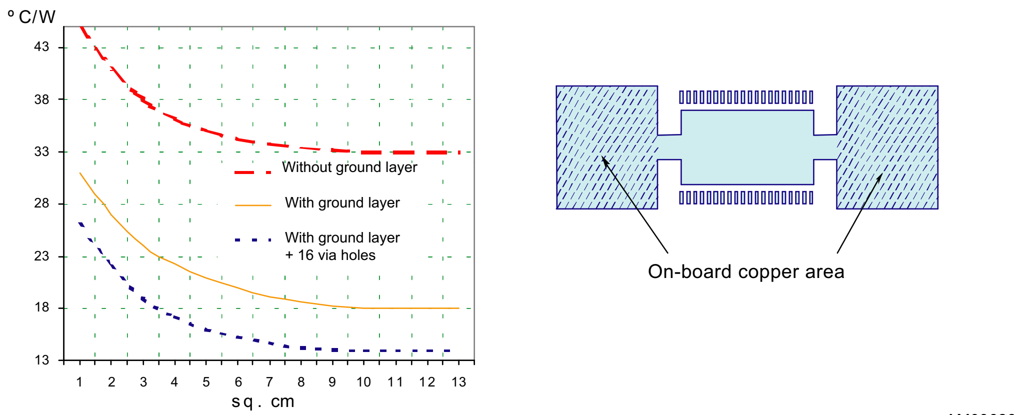


Figure 22. PowerDIP24 junction ambient thermal resistance versus on-board copper area

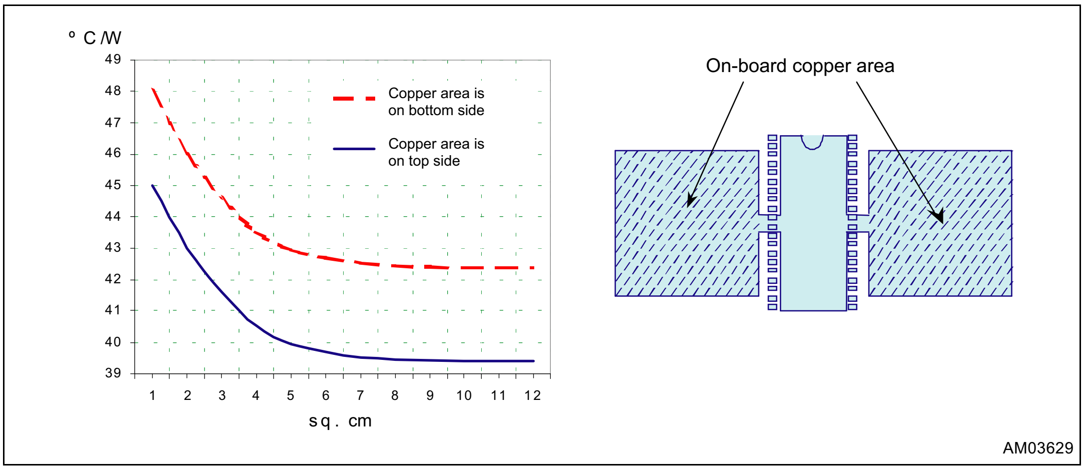


Figure 23. SO24 junction ambient thermal resistance versus on-board copper area

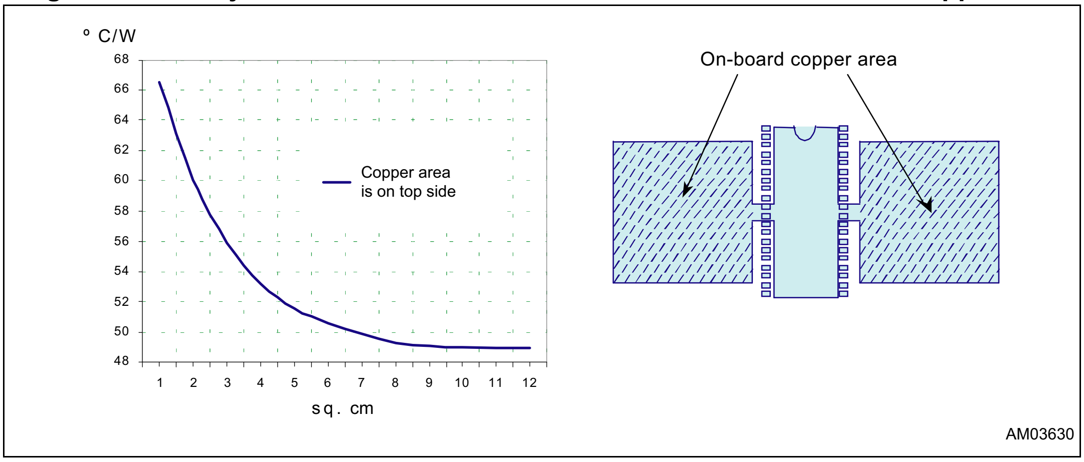


Figure 24. Typical quiescent current vs. supply voltage

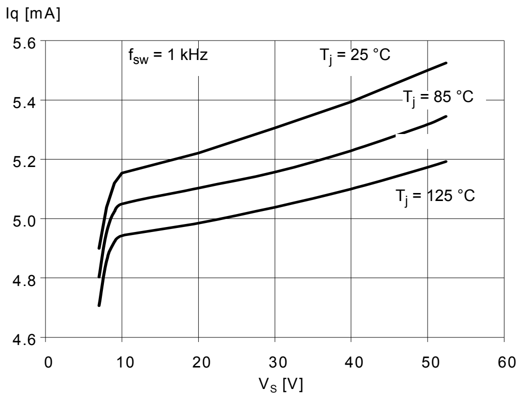


Figure 25. Typical high-side $R_{DS(ON)}$ vs. supply voltage

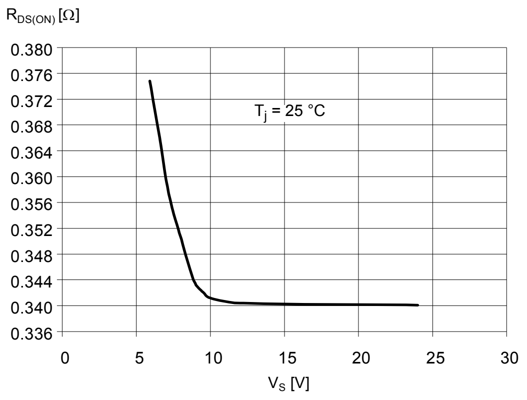


Figure 26. Normalized typical quiescent current vs. switching frequency

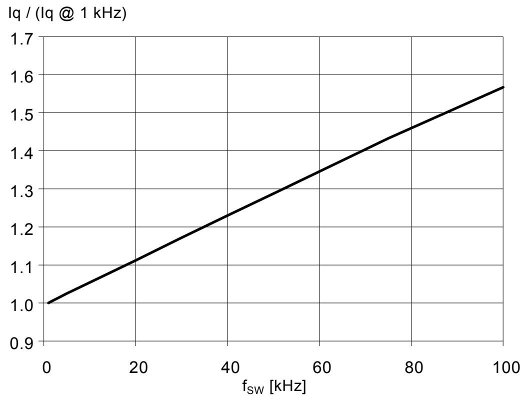


Figure 27. Normalized $R_{DS(ON)}$ vs.junction temperature (typical value)

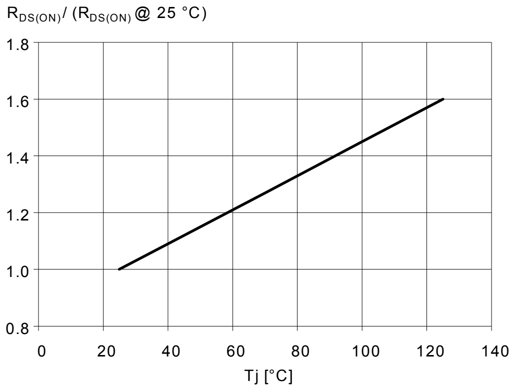


Figure 28. Typical low-side $R_{DS(ON)}$ vs. supply voltage

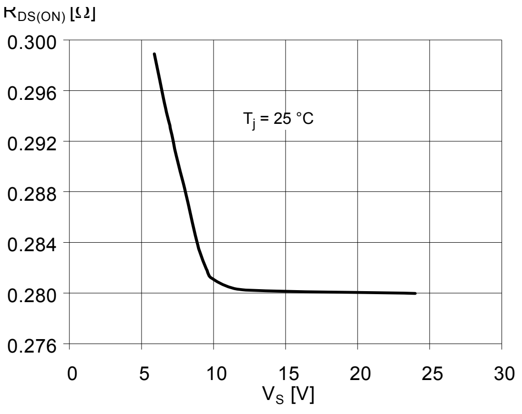
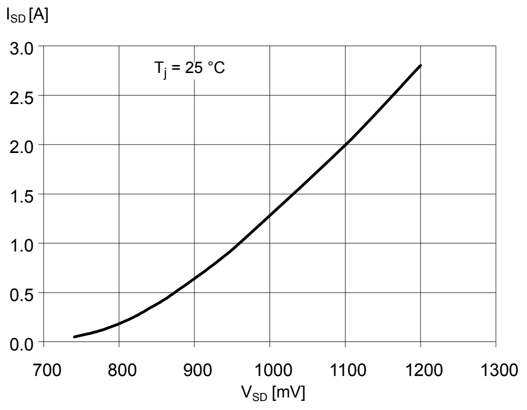


Figure 29. Typical drain-source diode forward ON characteristic



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSO36 package information

Figure 30. PowerSO36 package outline