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L6360

IO-Link communication master transceiver IC

Datasheet - production data


VFQFPN 26L (3.5x5x1 mm)

Features

- Supply voltage from 18 V to 32.5 V
- Programmable output stages: high-side, low-side or push-pull (< 2 Ω)
- Up to 500 mA L+ protected high-side driver
- COM1, COM2 and COM3 mode supported
- Additional IEC61131-2 type 1 input
- Short-circuit and overcurrent output protection through current limitation and programmable cut-off current
- 3.3 V / 5 V, 50 mA linear regulator
- 5 mA IO-Link digital input
- Fast mode I^2C for IC control, configuration and diagnostic
- Diagnostic dual LED sequence generator and driver
- 5 V and 3.3 V compatible I/Os
- Overvoltage protection (> 36 V)
- Overtemperature protection
- ESD protection
- Miniaturized VFQFPN 26L (3.5x5x1 mm) package

Applications

- Industrial sensors
- Factory automation
- Process control

Description

The L6360 is a monolithic IO-Link master port compliant with PHY2 (3-wire) supporting COM1 (4.8 kbaud), COM2 (38.4 kbaud) and COM3 (230.4 kbaud) modes. The C/Q_O output stage is programmable: high-side, low-side or push-pull; also cut-off current, cut-off current delay time, and restart delay are programmable. Cut-off current and cut-off current delay time, combined with thermal shutdown and automatic restart, protect the device against overload and short-circuit. C/Q_O and L+ output stages are able to drive resistive, inductive and capacitive loads. Inductive loads up to 10 mJ can be driven. Supply voltage is monitored and low voltage conditions are detected. The L6360 transfers, through the PHY2(C/Q_O pin), data received from a host microcontroller through the USART (IN C/Q_O pin), or to the USART (OUT C/Q_I pin) data received from PHY2 (C/Q_I pin). To enable full IC control, configuration and monitoring (i.e. fault conditions stored in the status register), the communication between the system microcontroller and the L6360 is based on a fast mode 2-wire I^2C. The L6360 has nine registers to manage the programmable parameters and the status of the IC. Monitored fault conditions are: L+ line, overtemperature, C/Q overload, linear regulator undervoltage, and parity check. Internal LED driver circuitries, in open drain configuration, provide two programmable sequences to drive two LEDs.

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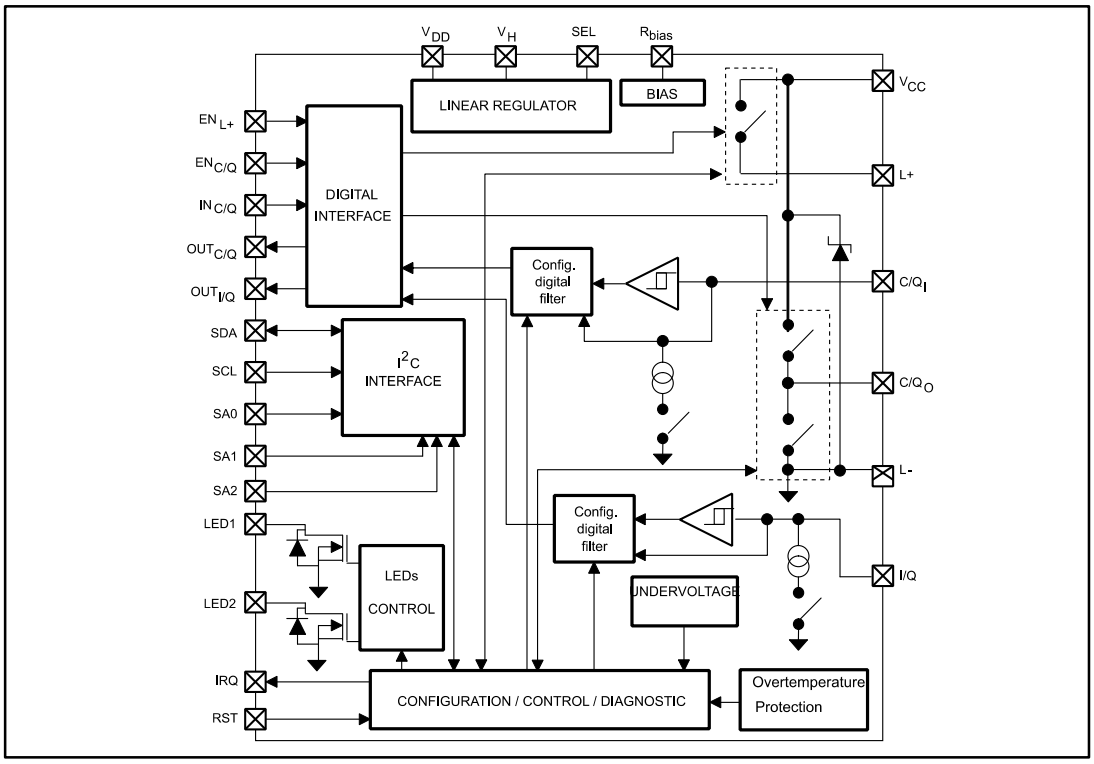
1 Block diagram

Figure 1: Block diagram



2 Pin description

Figure 2: Pin connection (top through view)

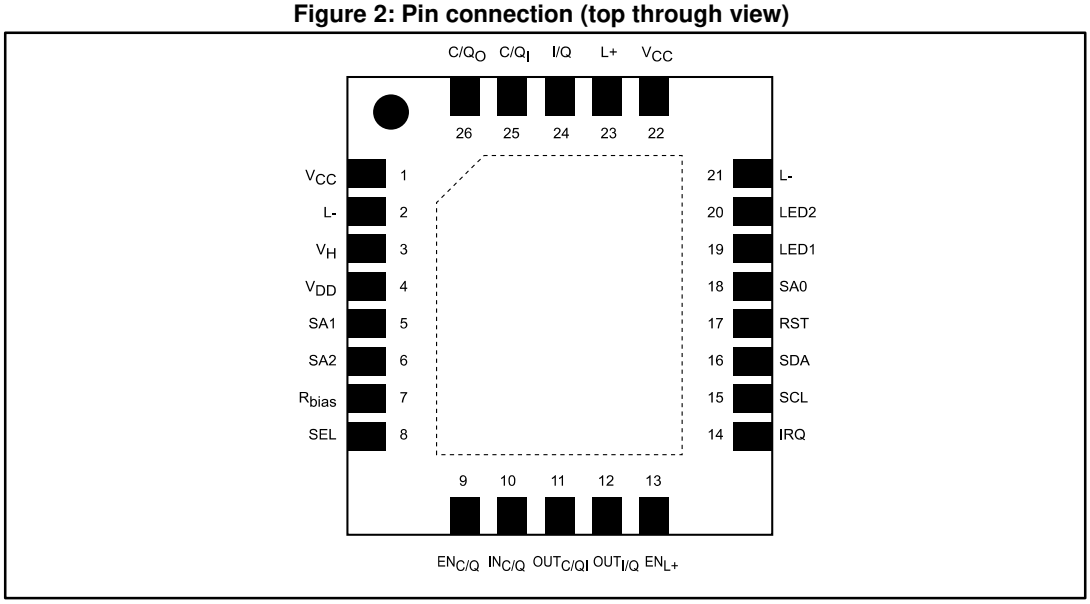


Table 1: Pin description

Number	Name	Function	Type
1	V_{CC}	IC power supply	Supply
2	L-	L- line (IC ground)	Supply
3	V_H	Linear regulator supply voltage	Supply
4	V_{DD}	Linear regulator output voltage	Output
5	SA1	Serial address 1	Input
6	SA2	Serial address 2	Input
7	R_{bias}	External resistor for internal reference generation	Input
8	SEL	Linear regulator 3.3 V/5 V voltage selection. Output is 5 V when SEL pin is pulled to GND	Input
9	$EN_{C/Q}$	C/Q output enable	Input
10	$IN_{C/Q}$	C/Q channel logic input	Input
11	$OUTH_{C/Q}$	C/Q channel logic output	Output
12	$OUTH_{I/Q}$	I/Q channel logic output	Output
13	EN_{L+}	L+ switch enable. When EN_{L+} is high the switch is closed	Input
14	IRQ	Interrupt request signal (open drain)	Output
15	SCL	Serial clock line	Input
16	SDA	Serial data line	Input/output
17	RST	Reset - active low	Input
18	SA0	Serial address 0	Input
19	LED1	Status/diagnostic LED (open drain)	Output
20	LED2	Status/diagnostic LED (open drain)	Output

Number	Name	Function	Type
21	L-	L- line (IC ground)	Supply
22	V_{CC}	IC power supply	Supply
23	L+	L+ line	Supply
24	I/Q	I/Q channel line	Input
25	C/Q_I	Transceiver (C/Q channel) line	Input
26	C/Q_O	Transceiver (C/Q channel) line	Output

3 Absolute maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	V_{CLAMP}	V
V_{SEL}	Linear regulator selection pin voltage	-0.3 to 4	
V_{DD}	Linear regulator output voltage	5.5	
V_H	Linear regulator input voltage	V_{CC}	
$V_{SDA, SCL, SA0, 1, 2}$	I^2C voltage	-0.3 to V_{DD} + 0.3	
$V_{LED1,2}$	LED1,2 voltage	-0.3 to V_{DD} + 0.3	
$V_{C/QI}$, $V_{I/Q}$	C/Q_I, I/Q voltage	-0.3 to V_{CC} + 0.3	
V_{RST}	Reset voltage	-0.3 to V_{DD} + 0.3	
V_{IRQ}	IRQ voltage	-0.3 to V_{DD} + 0.3	
V_{Rbias}	External precision resistance voltage	-03 to 4	
V_{ESD}	Electrostatic discharge (human body model)	2000	
I_{CLAMP}	Current through V_{CLAMP} in surge test (1 kV, 500 Ω) condition	2	A
$I_{C/QO}$, I_{L+}	C/Q_O, L+ current (continuous)	Internally limited	A
$IOUT_{C/Q}$, $IOUT_{I/Q}$	$OUT_{C/Q}$, $OUT_{I/Q}$ output current	±5	mA
I_{SDA}	I^2C transmission data current (open drain pin)	10	mA
I_{RQ}	Interrupt request signal current	2[(1)]	A
$I_{LED1,2}$	LED1, 2 current	10	mA
E_{load}	L+ demagnetization energy	10	mJ
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited	W
P_{LR}	Linear regulator power dissipation	200	mW
T_J	Junction operating temperature	Internally limited	°C
T_{STG}	Storage temperature range	-55 to 150	

Notes:

(1)Peak value during fast transient test only.

4 Recommended operating conditions

Table 3: Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	18		32.5	V
V_H	Linear regulator input voltage	7		V_{CC}	V
f_{SCL}	SCL clock frequency			400	kHz
R_{bias}	Precision resistance	-0.1%	124	0.1%	kΩ
T_J	Junction temperature	40		125	°C

Table 4: Thermal data

Symbol	Parameter	Typ.	Unit
$R_{thj\text{-}case}$	Thermal resistance, junction-to-case	6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance, junction-to-ambient(1)	50	°C/W

Notes:

(1)Mounted on FR4 PCB with 2 signal Cu layers and 2 power Cu layers interconnected through vias.

5 Electrical characteristics

(18 V < V_{CC} < 30 V; -25 °C < T_J < 125 °C; V_{DD} = 5 V; unless otherwise specified).

Table 5: Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Voltage clamp	I = 5 mA	36			V
V_{UV}	Undervoltage on threshold		16	17	18	V
V_{UVH}	Undervoltage hysteresis		0.3	1		V
$V_{REGLN5H}$	Linear regulator undervoltage high threshold	SEL = L	4.3		4.7	V
$V_{REGLN5L}$	Linear regulator undervoltage low threshold	SEL = L	3.6		4.2	
$V_{REG5HYS}$	Linear regulator undervoltage hysteresis	SEL = L	0.1			
$V_{REGLN33H}$	Linear regulator undervoltage high threshold	SEL = H	2.8		3.1	
$V_{REGLN33L}$	Linear regulator undervoltage low threshold	SEL = H	2.5		2.7	V
$V_{REG33HYS}$	Linear regulator undervoltage hysteresis	SEL = H	0.1			V
V_{QTHH}	C/Q_I and I/Q upper voltage threshold		10.5		12.9	V
V_{QTHL}	C/Q_I and I/Q lower voltage threshold		8		11.4	V
V_{QHY}	C/Q and I/Q hysteresis voltage		1			V
V_{demag}	L+ demagnetization voltage	I = 5 mA	-8.5	-6.5	-4.8	V
V_{fHS}	C/Q high-side freewheeling diode forward voltage	I = 10 mA		0.5		V
V_{fLS}	C/Q low-side freewheeling diode forward voltage	I = 10 mA		0.5		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{LTHOFF}	L+ line diagnostic lower threshold		9	10	11	V
V_{LTHY}	L+ line diagnostic hysteresis		0.1	1		V
V_{LTHON}	L+ line diagnostic upper threshold		10	11	12	V
I_S	Supply current	OFF-state		100		µA
		ON-state V_{CC} at 32.5 V		4		mA
I_{OFFCQ}	OFF-state C/Q_O current	$EN_{C/Q}$ = 0, $V_{C/Q}$ = 0 V			1	µA
I_{COQ}	C/Q_O low- and high-side cut-off current	Programmable	70	115	190	mA
			150	220	300	
			290	350	440	
			430	580	720	
I_{LIMQ}	C/Q_O low- and high-side limitation current		500		1600	mA
I_{OFFL}	L+ OFF-state current	EN_{L+} = 0, V_{L+} = 0 V	0		200	µA
I_{COL}	L+ cut-off current		480	580	730	mA
I_{LIML}	L+ limitation current		500		1600	mA
$I_{INC/Qi}$	C/Q_I pull-down current	Programmable	5		6.5	mA
			2		3.3	mA
$I_{INI/Q}$	I/Q pull-down current		2		3	mA
R_{ONL}	L+ high-side ON-state resistance	I_{OUT} = 0.2 A at T_J = 25 °C		1		Ω
		I_{OUT} = 0.2 A at T_J = 125 °C			2	Ω
R_{ONCQH}	C/Q_O high-side ON-state resistance	I_{OUT} = 0.2 A at T_J = 25 °C		1		Ω
		I_{OUT} = 0.2 A at T_J = 125 °C			2	Ω
R_{ONCQL}	C/Q_O low-side ON-state resistance	I_{OUT} = 0.2 A at T_J = 25 °C		0.6		Ω
		I_{OUT} = 0.2 A at T_J = 125 °C			1.2	Ω
$t_{dINC/Q}$	$IN_{C/Q}$ to C/Q_O propagation delay time	Push-pull (CQ_O rising edge)		140		ns
		Push-pull (CQ_O falling edge)		160		ns
$t_{ENC/Q}$	$EN_{C/Q}$ to C/Q_O propagation delay time	Push-pull (CQ_O rising edge)		110		ns
		Push-pull (CQ_O falling edge)		225		ns

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rPP}	C/Q rise time in push-pull configuration	10% to 90%	250		860	ns
t_{fPP}	C/Q fall time in push-pull configuration	10% to 90%	290		860	ns
t_{rHS}	C/Q rise time in high-side configuration			410		ns
t_{fHS}	C/Q fall time in high-side configuration			700		ns
t_{rLS}	C/Q rise time in low-side configuration			750		ns
t_{fLS}	C/Q fall time in low-side configuration			530		ns
t_{ENL}	ENL to L+ propagation delay time			1		µs
t_{rL+}	L+ rise time			3		µs
t_{fL+}	L+ fall time			25		µs
$t_{dC/Qi}$	C/Q_I to $OUT_{C/Q}$ (falling) propagation delay time			40		ns
	C/Q_I to $OUT_{C/Q}$ (rising) propagation delay time			100		ns
$t_{dI/Q}$	I/Q to $OUT_{I/Q}$ (falling) propagation delay time			40		ns
	I/Q to $OUT_{I/Q}$ (rising) propagation delay time			100		ns
t_{dcoq}	C/Q_O low- and high-side cut-off current delay time	Programmable		100		µs
				150		µs
				200		µs
				250		µs
t_{rcoq}	C/Q_O restart delay time	Programmable		$255 \times t_{dcoq}$		µs
				Latched[(1)]		
t_{dbq}	C/Q_I debounce time	Programmable		0		µs
				5		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
				20		
				100		
t_{dbl}	I/Q debounce time	Programmable		0		µs
				5		
				20		
				100		
t_{dcol}	L+ cut-off current delay time	Programmable		500		µs
				0		
t_{rcol}	L+ restart delay time	Programmable		64		ms
				Latched (1)		
T_{JSD}	Junction temperature shutdown			150		°C
T_{JHYST}	Junction temperature thermal hysteresis			20		°C
T_{JRST}	Junction temperature restart threshold			130		°C

Notes:

(1)Unlatch through I^2C communication.

Table 6: Electrical characteristics - linear regulator

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Linear regulator output voltage	SEL = L	4.84	5	5.13	V
		SEL = H	3.22	3.3	3.37	V
I_{LIMR}	Linear regulator output current limitation		65			mA

Table 7: Electrical characteristics - logic inputs and outputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level voltage				0.8	V
V_{IH}	Input high-level voltage		2.2			V
V_{IHIS}	Input hysteresis voltage			0.2		V
I_{IN}	Input current	V_{IN} = 5 V			1	µA
V_{OL}	Output low-level voltage	I_{OUT} = -2 mA			0.5	V
V_{OH}	Output high-level voltage	I_{OUT} = 2 mA	V_{DD} - 0.5 V			V
V_{LIRQ}	Open drain output low-level voltage	I_{OUT} = 2 mA			0.5	V

Table 8: Electrical characteristics - LED driving

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{LED1,2}$	Open drain output low-level voltage	I_{LED} = 2 mA			0.5	V
I_{LED}	LED1, 2 leakage current	V_{LED1} = V_{LED2} = 5 V		3		nA

Table 9: Electrical characteristics - I²C (fast mode)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
$V_{IL(SDA)}$	SDA high level input voltage			0.3	V
$V_{IH(SDA)}$	SDA high level input voltage		0.7 x V_{DD}		V
$V_{IL(SCL)}$	SCL low level input voltage			0.3	V
$V_{IH(SCL)}$	SCL high level input voltage		0.7 x V_{DD}		V
I_{IN}	I²C SDA, SCL input current	(0.1 x V_{DD}) <V_{IN} < (0.9 x V_{DD})	-10	10	µA
$t_{r(SDA)}$	I²C SDA rise time		20 + 0.1 C_b	300	ns
$t_{r(SCL)}$	I²C SCL rise time		20 + 0.1 C_b	300	ns
$t_{f(SDA)}$	I²SDA fall time		20 + 0.1 C_b	300	ns
$t_{f(SCL)}$	I²C SCL fall time		20 + 0.1 C_b	300	ns
$t_{su(SDA)}$	SDA set-up time		100		ns
$t_{h(SDA)}$	SDA hold time			0.9	µs
$t_{su(STA)}$	Repeated start condition setup		0.6		µs
$t_{su(STO)}$	Top condition set-up time		0.6		µs
$t_{w(START/STOP)}$	Stop to start condition time (bus free)		1.3		µs
$t_{w(SCLL)}$	SCL clock low time		1.3		µs
$t_{w(SCLH)}$	SCL clock high time		0.6		µs
C_b	Capacitance for each bus line			400	pF
C_I	Capacitance for each I/O pin			10	pF

Values based on standard I²C protocol requirement.

Figure 3: Rise/fall time test setup

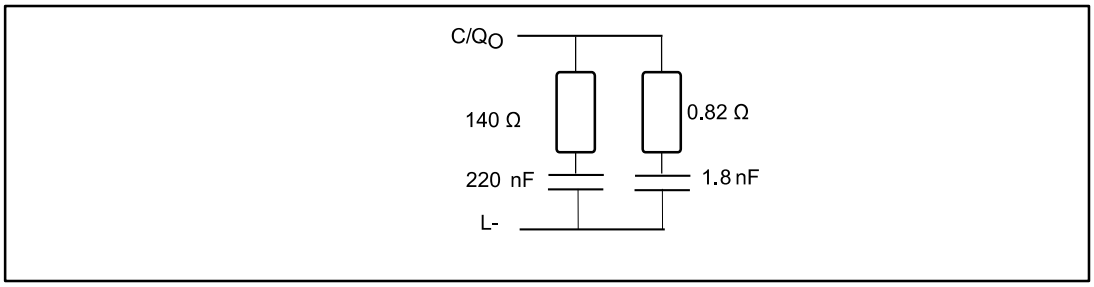


Figure 4: Normalized rise and fall time vs. output capacitor value (typ. values in push-pull configuration)

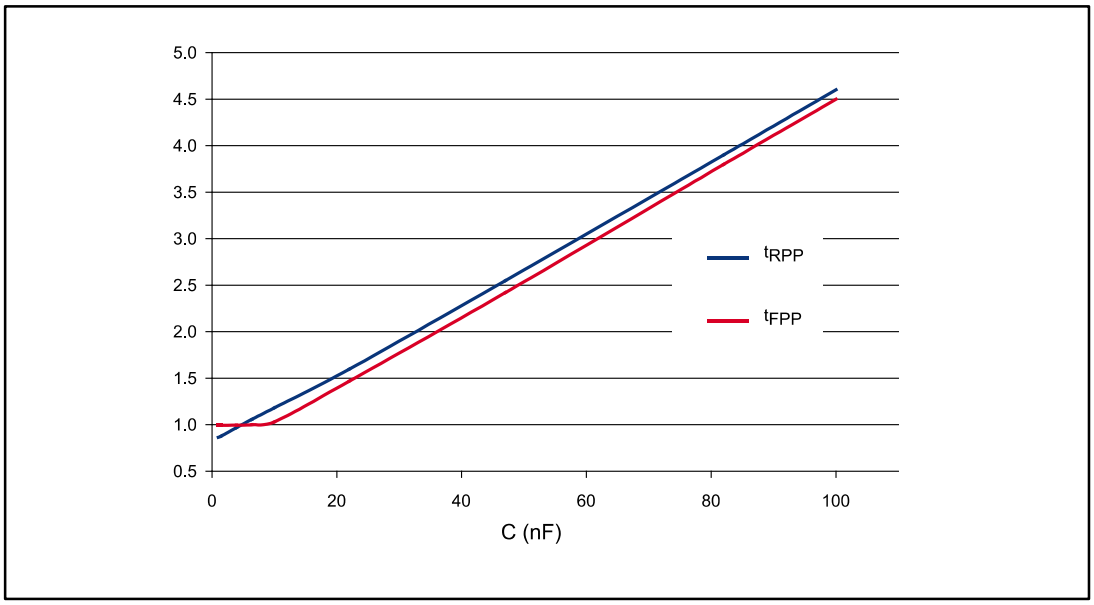


Table 10: Main parameter typical variations vs. +/- 1% variation of Rbias value

Symbol	Parameter	Typ. variation vs. R_{bias}		
		R_{bias} [kΩ]		
		122.74	124	125.24
I_s	Supply current	0.76%	0	-0.50%
$I_{INC/Qi}$	Input current C/Q$_I$ pin (5.5 mA)	0.93%	0	-0.93%
$I_{INC/Qi}$	Input current C/Q$_I$ pin (2.5 mA)	0.75%	0	-1.13%
$I_{INI/Q}$	Input current I/Q pin (2.5 mA)	0.85%	0	-0.85%
t_{dcoq}	C/Q$_O$ low- and high-side cut-off current delay time	-2.44%	0	2.00%
I_{COQ}	C/Q$_O$ low- and high-side cut-off current (115 mA)	1.19%	0	-1.28%
t_{dcol}	L+ cut-off current delay time (500 µs)	-0.95%	0	0.47%
I_{COL}	L+ cut-off current	1.36%	0	-0.91%
t_{rcol}	L+ restart delay time	-0.93%	0	0.97%
V_{UV}	Undervoltage ON-threshold	0.00%	0	0.00%

Symbol	Parameter	Typ. variation vs. R_{bias}		
		R_{bias} [kΩ]		
		122.74	124	125.24
V_{DD}	Linear regulator output voltage (3.3 V)	-0.03%	0	0.03%
V_{DD}	Linear regulator output voltage (5 V)	-0.02%	0	0.02%
I_{LIMQ}	C/Q_O high-side limitation current	0.64%	0	-0.71%
I_{LIMQ}	C/Q_O low-side limitation current	0.28%	0	-1.47%
I_{LIML}	L+ limitation current	0.47%	0	-2.09%
V_{QTHH}	C/Q_I and I/Q upper voltage threshold	0.00%	0	0.00%
V_{QTHL}	C/Q_I and I/Q lower voltage threshold	0.00%	0	0.00%
V_{QHY}	C/Q and I/Q hysteresis voltage	0.00%	0	0.00%
t_{rPP}	C/Q rise time in push-pull configuration	-1.59%	0	1.18%
t_{fPP}	C/Q fall time in push-pull configuration	-2.14%	0	0.94%
$t_{dINC/Q}$	$IN_{C/Q}$ to C/Q_O propagation delay time	-1.44%	0	0.75%
$t_{dINC/Q}$	$IN_{C/Q}$ to C/Q_O propagation delay time	-2.36%	0	0.18%
$t_{dC/Qi}$	C/Q_I to $OUT_{C/Q}$ propagation delay time	0.49%	0	1.13%
$t_{dC/Qi}$	C/Q_I to $OUT_{C/Q}$ propagation delay time	1.82%	0	0.03%
t_{dbq}	C/Q_I debounce time (100 µs)	-1.76%	0	1.50%
t_{dcoq}	C/Q_O low- and high-side cut-off current delay time (200 µs)	-1.27%	0	2.00%
I_{COQ}	C/Q_O low-side cut-off current (220 mA)	0.39%	0	-1.56%
I_{COQ}	C/Q_O low-side cut-off current (350 mA)	0.36%	0	-1.43%
I_{COQ}	C/Q_O low-side cut-off current (580 mA)	0.65%	0	-1.72%
t_{rcoq}	C/Q_O restart delay time	-0.90%	0	0.97%
I_{COQ}	C/Q_O high-side cut-off current (220 mA)	0.84%	0	-0.84%
I_{COQ}	C/Q_O high-side cut-off current (350 mA)	1.38%	0	-0.69%
I_{COQ}	C/Q_O high-side cut-off current (580 mA)	1.08%	0	-1.08%

6 Device configuration

SDA and SCL configure the L6360 device through I²C.

6.1 Introduction

The I²C bus interface serves as an interface between the microcontroller and the serial I²C bus. It provides single master functions, and controls all I²C bus-specific sequencing, protocol and timing. It supports fast I²C mode (400 kHz).

6.2 Main features

- Parallel bus/I²C protocol converter
- Interrupt generation
- Fast I²C mode
- 7-bit addressing

6.3 General description

In addition to receiving and transmitting data, this interface converts it from serial to parallel format and vice versa. The interface is connected to the I²C bus by a data pin (SDA) and a clock pin (SCL).

6.4 SDA/SCL line control

SDA is a bi-directional line, SCL is the clock input. SDA should be connected to a positive supply voltage via a current-source or pull-up resistor. When the bus is free, both lines are HIGH. The output stages of the devices connected to the bus must have an open drain or open collector output to perform the wired AND function. Data on the I²C bus can be transferred to rates up to 400 Kbit/s in fast mode. The number of interfaces connected to the bus is limited by the bus capacitance. For a single master application, the master's SCL output can be a push-pull driver provided that there are no devices on the bus which would stretch the clock. Transmitter mode: the microcontroller interface holds the clock line low before transmission. Receiver mode: the microcontroller interface holds the clock line low after reception. When the I²C microcontroller cell is enabled, the SDA and SCL ports must be configured as floating inputs. In this case, the value of the external pull-up resistors used depends on the application. When the I²C microcontroller cell is disabled, the SDA and SCL ports revert to being standard I/O port pins. On the L6360, the SDA output is an open drain pin.

6.5 Mode selection

Possible data transfer formats are:

- The master transmitter transmits to the slave receiver. The transfer direction is not changed
- The slave receiver acknowledges each byte
- The master reads data from the slave immediately after the first byte (see *Figure 6: "A master reads data from the slave immediately after the first byte"*). At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter

This first acknowledge is still generated by the slave. Subsequent acknowledges are generated by the master. The STOP condition is generated by the master which sends a not-acknowledge (A) just prior to the STOP condition.

Figure 5: A master transmitter addressing a slave receiver with a 7-bit address (the transfer is not changed)

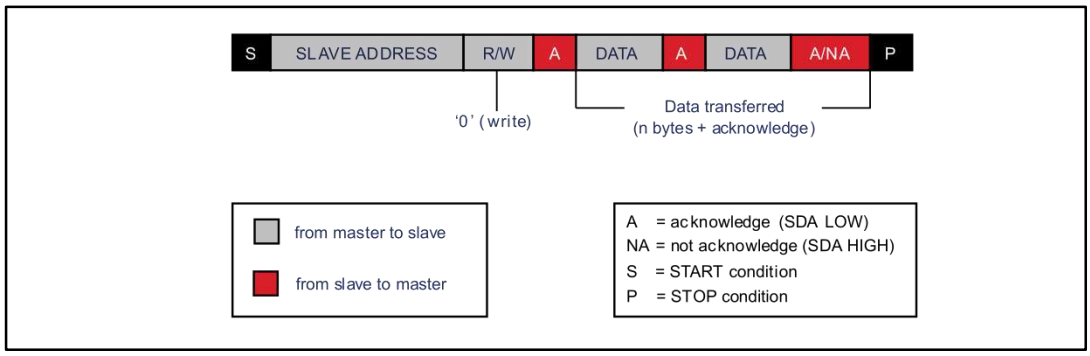
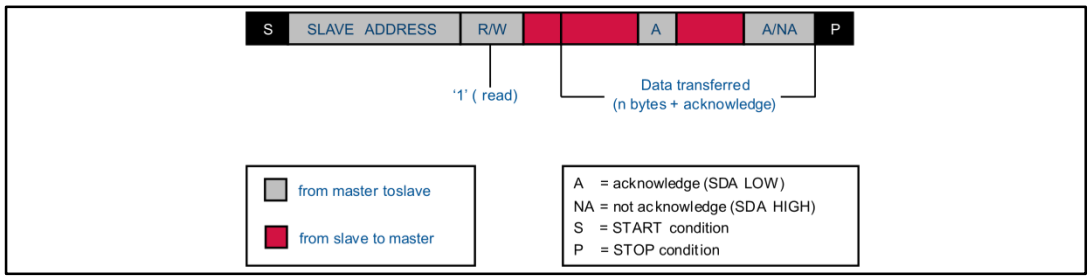


Figure 6: A master reads data from the slave immediately after the first byte



On the microcontroller, the interface can operate in the two following modes:

- Master transmitter/receiver
- Idle mode (default state)

The microcontroller interface automatically switches from idle to master receiver after it detects a START condition and from master receiver to idle after it detects a STOP condition. On the L6360 the interface can operate in the two following modes:

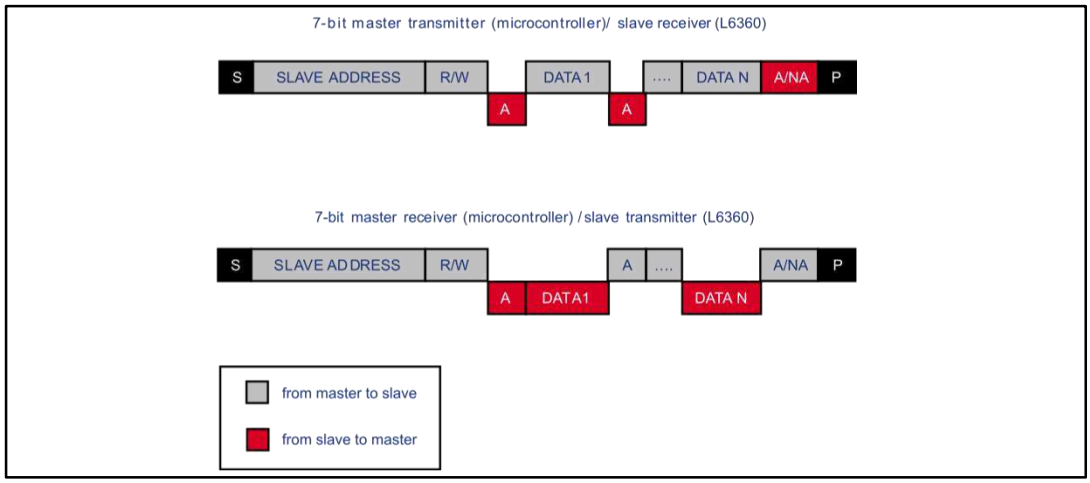
- Slave transmitter/receiver
- Idle mode (default state)

The interface automatically switches from idle to slave transmitter after it detects a START condition and from slave transmitter to idle after it detects a STOP condition.

6.6 Functional description

By default, the I²C microcontroller interface operates in idle; to switch from default idle mode to master mode a START condition generation is needed. The transfer sequencing is shown in the picture below.

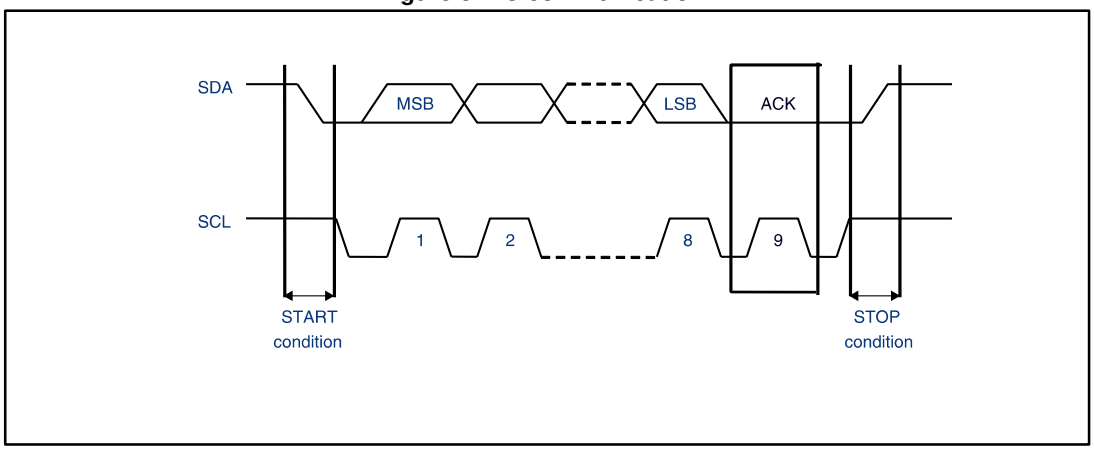
Figure 7: Transfer sequencing



6.7 Communication flow

The communication is managed by the microcontroller that generates the clock signal. A serial data transfer always begins with a START condition and ends with a STOP condition. Data is transferred as 8-bit bytes, MSB first. The first byte following the START condition contains the address (7 bits). The 9th clock pulse follows the 8th clock cycle of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter.

Figure 8: I²C communication



Each byte is followed by an acknowledgment bit as indicated by the A or A blocks in the sequence. A START condition immediately followed by a STOP condition (void message) is a prohibited format.

6.8 I²C address

Each I²C connected to the bus is addressable by a unique address. The I²C address is 7 bits long, and there is a simple master/slave relationship. The LSB of the L6360 address can be programmed by means of dedicated IC pins (SA0, SA1 and SA2, which can be hard wired to V_{DD} or GND, or handled by µC outputs): the microcontroller can interface up to 8 L6360 ICs. The I²C inside the device has 5 pins:

- SDA: data
- SCL: clock
- SA0: LSB of the L6360 address
- SA1: bit 1 of the L6360 address
- SA2: bit 2 of the L6360 address

The I²C L6360 IC address is:

- Fixed part (4 MSBits): set to “1100”
- Programmable part (3 LSBits) by hardware: from “000 to 111" connecting SAx pins to GND or VDD

In the L6360 the SDA is an open drain pin.

6.9 Internal register

The L6360 has some internal registers to perform control, configuration, and diagnostic operations. These registers are listed below:

- Status register
- Configuration register
- Control register 1
- Control register 2
- LED1 register MSB
- LED1 register LSB
- LED2 register MSB
- LED2 register LSB
- Parity register

Each register is addressable as follows:

Table 11: Register addresses

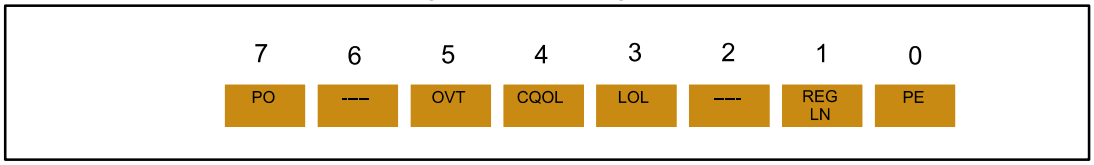
Address	Register name
0000	Status register
0001	Configuration register
0010	Control register 1
0011	Control register 2
0100	LED1 MSB
0101	LED1 LSB
0110	LED2 MSB
0111	LED2 LSB
1000	Parity register

Status register

Read only

Reset value: [00000000]

Figure 9: Status register

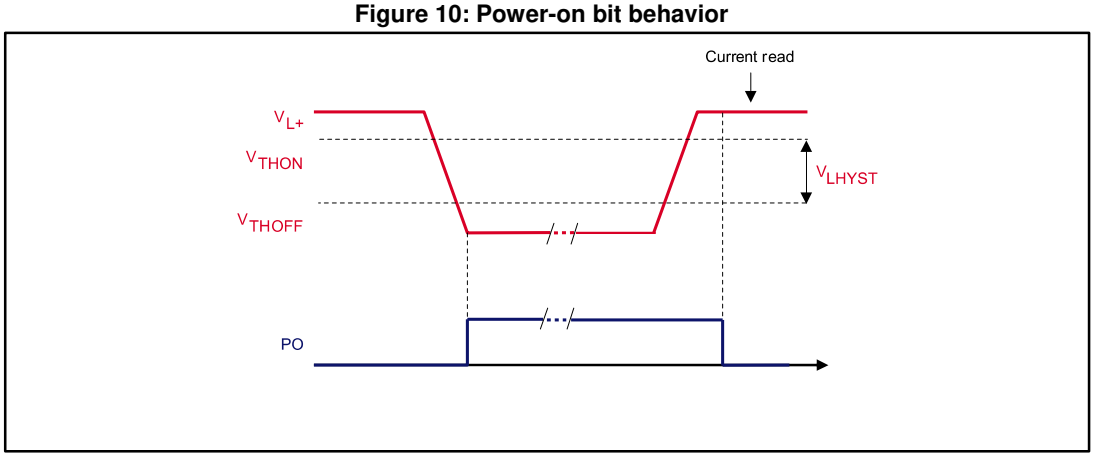


The status register stores diagnostic information. It can be read to check the status of the run-time of the device (faults, warning, transmission corrupted, etc.). When a fault condition occurs, a bit (corresponding to the fault condition) in the status register is set and an interrupt (via the IRQ pin) is generated. If there is no persistent fault condition, the status register is cleared after a successful current read.

Bit 7 = PO: Power-on (L+ line)

This bit indicates the status of L+ line voltage. If the voltage goes under the lower threshold (V_{LTHOFF}) and EN_{L+} is high, the PO bit is set. It is reset after a successful current read if the L+ voltage has returned above the upper threshold V_{LTHON} and the read operation has begun after the bit has been set. When the PO bit is high, IRQ is generated. During EN_{L+} transition (from low-level to high-level) and during L+ line voltage transition, a fault condition is reported setting the PO bit and activating the IRQ pin. To reset the fault a successful current read is necessary.

Figure 10: Power-on bit behavior

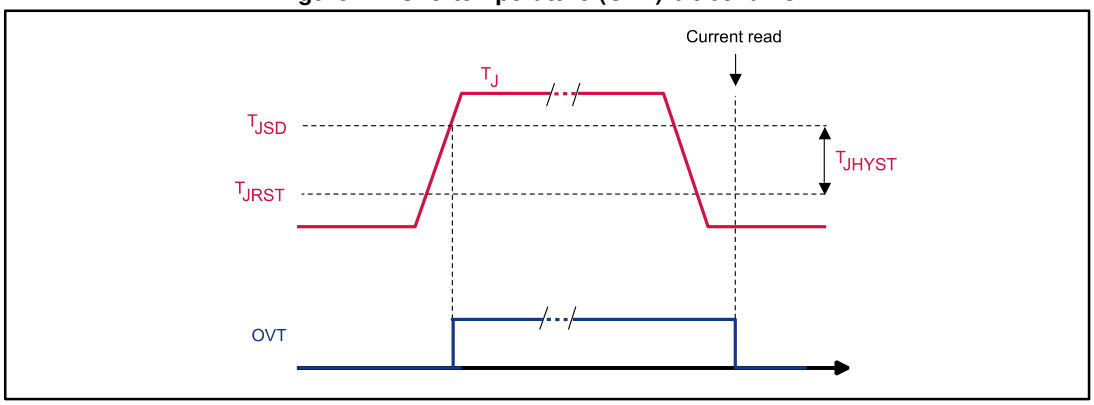


Bit 6 = not used: always at zero

Bit 5 = OVT: overtemperature fault

This bit indicates the status of the IC internal temperature. If the temperature goes above the thermal shutdown threshold ($T > T_{JSD}$) the OVT bit is set. It is reset after a successful current read if the temperature has returned below the thermal restart threshold (T_{JDS} - T_{JHIST}) and the read operation has begun after the bit has been set. When OVT bit is high, the power outputs are disabled and IRQ is generated.

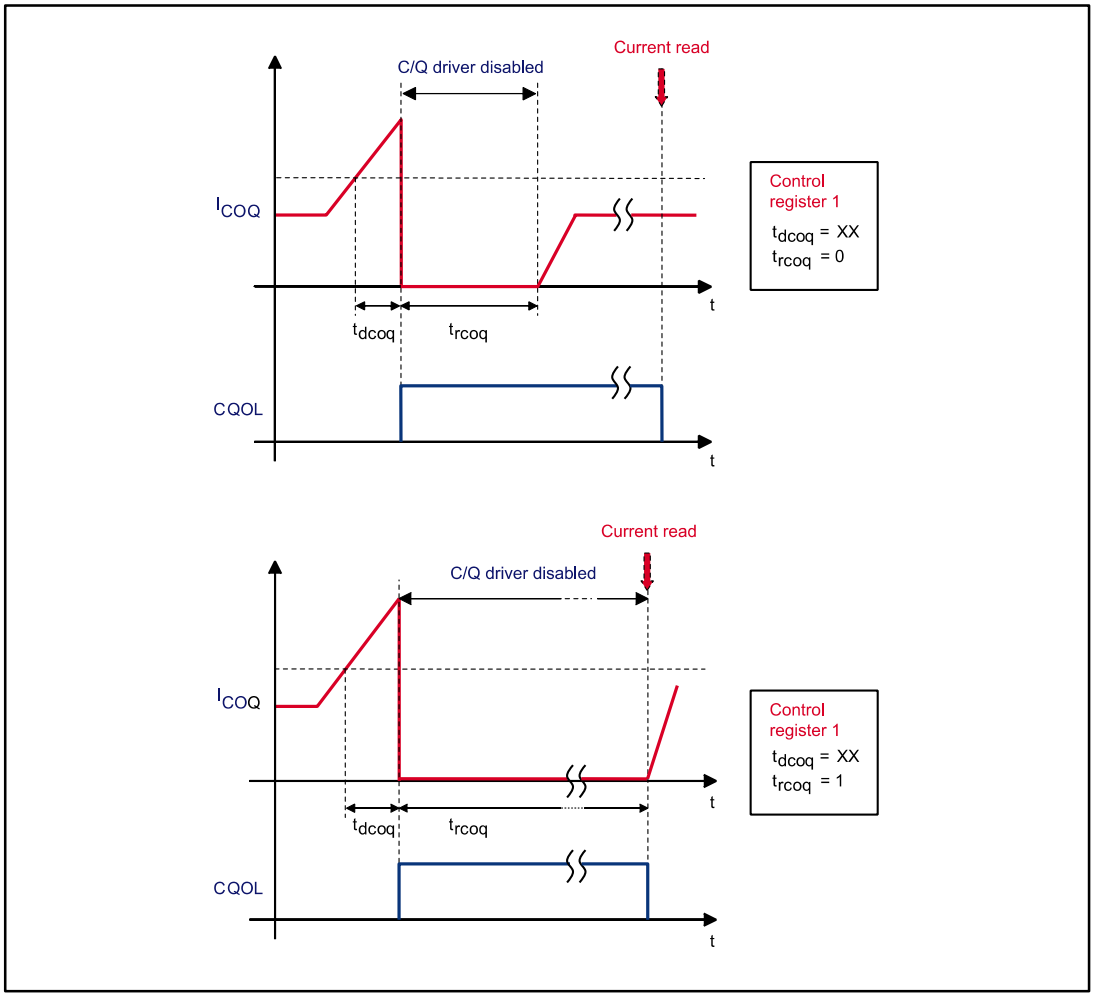
Figure 11: Overtemperature (OVT) bit behavior



Bit 4 = CQOL: C/Q overload

This bit is set if a cut-off occurs on the C/Q channel. It is reset after a successful current read if the restart delay time (t_{rcoq}) has elapsed or the protection is latched (bit t_{rcoq} = 1). The read operation should begin after the CQOL bit has been set. When CQOL bit is high, IRQ is generated. When CQOL bit is high and the protection is latched (bit t_{rcoq} = 1 in control register 1), the C/Q power output is disabled. See next figure.

Figure 12: Cut-off behavior



Bit 3 = LOL: L+ overload

This bit is set if a cut-off occurs on the L+ driver. It is reset after a successful current read if the restart delay time (t_{rcol}) has elapsed or the protection is latched (bit t_{rcol} = 1 in control register 2). The read operation should begin after the LOL bit has been set. When LOL bit is high, IRQ is generated. When LOL bit is high and the protection is latched (bit t_{rcol} = 1 in control register 2), the L+ power output is disabled. The behavior is the same as the C/Q driver (see *Figure 12: "Cut-off behavior"*).

Bit 2 = not used: always at zero

Bit 1 = REG LN: linear regulator undervoltage fault

This bit is set in case of undervoltage of the linear regulator output (V_{REGLNL}). It is reset after a successful current read if the linear regulator output has returned to normal operation and the read operation has begun after the bit has been set. When REGLN bit is high, IRQ is generated.

Bit 0 = PE: parity check error

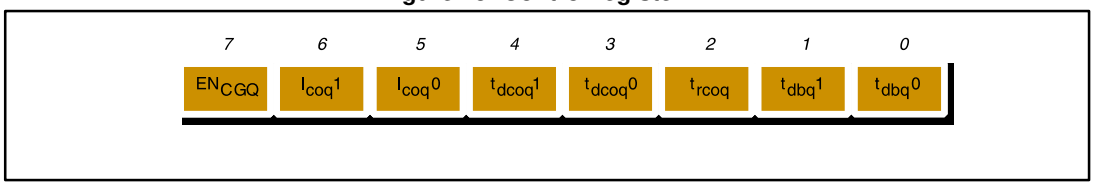
This flag is set if parity error occurs.

Control register 1

Read/write

Reset value: [00100001]

Figure 13: Control register 1



The control register holds the parameters to control the L6360.

Bit 7 = EN_{CGQ}: C/Q_I pull-down enable

Table 12: EN_{CGQ}: C/Q pull-down enable

EN_{CGQ}	Pull-down generator status	
0	Always OFF	
1	If $EN_{C/Q}$ = 0	ON
	If $EN_{C/Q}$ = 1	OFF

Bit 6:5 = I_{COQ} [1:0]: C/Q_O HS and LS cut-off current

This bit is used to configure the cut-off current value on the C/Q channel, as shown in the following table.

Table 13: I_{coq}: C/QO HS and LS cut-off current

I_{coq}[1]	I_{coq}[0]	Typ.
0	0	115 mA
0	1	220 mA
1	0	350 mA
1	1	580 mA

Bit 4:3 = t_{dcoq} [1:0]: C/Q_O HS and LS cut-off current delay time

The channel output driver is turned off after a delay (t_{dcoq}) programmable by means of these two bits.

Table 14: t_{dcoq}: C/QO HS and LS cut-off current delay time

t_{dcoq}[1]	t_{dcoq}[0]	Typ.
0	0	100 µs
0	1	150 µs
1	0	200 µs
1	1	250 µs(1)

Notes:

(1)According to power dissipation at 2 kHz switching, C < 1 µF and power dissipation 0.7 W.

Bit 2 = t_{rcoq}: C/Q_O restart delay time

After a cut-off event, the channel driver automatically restarts after a delay (t_{rcoq}) programmable by means of this bit.

Table 15: t_{rcoq}: C/QO restart delay time

t_{rcoq}	Typ.
0	255x t_{dcoq}
1	Latched(1)

Notes:

(1)Unlatch through I^2C communication (reading or writing any internal register).

Bit 1:0 = t_{dbq} [1:0]: C/Q_I debounce time

Debounce time is the minimum time that data must be in a given state after a transition. It is a programmable time, and can be configured as shown in the following table.

Table 16: t_{dbq}: C/QI debounce time

t_{dbq}[1]	t_{dbq}[0]	Typ.
0	0	0 µs
0	1	5 µs
1	0	20 µs
1	1	100 µs

Control register 2

Read/write

Reset value: [0x100001]