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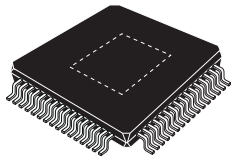
L6460

SPI configurable stepper and DC multi motor driver

Features

- Operating supply voltage from 13 V to 38 V
- 4 full bridge driver configurable in multi-motor application to drive:
  - 2 DC and 1 stepper motor
  - 4 DC motor
- Bridge 1 and 2 (R_{DSon} = 0.60 Ω) can be configured to work as:
  - Dual full bridge driver
  - Super DC driver
  - 2 half bridge driver
  - 1 super half bridge
  - 2 power switches
  - 1 super power switch
- Bridge 3 and 4 (R_{DSon} = 0.85 Ω) can be configured to work as:
  - Same as bridges 1 and 2, listed above
  - Stepper motor driver: up to 1/16 microstepping
  - 2 buck regulators (bridge 3)
  - 1 super buck regulator
  - Battery charger (bridge 4)
- Power supply management
  - One switching buck regulator
  - One switching regulator controller
  - One linear regulator
  - One battery charger
- Fully protected through
  - Thermal warning and shutdown
  - Overcurrent protection
  - Undervoltage lock-out
- SPI interface
- Programmable watchdog function
- Integrated power sequencing and supervisory functions with fault signaling through serial interface and external reset pin
- Very low power dissipation in shut-down mode (~35 mW)



TQFP64 exposed pad

- Auxiliary features
  - Multi-channels 9 bit ADC
  - 2 operational amplifiers
  - Digital comparator
  - 2 low voltage power switches
  - 3 general purpose PWM generators
  - 14 GPIOs

Description

The L6460 is optimized to control and drive multi-motor system providing a unique level of integration in term of control, power and auxiliary features. Thanks to the high configurability L6460 can be customized to drive different motor architectures and to optimize the number of embedded features, such as the voltage regulators, the high precision A/D converter, the operational amplifier and the voltage comparators. The possibility to drive simultaneously stepper and DC motor makes L6460 the ideal solution for all the application featuring multi motors.

Table 1. Device summary

Order code	Package	Packing
L6460	TQFP64	Tray
L6460TR		Tape and reel

Contents

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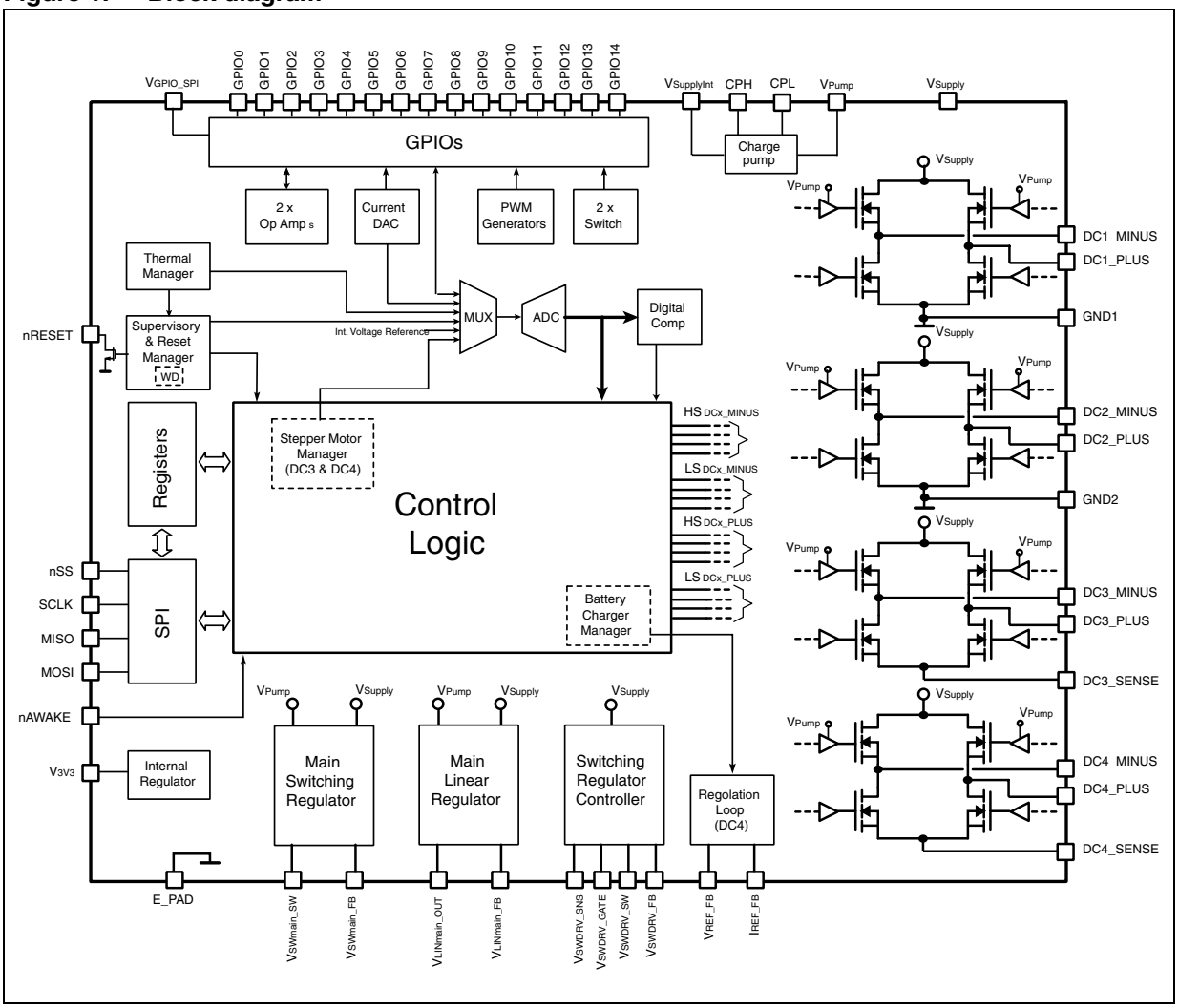
1 General description

1.1 Overview

L6460 offers the possibility to control and power multi motor systems, through the management of simultaneous driving of stepper and DC motor. A number of features can be configured through the digital interface (SPI), including 3 voltage regulators, 1 high precision A/D converter, 2 operational amplifiers and 14 configurable GPIOs.

The high flexibility allows the possibility to configure two, one full or half bridge to work as power stage featuring additional voltage buck regulators.

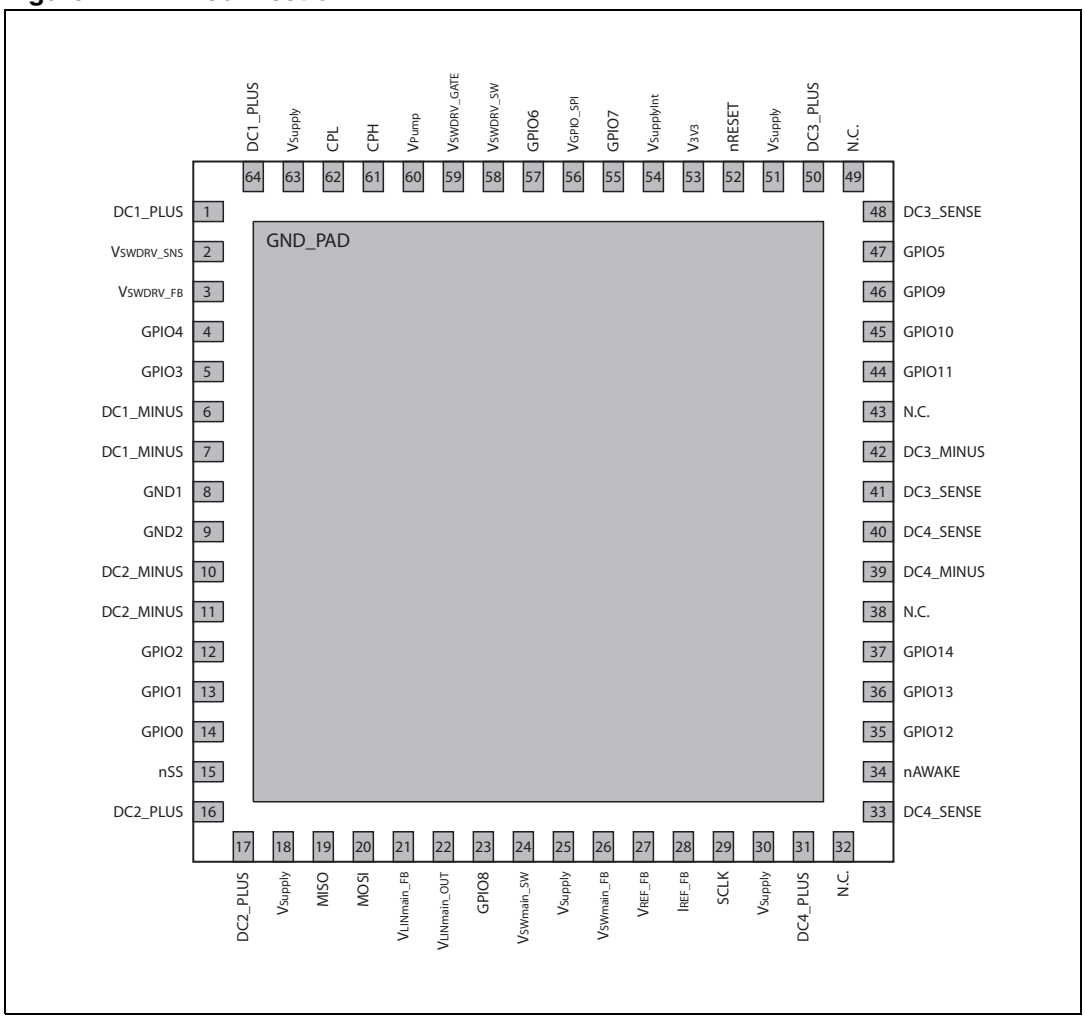
Figure 1. Block diagram



Note: See following Chapter 2 for a detailed description of possible configurations.

1.2 Pin connection

Figure 2. Pin connection



1.3 Pin list

Table 2. Pins configuration

Pin #	Pin name	Description	Type
1	DC1_PLUS	Bridge 1 phase “plus” output	Output
2	V_{SWDRV_SNS}	Switching regulator controller sense	Analog input
3	V_{SWDRV_FB}	Switching regulator controller feedback	Analog input
4	GPIO4	General purpose I/O	Analog In/Out - CMOS bi-dir
5	GPIO3	General purpose I/O	Analog In/Out - CMOS bi-dir
6	DC1_MINUS	Bridge 1 phase “minus” output	Output
7	DC1_MINUS	Bridge 1 phase “minus” output	Output
8	GND1	Ground pin for bridge1(1)(2)(3)	Power/digital
9	GND2	Ground pin for bridge2(1)(2)(3)	Power/digital
10	DC2_MINUS	Bridge 2 phase “minus” output	Output
11	DC2_MINUS	Bridge 2 phase “minus” output	Output
12	GPIO2	General purpose I/O	Analog In/Out - CMOS bi-dir
13	GPIO1	General purpose I/O	Analog In/Out - CMOS bi-dir
14	GPIO0	General purpose I/O	Analog Input - CMOS input
15	nSS	SPI chip select pin	CMOS input
16	DC2_PLUS	Bridge 2 phase “plus” output	Output
17	DC2_PLUS	Bridge 2 phase “plus” output	Output
18	V_{Supply}	Main voltage supply	Power input
19	MISO	SPI serial data output	CMOS output
20	MOSI	SPI serial data input	CMOS input
21	$V_{LINmain\_FB}$	Linear main regulator feedback	Analog input
22	$V_{LINmain\_OUT}$	Linear main regulator output	Power output
23	GPIO 8	General purpose I/O	Analog In/Out - CMOS bi-dir
24	V_{SWmain_SW}	Main switching regulator switching output	Power output
25	V_{Supply}	Main voltage supply	Power Input
26	V_{SWmain_FB}	Main switching regulator feedback pin	Analog input
27	V_{REF_FB}	Regulator voltage feedback	Analog input
28	I_{REF_FB}	Regulator current feedback	Analog input
29	SCLK	SPI input clock pin	CMOS input
30	V_{Supply}	Main voltage supply	Power input
31	DC4_PLUS	Bridge 4 phase “plus” output	Output
32	N.C.	Not connected	
33	DC4_SENSE	Bridge 4 sense output(4)	Output
34	nAWAKE	Device wake up	CMOS input

Table 2. Pins configuration (continued)

Pin #	Pin name	Description	Type
35	GPIO12	General purpose I/O	Analog In/Out - CMOS bi-dir
36	GPIO13	General purpose I/O	Analog In/Out - CMOS bi-dir
37	GPIO14	General purpose I/O	Analog In/Out - CMOS bi-dir
38	N.C.	Not connected	
39	DC4_MINUS	Bridge 4 phase “minus” output	Output
40	DC4_SENSE	Bridge 4 sense output(4)	Output
41	DC3_SENSE	Bridge 3 sense output(4)	Output
42	DC3_MINUS	Bridge 3 phase “minus” output	Output
43	N.C.	Not connected	
44	GPIO11	General purpose I/O	Analog In/Out - CMOS bi-dir
45	GPIO10	General purpose I/O	Analog In/Out - CMOS bi-dir
46	GPIO9	General purpose I/O	Analog In/Out - CMOS bi-dir
47	GPIO5	General purpose I/O	Analog In/Out - CMOS bi-dir
48	DC3_SENSE	Bridge 3 sense output(4)	Output
49	N.C.	Not connected	
50	DC3_PLUS	Bridge 3 phase “plus” output	Output
51	V_{Supply}	Main voltage supply	Power input
52	nRESET	Open drain system reset pin	CMOS Input/output
53	V_{3v3}	Internal 3.3 volt regulator	Power Input/output
54	$V_{SupplyInt}$	Internal voltage supply	Power Input
55	GPIO7	General purpose I/O	Analog In/Out - CMOS bi-dir
56	V_{GPIO_SPI}	Low voltage pins power supply	Power input
57	GPIO6	General purpose I/O	Analog In/Out - CMOS bi-dir
58	V_{SWDRV_SW}	Switching regulator controller source input	Power input
59	V_{SWDRV_GATE}	Switching driver gate drive pin	Analog output
60	V_{Pump}	Charge pump voltage	Power Input/output
61	CPH	Charge pump high switch pin	Power Input/output
62	CPL	Charge pump low switch pin	Power Input/output
63	V_{Supply}	Main voltage supply	Power input
64	DC1_plus	Bridge 1 phase “plus” output	Output
E_Pad	GND_PAD	(1)(2)(3)	

1. These pins must be connected all together to a unique PCB ground.
2. Bridges1 and 2 have 2 ground pads: one is bonded to the relative ground pin (GND1 or GND2) and the other is connected to exposed pad (E_Pad) ground ring. This makes the bond wires testing possible by forcing a current between E-Pad and GND1 or GND2 pins and using the other pin as sense pin to measure the resistance of E-Pad bonding. (N.B: grounds of two bridges are internally connected together).
3. The analog ground is connected to exposed pad E-Pad.
4. The pin must be tied to ground if bridge is not used as a stepper motor.

2 L6460's main features

L6460 includes the following circuits:

- Four widely configurable full bridges:
  - Bridges 1 and 2:
    - Diagonal R_{DSon}: 0.6 Ω typ.
    - Max operative current = 2.5 A.
  - Bridges 3 and 4:
    - Diagonal R_{DSon}: 0.85 Ω typ.
    - Max operative current = 1.5 A.
- Possible configurations for each bridge are the following:
  - Bridge 1:
    - DC motor driver.
    - Super DC (bridge 1 and 2 paralleled form superbridge1).
    - 2 independent half bridges.
    - 1 super half bridge (bridge 1 side A and bridge 1 side B paralleled form superhalfbridge1).
    - 2 independent switches (high or low side).
    - 1 super switch (high or low side).
  - Bridge 2 has the same configurations of bridge 1.
  - Bridge 3 has the same configurations of bridge 1 (bridge 3 and 4 paralleled form superbridge2) plus the following:
    - ½ stepper motor driver.
    - 2 buck regulators (V_{AUX1_SW}, V_{AUX2_SW}).
    - 1 Super buck regulator ($V_{AUX1//2\_SW}$).
  - Bridge 4 has the same configurations of bridge 1 plus the following:
    - ½ stepper motor driver.
    - 1 super buck regulator (V_{AUX3_SW}).
    - Battery charger.
- One buck type switching regulator (V_{SWmain}) with:
  - Output regulated voltage range: 1-5 Volts.
  - Output load current: 3.0 A.
  - Internal output power DMOS.
  - Internal soft start sequence.
  - Internal PWM generation.
  - Switching frequency: ~250 kHz.
  - Pulse skipping strategy control.
- One switching regulator controller (V_{SWDRV}) with:
  - Output regulated voltage range: 1-30 Volts.
  - Selectable current limitation.
  - Internal PWM generation.
  - Pulse skipping strategy control.
- One linear regulator ($V_{LINmain}$) that can be used to generate low current/low ripple

voltages. This regulator can be used to drive an external bipolar pass transistor to generate high current/low ripple output voltages.

- One bidirectional serial interface with address detection so that different ICs can share the same data bus.
- Integrated power sequencing and supervisory functions with fault signaling through serial interface and external reset pin.
- Fourteen general purpose I/Os that can be used to drive/read internal/external analog/logic signals.
- One 8-bit/9-bit A/D converter (100 kS/s @ 9-bit, 200 kS/s @8-bit). It can be used to measure most of the internal signals, of the input pins and a voltage proportional to IC temperature.
  - Current sink DAC:
  - Three output current ranges: up to 0.64/6.4/64 mA.
  - 64 (6-bit programmable) available current levels for each range.
  - 5 V output tolerant.
- Two operational amplifiers:
  - 3.3 V supply, rail to rail input compatibility, internally compensated.
  - They can have all pins externally accessible or can be internally configured as a buffer o make internal reference voltages available outside of the chip.
  - Unity gain bandwidth > 1 MHz.
  - They can also be set as comparators with 3.3 V input compatibility and low offset.
- Two 3.3 V pass switches with 1 Ω R_{DSon} and short circuit protected.
- Programmable watchdog function.
- Thermal shutdown protection with thermal warning capability.
- Very low power dissipation in "low power mode" (~35 mW)

L6460 is intended to maximize the use of its components, so when an internal circuit is not used it could be employed for other applications. Bridge 3, for example, can be used as a full bridge or to implement two switching regulators with synchronous rectification: to obtain this flexibility L6460 includes 2 separate regulation loops for these regulators; when the bridge is used as a motor driver, the 2 regulation loops can be redirected on general purpose I/Os to leave the possibility to assembly a switching regulator by only adding an external FET.

3 Electrical specifications

3.1 Absolute maximum rating

The following specifications define the maximum range of voltages or currents for L6460.

Stresses above these absolute maximum specifications may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Parameter	Description	Test condition	Min	Max	Unit
V_{Supply}	V_{Supply} voltage			40	V
V_{GPIO_SPI}	V_{GPIO_SPI} voltage			3.9	V
V_{3V3pin}	V_{3V3} voltage		-0.3	3.9	V
V_{SW}	Switching regulators output pin voltage range		-1	V_{Supply}	V
V_{SW_pulse}	Switching regulators min pulsed voltage	tpulse < 500ns	-3		V
V_{Pump}	Charge pump voltage	(1)		15	V
T_J	Junction temperature(2)	Storage	-40	190	°C
		Operating	-40	TSD	°C

1. This value is useful to define the voltage rating for external capacitor to be connected from V_{Pump} to V_{Supply}. V_{Pump} is internally generated and can never be supplied by external voltage source nor is intended to provide voltage to external loads.
2. TSD is the thermal shut down temperature of the device.

3.2 Operating ratings specifications

Table 4. IC operating ratings

Parameter	Description	Test condition	Min	Max	Unit
V_{Supply}	V_{Supply} voltage range		13 (1)	38	V
I_{Supply}	V_{Supply} operative current	(2)		15	mA
I_{Shut_down}	V_{Supply} shut down state current			1.5	mA
V_{GPIO_SPI}	V_{GPIO_SPI} voltage range		2.4	3.6	V
I_{VGPIO_SPI}	V_{GPIO_SPI} operative current	(3)		0.4	mA
V_{3v3}	3.3V input pin voltage range			3.6	V
$V_{LINmain\_OUT}$	Output pin voltage range	(4)	0	V_{Supply}	V
$V_{LINmain\_FB}$	Feedback pin voltage range		0	3.6	V
V_{SWmain_SW}	Output pin voltage range	(4)	-1	V_{supply}	V
V_{SWDRV_SW}	V_{SWDRV_SW} pin voltage range	(4)	-1	V_{Supply}	V

Table 4. IC operating ratings

Parameter	Description	Test condition	Min	Max	Unit
V_{SWDRV_GATE}	Gate drive pin voltage		0	V_{Pump}	V
V_{SWDRV_SNS}	Sense pin voltage		V_{Supply} -3V	V_{Supply}	V
T_J	Junction temperature	Operating	-40	125	°C

1. For V_{supply} lower than 21 V an external resistor between V_{supply} and $V_{supply\ Int}$ pins are required. For V_{supply} lower than 15 V external diodes for charge pump are required.
2. Operating supply current is measured with system regulators operating but not loaded.
3. Operating V_{GPIO_SPI} current is measured with all circuits supplied by V_{GPIO_SPI} (GPIO's, operational amplifiers and pass switches) enabled but not loaded.
4. The external components connected to the pin must be chosen to avoid that the voltage exceeds this operative range.

3.3 Electrical characteristics

Table 5. Electrical characteristics

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{SupplyInt}$ regulator						
V_{S_Int}	$V_{SupplyInt}$ output voltage	(1)	18	19.5	21	V
I_{S_Int}	$V_{SupplyInt}$ operative current	(2)		11		mA
Charge pump V_{Pump}						
V_{Pump}	Charge pump voltage	V_{Supply}=32V	V_{Supply} + 10.5	V_{Supply} +12.5	V_{Supply} + 14.5	V
F_{Pump}	V_{Pump} clock frequency	F_{OSC} = 16MHz typ		F_{OSC}/64		kHz
V3V3 regulator						
V_{3V3}	V_{3v3} output voltage	V_{Supply}=32V	3.15	3.3	3.45	V
Power on reset						
$V_{Supply\_POR\_valid}$	V_{Supply} voltage for POR valid	I_{nRESET} = 1mA	4			V
$V_{Supply\_POR\_fall}$	V_{Supply} POR falling threshold	V_{Supply} falling	6		8	V
$t_{Supply\_POR\_filt}$	V_{Supply} POR filter Time			3		µs
$V_{3V3\_POR\_fall}$	V_{3v3} POR falling threshold	V_{3V3} falling	1.9	2.2		V
$V_{3V3\_POR\_rise}$	V_{3v3} POR rising threshold	V_{3V3} rising		2.7		V
$V_{3V3\_POR\_hys}$	V_{3v3} POR hysteresis			0.5		V
$t_{3V3\_POR\_filt}$	V_{3v3} POR filter time			1.5		µs
nRESET circuit						
V_{nRST_L}	nRESET low level output voltage	I=10mA			0.4	V

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
t_{nRST_fall}	nRESET fall time	I=1mA C=50pF(3)			15	ns
t_{nRST_del}	nRESET delay time	(4)			150	ns
$V_{Supply\_UV\_f}$	V_{Supply} falling threshold		10.2	11	11.8	V
$V_{Supply\_UV\_r}$	V_{Supply} rising threshold		10.5	11.5	12.5	V
$V_{Supply\_UV\_hys}$	V_{Supply} hysteresis		0.3	0.5	0.7	V
t_{Supply_UV}	V_{Supply} UV filter time			3.5		µs
$V_{S\_Int\_UV\_f}$	$V_{SupplyInt}$ falling threshold		9.7	10.7	11.7	V
$V_{S\_Int\_UV\_r}$	$V_{SupplyInt}$ rising threshold		10.6	11.4	12.2	V
$V_{S\_Int\_UV\_hys}$	$V_{SupplyInt}$ hysteresis		0.4	0.7	1	V
$t_{S\_Int\_UV}$	$V_{SupplyInt}$ UV filter time			3.5		µs
$V_{Pump\_UV\_f}$	V_{Pump} falling threshold		V_{Supply} +7	V_{Supply} + 7.5	V_{Supply} + 8	V
$V_{Pump\_UV\_r}$	V_{Pump} rising threshold		V_{Supply} + 7.5	V_{Supply} + 8	V_{Supply} + 8.5	V
$V_{Pump\_UV\_hys}$	V_{Pump} hysteresis		0.3	0.5	0.7	V
t_{Pump_UV}	V_{Pump} UV filter time			3.5		µs
$V_{GPIO\_SPI\_UV\_f}$	V_{GPIO_SPI} falling threshold		1.8	2		V
$V_{GPIO\_SPI\_UV\_r}$	V_{GPIO_SPI} rising threshold			2.2	2.4	V
$V_{GPIO\_SPI\_hys}$	V_{GPIO_SPI} hysteresis		200	250	300	mV
$t_{GPIO\_SPI\_UV}$	V_{GPIO_SPI} UV filter time			3.5		µs
TSD circuit						
T_{TSD}	Thermal shut down temperature			170		°C
T_{WARM}	Warming temperature			140		°C
T_{DIFF}	Thermal shut down to warming difference			30		°C
t_{TSD_FILT}	Thermal shut down filter time			8		µs
t_{WARM_FILT}	Warming filter time			8		µs
Watchdog						
WD_T_{clk}	Watchdog clock period			$T_{osc} * 2^{22}$		s
Internal clock						
F_{osc}	Oscillator frequency	V_{3V3} = 3.3 V	14.1	16	17.6	MHz
nAWAKE function						
V_{IL}	nAWAKE low logic level voltage				0.8	V

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	nAWAKE high logic level voltage		1.6			V
V_{HYS}	nAWAKE input hysteresis			0.25		V
I_{OUT}	nAWAKE pin output current	nAWAKE=0V(5)	-0.72		-2	mA
I_{INP}	nAWAKE pin input current	nAWAKE=0.8V(5)	0.2		0.4	mA
$t_{AWAKEFILT}$	Filter time			1.2		µs
Main linear regulator						
V_{drop}	Drop out voltage	V_{drop}= V_{supply}-$V_{LINmain\_OUT}$	2			V
I_{PD}	Internal switch pull down current	Linear Main Regulator disabled; $V_{LINmain\_OUT}$=1V		3		mA
$V_{LINmain\_Ref}$	Feedback reference voltage		0.776	0.8	0.824	V
$I_{LINmain\_Ref}$	Feedback pin input current		-2		2	µA
$I_{outLINMax}$	Maximum output current	$V_{LINmain\_OUT}$= V_{supply}-2V	10			mA
I_{short}	Output short circuit current	$V_{LINmain\_OUT}$ =0V, $V_{LINmain\_FB}$ =0V	12	24	32	mA
$\Delta V_{out}/V_o$	Load regulation	$0 \le I_{load} \le I_{outLINMax}$(6)			0.8	%
$\Delta V_{out}/\Delta V_{Supply}$	Line regulation	I_{load} =10mA(6)			0.2	%
V_{loop_acc}	Loop voltage accuracy			±2.5		%
$V_{LIN\_UV\_f}$	Undervoltage falling threshold	(7)	84.5	87	89.5	%
$V_{LIN\_UV\_r}$	Undervoltage rising threshold	(7)	90.5	93	95.5	%
$V_{LIN\_UV\_hys}$	Undervoltage hysteresis			6		%
t_{prim_uv}	Under voltage deglitch filter			5		µs
Main switching regulator						
V_{FBREF}	Main switching regulator feedback reference voltage	SelFBref = ‘00’	0.776	0.8	0.824	V
		SelFBref = ‘01’ (8)	0.97	1	1.03	V
		SelFBref = ‘10’	2.425	2.5	2.575	V
		SelFBref = ‘11’	2.91	3	3.09	V
I_Q	Output leakage current	$T_{junction}$ = 125°C	-40		+40	µA
I_{Q_LP}	Output leakage current in “low power mode”	V_{Supply} = 36V $T_{junction}$ = 125°C	-15		+15	µA
I_{SWmain_FB}	V_{SWmain_FB} pin current	$T_{junction}$ = 125°C	-10		+10	µA
V_{SWmain_OUT}	Output voltage range	(9)	0.8		5	V
I_{load}	Maximum output load current	V_{Supply} = 36V	0.002		3	A
R_{DSonHS}	Internal high side R_{DSon}	I_{load}=1A $T_{junction}$ = 125°C		0.33	0.95	Ω

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{loop}	Loop voltage accuracy			±3%		
$V_{SW\_UV\_f}$	Under voltage falling threshold	(10)	84.5	87	89.5	%
$V_{SW\_UV\_r}$	Under voltage rising threshold	(10)	90.5	93	95.5	%
$V_{SW\_UV\_hys}$	Under voltage hysteresis			6		%
t_{prim_uv}	Under voltage deglitch filter			5		µs
I_{limit}	Current limit protection	SelIlimit ="0" SelIlimit ="1"	3.3 2.3	5 3.5		A A
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time	Normal operating mode (no UV)(11)		450	650	ns
t_{I_limUV}	Current limit response time in UV condition	UV condition (12)		200	400	ns
t_r	Switching output rise time	V_{Supply} = 36V, R_{LOAD} = 422 Ω(13)	5		30	ns
t_f	Switching output fall time	V_{Supply} = 36V, R_{LOAD} = 10 Ω(13)	5		30	ns
F_{SW_PWM}	Operating frequency			Fosc/64		kHz
Switching regulator controller						
V_{GS_ext}	Gate to source voltage for external FET			V_{Pump}		V
I_{SOURCE}	Source current	V_{Pump}=V_{Supply}+12V V_{SWCTR_GATE}=0V	25		50	mA
I_{SINK}	Sink current	V_{SWCTR_GATE} = V_{Supply}	20			mA
t_{SINK}	Sink discharge pulse time			600		ns
$R_{SUSTAIN}$	Gate-source sustain resistance	(V_{SWCTR_GATE} - V_{SWCTR_SRC}) = 0.2V		650		Ω
I_Q	Output leakage current	V_{Supply} = 36V, $T_{junction}$ = 125°C	-40		+40	µA
I_{Q_LP}	Output leakage current in "Low Power Mode"	V_{Supply} = 36V, $T_{junction}$ = 125°C	-5		+5	µA
V_{FBREF}	Switching regulator feedback controller feedback reference voltage	SelFBref = '00' (8)	0.776	0.8	0.824	V
		SelFBref = '01'	0.97	1	1.03	V
		SelFBref = '10'	2.425	2.5	2.575	V
		SelFBref = '11'	2.91	3	3.09	V
I_{SWDRV_FB}	V_{SWDRV_FB} pin current	V_{Supply} = 36V, $T_{junction}$ = 125°C	-10		+10	µA
V_{loop}	Loop voltage accuracy			±3%		

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{SWD\_UV\_f}$	Under voltage falling threshold	(14)	84.5	87	89.5	%
$V_{SWD\_UV\_r}$	Under voltage rising threshold	(14)	90.5	93	95.5	%
$V_{SWD\_UV\_hys}$	Under voltage hysteresis			6		%
t_{prim_uv}	Under voltage deglitch filter			5		µs
V_{ovc}	Over current threshold voltage		250	300	350	mV
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time	Normal operating mode (no UV) (11)		500	900	ns
t_{I_limUV}	Current Limit response time in UV condition.	UV condition (12)		380	550	ns
F_{SWD_PWM}	Operating frequency			$F_{osc}/64$		kHz
Power bridges						
R_{DSon1_2}	Bridge 1 and 2 diagonal R_{DSon}	I = 1.4A, V_{Supply} = 36V, $T_{junction}$ = 125°C		0.6	1.1	Ω
R_{DSon3_4}	Bridge 3 and 4 diagonal R_{DSon}	I = 1A, V_{Supply} = 36V, $T_{junction}$ = 125°C		0.85	1.65	Ω
I_{MAX1_2}	Bridge 1 and 2 operative rms current				2.5	A
I_{MAX3_4}	Bridge 3 and 4 operative rms current				1.5	A
I_{dss}	Output leakage current.	$T_{junction}$ = 125°C	-50		+50	µA
I_{Q_LP}	Output leakage current in “low power mode”	V_{Supply} = 36V, $T_{junction}$ = 125°C	-10		+10	µA
$I_{OC\_LS1\_2}$	Low side current protection for bridges 1 and 2(15)	MtrXSideYILimSel[1:0]=00 MtrXSideYILimSel[1:0]=01 MtrXSideYILimSel[1:0]=10 MtrXSideYILimSel[1:0]=11 (16)	0.6 1.4 2.4 2.4	1 2 3 3	1.6 2.6 3.6 3.6	A
$I_{OC\_HS1\_2}$	High side current protection for bridges 1 and 2(15)	MtrXSideYILimSel[1:0]=00 MtrXSideYILimSel[1:0]=01 MtrXSideYILimSel[1:0]=10 MtrXSideYILimSel[1:0]=11(16)	0.7 1.5 2.5 2.5	1 2 3 3	1.7 2.7 3.7 3.7	A
$I_{OC\_LS3\_4}$	Low side current protection for bridges 3 and 4(15)	MtrXSideYILimSel[1:0]=11 (17)(18)	1.55		2.5	A
$I_{OC\_HS3\_4}$	High side current protection for bridges 3 and 4(15)	MtrXSideYILimSel[1:0]=11(17)(18)	1.6		2.5	A
t_{filter}	Current limit filter time		2		5	µs

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
t_{delay}	Current limit delay time			5		µs
t_{OC_off}	Over current Off time	MtrXIlimitOffTimeY[1:0]=00 MtrXIlimitOffTimeY[1:0]=01 MtrXIlimitOffTimeY[1:0]=10 MtrXIlimitOffTimeY[1:0]=11 (19)		60 120 240 480		µs µs µs µs
t_{r1_2}	Output rise time bridges 1 and 2	V_{Supply} = 36V, resistive load between outputs: R= 25 Ω(20)	100	180	250	ns
t_{r3_4}	Output rise time bridges 3 and 4	V_{Supply} = 36V, resistive load between outputs: R= 36 Ω(20)	50	100	200	ns
t_{f1_2}	Output fall time bridges 1 and 2	V_{Supply} = 36V, resistive load between outputs: R= 25 Ω(20)	100	180	250	ns
t_{f3_4}	Output fall time bridges 3 and 4	V_{Supply} = 36V, resistive load between outputs: R= 36 Ω(20)	50	125	250	ns
$t_{deadRise}$	Anti crossover rising dead time		100	300	450	ns
$t_{deadFall}$	Anti crossover falling dead time		100	300	450	ns
F_{PWM}	Operating frequency			F_{osc}/512		kHz
t_{resp}	Delay from PWM to output transition			500		ns
Bipolar stepper circuitry						
$V_{STEPREF}$	Reference voltage	SelStepRef =0 SelStepRef =1	0.48 0.72	0.50 0.75	0.52 0.78	V
V_{offset}	Sense comparator offset		-12		12	mV
t_{blk}	Blanking time	StepBlkTime = ‘00’ (8)	0.65	0.95	1.25	µs
		StepBlkTime = ‘01’	1	1.45	1.9	µs
		StepBlkTime = ‘10’	1.5	2.25	3	µs
		StepBlkTime = ‘11’	3	4.25	5.5	µs
Synchronous buck regulator (bridge 3)						
V_{AUX_SW}	Output pin voltage range (DC3x)	(26)	-1		V_{Supply}	V
I_Q	Output leakage current	$T_{junction}$ = 125°C	-50		+50	µA
I_{QLP}	Output leakage current in “Low Power Mode”	V_{Supply} = 36V $T_{junction}$ = 125°C	-10		+10	µA

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{FBREF}	Synchronous buck regulator feedback reference voltage	SelFBRef = '00'	0.776	0.8	0.824	V
		SelFBRef = '01' (21)	0.97	1	1.03	V
		SelFBRef = '10' (22)	2.425	2.5	2.575	V
		SelFBRef = '11'	2.91	3	3.09	V
I_{GPIO_FB}	GPIO feedback pin current	$T_{junction}$ = 125°C 0V≤Feedback ≤ 3V	-15		15	µA
V_{out}	Output voltage range	V_{Supply} = 36V(23)	0.8		30	V
I_{load}	Output load current	V_{Supply} = 36V	0.002		1.5	A
R_{DSonHS}	Internal high/low side R_{DSon}	$T_{junction}$ = 125°C; I_{load}=1A		0.6	0.8	Ω
V_{loop}	Loop voltage accuracy			±3%		
$V_{REG\_UV\_f}$	Under voltage falling threshold	(24)	84.5	87	89.5	%
$V_{REG\_UV\_r}$	Under voltage rising threshold	(24)	90.5	93	95.5	%
$V_{REG\_UV\_hys}$	Under voltage hysteresis			6		%
t_{aux_UV}	Under voltage deglitch filter			5		µs
I_{limit}	Current limit protection		1.6		2.5	A
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time	Normal operating mode (no UV) (11)		480	700	ns
t_{I_limUV}	Current limit response time in UV condition.	UV condition (12)		350	500	ns
t_r	Switching output rise time	V_{Supply} = 36V, R_{LOAD} = 422 Ω(25)	5		30	ns
t_f	Switching output fall time	V_{Supply} = 36V, R_{LOAD} = 10 Ω (23)	10		50	ns
t_{dead}	Crossover dead time			100		ns
F_{REGPWM}	Operating frequency			F_{osc}/64		kHz
Battery charger (Bridge 4)						
V_{AUX3_SW}	Output pin voltage range (DC4x)	(26)	-1		V_{Supply}	V
I_Q	Output leakage current	$T_{junction}$ = 125°C	-100		+100	µA
V_{FBRef}	Battery charger control loop feedback reference voltage	SelFBRef = '00'	1.37	1.412	1.455	V
		SelFBRef = '01' (8)	1.746	1.8	1.854	V
		SelFBRef = '10'	2.079	2.143	2.207	V
		SelFBRef = '11'	2.425	2.5	2.575	V

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{CurrRef}$	Battery charger control loop feedback reference current	SelCurrRef = '00' (8)	0.873	0.9	0.927	V
		SelCurrRef = '01'	1.394	1.437	1.48	V
		SelCurrRef = '10'	1.746	1.8	1.854	V
		SelCurrRef = '11'	2.182	2.25	2.318	V
V_{out}	Output voltage range	V_{Supply} = 36V (27)	1.412		30	V
I_{load}	Output load current	V_{Supply} = 36V	0.002		3	A
R_{DSon}	Internal high/low side R_{DSon}	$T_{junction}$ = 125°C; I_{LOAD} = 1.5A		0.3	0.4	Ω
V_{loop}	Loop voltage accuracy			±3%		
$V_{BC\_UV\_f}$	Under voltage falling threshold	(28)	84.5	87	89.5	%
$V_{BC\_UV\_r}$	Under voltage rising threshold	(28)	90.5	93	95.5	%
$V_{BC\_UV\_hys}$	Under voltage hysteresis			6		%
t_{aux_UV}	Under voltage deglitch filter			5		µs
I_{limit}	Current limit protection		3.2		5	A
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time	Normal operating mode (no UV) (11)		480	700	ns
t_{I_limUV}	Current limit response time in UV condition.	UV condition (12)		350	500	ns
t_r	Switching output rise time	V_{Supply} = 36V, R_{LOAD} = 422 Ω (25)	5		30	ns
t_f	Switching output fall time	V_{Supply} = 36V, R_{LOAD} = 10 Ω (25)	10		50	ns
t_{dead}	Crossover dead time			100		ns
F_{BCPWM}	Operating frequency			F_{osc}/64		kHz
ADC with A2DType=0 (29)						
IMR	Measurement range	A2dType = 0	0		V_{3v3}	V
INL	Integral non-linearity	A2dType = 0 (30)(31)			±2	LSB
DNL	Differential non-linearity	A2dType = 0 (32)(31)			±2	LSB
OE	Offset error	A2dType = 0 (33)			±4	LSB
OE_{Drift}	Offset error drift	A2dType = 0 over time and temperature			±3	LSB
GE	Gain error	A2dType = 0 (34)			±4	LSB
GE_{Drift}	Gain error drift	A2dType = 0 over time and temperature			±4	LSB
t_{conv}	Minimum conversion time				55	µs
	Resolution	(35)		8		bits

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
C_{in}	Input sampling capacitance	(36)			4	pF
ADC with A2DType=1 (37)						
IMR	Measurement range	A2dType = 1	0		V_{3v3}	V
INL	Integral non-linearity	A2dType = 1 (30)(31)			±1	LSB
DNL	Differential Non-Linearity	A2dType = 1 (32)(31)			±1	LSB
OE	Offset error	A2dType = 1 (33)			±4	LSB
OE_{Drift}	Offset error drift	A2dType = 1 over time and temperature			±3	LSB
GE	Gain error	A2dType = 1 (34)			±4	LSB
GE_{Drift}	Gain error drift	A2dType = 1 over time and temperature			±4	LSB
t_{conv}	Minimum conversion time				10	µs
	Resolution			9		bits
C_{in}	Input sampling capacitance	(36)			4	pF
Current DAC						
V_R	Pin voltage operative range (GPIO8)	(38)	0.7		5.5	V
I_{OUT_OFF}	Output off leakage current	DacValue[5:0] = 000000	-1		+1	µA
I_{FULL_ERR}	Full scale current error	DacRange[1:0] =xx DacValue[5:0] = 111111	-15		+15	% of $I_{FULL\ typ}$
INL_{10_11}	Integral non-linearity for 10 and 11 ranges				±2	LSB
DNL_{10_11}	Differential non-linearity for 10 and 11 ranges				±2	LSB
INL_{01}	Integral non-linearity for 01 range				±1	LSB
DNL_{01}	Differential non-linearity for 01 range				±1	LSB
$R_{CurrDac\_res}$	Gpio[8] divider total resistance			45		kΩ
$R_{CurrDac\_ratio}$	Gpio[8] divider ratio			3/5		
t_{set}	Settling time	(39)			5	µs
Operational amplifier (40)						
V_{GPIO_SPI}	Operational amplifier supply voltage range		3.15	3.3	3.45	V
V_{ICM}	Input common mode voltage range		0		V_{GPIO_SPI}	V
V_{OUT_MAX}	Output voltage	I_{LOAD} =± 1mA	0.1		3.2	V