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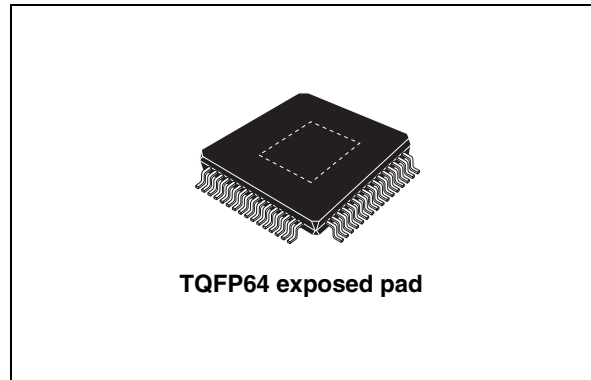
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## SPI configurable stepper and DC multi motor driver

### Features

- Operating supply voltage from 13 V to 38 V
- 4 full bridge driver configurable in multi-motor application to drive:
  - 2 DC and 1 stepper motor
  - 4 DC motor
- Bridge 1 and 2 ( $R_{DSon} = 0.60 \Omega$ ) can be configured to work as:
  - Dual full bridge driver
  - Super DC driver
  - 2 half bridge driver
  - 1 super half bridge
  - 2 power switches
  - 1 super power switch
- Bridge 3 and 4 ( $R_{DSon} = 0.85 \Omega$ ) can be configured to work as:
  - Same as bridges 1 and 2, listed above
  - Stepper motor driver: up to 1/16 microstepping
  - 2 buck regulators (bridge 3)
  - 1 super buck regulator
  - Battery charger (bridge 4)
- Power supply management
  - One switching buck regulator
  - One switching regulator controller
  - One linear regulator
  - One battery charger
- Fully protected through
  - Thermal warning and shutdown
  - Overcurrent protection
  - Undervoltage lock-out
- SPI interface
- Programmable watchdog function
- Integrated power sequencing and supervisory functions with fault signaling through serial interface and external reset pin
- Very low power dissipation in shut-down mode (~35 mW)



- Auxiliary features
  - Multi-channels 9 bit ADC
  - 2 operational amplifiers
  - Digital comparator
  - 2 low voltage power switches
  - 3 general purpose PWM generators
  - 14 GPIOs

### Description

The L6460 is optimized to control and drive multi-motor system providing a unique level of integration in term of control, power and auxiliary features. Thanks to the high configurability L6460 can be customized to drive different motor architectures and to optimize the number of embedded features, such as the voltage regulators, the high precision A/D converter, the operational amplifier and the voltage comparators. The possibility to drive simultaneously stepper and DC motor makes L6460 the ideal solution for all the application featuring multi motors.

**Table 1. Device summary**

Order code	Package	Packing
L6460	TQFP64	Tray
L6460TR		Tape and reel

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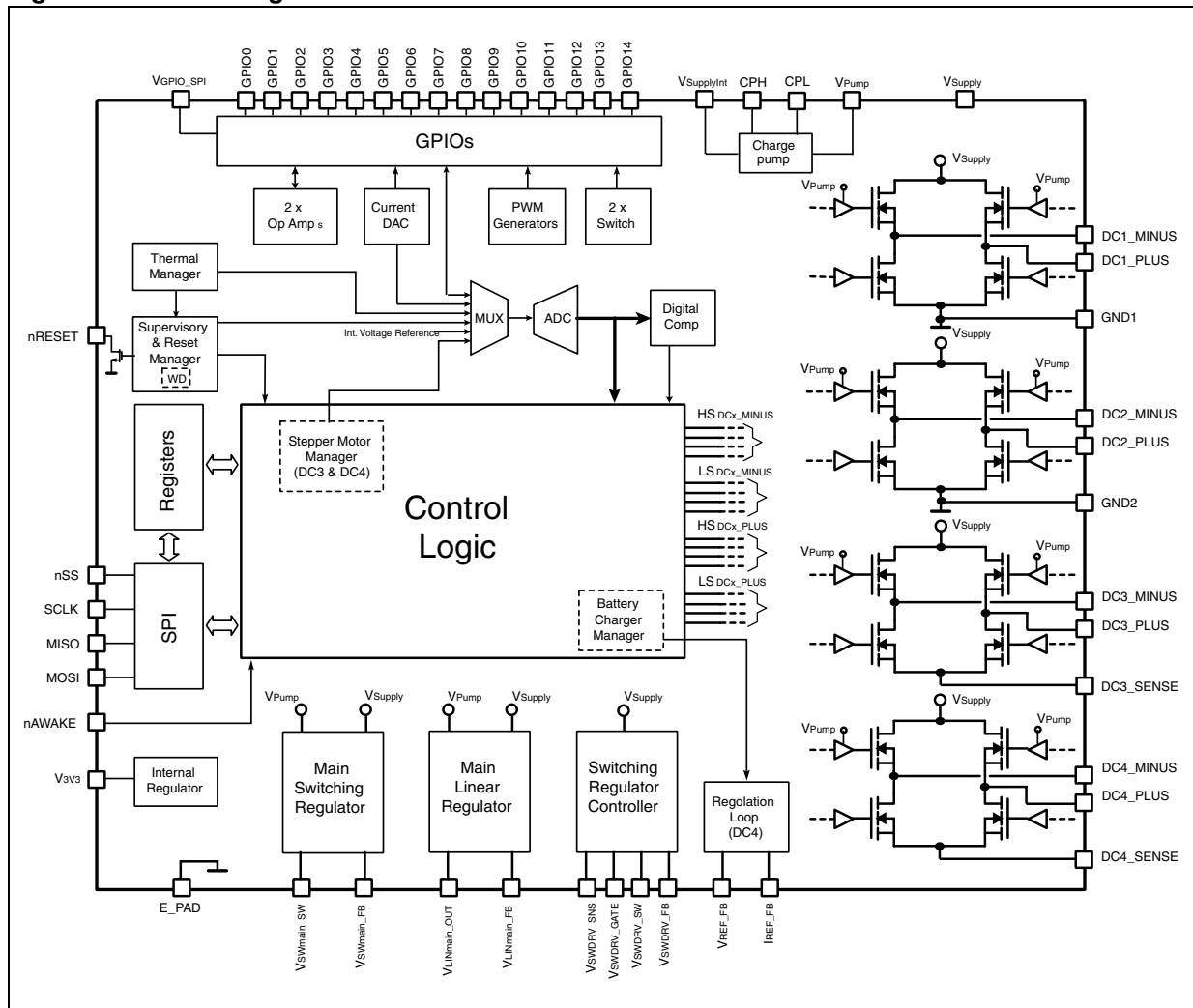
# 1 General description

## 1.1 Overview

L6460 offers the possibility to control and power multi motor systems, through the management of simultaneous driving of stepper and DC motor. A number of features can be configured through the digital interface (SPI), including 3 voltage regulators, 1 high precision A/D converter, 2 operational amplifiers and 14 configurable GPIOs.

The high flexibility allows the possibility to configure two, one full or half bridge to work as power stage featuring additional voltage buck regulators.

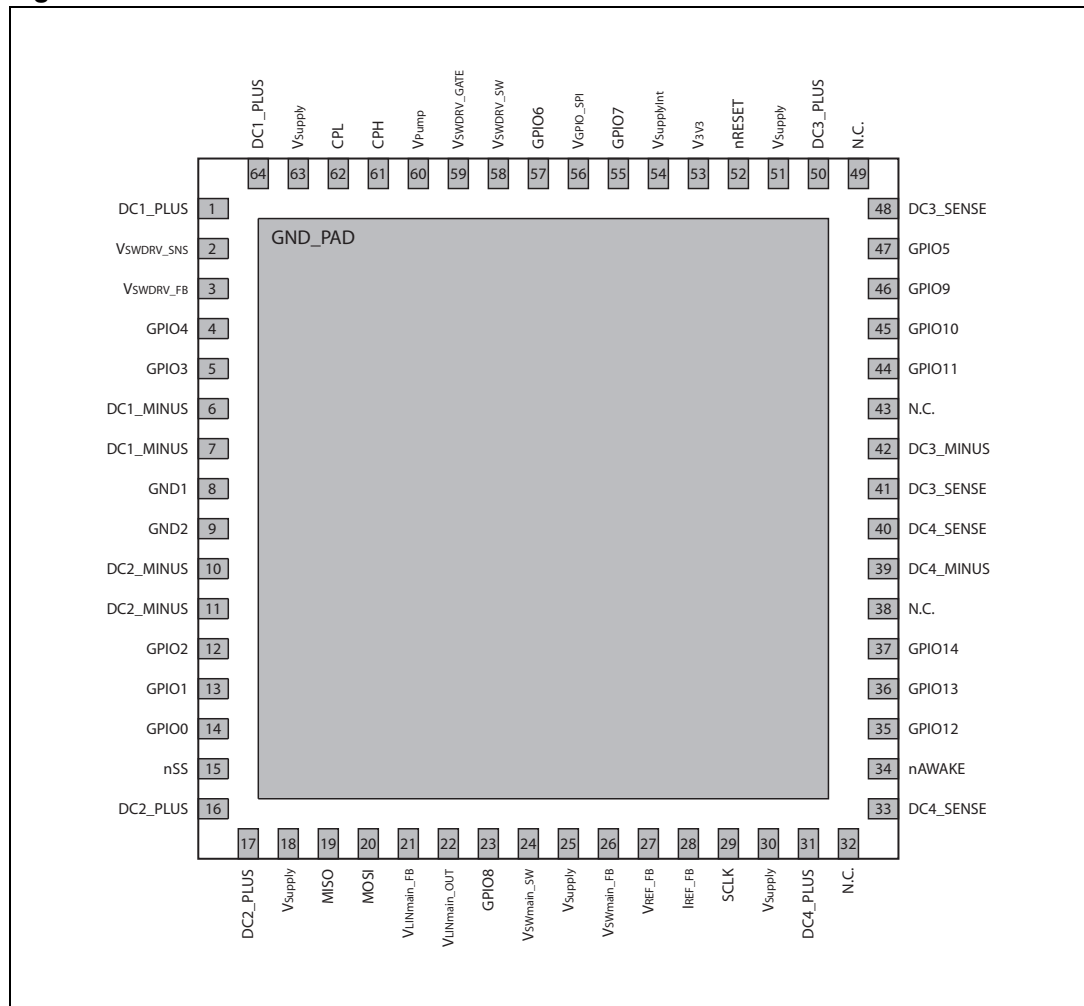
Figure 1. Block diagram



Note: See following Chapter 2 for a detailed description of possible configurations.

## 1.2 Pin connection

Figure 2. Pin connection



## 1.3 Pin list

**Table 2. Pins configuration**

Pin #	Pin name	Description	Type
1	DC1_PLUS	Bridge 1 phase “plus” output	Output
2	V <sub>SWDRV_SNS</sub>	Switching regulator controller sense	Analog input
3	V <sub>SWDRV_FB</sub>	Switching regulator controller feedback	Analog input
4	GPIO4	General purpose I/O	Analog In/Out - CMOS bi-dir
5	GPIO3	General purpose I/O	Analog In/Out - CMOS bi-dir
6	DC1_MINUS	Bridge 1 phase “minus” output	Output
7	DC1_MINUS	Bridge 1 phase “minus” output	Output
8	GND1	Ground pin for bridge1 <sup>(1)(2)(3)</sup>	Power/digital
9	GND2	Ground pin for bridge2 <sup>(1)(2)(3)</sup>	Power/digital
10	DC2_MINUS	Bridge 2 phase “minus” output	Output
11	DC2_MINUS	Bridge 2 phase “minus” output	Output
12	GPIO2	General purpose I/O	Analog In/Out - CMOS bi-dir
13	GPIO1	General purpose I/O	Analog In/Out - CMOS bi-dir
14	GPIO0	General purpose I/O	Analog Input - CMOS input
15	nSS	SPI chip select pin	CMOS input
16	DC2_PLUS	Bridge 2 phase “plus” output	Output
17	DC2_PLUS	Bridge 2 phase “plus” output	Output
18	V <sub>Supply</sub>	Main voltage supply	Power input
19	MISO	SPI serial data output	CMOS output
20	MOSI	SPI serial data input	CMOS input
21	V <sub>LINmain_FB</sub>	Linear main regulator feedback	Analog input
22	V <sub>LINmain_OUT</sub>	Linear main regulator output	Power output
23	GPIO 8	General purpose I/O	Analog In/Out - CMOS bi-dir
24	V <sub>SWmain_SW</sub>	Main switching regulator switching output	Power output
25	V <sub>Supply</sub>	Main voltage supply	Power Input
26	V <sub>SWmain_FB</sub>	Main switching regulator feedback pin	Analog input
27	V <sub>REF_FB</sub>	Regulator voltage feedback	Analog input
28	I <sub>REF_FB</sub>	Regulator current feedback	Analog input
29	SCLK	SPI input clock pin	CMOS input
30	V <sub>Supply</sub>	Main voltage supply	Power input
31	DC4_PLUS	Bridge 4 phase “plus” output	Output
32	N.C.	Not connected	
33	DC4_SENSE	Bridge 4 sense output <sup>(4)</sup>	Output
34	nAWAKE	Device wake up	CMOS input

**Table 2. Pins configuration (continued)**

Pin #	Pin name	Description	Type
35	GPIO12	General purpose I/O	Analog In/Out - CMOS bi-dir
36	GPIO13	General purpose I/O	Analog In/Out - CMOS bi-dir
37	GPIO14	General purpose I/O	Analog In/Out - CMOS bi-dir
38	N.C.	Not connected	
39	DC4_MINUS	Bridge 4 phase "minus" output	Output
40	DC4_SENSE	Bridge 4 sense output <sup>(4)</sup>	Output
41	DC3_SENSE	Bridge 3 sense output <sup>(4)</sup>	Output
42	DC3_MINUS	Bridge 3 phase "minus" output	Output
43	N.C.	Not connected	
44	GPIO11	General purpose I/O	Analog In/Out - CMOS bi-dir
45	GPIO10	General purpose I/O	Analog In/Out - CMOS bi-dir
46	GPIO9	General purpose I/O	Analog In/Out - CMOS bi-dir
47	GPIO5	General purpose I/O	Analog In/Out - CMOS bi-dir
48	DC3_SENSE	Bridge 3 sense output <sup>(4)</sup>	Output
49	N.C.	Not connected	
50	DC3_PLUS	Bridge 3 phase "plus" output	Output
51	V <sub>Supply</sub>	Main voltage supply	Power input
52	nRESET	Open drain system reset pin	CMOS Input/output
53	V <sub>3v3</sub>	Internal 3.3 volt regulator	Power Input/output
54	V <sub>SupplyInt</sub>	Internal voltage supply	Power Input
55	GPIO7	General purpose I/O	Analog In/Out - CMOS bi-dir
56	V <sub>GPIO_SPI</sub>	Low voltage pins power supply	Power input
57	GPIO6	General purpose I/O	Analog In/Out - CMOS bi-dir
58	V <sub>SWDRV_SW</sub>	Switching regulator controller source input	Power input
59	V <sub>SWDRV_GATE</sub>	Switching driver gate drive pin	Analog output
60	V <sub>Pump</sub>	Charge pump voltage	Power Input/output
61	CPH	Charge pump high switch pin	Power Input/output
62	CPL	Charge pump low switch pin	Power Input/output
63	V <sub>Supply</sub>	Main voltage supply	Power input
64	DC1_plus	Bridge 1 phase "plus" output	Output
E_Pad	GND_PAD	(1)(2)(3)	

1. These pins must be connected all together to a unique PCB ground.
2. Bridges 1 and 2 have 2 ground pads: one is bonded to the relative ground pin (GND1 or GND2) and the other is connected to exposed pad (E\_Pad) ground ring. This makes the bond wires testing possible by forcing a current between E-Pad and GND1 or GND2 pins and using the other pin as sense pin to measure the resistance of E-Pad bonding. (N.B: grounds of two bridges are internally connected together).
3. The analog ground is connected to exposed pad E-Pad.
4. The pin must be tied to ground if bridge is not used as a stepper motor.

## 2 L6460's main features

L6460 includes the following circuits:

- Four widely configurable full bridges:
  - Bridges 1 and 2:
    - Diagonal  $R_{DSon}$ : 0.6  $\Omega$  typ.
    - Max operative current = 2.5 A.
  - Bridges 3 and 4:
    - Diagonal  $R_{DSon}$ : 0.85  $\Omega$  typ.
    - Max operative current = 1.5 A.
- Possible configurations for each bridge are the following:
  - Bridge 1:
    - DC motor driver.
    - Super DC (bridge 1 and 2 paralleled form superbridge1).
    - 2 independent half bridges.
    - 1 super half bridge (bridge 1 side A and bridge 1 side B paralleled form superhalfbridge1).
    - 2 independent switches (high or low side).
    - 1 super switch (high or low side).
  - Bridge 2 has the same configurations of bridge 1.
  - Bridge 3 has the same configurations of bridge 1 (bridge 3 and 4 paralleled form superbridge2) plus the following:
    - $\frac{1}{2}$  stepper motor driver.
    - 2 buck regulators ( $V_{AUX1\_SW}$ ,  $V_{AUX2\_SW}$ ).
    - 1 Super buck regulator ( $V_{AUX1//2\_SW}$ ).
  - Bridge 4 has the same configurations of bridge 1 plus the following:
    - $\frac{1}{2}$  stepper motor driver.
    - 1 super buck regulator ( $V_{AUX3\_SW}$ ).
    - Battery charger.
- One buck type switching regulator ( $V_{SWmain}$ ) with:
  - Output regulated voltage range: 1-5 Volts.
  - Output load current: 3.0 A.
  - Internal output power DMOS.
  - Internal soft start sequence.
  - Internal PWM generation.
  - Switching frequency: ~250 kHz.
  - Pulse skipping strategy control.
- One switching regulator controller ( $V_{SWDRV}$ ) with:
  - Output regulated voltage range: 1-30 Volts.
  - Selectable current limitation.
  - Internal PWM generation.
  - Pulse skipping strategy control.
- One linear regulator ( $V_{LINmain}$ ) that can be used to generate low current/low ripple

voltages. This regulator can be used to drive an external bipolar pass transistor to generate high current/low ripple output voltages.

- One bidirectional serial interface with address detection so that different ICs can share the same data bus.
- Integrated power sequencing and supervisory functions with fault signaling through serial interface and external reset pin.
- Fourteen general purpose I/Os that can be used to drive/read internal/external analog/logic signals.
- One 8-bit/9-bit A/D converter (100 kS/s @ 9-bit, 200 kS/s @8-bit). It can be used to measure most of the internal signals, of the input pins and a voltage proportional to IC temperature.
  - Current sink DAC:
  - Three output current ranges: up to 0.64/6.4/64 mA.
  - 64 (6-bit programmable) available current levels for each range.
  - 5 V output tolerant.
- Two operational amplifiers:
  - 3.3 V supply, rail to rail input compatibility, internally compensated.
  - They can have all pins externally accessible or can be internally configured as a buffer or make internal reference voltages available outside of the chip.
  - Unity gain bandwidth > 1 MHz.
  - They can also be set as comparators with 3.3 V input compatibility and low offset.
- Two 3.3 V pass switches with  $1 \Omega$   $R_{DSon}$  and short circuit protected.
- Programmable watchdog function.
- Thermal shutdown protection with thermal warning capability.
- Very low power dissipation in “low power mode” (~35 mW)

L6460 is intended to maximize the use of its components, so when an internal circuit is not used it could be employed for other applications. Bridge 3, for example, can be used as a full bridge or to implement two switching regulators with synchronous rectification: to obtain this flexibility L6460 includes 2 separate regulation loops for these regulators; when the bridge is used as a motor driver, the 2 regulation loops can be redirected on general purpose I/Os to leave the possibility to assembly a switching regulator by only adding an external FET.



### 3 Electrical specifications

#### 3.1 Absolute maximum rating

The following specifications define the maximum range of voltages or currents for L6460.

Stresses above these absolute maximum specifications may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

Parameter	Description	Test condition	Min	Max	Unit
V <sub>Supply</sub>	V <sub>Supply</sub> voltage			40	V
V <sub>GPIO_SPI</sub>	V <sub>GPIO_SPI</sub> voltage			3.9	V
V <sub>3V3pin</sub>	V <sub>3V3</sub> voltage		-0.3	3.9	V
V <sub>SW</sub>	Switching regulators output pin voltage range		-1	V <sub>Supply</sub>	V
V <sub>SW_pulse</sub>	Switching regulators min pulsed voltage	tpulse < 500ns	-3		V
V <sub>Pump</sub>	Charge pump voltage	(1)		15	V
T <sub>J</sub>	Junction temperature <sup>(2)</sup>	Storage	-40	190	°C
		Operating	-40	TSD	°C

1. This value is useful to define the voltage rating for external capacitor to be connected from V<sub>Pump</sub> to V<sub>Supply</sub>; V<sub>Pump</sub> is internally generated and can never be supplied by external voltage source nor is intended to provide voltage to external loads.

2. TSD is the thermal shut down temperature of the device.

#### 3.2 Operating ratings specifications

**Table 4. IC operating ratings**

Parameter	Description	Test condition	Min	Max	Unit
V <sub>Supply</sub>	V <sub>Supply</sub> voltage range		13 <sup>(1)</sup>	38	V
I <sub>Supply</sub>	V <sub>Supply</sub> operative current	(2)		15	mA
I <sub>Shut_down</sub>	V <sub>Supply</sub> shut down state current			1.5	mA
V <sub>GPIO_SPI</sub>	V <sub>GPIO_SPI</sub> voltage range		2.4	3.6	V
I <sub>VGPIO_SPI</sub>	V <sub>GPIO_SPI</sub> operative current	(3)		0.4	mA
V <sub>3V3</sub>	3.3V input pin voltage range			3.6	V
V <sub>LINmain_OUT</sub>	Output pin voltage range	(4)	0	V <sub>Supply</sub>	V
V <sub>LINmain_FB</sub>	Feedback pin voltage range		0	3.6	V
V <sub>SWmain_SW</sub>	Output pin voltage range	(4)	-1	V <sub>supply</sub>	V
V <sub>SWDRV_SW</sub>	V <sub>SWDRV_SW</sub> pin voltage range	(4)	-1	V <sub>Supply</sub>	V

**Table 4. IC operating ratings**

Parameter	Description	Test condition	Min	Max	Unit
V <sub>SWDRV_GATE</sub>	Gate drive pin voltage		0	V <sub>Pump</sub>	V
V <sub>SWDRV_SNS</sub>	Sense pin voltage		V <sub>Supply</sub> -3V	V <sub>Supply</sub>	V
T <sub>J</sub>	Junction temperature	Operating	-40	125	°C

1. For V<sub>Supply</sub> lower than 21 V an external resistor between V<sub>Supply</sub> and V<sub>SupplyInt</sub> pins are required. For V<sub>Supply</sub> lower than 15 V external diodes for charge pump are required.
2. Operating supply current is measured with system regulators operating but not loaded.
3. Operating V<sub>GPIO\_SPI</sub> current is measured with all circuits supplied by V<sub>GPIO\_SPI</sub> (GPIO's, operational amplifiers and pass switches) enabled but not loaded.
4. The external components connected to the pin must be chosen to avoid that the voltage exceeds this operative range.

### 3.3 Electrical characteristics

**Table 5. Electrical characteristics**

Parameter	Description	Test condition	Min	Typ	Max	Unit
<b>V<sub>SupplyInt</sub> regulator</b>						
V <sub>S_Int</sub>	V <sub>SupplyInt</sub> output voltage	(1)	18	19.5	21	V
I <sub>S_Int</sub>	V <sub>SupplyInt</sub> operative current	(2)		11		mA
<b>Charge pump V<sub>Pump</sub></b>						
V <sub>Pump</sub>	Charge pump voltage	V <sub>Supply</sub> =32V	V <sub>Supply</sub> + 10.5	V <sub>Supply</sub> +12.5	V <sub>Supply</sub> + 14.5	V
F <sub>Pump</sub>	V <sub>Pump</sub> clock frequency	F <sub>OSC</sub> = 16MHz typ		F <sub>OSC</sub> /6 4		kHz
<b>V3V3 regulator</b>						
V <sub>3V3</sub>	V <sub>3V3</sub> output voltage	V <sub>Supply</sub> =32V	3.15	3.3	3.45	V
<b>Power on reset</b>						
V <sub>Supply_POR_valid</sub>	V <sub>Supply</sub> voltage for POR valid	I <sub>nRESET</sub> = 1mA	4			V
V <sub>Supply_POR_fall</sub>	V <sub>Supply</sub> POR falling threshold	V <sub>Supply</sub> falling	6		8	V
t <sub>Supply_POR_filt</sub>	V <sub>Supply</sub> POR filter Time			3		µs
V <sub>3V3_POR_fall</sub>	V <sub>3V3</sub> POR falling threshold	V <sub>3V3</sub> falling	1.9	2.2		V
V <sub>3V3_POR_rise</sub>	V <sub>3V3</sub> POR rising threshold	V <sub>3V3</sub> rising		2.7		V
V <sub>3V3_POR_hys</sub>	V <sub>3V3</sub> POR hysteresis			0.5		V
t <sub>3V3_POR_filt</sub>	V <sub>3V3</sub> POR filter time			1.5		µs
<b>nRESET circuit</b>						
V <sub>nRST_L</sub>	nRESET low level output voltage	I=10mA			0.4	V

**Table 5. Electrical characteristics (continued)**

Parameter	Description	Test condition	Min	Typ	Max	Unit
$t_{nRST\_fall}$	nRESET fall time	$I=1mA$ $C=50pF^{(3)}$			15	ns
$t_{nRST\_del}$	nRESET delay time	(4)			150	ns
$V_{Supply\_UV\_f}$	$V_{Supply}$ falling threshold		10.2	11	11.8	V
$V_{Supply\_UV\_r}$	$V_{Supply}$ rising threshold		10.5	11.5	12.5	V
$V_{Supply\_UV\_hys}$	$V_{Supply}$ hysteresis		0.3	0.5	0.7	V
$t_{Supply\_UV}$	$V_{Supply}$ UV filter time			3.5		$\mu s$
$V_{S\_Int\_UV\_f}$	$V_{SupplyInt}$ falling threshold		9.7	10.7	11.7	V
$V_{S\_Int\_UV\_r}$	$V_{SupplyInt}$ rising threshold		10.6	11.4	12.2	V
$V_{S\_Int\_UV\_hys}$	$V_{SupplyInt}$ hysteresis		0.4	0.7	1	V
$t_{S\_Int\_UV}$	$V_{SupplyInt}$ UV filter time			3.5		$\mu s$
$V_{Pump\_UV\_f}$	$V_{Pump}$ falling threshold		$V_{Supply} + 7$	$V_{Supply} + 7.5$	$V_{Supply} + 8$	V
$V_{Pump\_UV\_r}$	$V_{Pump}$ rising threshold		$V_{Supply} + 7.5$	$V_{Supply} + 8$	$V_{Supply} + 8.5$	V
$V_{Pump\_UV\_hys}$	$V_{Pump}$ hysteresis		0.3	0.5	0.7	V
$t_{Pump\_UV}$	$V_{Pump}$ UV filter time			3.5		$\mu s$
$V_{GPIO\_SPI\_UV\_f}$	$V_{GPIO\_SPI}$ falling threshold		1.8	2		V
$V_{GPIO\_SPI\_UV\_r}$	$V_{GPIO\_SPI}$ rising threshold			2.2	2.4	V
$V_{GPIO\_SPI\_hys}$	$V_{GPIO\_SPI}$ hysteresis		200	250	300	mV
$t_{GPIO\_SPI\_UV}$	$V_{GPIO\_SPI}$ UV filter time			3.5		$\mu s$
<b>TSD circuit</b>						
$T_{TSD}$	Thermal shut down temperature			170		$^{\circ}C$
$T_{WARM}$	Warming temperature			140		$^{\circ}C$
$T_{DIFF}$	Thermal shut down to warming difference			30		$^{\circ}C$
$t_{TSD\_FILT}$	Thermal shut down filter time			8		$\mu s$
$t_{WARM\_FILT}$	Warming filter time			8		$\mu s$
<b>Watchdog</b>						
$WD\_T_{clk}$	Watchdog clock period			$T_{osc}^{*22}$		s
<b>Internal clock</b>						
$F_{osc}$	Oscillator frequency	$V_{3V3} = 3.3 V$	14.1	16	17.6	MHz
<b>nAWAKE function</b>						
$V_{IL}$	nAWAKE low logic level voltage				0.8	V

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{IH}$	nAWAKE high logic level voltage		1.6			V
$V_{HYS}$	nAWAKE input hysteresis			0.25		V
$I_{OUT}$	nAWAKE pin output current	nAWAKE=0V <sup>(5)</sup>	-0.72		-2	mA
$I_{INP}$	nAWAKE pin input current	nAWAKE=0.8V <sup>(5)</sup>	0.2		0.4	mA
$t_{AWAKEFILT}$	Filter time			1.2		μs
<b>Main linear regulator</b>						
$V_{drop}$	Drop out voltage	$V_{drop} = V_{supply} - V_{LINmain\_OUT}$	2			V
$I_{PD}$	Internal switch pull down current	Linear Main Regulator disabled; $V_{LINmain\_OUT}=1V$		3		mA
$V_{LINmain\_Ref}$	Feedback reference voltage		0.776	0.8	0.824	V
$I_{LINmain\_Ref}$	Feedback pin input current		-2		2	μA
$I_{outLINMax}$	Maximum output current	$V_{LINmain\_OUT} = V_{supply} - 2V$	10			mA
$I_{short}$	Output short circuit current	$V_{LINmain\_OUT} = 0V$ , $V_{LINmain\_FB} = 0V$	12	24	32	mA
$\Delta V_{out}/V_o$	Load regulation	$0 \leq I_{load} \leq I_{outLINMax}$ <sup>(6)</sup>			0.8	%
$\Delta V_{out}/\Delta V_{Supply}$	Line regulation	$I_{load} = 10mA$ <sup>(6)</sup>			0.2	%
$V_{loop\_acc}$	Loop voltage accuracy			±2.5		%
$V_{LIN\_UV\_f}$	Undervoltage falling threshold	<sup>(7)</sup>	84.5	87	89.5	%
$V_{LIN\_UV\_r}$	Undervoltage rising threshold	<sup>(7)</sup>	90.5	93	95.5	%
$V_{LIN\_UV\_hys}$	Undervoltage hysteresis			6		%
$t_{prim\_uv}$	Under voltage deglitch filter			5		μs
<b>Main switching regulator</b>						
$V_{FBREF}$	Main switching regulator feedback reference voltage	SelFBref = '00'	0.776	0.8	0.824	V
		SelFBref = '01' <sup>(8)</sup>	0.97	1	1.03	V
		SelFBref = '10'	2.425	2.5	2.575	V
		SelFBref = '11'	2.91	3	3.09	V
$I_Q$	Output leakage current	$T_{junction} = 125^\circ C$	-40		+40	μA
$I_{Q\_LP}$	Output leakage current in "low power mode"	$V_{Supply} = 36V$ $T_{junction} = 125^\circ C$	-15		+15	μA
$I_{SWmain\_FB}$	$V_{SWmain\_FB}$ pin current	$T_{junction} = 125^\circ C$	-10		+10	μA
$V_{SWmain\_OUT}$	Output voltage range	<sup>(9)</sup>	0.8		5	V
$I_{load}$	Maximum output load current	$V_{Supply} = 36V$	0.002		3	A
$R_{DSonHS}$	Internal high side $R_{DSon}$	$I_{load}=1A$ $T_{junction} = 125^\circ C$		0.33	0.95	Ω

**Table 5. Electrical characteristics (continued)**

Parameter	Description	Test condition	Min	Typ	Max	Unit
V <sub>loop</sub>	Loop voltage accuracy			±3%		
V <sub>SW_UV_f</sub>	Under voltage falling threshold	(10)	84.5	87	89.5	%
V <sub>SW_UV_r</sub>	Under voltage rising threshold	(10)	90.5	93	95.5	%
V <sub>SW_UV_hys</sub>	Under voltage hysteresis			6		%
t <sub>prim_uv</sub>	Under voltage deglitch filter			5		µs
I <sub>limit</sub>	Current limit protection	Sellimit = "0"	3.3	5		A
		Sellimit = "1"	2.3	3.5		A
t <sub>deglitch</sub>	Current limit deglitch time		50			ns
t <sub>I_lim</sub>	Current limit response time	Normal operating mode (no UV) <sup>(11)</sup>		450	650	ns
t <sub>I_limUV</sub>	Current limit response time in UV condition	UV condition <sup>(12)</sup>		200	400	ns
t <sub>r</sub>	Switching output rise time	V <sub>Supply</sub> = 36V, R <sub>LOAD</sub> = 422 Ω <sup>(13)</sup>	5		30	ns
t <sub>f</sub>	Switching output fall time	V <sub>Supply</sub> = 36V, R <sub>LOAD</sub> = 10 Ω <sup>(13)</sup>	5		30	ns
F <sub>SW_PWM</sub>	Operating frequency			Fosc/6 4		kHz
<b>Switching regulator controller</b>						
V <sub>GS_ext</sub>	Gate to source voltage for external FET			V <sub>Pump</sub>		V
I <sub>SOURCE</sub>	Source current	V <sub>Pump</sub> =V <sub>Supply</sub> +12V V <sub>SWCTR_GATE</sub> =0V	25		50	mA
I <sub>SINK</sub>	Sink current	V <sub>SWCTR_GATE</sub> = V <sub>Supply</sub>	20			mA
t <sub>SINK</sub>	Sink discharge pulse time			600		ns
R <sub>SUSTAIN</sub>	Gate-source sustain resistance	(V <sub>SWCTR_GATE</sub> - V <sub>SWCTR_SRC</sub> ) = 0.2V		650		Ω
I <sub>Q</sub>	Output leakage current	V <sub>Supply</sub> = 36V, T <sub>junction</sub> = 125°C	-40		+40	µA
I <sub>Q_LP</sub>	Output leakage current in "Low Power Mode"	V <sub>Supply</sub> = 36V, T <sub>junction</sub> = 125°C	-5		+5	µA
V <sub>FBREF</sub>	Switching regulator feedback controller feedback reference voltage	SelFBref = '00' <sup>(8)</sup>	0.776	0.8	0.824	V
		SelFBref = '01'	0.97	1	1.03	V
		SelFBref = '10'	2.425	2.5	2.575	V
		SelFBref = '11'	2.91	3	3.09	V
I <sub>SWDRV_FB</sub>	V <sub>SWDRV_FB</sub> pin current	V <sub>Supply</sub> = 36V, T <sub>junction</sub> = 125°C	-10		+10	µA
V <sub>loop</sub>	Loop voltage accuracy			±3%		

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V <sub>SWD_UV_f</sub>	Under voltage falling threshold	(14)	84.5	87	89.5	%
V <sub>SWD_UV_r</sub>	Under voltage rising threshold	(14)	90.5	93	95.5	%
V <sub>SWD_UV_hys</sub>	Under voltage hysteresis			6		%
t <sub>prim_uv</sub>	Under voltage deglitch filter			5		µs
V <sub>ovc</sub>	Over current threshold voltage		250	300	350	mV
t <sub>deglitch</sub>	Current limit deglitch time		50			ns
t <sub>I_lim</sub>	Current limit response time	Normal operating mode (no UV) (11)		500	900	ns
t <sub>I_limUV</sub>	Current Limit response time in UV condition.	UV condition (12)		380	550	ns
F <sub>SWD_PWM</sub>	Operating frequency			F <sub>osc</sub> /64		kHz
<b>Power bridges</b>						
R <sub>DSon1_2</sub>	Bridge 1 and 2 diagonal R <sub>DSon</sub>	I = 1.4A, V <sub>Supply</sub> = 36V, T <sub>junction</sub> = 125°C		0.6	1.1	Ω
R <sub>DSon3_4</sub>	Bridge 3 and 4 diagonal R <sub>DSon</sub>	I = 1A, V <sub>Supply</sub> = 36V, T <sub>junction</sub> = 125°C		0.85	1.65	Ω
I <sub>MAX1_2</sub>	Bridge 1 and 2 operative rms current				2.5	A
I <sub>MAX3_4</sub>	Bridge 3 and 4 operative rms current				1.5	A
I <sub>dss</sub>	Output leakage current.	T <sub>junction</sub> = 125°C	-50		+50	µA
I <sub>Q_LP</sub>	Output leakage current in "low power mode"	V <sub>Supply</sub> = 36V, T <sub>junction</sub> = 125°C	-10		+10	µA
I <sub>OC_LS1_2</sub>	Low side current protection for bridges 1 and 2(15)	MtrXSideYILimSel[1:0]=00	0.6	1	1.6	A
		MtrXSideYILimSel[1:0]=01	1.4	2	2.6	
		MtrXSideYILimSel[1:0]=10	2.4	3	3.6	
		MtrXSideYILimSel[1:0]=11 (16)	2.4	3	3.6	
I <sub>OC_HS1_2</sub>	High side current protection for bridges 1 and 2(15)	MtrXSideYILimSel[1:0]=00	0.7	1	1.7	A
		MtrXSideYILimSel[1:0]=01	1.5	2	2.7	
		MtrXSideYILimSel[1:0]=10	2.5	3	3.7	
		MtrXSideYILimSel[1:0]=11(16)	2.5	3	3.7	
I <sub>OC_LS3_4</sub>	Low side current protection for bridges 3 and 4(15)	MtrXSideYILimSel[1:0]=11 (17)(18)	1.55		2.5	A
I <sub>OC_HS3_4</sub>	High side current protection for bridges 3 and 4(15)	MtrXSideYILimSel[1:0]=11(17)(18)	1.6		2.5	A
t <sub>filter</sub>	Current limit filter time		2		5	µs

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
$t_{\text{delay}}$	Current limit delay time			5		$\mu\text{s}$
$t_{\text{OC\_off}}$	Over current Off time	MtrXlLimitOffTimeY[1:0]=00 MtrXlLimitOffTimeY[1:0]=01 MtrXlLimitOffTimeY[1:0]=10 MtrXlLimitOffTimeY[1:0]=11 (19)		60 120 240 480		$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
$t_{r1\_2}$	Output rise time bridges 1 and 2	$V_{\text{Supply}} = 36\text{V}$ , resistive load between outputs: $R = 25 \Omega^{(20)}$	100	180	250	ns
$t_{r3\_4}$	Output rise time bridges 3 and 4	$V_{\text{Supply}} = 36\text{V}$ , resistive load between outputs: $R = 36 \Omega^{(20)}$	50	100	200	ns
$t_{f1\_2}$	Output fall time bridges 1 and 2	$V_{\text{Supply}} = 36\text{V}$ , resistive load between outputs: $R = 25 \Omega^{(20)}$	100	180	250	ns
$t_{f3\_4}$	Output fall time bridges 3 and 4	$V_{\text{Supply}} = 36\text{V}$ , resistive load between outputs: $R = 36 \Omega^{(20)}$	50	125	250	ns
$t_{\text{deadRise}}$	Anti crossover rising dead time		100	300	450	ns
$t_{\text{deadFall}}$	Anti crossover falling dead time		100	300	450	ns
$F_{\text{PWM}}$	Operating frequency			$F_{\text{osc}}/51$ 2		kHz
$t_{\text{resp}}$	Delay from PWM to output transition			500		ns
<b>Bipolar stepper circuitry</b>						
$V_{\text{STEPREF}}$	Reference voltage	SelStepRef = 0 SelStepRef = 1	0.48 0.72	0.50 0.75	0.52 0.78	V
$V_{\text{offset}}$	Sense comparator offset		-12		12	mV
$t_{\text{blk}}$	Blanking time	StepBlkTime = '00' <sup>(8)</sup>	0.65	0.95	1.25	$\mu\text{s}$
		StepBlkTime = '01'	1	1.45	1.9	$\mu\text{s}$
		StepBlkTime = '10'	1.5	2.25	3	$\mu\text{s}$
		StepBlkTime = '11'	3	4.25	5.5	$\mu\text{s}$
<b>Synchronous buck regulator (bridge 3)</b>						
$V_{\text{AUX\_SW}}$	Output pin voltage range (DC3x)	(26)	-1		$V_{\text{Supply}}$	V
$I_{\text{Q}}$	Output leakage current	$T_{\text{junction}} = 125^\circ\text{C}$	-50		+50	$\mu\text{A}$
$I_{\text{QLP}}$	Output leakage current in "Low Power Mode"	$V_{\text{Supply}} = 36\text{V}$ $T_{\text{junction}} = 125^\circ\text{C}$	-10		+10	$\mu\text{A}$

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{FBREF}$	Synchronous buck regulator feedback reference voltage	SelFBRef = '00'	0.776	0.8	0.824	V
		SelFBRef = '01' <sup>(21)</sup>	0.97	1	1.03	V
		SelFBRef = '10' <sup>(22)</sup>	2.425	2.5	2.575	V
		SelFBRef = '11'	2.91	3	3.09	V
$I_{GPIO\_FB}$	GPIO feedback pin current	$T_{junction} = 125^{\circ}C$ $0V \leq Feedback \leq 3V$	-15		15	$\mu A$
$V_{out}$	Output voltage range	$V_{Supply} = 36V^{(23)}$	0.8		30	V
$I_{load}$	Output load current	$V_{Supply} = 36V$	0.002		1.5	A
$R_{DSonHS}$	Internal high/low side $R_{DSon}$	$T_{junction} = 125^{\circ}C$ ; $I_{load}=1A$		0.6	0.8	$\Omega$
$V_{loop}$	Loop voltage accuracy			$\pm 3\%$		
$V_{REG\_UV\_f}$	Under voltage falling threshold	<sup>(24)</sup>	84.5	87	89.5	%
$V_{REG\_UV\_r}$	Under voltage rising threshold	<sup>(24)</sup>	90.5	93	95.5	%
$V_{REG\_UV\_hys}$	Under voltage hysteresis			6		%
$t_{aux\_UV}$	Under voltage deglitch filter			5		$\mu s$
$I_{limit}$	Current limit protection		1.6		2.5	A
$t_{deglitch}$	Current limit deglitch time		50			ns
$t_{lim}$	Current limit response time	Normal operating mode (no UV) <sup>(11)</sup>		480	700	ns
$t_{limUV}$	Current limit response time in UV condition.	UV condition <sup>(12)</sup>		350	500	ns
$t_r$	Switching output rise time	$V_{Supply} = 36V$ , $R_{LOAD} = 422 \Omega^{(25)}$	5		30	ns
$t_f$	Switching output fall time	$V_{Supply} = 36V$ , $R_{LOAD} = 10 \Omega^{(23)}$	10		50	ns
$t_{dead}$	Crossover dead time			100		ns
$F_{REGPWM}$	Operating frequency			$F_{osc}/64$		kHz
<b>Battery charger (Bridge 4)</b>						
$V_{AUX3\_SW}$	Output pin voltage range (DC4x)	<sup>(26)</sup>	-1		$V_{Supply}$	V
$I_Q$	Output leakage current	$T_{junction} = 125^{\circ}C$	-100		+100	$\mu A$
$V_{FBRef}$	Battery charger control loop feedback reference voltage	SelFBRef = '00'	1.37	1.412	1.455	V
		SelFBRef = '01' <sup>(8)</sup>	1.746	1.8	1.854	V
		SelFBRef = '10'	2.079	2.143	2.207	V
		SelFBRef = '11'	2.425	2.5	2.575	V



Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V <sub>CurrRef</sub>	Battery charger control loop feedback reference current	SelCurrRef = '00' <sup>(8)</sup>	0.873	0.9	0.927	V
		SelCurrRef = '01'	1.394	1.437	1.48	V
		SelCurrRef = '10'	1.746	1.8	1.854	V
		SelCurrRef = '11'	2.182	2.25	2.318	V
V <sub>out</sub>	Output voltage range	V <sub>Supply</sub> = 36V <sup>(27)</sup>	1.412		30	V
I <sub>load</sub>	Output load current	V <sub>Supply</sub> = 36V	0.002		3	A
R <sub>DSon</sub>	Internal high/low side R <sub>DSon</sub>	T <sub>junction</sub> = 125°C; I <sub>LOAD</sub> = 1.5A		0.3	0.4	Ω
V <sub>loop</sub>	Loop voltage accuracy			±3%		
V <sub>BC_UV_f</sub>	Under voltage falling threshold	<sup>(28)</sup>	84.5	87	89.5	%
V <sub>BC_UV_r</sub>	Under voltage rising threshold	<sup>(28)</sup>	90.5	93	95.5	%
V <sub>BC_UV_hys</sub>	Under voltage hysteresis			6		%
t <sub>aux_UV</sub>	Under voltage deglitch filter			5		μs
I <sub>limit</sub>	Current limit protection		3.2		5	A
t <sub>deglitch</sub>	Current limit deglitch time		50			ns
t <sub>I_lim</sub>	Current limit response time	Normal operating mode (no UV) <sup>(11)</sup>		480	700	ns
t <sub>I_limUV</sub>	Current limit response time in UV condition.	UV condition <sup>(12)</sup>		350	500	ns
t <sub>r</sub>	Switching output rise time	V <sub>Supply</sub> = 36V, R <sub>LOAD</sub> = 422 Ω <sup>(25)</sup>	5		30	ns
t <sub>f</sub>	Switching output fall time	V <sub>Supply</sub> = 36V, R <sub>LOAD</sub> = 10 Ω <sup>(25)</sup>	10		50	ns
t <sub>dead</sub>	Crossover dead time			100		ns
F <sub>BCPWM</sub>	Operating frequency			F <sub>osc</sub> /64		kHz
<b>ADC with A2DType=0 <sup>(29)</sup></b>						
IMR	Measurement range	A2dType = 0	0		V <sub>3v3</sub>	V
INL	Integral non-linearity	A2dType = 0 <sup>(30)(31)</sup>			±2	LSB
DNL	Differential non-linearity	A2dType = 0 <sup>(32)(31)</sup>			±2	LSB
OE	Offset error	A2dType = 0 <sup>(33)</sup>			±4	LSB
OE <sub>Drift</sub>	Offset error drift	A2dType = 0 over time and temperature			±3	LSB
GE	Gain error	A2dType = 0 <sup>(34)</sup>			±4	LSB
GE <sub>Drift</sub>	Gain error drift	A2dType = 0 over time and temperature			±4	LSB
t <sub>conv</sub>	Minimum conversion time				55	μs
	Resolution	<sup>(35)</sup>		8		bits

Table 5. Electrical characteristics (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
$C_{in}$	Input sampling capacitance	(36)			4	pF
<b>ADC with A2DType=1 (37)</b>						
IMR	Measurement range	A2dType = 1	0		$V_{3v3}$	V
INL	Integral non-linearity	A2dType = 1 (30)(31)			$\pm 1$	LSB
DNL	Differential Non-Linearity	A2dType = 1 (32)(31)			$\pm 1$	LSB
OE	Offset error	A2dType = 1 (33)			$\pm 4$	LSB
$OE_{Drift}$	Offset error drift	A2dType = 1 over time and temperature			$\pm 3$	LSB
GE	Gain error	A2dType = 1 (34)			$\pm 4$	LSB
$GE_{Drift}$	Gain error drift	A2dType = 1 over time and temperature			$\pm 4$	LSB
$t_{conv}$	Minimum conversion time				10	$\mu s$
	Resolution			9		bits
$C_{in}$	Input sampling capacitance	(36)			4	pF
<b>Current DAC</b>						
$V_R$	Pin voltage operative range (GPIO8)	(38)	0.7		5.5	V
$I_{OUT\_OFF}$	Output off leakage current	DacValue[5:0] = 000000	-1		+1	$\mu A$
$I_{FULL\_ERR}$	Full scale current error	DacRange[1:0] = xx DacValue[5:0] = 111111	-15		+15	% of $I_{FULL}$ typ
$INL_{10\_11}$	Integral non-linearity for 10 and 11 ranges				$\pm 2$	LSB
$DNL_{10\_11}$	Differential non-linearity for 10 and 11 ranges				$\pm 2$	LSB
$INL_{01}$	Integral non-linearity for 01 range				$\pm 1$	LSB
$DNL_{01}$	Differential non-linearity for 01 range				$\pm 1$	LSB
$R_{CurrDac\_res}$	Gpio[8] divider total resistance			45		k $\Omega$
$R_{CurrDac\_ratio}$	Gpio[8] divider ratio			3/5		
$t_{set}$	Settling time	(39)			5	$\mu s$
<b>Operational amplifier (40)</b>						
$V_{GPIO\_SPI}$	Operational amplifier supply voltage range		3.15	3.3	3.45	V
$V_{ICM}$	Input common mode voltage range		0		$V_{GPIO\_SPI}$	V
$V_{OUT\_MAX}$	Output voltage	$I_{LOAD} = \pm 1mA$	0.1		3.2	V