Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

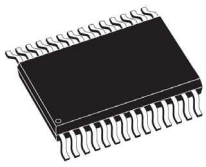

## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

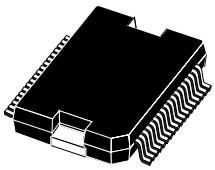
# L6472

## Fully integrated microstepping motor driver

**Datasheet - production data**



**HTSSOP28**



**POWERSO36**

## Features

- Operating voltage: 8 - 45 V
- 7.0 A output peak current (3.0 A $_{r.m.s.}$)
- Low $R_{DS(on)}$ power MOSFETs
- Programmable speed profile
- Programmable power MOSFET slew rate
- Up to 1/16 microstepping
- Predictive current control with adaptive decay
- Non dissipative current sensing
- SPI interface
- Low quiescent and standby currents
- Programmable non dissipative overcurrent protection on all power MOSFETs
- Two levels of overtemperature protection

## Applications

- Bipolar stepper motor

## Description

The L6472 device, realized in analog mixed signal technology, is an advanced fully integrated solution suitable for driving two-phase bipolar stepper motors with microstepping. It integrates a dual low $R_{DS(on)}$ DMOS full bridge with all of the power switches equipped with an accurate on-chip current sensing circuitry suitable for non dissipative current control and overcurrent protection. Thanks to a new current control, a 1/16 microstepping is achieved through an adaptive decay mode which outperforms traditional implementations. The digital control core can generate user defined motion profiles with acceleration, deceleration, speed or target position, easily programmed through a dedicated register set.

All application commands and data registers, including those used to set analog values (i.e.: current control value, current protection trip point, deadtime, etc.) are sent through a standard 5-Mbit/s SPI.

A very rich set of protections (thermal, low bus voltage, overcurrent) makes the L6472 device “bullet proof”, as required by the most demanding motor control applications.

**Table 1. Device summary**

| Order codes | Package | Packing |
|---|---|---|
| L6472H | HTSSOP28 | Tube |
| L6472HTR | HTSSOP28 | Tape and reel |
| L6472PD | POWERSO36 | Tube |
| L6472PDTR | POWERSO36 | Tape and reel |

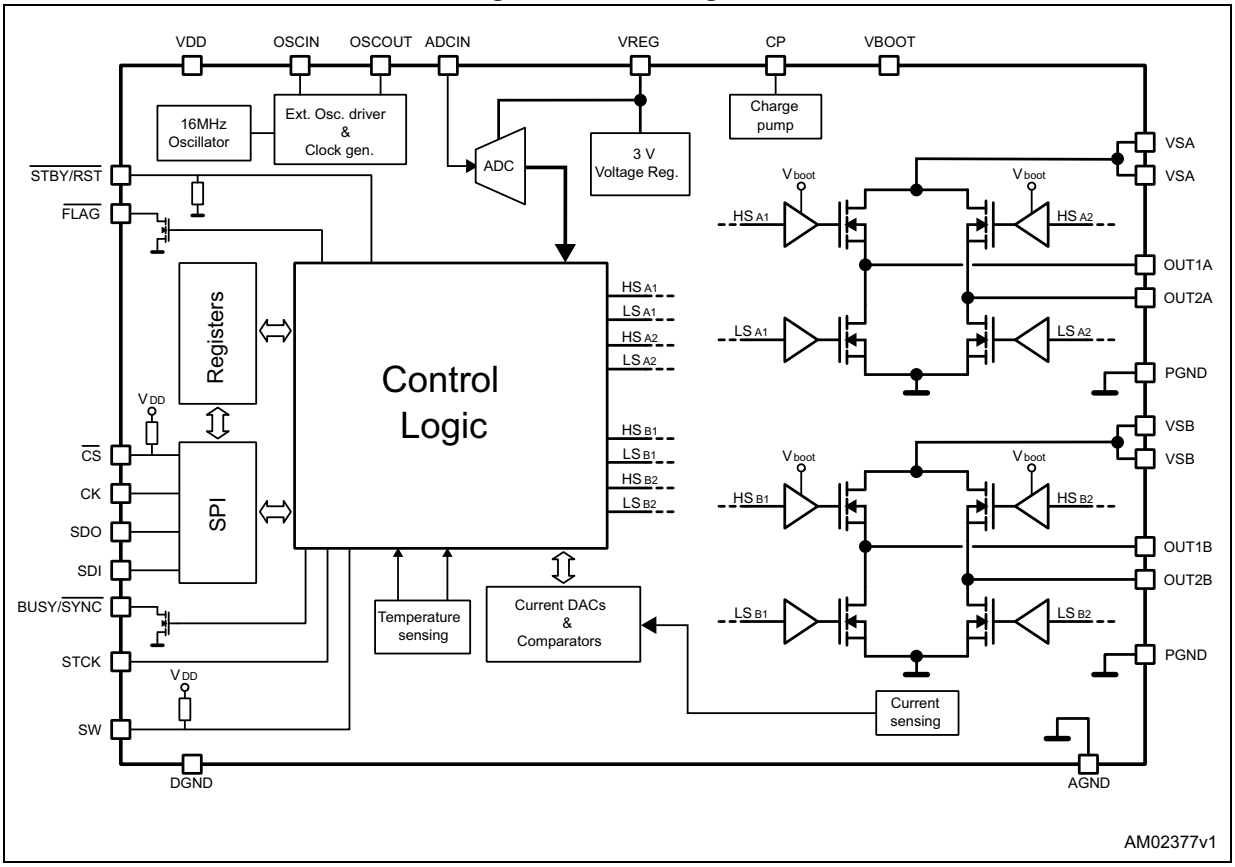
# Contents

# List of tables

# List of figures

# 1 Block diagram

**Figure 1. Block diagram**



# 2 Electrical data

## 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Test condition | Value | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Logic interface supply voltage | | 5.5 | V |
| $V_S$ | Motor supply voltage | $V_{SA} = V_{SB} = V_S$ | 48 | V |
| $V_{GND, diff}$ | Differential voltage between AGND, PGND and DGND | | ±0.3 | V |
| $V_{boot}$ | Bootstrap peak voltage | | 55 | V |
| $V_{REG}$ | Internal voltage regulator output pin and logic supply voltage | | 3.6 | V |
| $V_{ADCIN}$ | Integrated ADC input voltage range (ADCIN pin) | | -0.3 to +3.6 | V |
| $V_{OSC}$ | OSCIN and OSCOUT pin voltage range | | -0.3 to +3.6 | V |
| $V_{out\_diff}$ | Differential voltage between $V_{SA}$, $OUT1_A$, $OUT2_A$, PGND and $V_{SB}$, $OUT1_B$, $OUT2_B$, PGND pins | $V_{SA} = V_{SB} = V_S$ | 48 | V |
| $V_{LOGIC}$ | Logic inputs voltage range | | -0.3 to +5.5 | V |
| $I_{out}$ (1) | R.m.s. output current | | 3 | A |
| $I_{out\_peak}$ (1) | Pulsed output current | $T_{PULSE}$ < 1 ms | 7 | A |
| $T_{OP}$ | Operating junction temperature | | -40 to 150 | °C |
| $T_s$ | Storage temperature range | | -55 to 150 | °C |
| $P_{tot}$ | Total power dissipation ($T_A$ = 25 °C) | (2) | 5 | W |

1. Maximum output current limit is related to metal connection and bonding characteristics. Actual limit must satisfy maximum thermal dissipation constraints.
2. HTSSOP28 mounted on the EVAL6472H.

## 2.2 Recommended operating conditions

**Table 3. Recommended operating conditions**

| Symbol | Parameter | Test condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Logic interface supply voltage | 3.3 V logic outputs | | 3.3 | | V |
| | | 5 V logic outputs | | 5 | | |
| $V_S$ | Motor supply voltage | $V_{SA} = V_{SB} = V_S$ | 8 | | 45 | V |
| $V_{out\_diff}$ | Differential voltage between $V_{SA}$, $OUT1_A$, $OUT2_A$, PGND and $V_{SB}$, $OUT1_B$, $OUT2_B$, PGND pins | $V_{SA} = V_{SB} = V_S$ | | | 45 | V |
| $V_{REG,in}$ | Logic supply voltage | $V_{REG}$ voltage imposed by external source | 3.2 | 3.3 | | V |
| $V_{ADC}$ | Integrated ADC input voltage (ADCIN pin) | | 0 | | $V_{REG}$ | V |

## 2.3 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Package | Typ. | Unit |
|---|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction ambient | HTSSOP28(1) | 22 | °C/W |
| | | POWERSO36(2) | 12 | |

1. HTSSOP28 mounted on the EVAL6472H Rev 1.0 board: four-layer FR4 PCB with a dissipating copper surface of about 40 $cm^2$ on each layer and 15 via holes below the IC.
2. POWERSO36 mounted on the EVAL6472PD Rev 1.0 board: four-layer FR4 PCB with a dissipating copper surface of about 40 $cm^2$ on each layer and 22 via holes below the IC.

# 3 Electrical characteristics

$V_{SA}$ = $V_{SB}$ = 36 V; $V_{DD}$ = 3.3 V; internal 3 V regulator; $T_J$ = 25 °C, unless otherwise specified.

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| $V_{SthOn}$ | $V_S$ UVLO turn-on threshold | | 7.5 | 8.2 | 8.9 | V |
| $V_{SthOff}$ | $V_S$ UVLO turn-off threshold | | 6.6 | 7.2 | 7.8 | V |
| $V_{SthHyst}$ | $V_S$ UVLO threshold hysteresis | | 0.7 | 1 | 1.3 | V |
| $I_q$ | Quiescent motor supply current | Internal oscillator selected; $V_{REG}$ = 3.3 V ext; CP floating | | 0.5 | 0.65 | mA |
| $T_{j(WRN)}$ | Thermal warning temperature | | | 130 | | °C |
| $T_{j(SD)}$ | Thermal shutdown temperature | | | 160 | | °C |
| **Charge pump** | | | | | | |
| $V_{pump}$ | Voltage swing for charge pump oscillator | | | 10 | | V |
| $f_{pump,min}$ | Minimum charge pump oscillator frequency(1) | | | 660 | | kHz |
| $f_{pump,max}$ | Maximum charge pump oscillator frequency(1) | | | 800 | | kHz |
| $I_{boot}$ | Average boot current | $f_{sw,A}$ = $f_{sw,B}$ = 15.6 kHz POW_SR = ‘10’ | | 1.1 | 1.4 | mA |
| **Output DMOS transistor** | | | | | | |
| $R_{DS(on)}$ | High-side switch on-resistance | $T_j$ = 25 °C, $I_{out}$ = 3 A | | 0.37 | | Ω |
| | | $T_j$ = 125 °C,(2) $I_{out}$ = 3 A | | 0.51 | | |
| | Low-side switch on-resistance | $T_j$ = 25 °C, $I_{out}$ = 3 A | | 0.18 | | |
| | | $T_j$ = 125 °C,(2) $I_{out}$ = 3 A | | 0.23 | | |
| $I_{DSS}$ | Leakage current | OUT = $V_S$ | | | 3.1 | mA |
| | | OUT = GND | -0.3 | | | |
| $t_r$ | Rise time(3) | POW_SR = '00', $I_{out}$ = +1 A | | 100 | | ns |
| | | POW_SR = '00', $I_{out}$ = -1 A | | 80 | | |
| | | POW_SR = ‘11’, $I_{out}$ = ±1 A | | 100 | | |
| | | POW_SR = ‘10’, $I_{out}$ = ±1 A | | 200 | | |
| | | POW_SR = ‘01’, $I_{out}$ = ±1 A | | 300 | | |

Table 5. Electrical characteristics (continued)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_f$ | Fall time (3) | POW_SR = '00'; $I_{out}$ = +1 A | | 90 | | ns |
| | | POW_SR = '00'; $I_{out}$ = -1 A | | 110 | | |
| | | POW_SR = '11', $I_{out}$ = ±1 A | | 110 | | |
| | | POW_SR = '10', $I_{out}$ = ±1 A | | 260 | | |
| | | POW_SR = '01', $I_{load}$ = ±1 A | | 375 | | |
| $SR_{out\_r}$ | Output rising slew rate | POW_SR = '00', $I_{out}$ = +1 A | | 285 | | V/µs |
| | | POW_SR = '00', $I_{out}$ = -1 A | | 360 | | |
| | | POW_SR = '11', $I_{out}$ = ±1 A | | 285 | | |
| | | POW_SR = '10', $I_{out}$ = ±1 A | | 150 | | |
| | | POW_SR = '01', $I_{out}$ = ±1 A | | 95 | | |
| $SR_{out\_f}$ | Output falling slew rate | POW_SR = '00', $I_{out}$ = +1 A | | 320 | | V/µs |
| | | POW_SR = '00', $I_{out}$ = -1 A | | 260 | | |
| | | POW_SR = '11', $I_{out}$ = ±1 A | | 260 | | |
| | | POW_SR = '10', $I_{out}$ = ±1 A | | 110 | | |
| | | POW_SR = '01', $I_{out}$ = ±1 A | | 75 | | |
| **Deadtime and blanking** | | | | | | |
| $t_{DT}$ | Deadtime(1) | POW_SR = '00' | | 250 | | ns |
| | | POW_SR = '11', $f_{OSC}$ = 16 MHz | | 375 | | |
| | | POW_SR = '10', $f_{OSC}$ = 16 MHz | | 625 | | |
| | | POW_SR = '01', $f_{OSC}$ = 16 MHz | | 875 | | |
| $t_{blank}$ | Blanking time(1) | POW_SR = '00' | | 250 | | ns |
| | | POW_SR = '11', $f_{OSC}$ = 16 MHz | | 375 | | |
| | | POW_SR = '10', $f_{OSC}$ = 16 MHz | | 625 | | |
| | | POW_SR = '01', $f_{OSC}$ = 16 MHz | | 875 | | |
| **Source-drain diodes** | | | | | | |
| $V_{SD,HS}$ | High-side diode forward ON voltage | $I_{out}$ = 1 A | | 1 | 1.1 | V |
| $V_{SD,LS}$ | Low-side diode forward ON voltage | $I_{out}$ = 1 A | | 1 | 1.1 | V |
| $t_{rrHS}$ | High-side diode reverse recovery time | $I_{out}$ = 1 A | | 30 | | ns |
| $t_{rrLS}$ | Low-side diode reverse recovery time | $I_{out}$ = 1 A | | 100 | | ns |
| **Logic inputs and outputs** | | | | | | |
| $V_{IL}$ | Low logic level input voltage | | | | 0.8 | V |
| $V_{IH}$ | High logic level input voltage | | 2 | | | V |
| $I_{IH}$ | High logic level input current(4) | $V_{IN}$ = 5 V | | | 1 | µA |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Low logic level input current(5) | $V_{IN}$ = 0 V | -1 | | | µA |
| $V_{OL}$ | Low logic level output voltage (6) | $V_{DD}$ = 3.3 V, $I_{OL}$ = 4 mA | | | 0.3 | V |
| | | $V_{DD}$ = 5 V, $I_{OL}$ = 4 mA | | | 0.3 | |
| $V_{OH}$ | High logic level output voltage | $V_{DD}$ = 3.3 V, $I_{OH}$ = 4 mA | 2.4 | | | V |
| | | $V_{DD}$ = 5 V, $I_{OH}$ = 4 mA | 4.7 | | | |
| $R_{PU}$ $R_{PD}$ | CS pull-up and STBY pull-down resistors | $\overline{CS}$ = GND; $\overline{STBY/RST}$ = 5 V | 335 | 430 | 565 | kΩ |
| $I_{logic}$ | Internal logic supply current | 3.3 V $V_{REG}$ externally supplied, internal oscillator | | 3.7 | 4.3 | mA |
| $I_{logic,STBY}$ | Standby mode internal logic supply current | 3.3 V $V_{REG}$ externally supplied | | 2 | 2.5 | µA |
| $f_{STCK}$ | Step-clock input frequency | | | | 2 | MHz |
| **Internal oscillator and external oscillator driver** | | | | | | |
| $f_{osc,i}$ | Internal oscillator frequency | $T_j$ = 25 °C, $V_{REG}$ = 3.3 V | -3% | 16 | +3% | MHz |
| $f_{osc,e}$ | Programmable external oscillator frequency | | 8 | | 32 | MHz |
| $V_{OSCOUTH}$ | OSCOUT clock source high level voltage | Internal oscillator 3.3 V $V_{REG}$ externally supplied; $I_{OSCOUT}$ = 4 mA | 2.4 | | | V |
| $V_{OSCOUTL}$ | OSCOUT clock source low level voltage | Internal oscillator 3.3 V $V_{REG}$ externally supplied; $I_{OSCOUT}$ = 4 mA | | | 0.3 | V |
| $t_{rOSCOUT}$ $t_{fOSCOUT}$ | OSCOUT clock source rise and fall time | Internal oscillator | | | 20 | ns |
| $t_{extosc}$ | Internal to external oscillator switching delay | | | 3 | | ms |
| $t_{intosc}$ | External to internal oscillator switching delay | | | 1.5 | | µs |
| **SPI** | | | | | | |
| $f_{CK,MAX}$ | Maximum SPI clock frequency(7) | | 5 | | | MHz |
| $t_{rCK}$ $t_{fCK}$ | SPI clock rise and fall time(7) | $C_L$ = 30 pF | | | 25 | ns |
| $t_{hCK}$ $t_{lCK}$ | SPI clock high and low time(7) | | 75 | | | ns |
| $t_{setCS}$ | Chip select setup time(7) | | 350 | | | ns |
| $t_{holCS}$ | Chip select hold time(7) | | 10 | | | ns |
| $t_{disCS}$ | De-select time(7) | | 800 | | | ns |
| $t_{setSDI}$ | Data input setup time(7) | | 25 | | | ns |
| $t_{holSDI}$ | Data input hold time(7) | | 20 | | | ns |
| $t_{enSDO}$ | Data output enable time(7) | | | | 38 | ns |

Table 5. Electrical characteristics (continued)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{disSDO}$ | Data output disable time(7) | | | | 47 | ns |
| $t_{vSDO}$ | Data output valid time(7) | | | | 57 | ns |
| $t_{holSDO}$ | Data output hold time(7) | | 37 | | | ns |
| **Switch input (SW)** | | | | | | |
| $R_{PUSW}$ | SW input pull-up resistance | SW = GND | 60 | 85 | 110 | kΩ |
| **Current control** | | | | | | |
| $I_{STEP,max}$ | Max. programmable reference current | | | 4 | | A |
| $I_{STEP,min}$ | Min. programmable reference current | | | 31 | | mA |
| **Overcurrent protection** | | | | | | |
| $I_{OCD,MAX}$ | Maximum programmable overcurrent detection threshold | OCD_TH = ‘1111’ | | 6 | | A |
| $I_{OCD,MIN}$ | Minimum programmable overcurrent detection threshold | OCD_TH = ‘0000’ | | 0.375 | | A |
| $I_{OCD,RES}$ | Programmable overcurrent detection threshold resolution | | | 0.375 | | A |
| $t_{OCD,Flag}$ | OCD to flag signal delay time | $dI_{out}/d_t$ = 350 A/µs | | 650 | 1000 | ns |
| $t_{OCD,SD}$ | OCD to shutdown delay time | $dI_{out}/d_t$ = 350 A/µs POW_SR = '10' | | 600 | | µs |
| **Standby** | | | | | | |
| $I_{qSTBY}$ | Quiescent motor supply current in standby conditions | $V_S$ = 8 V | | 26 | 34 | µA |
| | | $V_S$ = 36 V | | 30 | 36 | |
| $t_{STBY,min}$ | Minimum standby time | | | 10 | | µs |
| $t_{logicwu}$ | Logic power-on and wake-up time | | | 38 | 45 | µs |
| $t_{cpwu}$ | Charge pump power-on and wake-up time | Power bridges disabled, $C_p$ = 10 nF, $C_{boot}$ = 220 nF | | 650 | | µs |
| **Internal voltage regulator** | | | | | | |
| $V_{REG}$ | Voltage regulator output voltage | | 2.9 | 3 | 3.2 | V |
| $I_{REG}$ | Voltage regulator output current | | | | 40 | mA |
| $V_{REG, drop}$ | Voltage regulator output voltage drop | $I_{REG}$ = 40 mA | | 50 | | mV |
| $I_{REG,STBY}$ | Voltage regulator standby output current | | | | 10 | mA |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Integrated analog-to-digital converter** | | | | | | |
| $N_{ADC}$ | Analog-to-digital converter resolution | | | 5 | | bit |
| $V_{ADC,ref}$ | Analog-to-digital converter reference voltage | | | $V_{REG}$ | | V |
| $f_S$ | Analog-to-digital converter sampling frequency | | | $f_{OSC}$/ 512 | | kHz |

1. Accuracy depends on oscillator frequency accuracy.
2. Tested at 25 °C in a restricted range and guaranteed by characterization.
3. Rise and fall time depends on motor supply voltage value. Refer to $SR_{out}$ values in order to evaluate the actual rise and fall time.
4. Not valid for the $\overline{\text{STBY/RST}}$ pin which has an internal pull-down resistor.
5. Not valid for the SW and CS pins which have an internal pull-up resistor.
6. $\overline{\text{FLAG}}$, $\overline{\text{BUSY}}$ and SYNC open drain outputs included.
7. See *Figure 19: SPI timings diagram on page 38* for details.

# 4 Pin connection

**Figure 2. HTSSOP28 pin connection (top view)**

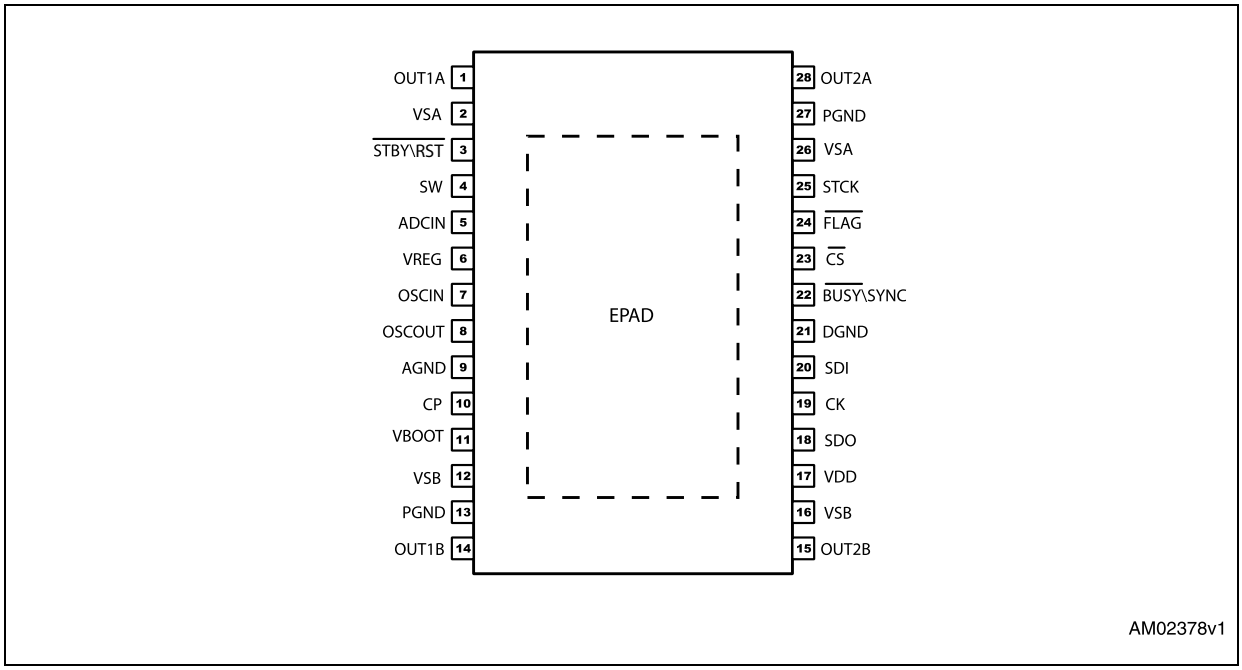
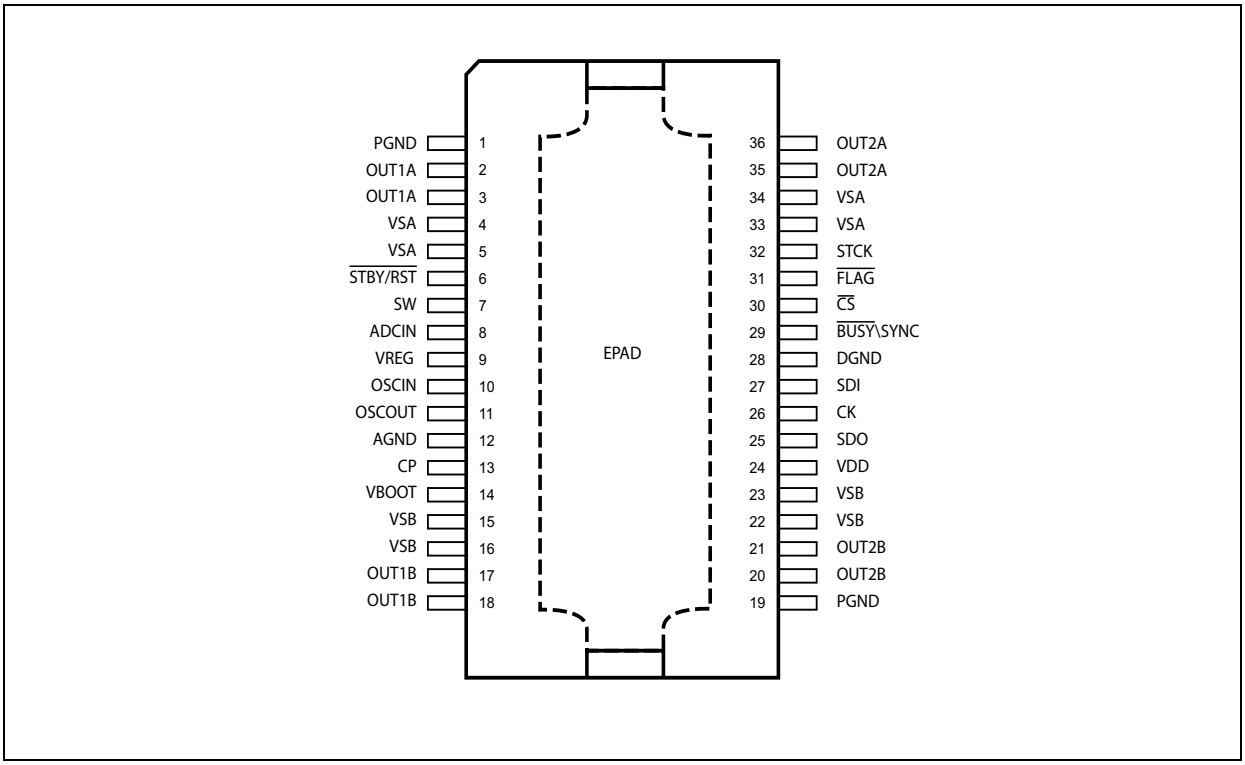



**Figure 3. POWERSO36 pin connection (top view)**



# Pin list

**Table 6. Pin description**

| Number | | Name | Type | Function |
|---|---|---|---|---|
| POWERSO | HTSSOP | | | |
| 24 | 17 | VDD | Power | Logic output supply voltage (pull-up reference) |
| 9 | 6 | VREG | Power | Internal 3 V voltage regulator output and 3.3 V external logic supply |
| 10 | 7 | OSCIN | Analog input | Oscillator pin 1. To connect an external oscillator or clock source. If this pin is unused, it should be left floating. |
| 11 | 8 | OSCOUT | Analog output | Oscillator pin 2. To connect an external oscillator. When the internal oscillator is used this pin can supply 2/4/8/16 MHz. If this pin is unused, it should be left floating. |
| 13 | 10 | CP | Output | Charge pump oscillator output |
| 14 | 11 | Vboot | Supply voltage | Bootstrap voltage needed for driving the high-side power DMOS of both bridges (A and B). |
| 8 | 5 | ADCIN | Analog input | Internal analog-to-digital converter input |
| 4, 5 | 2 | VSA | Power supply | Full bridge A power supply pin. It must be connected to VSB. |
| 33, 34 | 26 | | | |
| 15, 16 | 12 | VSB | Power supply | Full bridge B power supply pin. It must be connected to VSA. |
| 22, 23 | 16 | | | |
| 1 | 27 | PGND | Ground | Power ground pin |
| 19 | 13 | | | |
| 2, 3 | 1 | OUT1A | Power output | Full bridge A output 1 |
| 35, 36 | 28 | OUT2A | Power output | Full bridge A output 2 |
| 17, 18 | 14 | OUT1B | Power output | Full bridge B output 1 |
| 20, 21 | 15 | OUT2B | Power output | Full bridge B output 2 |
| 12 | 9 | AGND | Ground | Analog ground. |
| 7 | 4 | SW | Logical input | External switch input pin. If not used the pin should be connected to VDD. |
| 28 | 21 | DGND | Ground | Digital ground |
| 29 | 22 | $\overline{\text{BUSY}}$\SYNC | Open drain output | By default, this BUSY pin is forced low when the device is performing a command. Otherwise the pin can be configured to generate a synchronization signal. |
| 25 | 18 | SDO | Logic output | Data output pin for serial interface |
| 27 | 20 | SDI | Logic input | Data input pin for serial interface |
| 26 | 19 | CK | Logic input | Serial interface clock |
| 30 | 23 | $\overline{\text{CS}}$ | Logic input | Chip select input pin for serial interface |

Table 6. Pin description (continued)

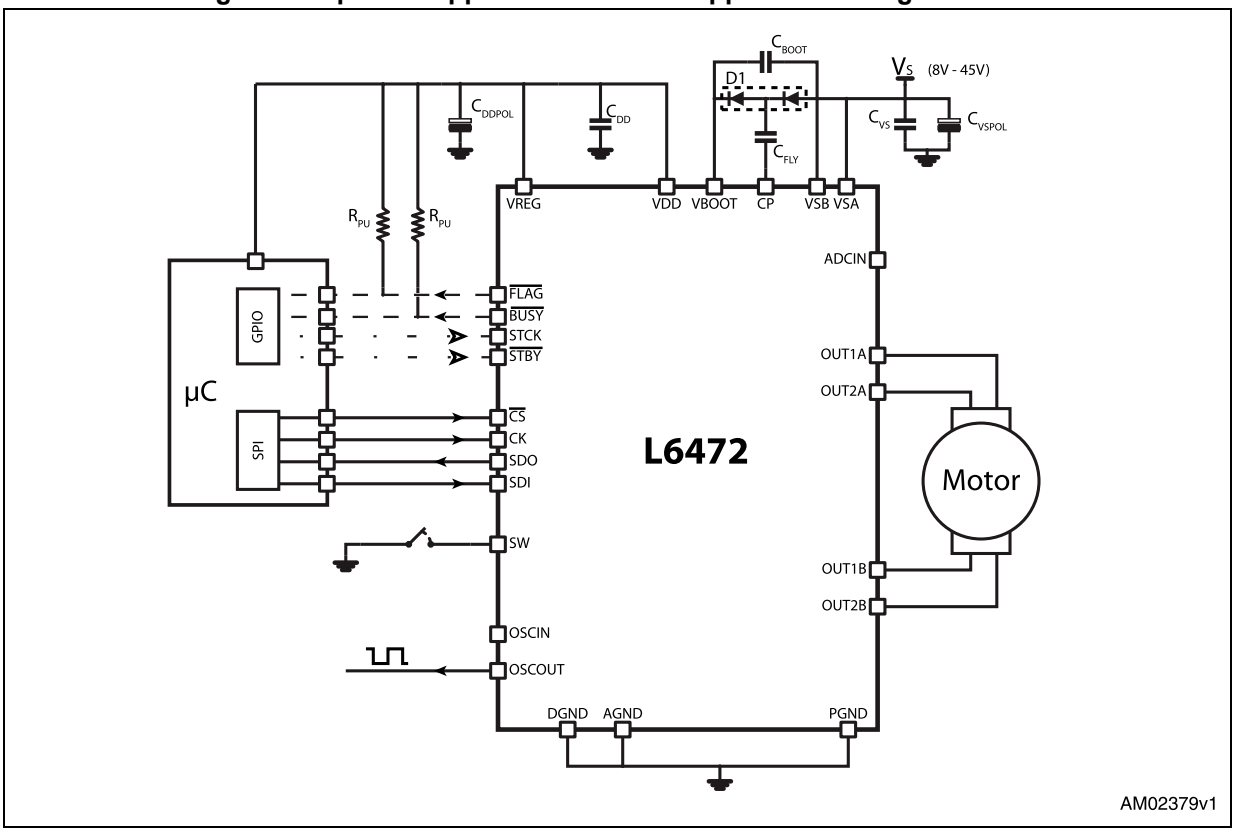
| Number | | Name | Type | Function |
|---|---|---|---|---|
| POWERSO | HTSSOP | | | |
| 31 | 24 | $\overline{\text{FLAG}}$ | Open drain output | Status flag pin. An internal open drain transistor can pull the pin to GND when a programmed alarm condition occurs (step loss, OCD, thermal pre-warning or shutdown, UVLO, wrong command, non-performable command). |
| 6 | 3 | $\overline{\text{STBY\RST}}$ | Logic input | Standby and reset pin. LOW logic level resets the logic and puts the device into standby mode. If not used, it should be connected to VDD |
| 32 | 25 | STCK | Logic input | Step-clock input |
| | EPAD | Exposed pad | Ground | Internally connected to PGND, AGND and DGND pins |

# 5 Typical applications

**Table 7. Typical application values**

| Name | Value |
|---|---|
| $C_{VS}$ | 220 nF |
| $C_{VSPOL}$ | 100 µF |
| $C_{REG}$ | 100 nF |
| $C_{REGPOL}$ | 47 µF |
| $C_{DD}$ | 100 nF |
| $C_{DDPOL}$ | 10 µF |
| D1 | Charge pump diodes |
| $C_{BOOT}$ | 220 nF |
| $C_{FLY}$ | 10 nF |
| $R_{PU}$ | 39 kΩ |
| $R_{SW}$ | 100 Ω |
| $C_{SW}$ | 10 nF |

**Figure 4. Bipolar stepper motor control application using the L6472**



# 6 Functional description

## 6.1 Device power-up

At the end of power-up, the device state is the following:

- Registers are set to default
- Internal logic is driven by the internal oscillator and a 2 MHz clock is provided by the OSCOUT pin
- Bridges are disabled (High Z)
- UVLO bit in the STATUS register is forced low (fail condition)
- FLAG output is forced low.

During power-up the device is under reset (all logic IO disabled and power bridges in high-impedance state) until the following conditions are satisfied:

- $V_S$ is greater than $V_{SthOn}$
- $V_{REG}$ is greater than $V_{REGth}$ = 2.8 V (typ.)
- Internal oscillator is operative.

Any motion command causes the device to exit from High Z state (HardStop and SoftStop included).

## 6.2 Logic I/O

Pins $\overline{CS}$, CK, SDI, STCK, SW and $\overline{STBY\backslash RST}$ are TTL/CMOS 3.3 V - 5 V compatible logic inputs.

Pin SDO is a TTL/CMOS compatible logic output. The VDD pin voltage sets the logic output pin voltage range; when it is connected to VREG or a 3.3 V external supply voltage, the output is 3.3 V compatible. When VDD is connected to a 5 V supply voltage, SDO is 5 V compatible.

VDD is not internally connected to $V_{REG}$, an external connection is always needed.

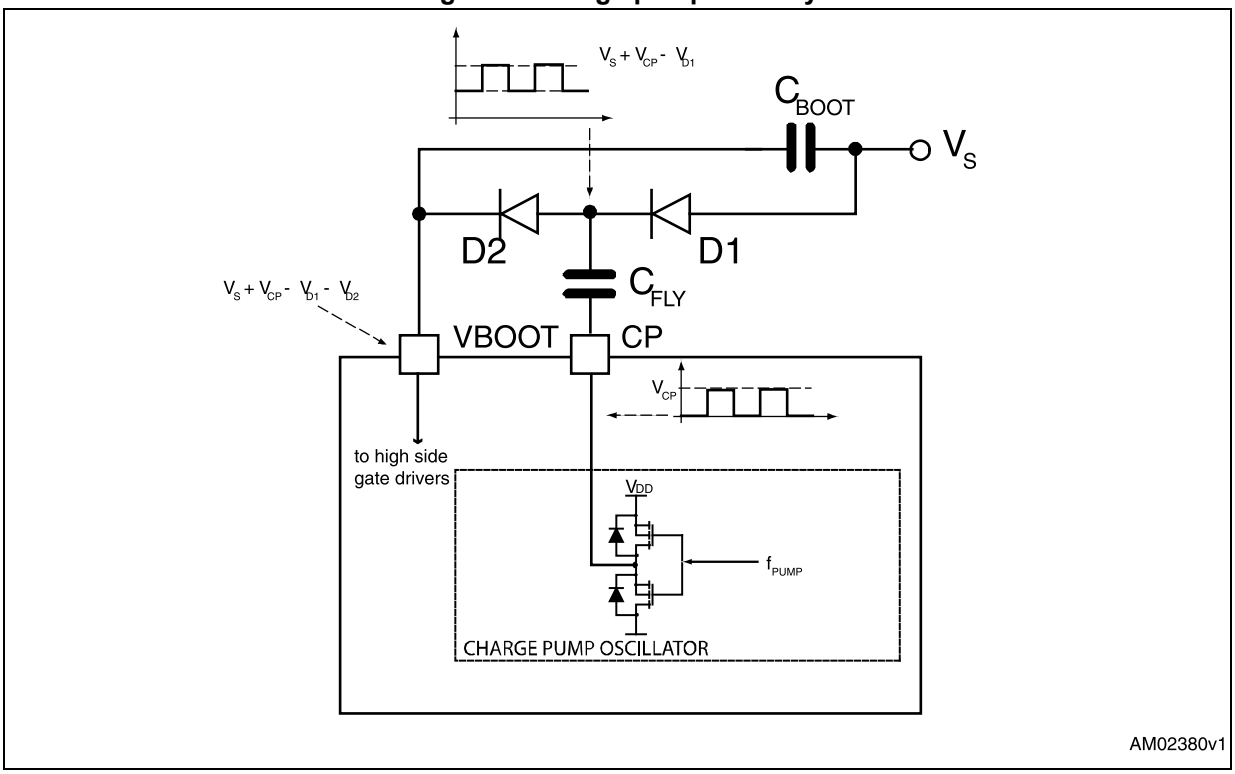
A 10 µF capacitor should be connected to the VDD pin in order to obtain a proper operation.

Pins $\overline{FLAG}$ and $\overline{BUSY\backslash SYNC}$ are open drain outputs.

## 6.3 Charge pump

To ensure the correct driving of the high-side integrated MOSFETs, a voltage higher than the motor power supply voltage needs to be applied to the Vboot pin. The high-side gate driver supply voltage Vboot is obtained through an oscillator and a few external components realizing a charge pump (see *Figure 5*).

**Figure 5. Charge pump circuitry**

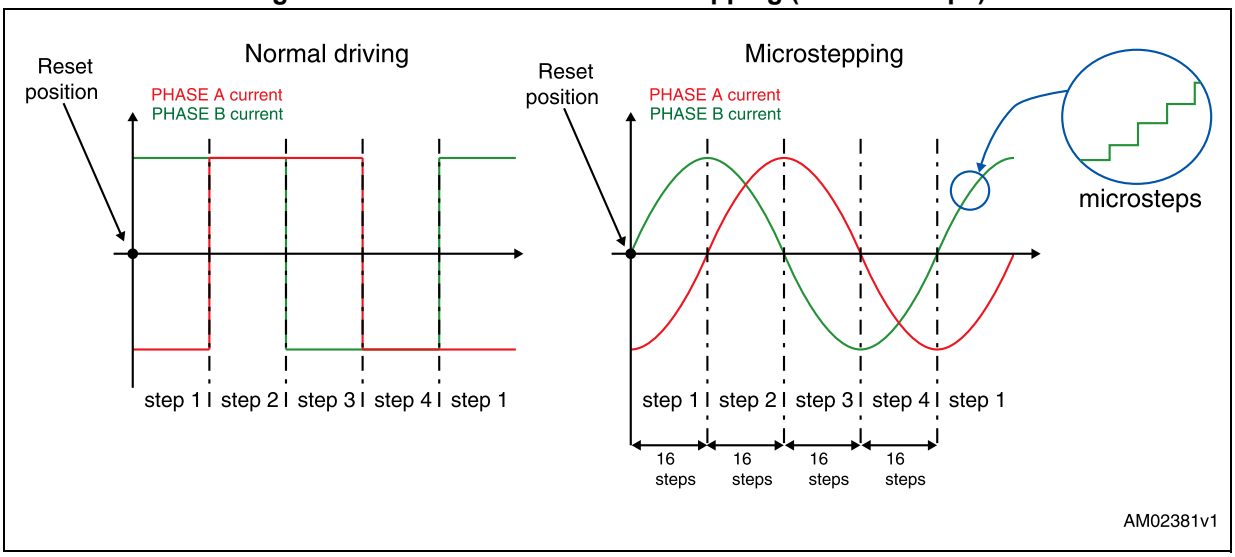



## 6.4 Microstepping

The driver is able to divide the single step into up to 16 microsteps. Step mode can be programmed by the STEP_SEL parameter in the STEP_MODE register (see *Table 20 on page 47*).

Step mode can only be changed when bridges are disabled. Every time step mode is changed, the electrical position (i.e. the point of microstepping sine wave that is generated) is reset to zero, and the absolute position counter value (see *Section 6.5*) becomes meaningless.

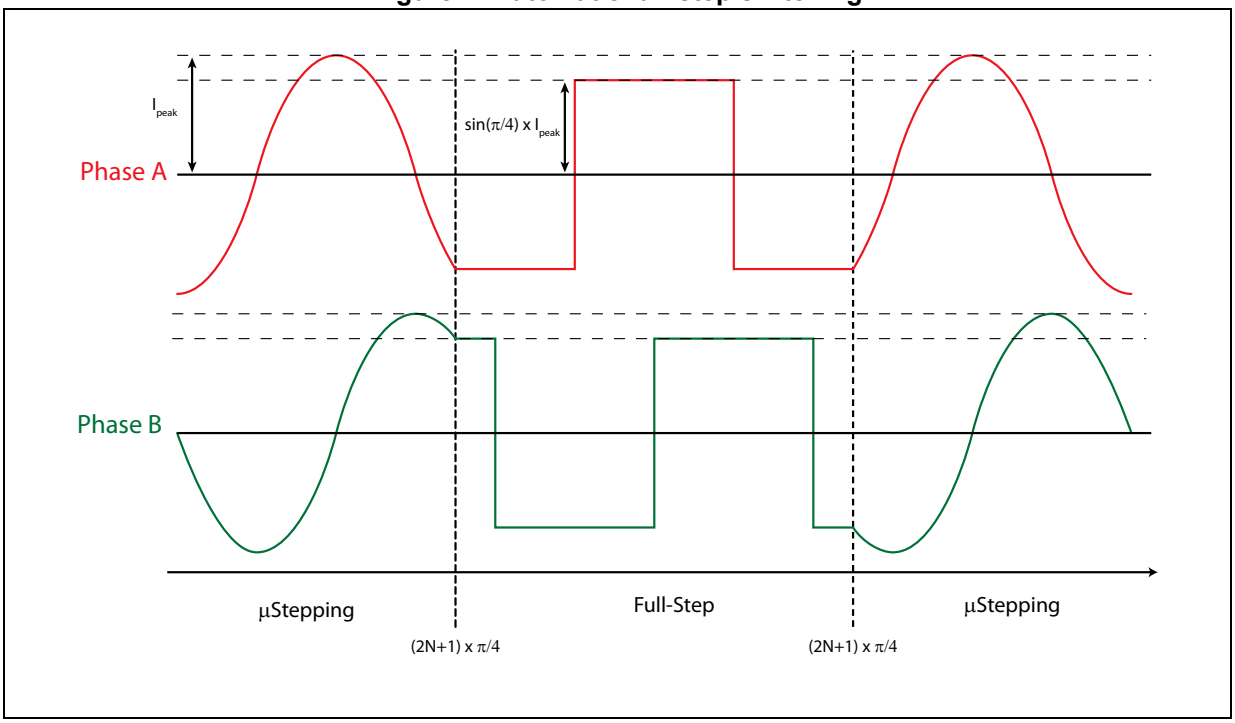
**Figure 6. Normal mode and microstepping (16 microsteps)**




## Automatic full-step mode

When motor speed is greater than a programmable full-step speed threshold, the L6472 switches automatically to full-step mode (see *Figure 7*); the driving mode returns to microstepping when motor speed decreases below the full-step speed threshold. The full-step speed threshold is set through the FS_SPD register (see *Section 9.1.9 on page 44*).

**Figure 7. Automatic full-step switching**



## 6.5 Absolute position counter

An internal 22-bit register (ABS_POS) keeps track of the motor motion according to the selected step mode; the stored value unit is equal to the selected step mode (full, half, quarter, etc.). The position range is from $-2^{21}$ to $+2^{21}-1$ (μ) steps (see *Section 9.1.1 on page 41*).

## 6.6 Programmable speed profiles

The user can easily program a customized speed profile, independently defining acceleration, deceleration, maximum and minimum speed values through the ACC, DEC, MAX_SPEED and MIN_SPEED registers respectively (see *Section 9.1.5 on page 42*, *9.1.6 on page 42*, *9.1.7 on page 43* and *9.1.8 on page 43*).

When a command is sent to the device, the integrated logic generates the microstep frequency profile that performs a motor motion compliant to speed profile boundaries.

All acceleration parameters are expressed in step/tick$^2$ and all speed parameters are expressed in step/tick; the unit of measurement does not depend on selected step mode.

Acceleration and deceleration parameters range from $2^{-40}$ to $(2^{12}-2) \cdot 2^{-40}$ step/tick2 (equivalent to 14.55 to 59590 step/s2).

Minimum speed parameter ranges from 0 to $(2^{12}-1) \cdot 2^{-24}$ step/tick (equivalent to 0 to 976.3 step/s).

Maximum speed parameter ranges from $2^{-18}$ to $(2^{10}-1) \cdot 2^{-18}$ step/tick (equivalent to 15.25 to 15610 step/s).

## 6.7 Motor control commands

The L6472 can accept different types of commands:

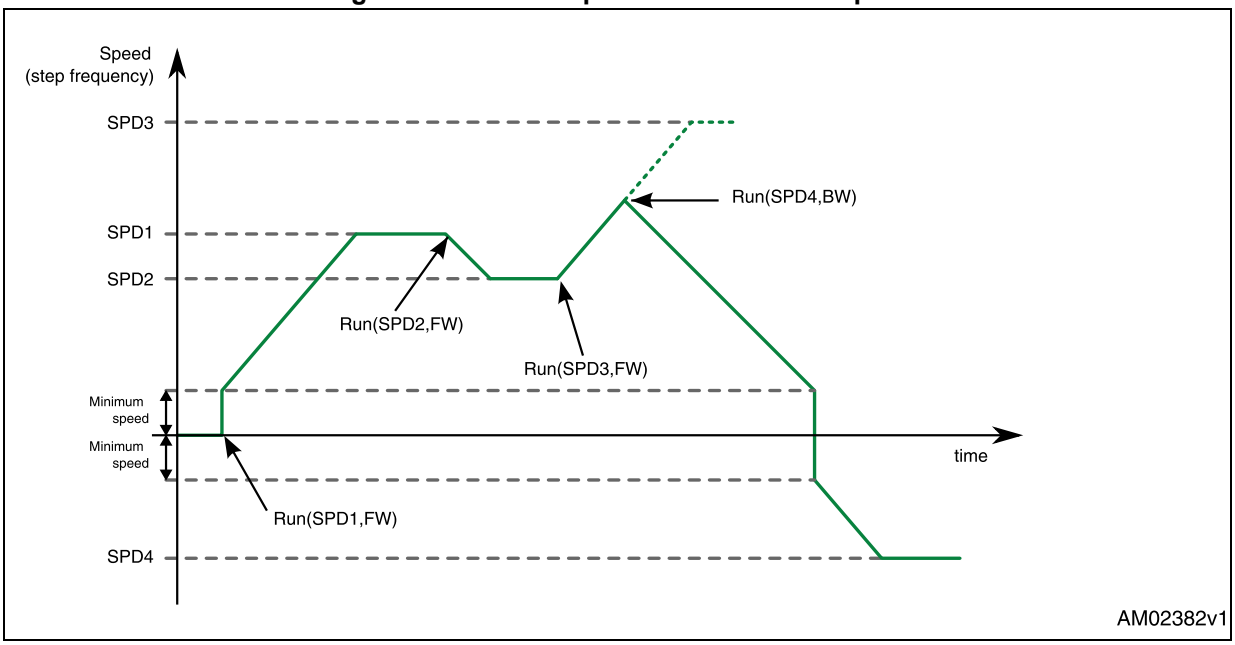
- constant speed commands (Run, GoUntil, ReleaseSW)
- absolute positioning commands (GoTo, GoTo_DIR, GoHome, GoMark)
- motion commands (Move)
- stop commands (SoftStop, HardStop, SoftHiz, HardHiz).

For detailed command descriptions refer to *Section 9.2 on page 54*.

### 6.7.1 Constant speed commands

A constant speed command produces a motion in order to reach and maintain a user defined target speed starting from the programmed minimum speed (set in the MIN_SPEED register) and with the programmed acceleration/deceleration value (set in the ACC and DEC registers). A new constant speed command can be requested anytime.

**Figure 8. Constant speed command examples**



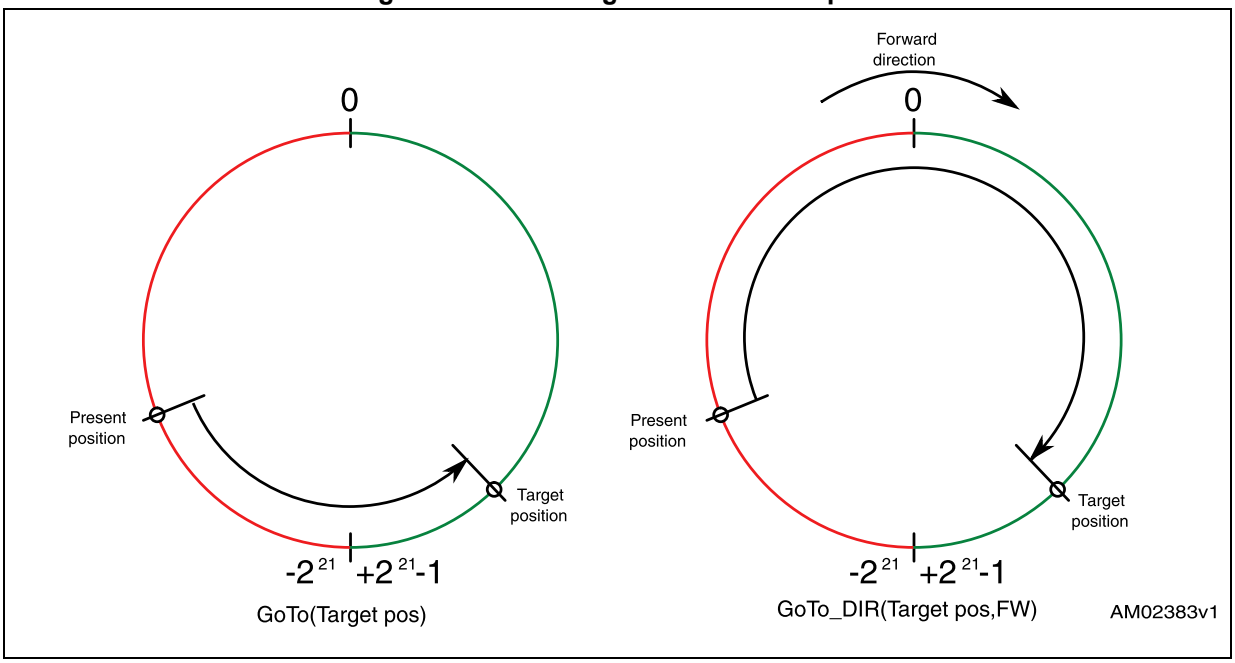

### 6.7.2 Positioning commands

An absolute positioning command produces a motion in order to reach a user-defined position that is sent to the device together with the command. The position can be reached by performing the minimum path (minimum physical distance) or forcing a direction (see *Figure 9*).

The performed motor motion is compliant to programmed speed profile boundaries (acceleration, deceleration, minimum and maximum speed).

Note that with some speed profiles or positioning commands, the deceleration phase can start before the maximum speed is reached.

**Figure 9. Positioning command examples**



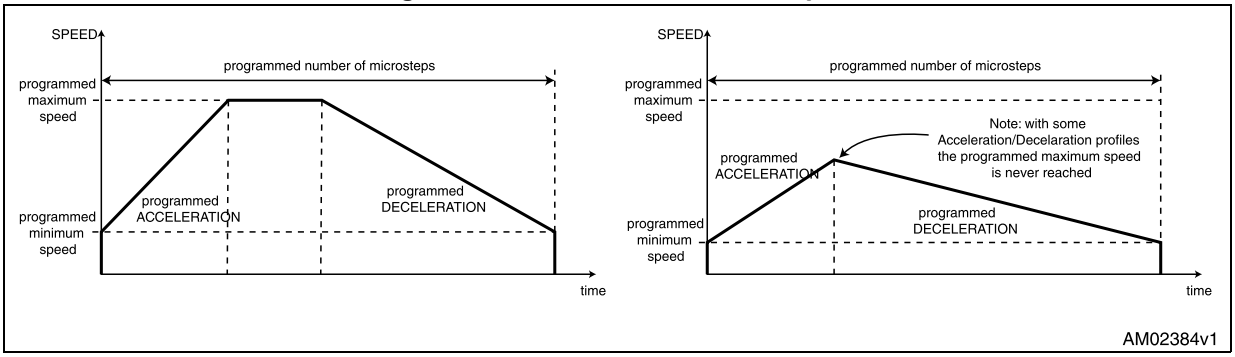

## 6.7.3 Motion commands

Motion commands produce a motion in order to perform a user-defined number of microsteps in a user-defined direction that are sent to the device together with the command (see *Figure 10*).

The performed motor motion is compliant to programmed speed profile boundaries (acceleration, deceleration, minimum and maximum speed).

Note that with some speed profiles or motion commands, the deceleration phase can start before the maximum speed is reached.

**Figure 10. Motion command examples**




## 6.7.4 Stop commands

A stop command forces the motor to stop. Stop commands can be sent anytime.

The SoftStop command causes the motor to decelerate with a programmed deceleration value until the MIN_SPEED value is reached and then stops the motor maintaining the rotor position (a holding torque is applied).