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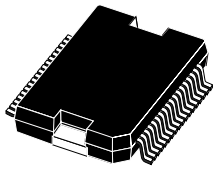
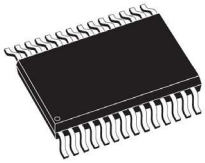
L6474

Fully integrated microstepping motor driver

Datasheet - production data



POWERSO36



HTSSOP28

Features

- Operating voltage: 8 - 45 V
- 7.0 A output peak current (3.0 $A_{r.m.s.}$)
- Low $R_{DS(on)}$ power MOSFETs
- Programmable power MOS slew rate
- Up to 1/16 microstepping
- Current control with adaptive decay
- Non-dissipative current sensing
- SPI interface
- Low quiescent and standby currents
- Programmable non-dissipative overcurrent protection on all power MOS
- Two-level overtemperature protection

Applications

- Bipolar stepper motor

Description

The L6474 device, realized in analog mixed signal technology, integrates a dual low $R_{DS(on)}$ DMOS full bridge with all power switches equipped with an accurate on-chip current sensing circuitry suitable for non-dissipative current control and overcurrent protections. Thanks to a new current control, a 1/16 microstepping is achieved through an adaptive decay mode which outperforms traditional implementations.

All data registers, including those used to set analogue values (i.e.: current control value, current protection trip point, deadtime, etc.) are sent through a standard 5 Mbit/s SPI.

A very rich set of protections (thermal, low bus voltage, overcurrent) makes the L6474 device “bullet proof” as required by the most demanding motor control applications.

Table 1. Device summary

Order code	Package	Packing
L6474H	HTSSOP28	Tube
L6474HTR	HTSSOP28	Tape and reel
L6474PD	POWERSO36	Tube
L6474PDTR	POWERSO36	Tape and reel

Contents

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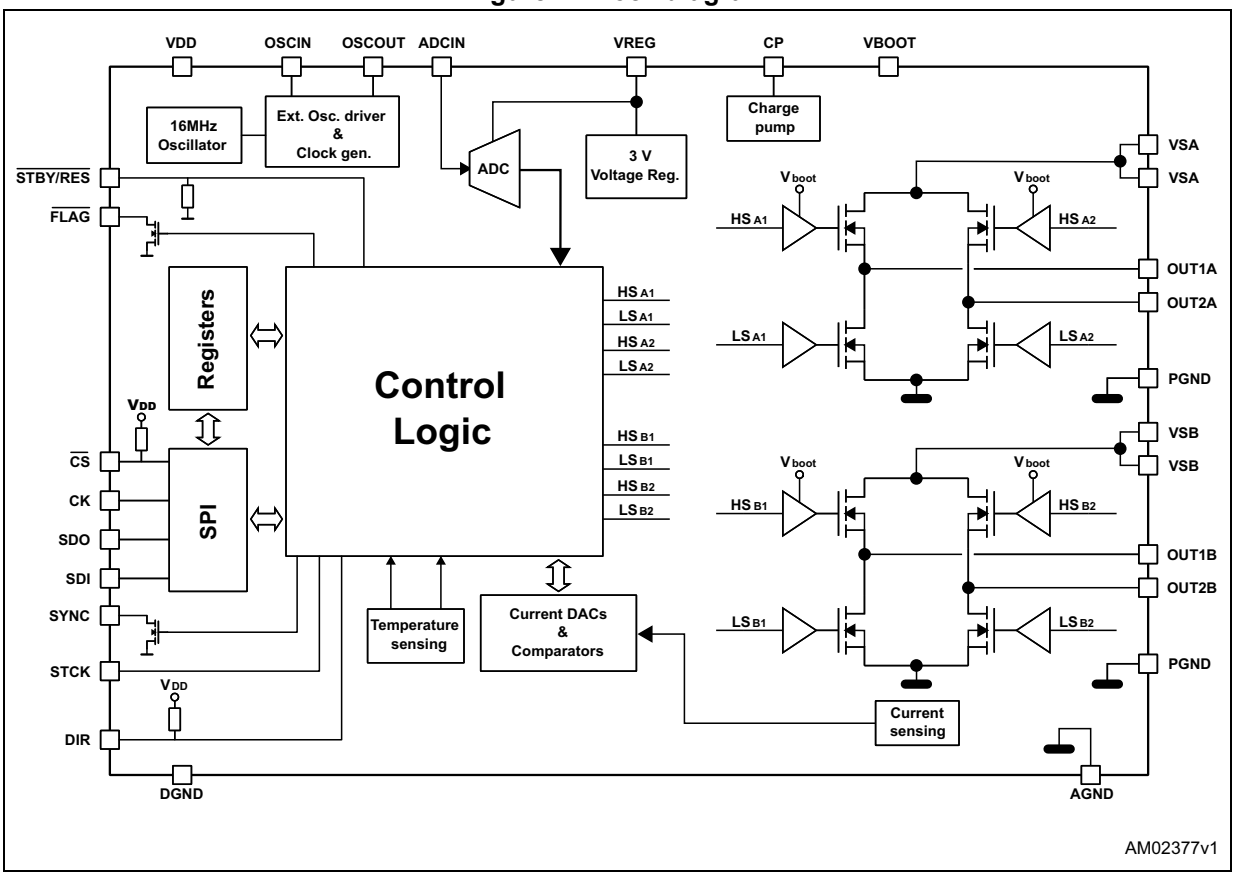
1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_{DD}	Logic interface supply voltage		5.5	V
V_S	Motor supply voltage	$V_{SA} = V_{SB} = V_S$	48	V
$V_{GND, diff}$	Differential voltage between AGND, PGND and DGND		±0.3	V
V_{boot}	Bootstrap peak voltage		55	V
V_{REG}	Internal voltage regulator output pin and logic supply voltage		3.6	V
V_{ADCIN}	Integrated ADC input voltage range (ADCIN pin)		-0.3 to +3.6	V
V_{OSC}	OSCIN and OSCOUT pin voltage range		-0.3 to +3.6	V
V_{out_diff}	Differential voltage between V_{SA}, $OUT1_A$, $OUT2_A$, PGND and V_{SB}, $OUT1_B$, $OUT2_B$, PGND pins	$V_{SA} = V_{SB} = V_S$	48	V
V_{LOGIC}	Logic inputs voltage range		-0.3 to +5.5	V
I_{out} (1)	R.m.s. output current		3	A
I_{out_peak} (1)	Pulsed output current	T_{PULSE} < 1 ms	7	A
T_{OP}	Operating junction temperature		-40 to 150	°C
T_s	Storage temperature range		-55 to 150	°C
P_{tot}	Total power dissipation (T_A = 25 ºC)	(2)	5	W

1. Maximum output current limit is related to metal connection and bonding characteristics. Actual limit must satisfy maximum thermal dissipation constraints.
2. HTSSOP28 mounted on EVAL6474H.

2.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test condition	Value			Unit
V_{DD}	Logic interface supply voltage	3.3 V logic outputs		3.3		V
		5 V logic outputs		5		
V_S	Motor supply voltage	$V_{SA} = V_{SB} = V_S$	8		45	V
V_{out_diff}	Differential voltage between V_{SA}, $OUT1_A$, $OUT2_A$, PGND and V_{SB}, $OUT1_B$, $OUT2_B$, PGND pins	$V_{SA} = V_{SB} = V_S$			45	V
$V_{REG,in}$	Logic supply voltage	V_{REG} voltage imposed by external source	3.2	3.3		V
V_{ADC}	Integrated ADC input voltage (ADCIN pin)		0		V_{REG}	V

2.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Package	Typ.	Unit
R_{thJA}	Thermal resistance junction-ambient	HTSSOP28(1)	22	°C/W
		POWERSO36(2)	12	

1. HTSSOP28 mounted on EVAL6474H Rev 1.0 board: four-layer FR4 PCB with a dissipating copper surface of about 40 cm2 on each layer and 15 via holes below the IC.
2. POWERSO36 mounted on EVAL6474PD Rev 1.0 board: four-layer FR4 PCB with a dissipating copper surface of about 40 cm2 on each layer and 22 via holes below the IC.

3 Electrical characteristics

V_{SA} = V_{SB} = 36 V; V_{DD} = 3.3 V; internal 3 V regulator; T_J = 25 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
V_{SthOn}	V_S UVLO turn-on threshold		7.5	8.2	8.9	V
V_{SthOff}	V_S UVLO turn-off threshold		6.6	7.2	7.8	V
$V_{SthHyst}$	V_S UVLO threshold hysteresis		0.7	1	1.3	V
I_q	Quiescent motor supply current	Internal oscillator selected; V_{REG} = 3.3 V ext; CP floating		0.5	0.65	mA
$T_{j(WRN)}$	Thermal warning temperature			130		°C
$T_{j(SD)}$	Thermal shutdown temperature			160		°C
Charge pump						
V_{pump}	Voltage swing for charge pump oscillator			10		V
$f_{pump,min}$	Minimum charge pump oscillator frequency(1)			660		kHz
$f_{pump,max}$	Maximum charge pump oscillator frequency(1)			800		kHz
I_{boot}	Average boot current	$f_{sw,A}$ = $f_{sw,B}$ = 15.6 kHz POW_SR = ‘10’		1.1	1.4	mA
Output DMOS transistor						
$R_{DS(on)}$	High-side switch ON resistance	T_j = 25 °C, I_{out} = 3 A		0.37		Ω
		T_j = 125 °C, (2) I_{out} = 3 A		0.51		
	Low-side switch ON resistance	T_j = 25 °C, I_{out} = 3A		0.18		
		T_j = 125 °C, (2) I_{out} = 3 A		0.23		
I_{DSS}	Leakage current	OUT = V_S			3.1	mA
		OUT = GND	-0.3			
t_r	Rise time(3)	POW_SR = '00', I_{out} = +1 A		100		ns
		POW_SR = '00', I_{out} = -1 A		80		
		POW_SR = ‘11’, I_{out} = ±1 A		100		
		POW_SR = ‘10’, I_{out} = ±1 A		200		
		POW_SR = ‘01’, I_{out} = ±1 A		300		

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_f	Fall time(3)	POW_SR = '00'; I_{out} = +1 A		90		ns
		POW_SR = '00'; I_{out} = -1 A		110		
		POW_SR = '11', I_{out} = ±1 A		110		
		POW_SR = '10', I_{out} = ±1 A		260		
		POW_SR = '01', I_{load} = ±1 A		375		
SR_{out_r}	Output rising slew rate	POW_SR = '00', I_{out} = +1 A		285		V/µs
		POW_SR = '00', I_{out} = -1 A		360		
		POW_SR = '11', I_{out} = ±1 A		285		
		POW_SR = '10', I_{out} = ±1 A		150		
		POW_SR = '01', I_{out} = ±1 A		95		
SR_{out_f}	Output falling slew rate	POW_SR = '00', I_{out} = +1 A		320		V/µs
		POW_SR = '00', I_{out} = -1 A		260		
		POW_SR = '11', I_{out} = ±1 A		260		
		POW_SR = '10', I_{out} = ±1 A		110		
		POW_SR = '01', I_{out} = ±1 A		75		
Deadtime and blanking						
t_{DT}	Deadtime(1)	POW_SR = '00'		250		ns
		POW_SR = '11', f_{OSC} = 16 MHz		375		
		POW_SR = '10', f_{OSC} = 16 MHz		625		
		POW_SR = '01', f_{OSC} = 16 MHz		875		
t_{blank}	Blanking time(1)	POW_SR = '00'		250		ns
		POW_SR = '11', f_{OSC} = 16 MHz		375		
		POW_SR = '10', f_{OSC} = 16 MHz		625		
		POW_SR = '01', f_{OSC} = 16 MHz		875		
Source-drain diodes						
$V_{SD,HS}$	High-side diode forward ON voltage	I_{out} = 1 A		1	1.1	V
$V_{SD,LS}$	Low-side diode forward ON voltage	I_{out} = 1 A		1	1.1	V
t_{rrHS}	High-side diode reverse recovery time	I_{out} = 1 A		30		ns
t_{rrLS}	Low-side diode reverse recovery time	I_{out} = 1 A		100		ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic inputs and outputs						
V_{IL}	Low logic level input voltage				0.8	V
V_{IH}	High logic level input voltage		2			V
I_{IH}	High logic level input current(4)	V_{IN} = 5 V			1	µA
I_{IL}	Low logic level input current(5)	V_{IN} = 0 V	-1			µA
V_{OL}	Low logic level output voltage(6)	V_{DD} = 3.3 V, I_{OL} = 4 mA			0.3	V
		V_{DD} = 5 V, I_{OL} = 4 mA			0.3	
V_{OH}	High logic level output voltage	V_{DD} = 3.3 V, I_{OH} = 4 mA	2.4			V
		V_{DD} = 5 V, I_{OH} = 4 mA	4.7			
R_{PU} R_{PD}	CS pull-up and STBY pull-down resistors	$\overline{CS}$ = GND; $\overline{STBY/RST}$ = 5 V	335	430	565	kΩ
R_{PUDIR}	DIR input pull-up resistance	DIR = GND	60	85	110	kΩ
I_{logic}	Internal logic supply current	3.3 V V_{REG} externally supplied, internal oscillator		3.7	4.3	mA
$I_{logic,STBY}$	Standby mode internal logic supply current	3.3 V V_{REG} externally supplied		2	2.5	µA
f_{STCK}	Step clock input frequency				2	MHz
Internal oscillator and external oscillator driver						
$f_{osc,i}$	Internal oscillator frequency	T_j = 25 °C, V_{REG} = 3.3 V	-3%	16	+3%	MHz
$f_{osc,e}$	Programmable external oscillator frequency		8		32	MHz
$V_{OSCOUTH}$	OSCOUT clock source high level voltage	Internal oscillator 3.3 V V_{REG} externally supplied; I_{OSCOUT} = 4 mA	2.4			V
$V_{OSCOUTL}$	OSCOUT clock source low level voltage	Internal oscillator 3.3 V V_{REG} externally supplied; I_{OSCOUT} = 4 mA			0.3	V
$t_{rOSCOUT}$ $t_{fOSCOUT}$	OSCOUT clock source rise and fall time	Internal oscillator			20	ns
t_{extosc}	Internal to external oscillator switching delay			3		ms
t_{intosc}	External to internal oscillator switching delay			1.5		µs
SPI						
$f_{CK,MAX}$	Maximum SPI clock frequency(7)		5			MHz
t_{rCK} t_{fCK}	SPI clock rise and fall time(7)	C_L = 30 pF			25	ns
t_{hCK} t_{lCK}	SPI clock high and low time(7)		75			ns
t_{setCS}	Chip select setup time(7)		350			ns
t_{holCS}	Chip select hold time(7)		10			ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{disCS}	Deselect time(7)		800			ns
t_{setSDI}	Data input setup time(7)		25			ns
t_{holSDI}	Data input hold time(7)		20			ns
t_{enSDO}	Data output enable time(7)				38	ns
t_{disSDO}	Data output disable time(7)				47	ns
t_{vSDO}	Data output valid time(7)				57	ns
t_{holSDO}	Data output hold time(7)		37			ns
Current control						
$I_{STEP,max}$	Max. programmable reference current			4		A
$I_{STEP,min}$	Min. programmable reference current			31		mA
Overcurrent protection						
$I_{OCD,MAX}$	Maximum programmable overcurrent detection threshold	OCD_TH = ‘1111’		6		A
$I_{OCD,MIN}$	Minimum programmable overcurrent detection threshold	OCD_TH = ‘0000’		0.375		A
$I_{OCD,RES}$	Programmable overcurrent detection threshold resolution			0.375		A
$t_{OCD,Flag}$	OCD to flag signal delay time	dI_{out}/d_t = 350A/µs		650	1000	ns
$t_{OCD,SD}$	OCD to shut down delay time	dI_{out}/d_t = 350A/µs POW_SR = '10'		600		µs
Standby						
I_{qSTBY}	Quiescent motor supply current in standby conditions	V_S = 8 V		26	34	µA
		Vs = 36 V		30	36	
$t_{STBY,min}$	Minimum standby time			10		µs
$t_{logicwu}$	Logic power-on and wake-up time			38	45	µs
t_{cpwu}	Charge pump power-on and wake-up time	Power bridges disabled, C_p = 10 nF, C_{boot} = 220 nF		650		µs
Internal voltage regulator						
V_{REG}	Voltage regulator output voltage		2.9	3	3.2	V
I_{REG}	Voltage regulator output current				40	mA
$V_{REG, drop}$	Voltage regulator output voltage drop	I_{REG} = 40 mA		50		mV
$I_{REG,STBY}$	Voltage regulator standby output current				10	mA
Integrated analog to digital converter						
N_{ADC}	Analog to digital converter resolution			5		bit

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{ADC,ref}$	Analog to digital converter reference voltage			V_{REG}		V
f_S	Analog to digital converter sampling frequency			f_{OSC}/ 512		kHz

1. Accuracy depends on oscillator frequency accuracy.
2. Tested at 25 °C in a restricted range and guaranteed by characterization.
3. Rise and fall time depends on motor supply voltage value. Refer to SR_{out} values (*Table 5*) in order to evaluate the actual rise and fall time.
4. Not valid for $\overline{\text{STBY/RST}}$ pins which have internal pull-down resistor.
5. Not valid for SW and CS pins which have internal pull-up resistor.
6. $\overline{\text{FLAG}}$ and SYNC open drain outputs included.
7. See *Figure 13: SPI timings diagram* for details.

4 Pin connection

Figure 2. HTSSOP28 pin connection (top view)

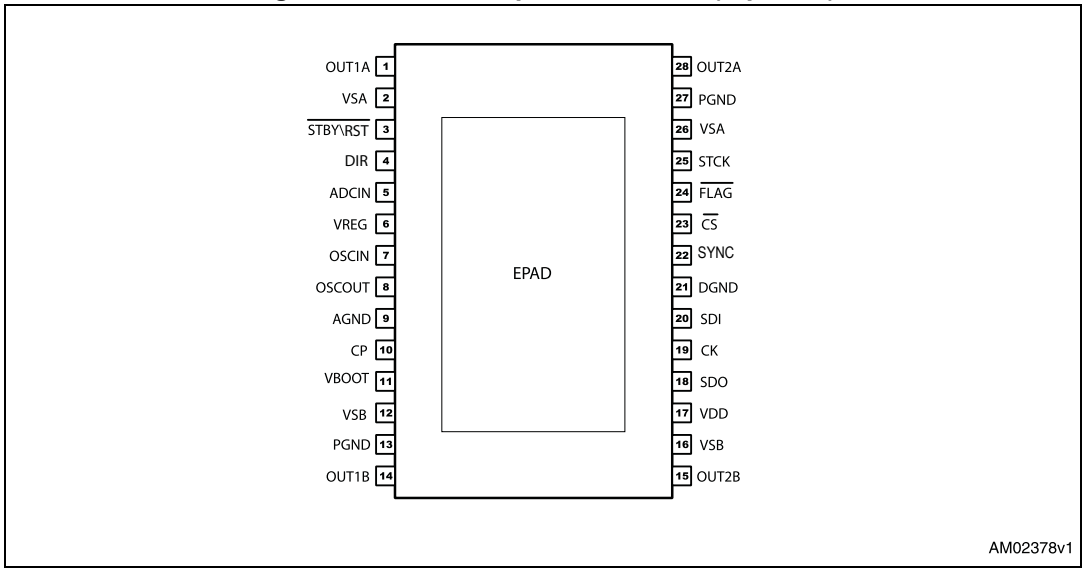
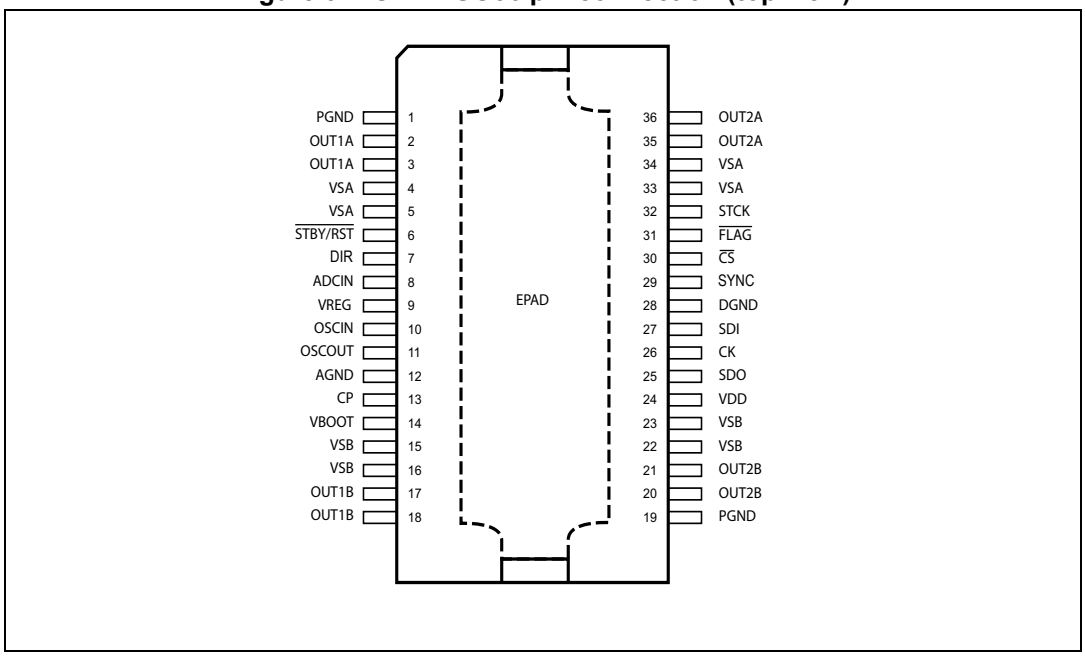


Figure 3. POWERSO36 pin connection (top view)



Pin list

Table 6. Pin description

Number		Name	Type	Function
POWERSO	HTSSOP			
24	17	VDD	Power	Logic outputs supply voltage (pull-up reference)
9	6	VREG	Power	Internal 3 V voltage regulator output and 3.3 V external logic supply
10	7	OSCIN	Analog input	Oscillator pin 1. To connect an external oscillator or clock source. If this pin is unused, it should be left floating.
11	8	OSCOUT	Analog output	Oscillator pin 2. To connect an external oscillator. When the internal oscillator is used this pin can supply 2/4/8/16 MHz. If this pin is unused, it should be left floating.
13	10	CP	Output	Charge pump oscillator output
14	11	VBOOT	Supply voltage	Bootstrap voltage needed for driving the high-side power DMOS of both bridges (A and B)
8	5	ADCIN	Analog input	Internal analog to digital converter input
4, 5	2	VSA	Power supply	Full bridge A power supply pin. It must be connected to VSB
33, 34	26			
15, 16	12	VSB	Power supply	Full bridge B power supply pin. It must be connected to VSA
22, 23	16			
1	27	PGND	Ground	Power ground pin
19	13			
2, 3	1	OUT1A	Power output	Full bridge A output 1
35, 36	28	OUT2A	Power output	Full bridge A output 2
17, 18	14	OUT1B	Power output	Full bridge B output 1
20, 21	15	OUT2B	Power output	Full bridge B output 2
12	9	AGND	Ground	Analog ground
7	4	DIR	Logical input	Direction input
28	21	DGND	Ground	Digital ground
29	22	SYNC	Open drain output	Synchronization signal.
25	18	SDO	Logic output	Data output pin for serial interface
27	20	SDI	Logic input	Data input pin for serial interface
26	19	CK	Logic input	Serial interface clock
30	23	$\overline{CS}$	Logic input	Chip select input pin for serial interface

Table 6. Pin description (continued)

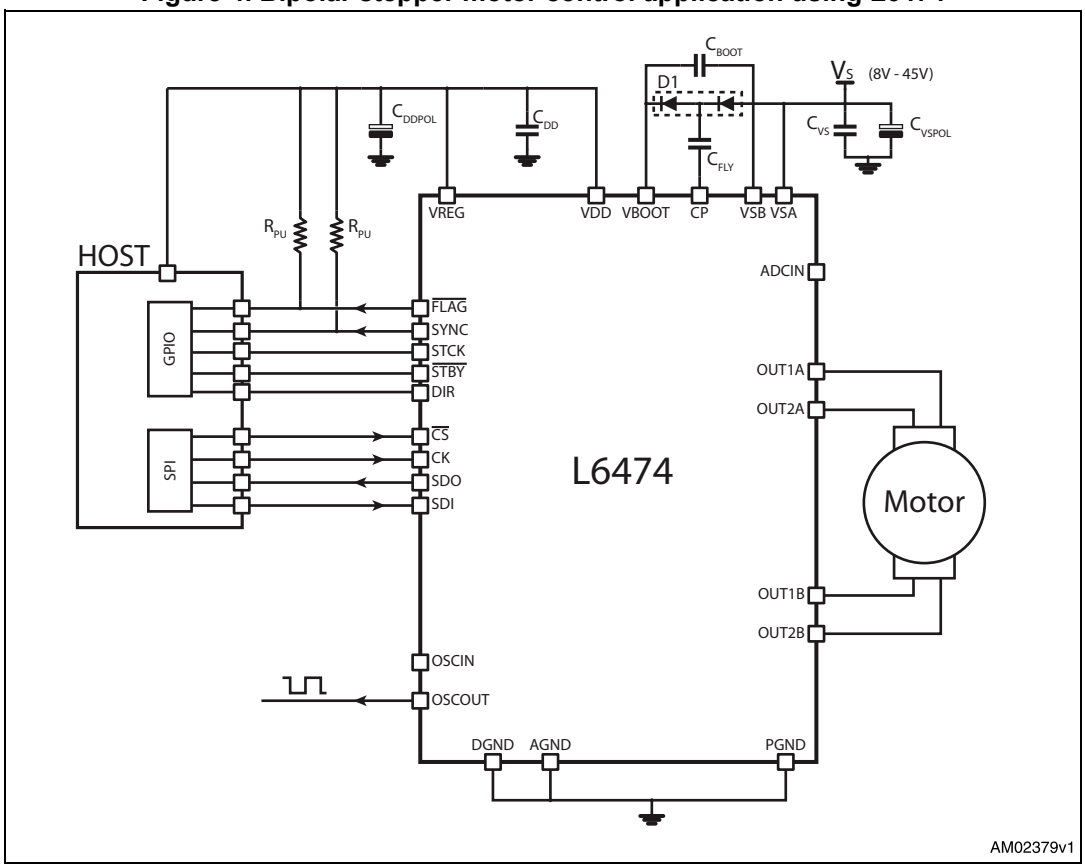
Number		Name	Type	Function
POWERSO	HTSSOP			
31	24	$\overline{\text{FLAG}}$	Open drain output	Status flag pin. An internal open drain transistor can pull the pin to GND when a programmed alarm condition occurs (step loss, OCD, thermal pre-warning or shutdown, UVLO, wrong command, non performable command)
6	3	$\overline{\text{STBY\RST}}$	Logic input	Standby and reset pin. LOW logic level resets the logic and puts the device into standby mode. If not used, should be connected to VDD
32	25	STCK	Logic input	Step clock input
	EPAD	Exposed pad	Ground	Internally connected to PGND, AGND and DGND pins

5 Typical applications

Table 7. Typical application values

Name	Value
C_{VS}	220 nF
C_{VSPOL}	100 µF
C_{REG}	100 nF
C_{REGPOL}	47 µF
C_{DD}	100 nF
C_{DDPOL}	10 µF
D1	Charge pump diodes
C_{BOOT}	220 nF
C_{FLY}	10 nF
R_{PU}	39 kΩ
R_{SW}	100 Ω
C_{SW}	10 nF

Figure 4. Bipolar stepper motor control application using L6474



6 Functional description

6.1 Device power-up

At power-up end, the device state is the following:

- Registers are set to default
- Internal logic is driven by internal oscillator and a 2 MHz clock is provided by the OSCOUT pin
- Bridges are disabled (High Z)
- UVLO bit in STATUS register is forced low (fail condition)
- FLAG output is forced low.

During power-up the device is under reset (all logic IO disabled and power bridges in high impedance state) until the following conditions are satisfied:

- V_S is greater than V_{SthOn}
- V_{REG} is greater than V_{REGth} = 2.8 V typical
- Internal oscillator is operative.

6.2 Logic I/O

Pins $\overline{CS}$, CK, SDI, STCK, DIR and $\overline{STBY\backslash RST}$ are TTL/CMOS 3.3 V - 5 V compatible logic inputs.

Pin SDO is a TTL/CMOS compatible logic output. VDD pin voltage sets the logic output pin voltage range; when it is connected to VREG or 3.3 V external supply voltage, the output is 3.3 V compatible. When VDD is connected to a 5 V supply voltage, SDO is 5 V compatible.

VDD is not internally connected to V_{REG}, an external connection is always needed.

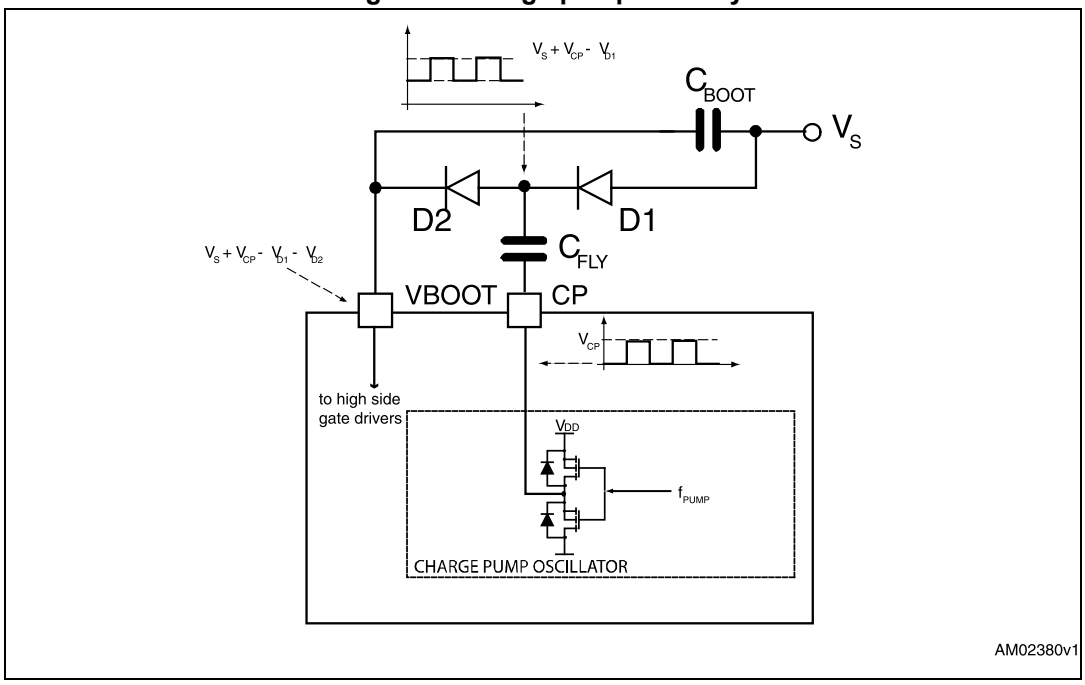
A 10 µF capacitor should be connected to the VDD pin in order to obtain a proper operation.

Pins $\overline{FLAG}$ and SYNC are open drain outputs.

6.3 Charge pump

To ensure the correct driving of the high-side integrated MOSFETs, a voltage higher than the motor power supply voltage needs to be applied to the VBOOT pin. The high-side gate driver supply voltage VBOOT is obtained through an oscillator and a few external components realizing a charge pump (see *Figure 5*).

Figure 5. Charge pump circuitry

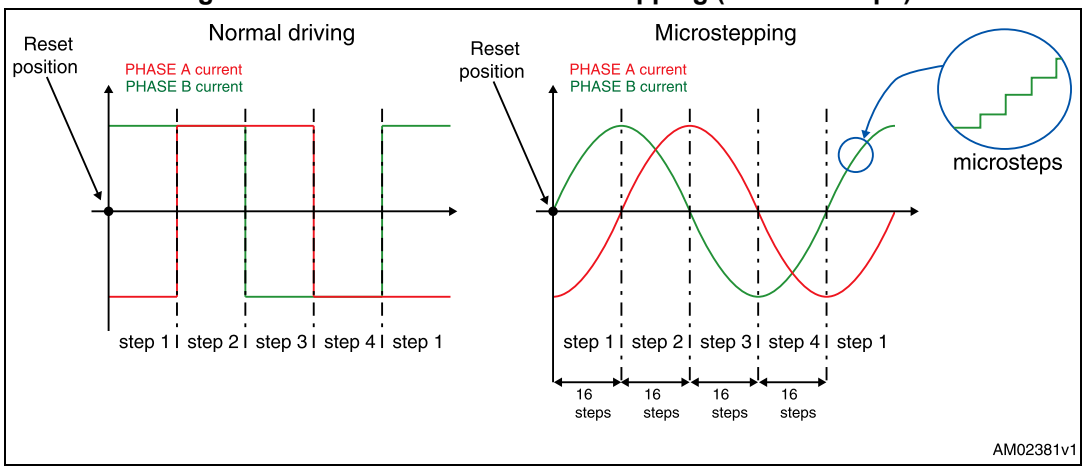


6.4 Microstepping

The driver is able to divide the single step into up to 16 microsteps. Stepping mode can be programmed by STEP_SEL parameter in STEP_MODE register (see *Table 19 on page 38*).

Step mode can only be changed when bridges are disabled. Every time the step mode is changed, the electrical position (i.e. the point of microstepping sinewave that is generated) is reset to the first microstep and the absolute position counter value (see *Section 6.5*) becomes meaningless.

Figure 6. Normal mode and microstepping (16 microsteps)



6.5 Absolute position counter

An internal 22 bit register (ABS_POS) takes memory of motor motion according to the selected step mode; the stored value unit is equal to the selected step mode (full, half, quarter, etc.). The position range is from -2^{21} to $+2^{21}-1$ (µ) steps (see *Section 9.1.1 on page 34*).

6.6 Step sequence control

The motor movement is defined by the step clock signal applied to the STCK pin. At each step clock rising edge, the motor is moved by one microstep in the direction selected by DIR input (high for forward direction and low for reverse direction) and absolute position is consequently updated.

6.7 Enable and disable commands

The power stage of the device can be enabled and disabled through the respective SPI commands.

The enable command turns on the power outputs and starts the current control algorithm. The phase currents are controlled according to present EL_POS value. If a fault condition requires the power stage to be disabled, the command is ignored.

The disable command immediately forces the power outputs in a high impedance condition.

6.8 Internal oscillator and oscillator driver

The control logic clock can be supplied by the internal 16 MHz oscillator, an external oscillator (crystal or ceramic resonator) or a direct clock signal.

These working modes can be selected by EXT_CLK and OSC_SEL parameters in the CONFIG register (see *Table 23 on page 40*).

At power-up the device starts using the internal oscillator and provides a 2 MHz clock signal on the OSCOUT pin.

Attention: In any case, before changing clock source configuration, a hardware reset is mandatory. Switching to different clock configurations during operation could cause unexpected behavior.

6.8.1 Internal oscillator

In this mode the internal oscillator is activated and OSCIN is unused. If OSCOUT clock source is enabled, the OSCOUT pin provides a 2, 4, 8 or 16 MHz clock signal (according to OSC_SEL value); otherwise it is unused (see *Figure 7*).

6.8.2 External clock source

Two types of external clock source can be selected: crystal/ceramic resonator or direct clock source. Four programmable clock frequencies are available for each external clock source: 8, 16, 24 and 32 MHz.

When an external crystal/resonator is selected, the OSCIN and OSCOUT pins are used to drive the crystal/resonator (see *Figure 7*). The crystal/resonator and load capacitors (CL) must be placed as close as possible to the pins. Refer to *Table 8* for the choice of the load capacitor value according to the external oscillator frequency.

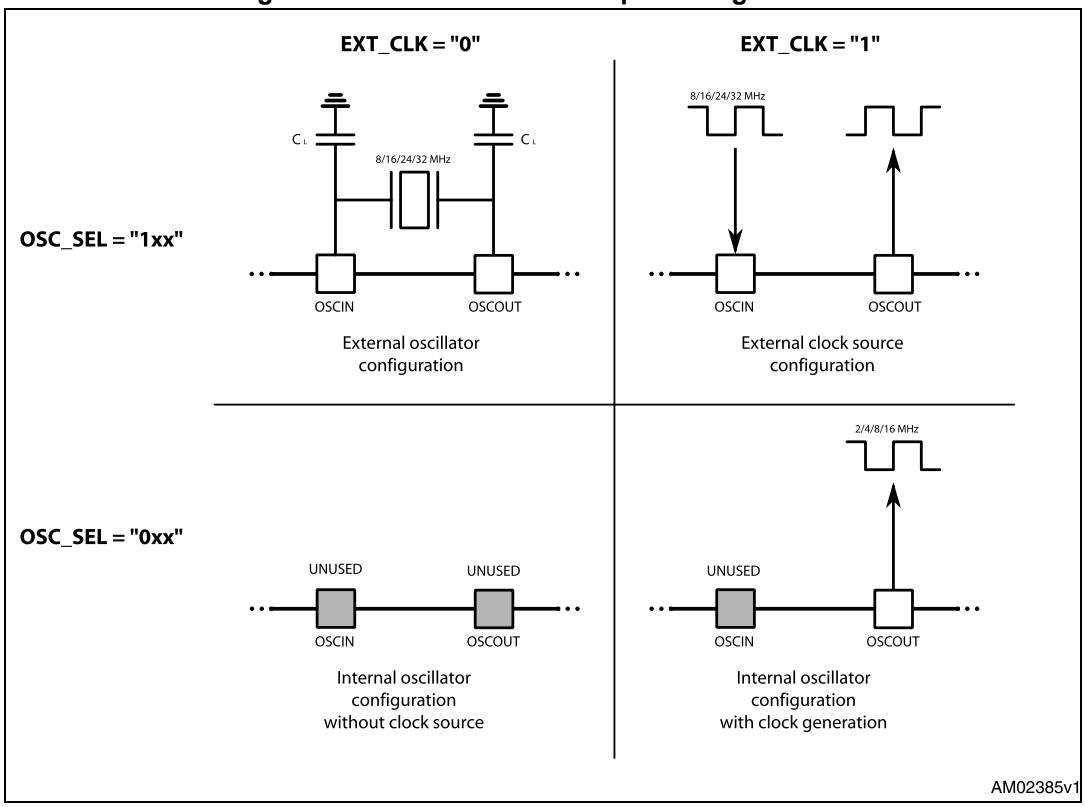
Table 8. CL values according to external oscillator frequency

Crystal/resonator freq. (1)	CL(2)
8 MHz	25 pF (ESR_{max} = 80 Ω)
16 MHz	18 pF (ESR_{max} = 50 Ω)
24 MHz	15 pF (ESR_{max} = 40 Ω)
32 MHz	10 pF (ESR_{max} = 40 Ω)

1. First harmonic resonance frequency.
2. Lower ESR value allows driving greater load capacitors.

If a direct clock source is used, it must be connected to the OSCIN pin and the OSCOUT pin supplies the inverted OSCIN signal (see *Figure 7*).

Figure 7. OSCIN and OSCOUT pin configurations



Note: When OSCIN is UNUSED, it should be left floating.
When OSCOUT is UNUSED it should be left floating.

6.9 Overcurrent detection

When the current in any of the power MOSFETs exceeds a programmed overcurrent threshold, the STATUS register OCD flag is forced low until the overcurrent event has expired and a GetStatus command is sent to the IC (see *Section 9.1.13 on page 41* and *Section 9.1.9 on page 37*). Overcurrent event expires when all the power MOSFET currents fall below the programmed overcurrent threshold.

The overcurrent threshold can be programmed through the OCD_TH register in one of 16 available values ranging from 375 mA to 6 A with steps of 375 mA (see *Section 9.1.9 on page 37*).

It is possible to set whether or not an overcurrent event causes the MOSFET turn-off (bridges in high impedance status) acting on the OC_SD bit in the CONFIG register (see *Section 9.1.12 on page 39*). The OCD flag in the STATUS register is raised anyway (see *Table 28 on page 41*, *Section 9.1.13*).

When the IC outputs are turned off by an OCD event, they cannot be turned on until the OCD flag is released by a GetStatus command.

Attention: **The overcurrent shutdown is a critical protection feature. It is not recommended to disable it.**

6.10 Undervoltage lockout (UVLO)

The L6474 provides a motor supply UVLO protection. When the motor supply voltage falls below the VSthOff threshold voltage, the STATUS register UVLO flag is forced low. When a GetStatus command is sent to the IC, and the undervoltage condition has expired, the UVLO flag is released (see *Section 9.1.13 on page 41* and *Section 9.2.7 on page 46*). Undervoltage condition expires when the motor supply voltage goes over the VSthOn threshold voltage. When the device is in undervoltage condition no motion can be performed. The UVLO flag is forced low by logic reset (power-up included) even if no UVLO condition is present.

6.11 Thermal warning and thermal shutdown

An internal sensor allows the L6474 to detect when the device internal temperature exceeds a thermal warning or an overtemperature threshold.

When the thermal warning threshold ($T_{j(WRN)}$) is reached, the TH_WRN bit in the STATUS register is forced low (see *Section 9.1.13*) until the temperature decreases below $T_{j(WRN)}$ and a GetStatus command is sent to the IC (see *Section 9.1.13* and *Section 9.2.7*).

When the thermal shutdown threshold ($T_{j(OFF)}$) is reached, the device goes into thermal shutdown condition: the TH_SD bit in the STATUS register is forced low, the power bridges are disabled, bridges in high impedance state and the HiZ bit in the STATUS register are raised (see *Section 9.1.13*).

Thermal shutdown condition only expires when the temperature goes below the thermal warning threshold ($T_{j(WRN)}$).

On exiting thermal shutdown condition, the bridges are still disabled (HiZ flag high).

6.12 Reset and standby

The device can be reset and put into standby mode through a dedicated pin. When the STBY\RST pin is driven low, the bridges are left open (High Z state), the internal charge pump is stopped, the SPI interface and control logic are disabled, and the internal 3 V voltage regulator maximum output current is reduced to $I_{REG,STBY}$; as a result the L6474 heavily reduces the power consumption. At the same time the register values are reset to default and all protection functions are disabled. STBY\RST input must be forced low at least for $t_{STBY,\ min}$. in order to ensure the complete switch to standby mode.

On exiting standby mode, as well as for IC power-up, a delay of up to $t_{logicwu}$ must be given before applying a new command to allow proper oscillator and logic startup and a delay of up to t_{cpwu} must be given to allow the charge pump startup.

On exiting standby mode the bridges are disabled (HiZ flag high).

Attention: **It is not recommended to reset the device when outputs are active. The device should be switched to high impedance state before being reset.**

6.13 Programmable DMOS slew rate, deadtime and blanking-time

Using the POW_SR parameter in the CONFIG register, it is possible to set the commutation speed of the power bridges output (see *Table 25 on page 41*).

6.14 Integrated analog to digital converter

The L6474 integrates a N_{ADC} bit ramp-compare analog to digital converter with a reference voltage equal to VREG. The analog to digital converter input is available through the ADCIN pin and the conversion result is available in the ADC_OUT register (see *Section 9.1.13 on page 41*). Sampling frequency is equal to the clock frequency divided by 512.

The ADC_OUT value can be used for the torque regulation or is at the user's disposal.

6.15 Internal voltage regulator

The L6474 integrates a voltage regulator which generates a 3 V voltage starting from the motor power supply (VSA and VSB). In order to make the voltage regulator stable, at least 22 µF should be connected between the VREG pin and ground (suggested value is 47 µF).

The internal voltage regulator can be used to supply the VDD pin in order to make the device digital output range 3.3 V compatible (*Figure 8*). A digital output range 5 V compatible can be obtained connecting the VDD pin to an external 5 V voltage source. In both cases, a 10 µF capacitance should be connected to the VDD pin in order to obtain a correct operation.

The internal voltage regulator is able to supply a current up to $I_{REG,MAX}$, internal logic consumption included (I_{logic}). When the device is in standby mode the maximum current that can be supplied is $I_{REG, STBY}$, internal consumption included ($I_{logic, STBY}$).

If an external 3.3 V regulated voltage is available, it can be applied to the VREG pin in order to supply all the internal logic and avoid power dissipation of the internal 3 V voltage regulator (*Figure 8*). The external voltage regulator should never sink current from the VREG pin.