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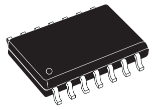
Advanced transition-mode PFC controller

Features

- Very precise adjustable output overvoltage protection
- Tracking boost function
- Protection against feedback loop failure (Latched shutdown)
- Interface for cascaded converter's PWM controller
- Input voltage feedforward (1/V^2)
- Inductor saturation detection (L6563 only)
- Remote ON/OFF control
- Low (≤ 90µA) start-up current
- 5mA max. quiescent current
- 1.5% (@ T_J = 25°C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SO14 package



SO-14

Applications

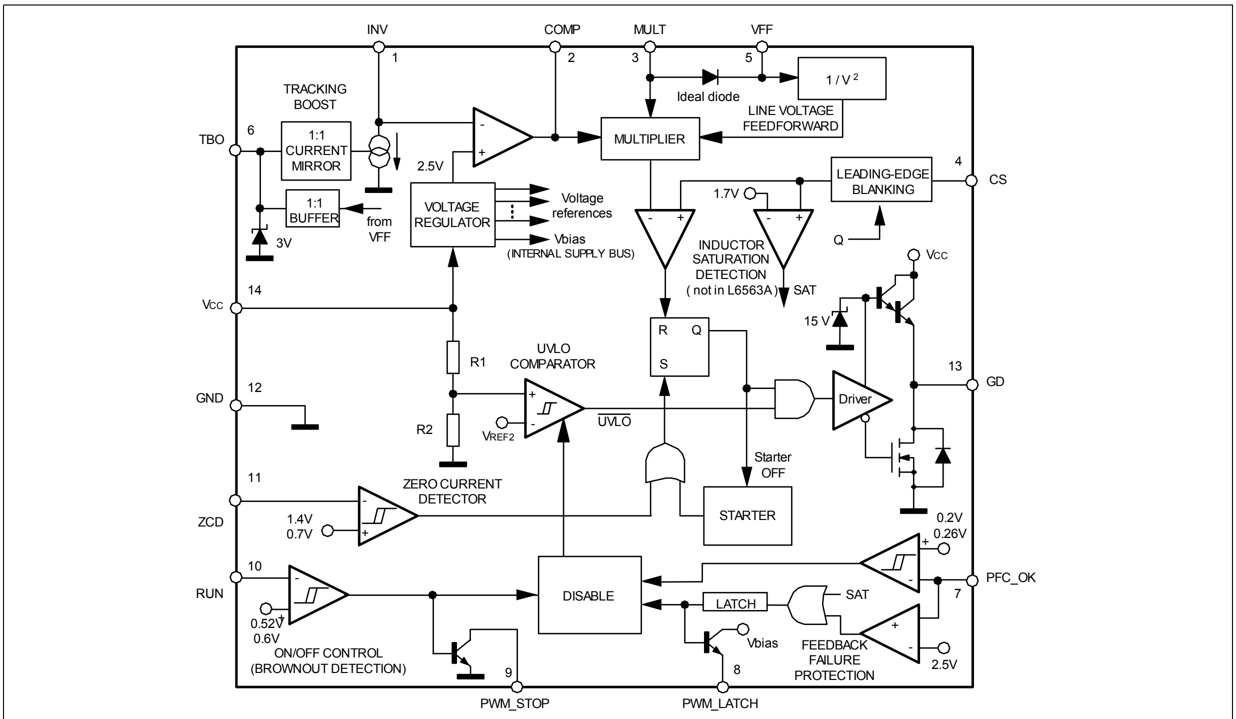
PFC pre-regulators for:

- HI-END AC-DC adapter/charger
- Desktop PC, server, WEB server
- IEC61000-3-2 OR JEIDA-MITI compliant SMPS, in excess of 350W

Table 1. Device summary

Part number	Package	Packaging
L6563	SO-14	Tube
L6563TR	SO-14	Tape & Reel
L6563A	SO-14	Tube
L6563ATR	SO-14	Tape & Reel

Figure 1. Block diagram



Contents

1 Description

The device is a current-mode PFC controller operating in Transition Mode (TM). Based on the core of a standard TM PFC controller, it offers improved performance and additional functions.

The highly linear multiplier, along with a special correction circuit that reduces crossover distortion of the mains current, allows wide-range-mains operation with an extremely low THD even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and a precise (1.5% @T_J = 25°C) internal voltage reference. The stability of the loop and the transient response to sudden mains voltage changes are improved by the voltage feedforward function ($1/V^2$ correction).

Additionally, the IC provides the option for tracking boost operation (where the output voltage is changed tracking the mains voltage). The device features extremely low consumption (≤ 90 µA before start-up and ≤ 5 mA running).

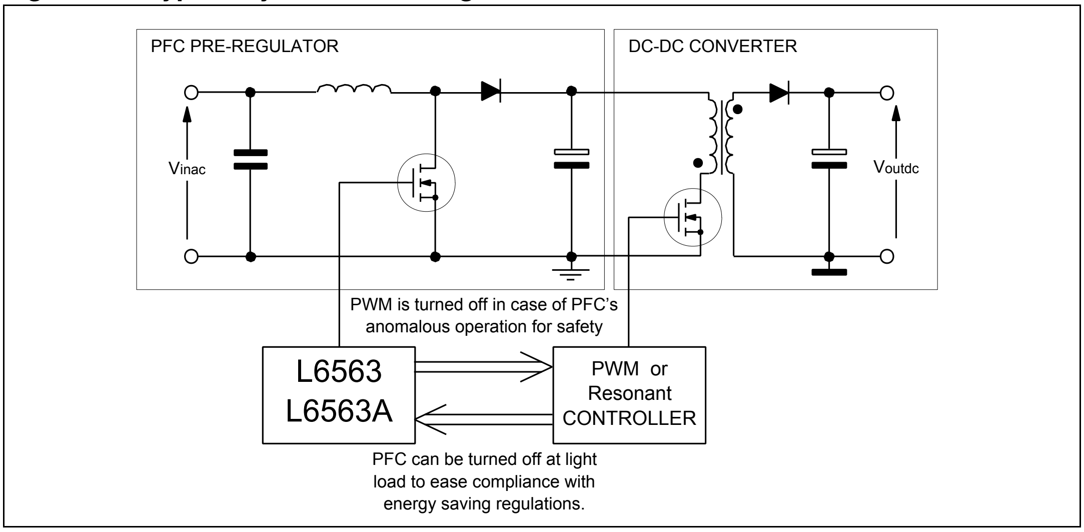
In addition to an effective two-step OVP that handles normal operation overvoltages, the IC provides also a protection against feedback loop failures or erroneous output voltage setting.

In the L6563 a protection is added to stop the PFC stage in case the boost inductor saturates. This function is not included in the L6563A. This is the only difference between the two part numbers.

An interface with the PWM controller of the DC-DC converter supplied by the PFC pre-regulator is provided: the purpose is to stop the operation of the converter in case of anomalous conditions for the PFC stage (feedback loop failure, boost inductor's core saturation) in the L6563 only and to disable the PFC stage in case of light load for the DC-DC converter, so as to make it easier to comply with energy saving norms (Blue Angel, EnergyStar, Energy2000, etc.). The device includes disable functions suitable for remote ON/OFF control both in systems where the PFC pre-regulator works as a master and in those where it works as a slave.

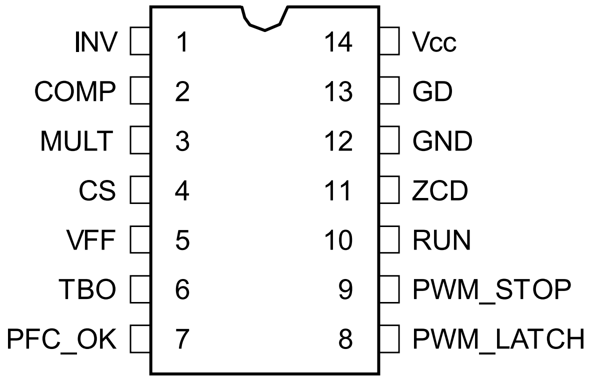
The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable to drive high current MOSFETs or IGBTs. This, combined with the other features and the possibility to operate with the proprietary Fixed-Off-Time control, makes the device an excellent low-cost solution for EN61000-3-2 compliant SMPS in excess of 350W.

Figure 2. Typical system block diagram



1.1 Pin connection

Figure 3. Pin connection (top view)



1.2 Pin description

Table 2. Pin description

Pin N°	Name	Description
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. The pin normally features high impedance but, if the tracking boost function is used, an internal current generator programmed by TBO (pin 6) is activated. It sinks current from the pin to change the output voltage so that it tracks the mains voltage.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin 1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop. The voltage on this pin is used also to derive the information on the RMS mains voltage.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET's turn-off. A second comparison level at 1.7V detects abnormal currents (e.g. due to boost inductor saturation) and, on this occurrence, shuts down the IC, reduces its consumption almost to the start-up level and asserts PWM_LATCH (pin 8) high. This function is not present in the L6563A.
5	VFF	Second input to the multiplier for $1/V^2$ function. A capacitor and a parallel resistor must be connected from the pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage at this pin, a DC level equal to the peak voltage at pin MULT (pin 3), compensates the control loop gain dependence on the mains voltage. Never connect the pin directly to GND.

Table 2. Pin description (continued)

Pin N°	Name	Description
6	TBO	Tracking Boost function. This pin provides a buffered VFF voltage. A resistor connected between this pin and GND defines a current that is sunk from pin INV (pin 1). In this way, the output voltage is changed proportionally to the mains voltage (tracking boost). If this function is not used leave this pin open.
7	PFC_OK	PFC pre-regulator output voltage monitoring/disable function. This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage at the pin exceeds 2.5V the IC is shut down, its consumption goes almost to the start-up level and this condition is latched. PWM_LATCH pin is asserted high. Normal operation can be resumed only by cycling the Vcc. This function is used for protection in case the feedback loop fails. If the voltage on this pin is brought below 0.2V the IC is shut down and its consumption is considerably reduced. To restart the IC the voltage on the pin must go above 0.26V. If these functions are not needed, tie the pin to a voltage between 0.26 and 2.5 V.
8	PWM_LATCH	Output pin for fault signaling. During normal operation this pin features high impedance. If either a voltage above 2.5V at PFC_OK (pin 7) or a voltage above 1.7V on CS (pin 4) of L6563 is detected the pin is asserted high. Normally, this pin is used to stop the operation of the DC-DC converter supplied by the PFC pre-regulator by invoking a latched disable of its PWM controller. If not used, the pin will be left floating.
9	PWM_STOP	Output pin for fault signaling. During normal operation this pin features high impedance. If the IC is disabled by a voltage below 0.5V on RUN (pin 10) the voltage at the pin is pulled to ground. Normally, this pin is used to temporarily stop the operation of the DC-DC converter supplied by the PFC pre-regulator by disabling its PWM controller. If not used, the pin will be left floating.
10	RUN	Remote ON/OFF control. A voltage below 0.52V shuts down (not latched) the IC and brings its consumption to a considerably lower level. PWM_STOP is asserted low. The IC restarts as the voltage at the pin goes above 0.6V. Connect this pin to VFF (pin 5) either directly or through a resistor divider to use this function as brownout (AC mains undervoltage) protection, tie to INV (pin 1) if the function is not used.
11	ZCD	Boost inductor’s demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET’s turn-on.
12	GND	Ground. Current return for both the signal part of the IC and the gate driver.
13	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET’s and IGBT’s with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages.
14	VCC	Supply Voltage of both the signal part of the IC and the gate driver.

2 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	14	IC supply voltage (Icc = 20mA)	self-limited	V
---	2, 4 to 6, 8 to 10	Analog inputs & outputs	-0.3 to 8	V
---	1, 3, 7	Max. pin voltage (I_{pin} = 1 mA)	Self-limited	V
I_{PWM_STOP}	10	Max. sink current	3	mA
I_{ZCD}	9	Zero current detector max. current	-10 (source) 10 (sink)	mA
P_{TOT}		Power dissipation @T_A = 50°C	0.75	W
T_J		Junction temperature operating range	-25 to 150	°C
T_{STG}		Storage temperature	-55 to 150	°C

3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient	120	°C/W

4 Electrical characteristics

Table 5. Electrical characteristics

(-25°C < T_J < +125°C, V_{CC} = 12V, C_o = 1nF between pin GD and GND, C_{FF} =1µF between pin V_{FF} and GND; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply voltage						
Vcc	Operating range	After turn-on	10.3		22	V
Vcc_{On}	Turn-on threshold	(1)	11	12	13	V
Vcc_{Off}	Turn-off threshold	(1)	8.7	9.5	10.3	V
Hys	Hysteresis		2.3		2.7	V
V_Z	Zener Voltage	Icc = 20 mA	22	25	28	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, Vcc = 10V		50	90	µA
I_q	Quiescent current	After turn-on		3	5	mA
I_{CC}	Operating supply current	@ 70kHz		3.8	5.5	mA
I_{qdis}	Idle state quiescent Current	Latched by PFC_OK > Vthl or Vcs > V_{CSdis}		180	250	µA
		Disabled by PFC_OK < Vth or RUN < V_{DIS}		1.5	2.2	mA
I_q	Quiescent current	During static/dynamic OVP		2	3	mA
Multiplier input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 3 V		-0.2	-1	µA
V_{MULT}	Linear operation range		0 to 3			V
V_{CLAMP}	Internal clamp level	I_{MULT} = 1 mA	9	9.5		V
$\frac{\Delta V_{cs}}{\Delta V_{MULT}}$	Output max. slope	V_{MULT}=0 to 0.5V, V_{FF}=0.8V V_{COMP} = Upper clamp	2.2	2.34		V/V
K_M	Gain (3)	V_{MULT} = 1 V, V_{COMP}= 4 V, V_{VFF} = V_{MULT}	0.375	0.45	0.525	V
Error amplifier						
V_{INV}	Voltage feedback input threshold	T_J = 25 °C	2.465	2.5	2.535	V
		10.3 V < Vcc < 22 V (2)	2.44		2.56	
	Line regulation	Vcc = 10.3 V to 22V		2	5	mV
I_{INV}	Input bias current	TBO open, V_{INV} = 0 to 4 V		-0.2	-1	µA

Table 5. Electrical characteristics (continued)
(-25°C < T_J < +125°C, V_{CC} = 12V, C_o = 1nF between pin GD and GND, C_{FF} =1µF between pin V_{FF} and GND; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V_{INVCLAMP}$	Internal clamp level	I_{INV} = 1 mA	9	9.5		V
Gv	Voltage gain	Open loop	60	80		dB
GB	Gain-bandwidth product			1		MHz
I_{COMP}	Source current	V_{COMP} = 4V, V_{INV} = 2.4 V	-2	-3.5	-5	mA
	Sink current	V_{COMP} = 4V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5 mA	5.7	6.2	6.7	V
	Lower clamp voltage	I_{SINK} = 0.5 mA (2)	2.1	2.25	2.4	V
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			-1	µA
t_{LEB}	Leading edge blanking		100	200	300	ns
$td_{(H-L)}$	Delay to output			120		ns
$V_{CSclamp}$	Current sense reference clamp	V_{COMP} = Upper clamp, V_{VFF} = V_{MULT} =0.5V	1.0	1.08	1.16	V
Vcs_{offset}	Current sense offset	V_{MULT} = 0, V_{VFF} = 3V		25		mV
		V_{MULT} = 3V, V_{VFF} = 3V		5		
V_{CSdis}	Ic latch-off level (L6563 only)	(2)	1.6	1.7	1.8	V
Output overvoltage						
I_{OVP}	Dynamic OVP triggering current		17	20	23	µA
Hys	Hysteresis	(4)		15		µA
	Static OVP threshold	(2)	2	2.15	2.3	V
Voltage feedforward						
V_{VFF}	Linear operation range	R_{FF} = 47 kΩ to GND	0.5		3	V
ΔV	Dropout V_{MULTpk}-V_{VFF}				20	mV

Table 5. Electrical characteristics (continued)
(-25°C < T_J < +125°C, V_{CC} = 12V, C_o = 1nF between pin GD and GND, C_{FF} =1µF between pin V_{FF} and GND; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	5.0	5.7		V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 2.5 mA	-0.3	0	0.3	V
V_{ZCDA}	Arming voltage (positive-going edge)	(4)		1.4		V
V_{ZCDT}	Triggering voltage (negative-going edge)	(4)		0.7		V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 4.5 V			1	µA
I_{ZCDsrc}	Source current capability		-2.5			mA
I_{ZCDsnk}	Sink current capability		2.5			mA
Tracking boost function						
ΔV	Dropout voltage V_{VFF} - V_{TBO}	I_{TBO} = 0.25 mA			20	mV
I_{TBO}	Linear operation		0		0.25	mA
	I_{INV} - I_{TBO} current mismatch	I_{TBO} = 25 µA to 0.25 mA	-3.5		3.5	%
$V_{TBOclamp}$	Clamp voltage	V_{VFF} = 4V (2)	2.9	3	3.1	V
PFC_OK						
V_{thl}	Latch-off threshold	Voltage rising (2)	2.4	2.5	2.6	V
V_{th}	Disable threshold	Voltage falling (2)		0.2		V
V_{EN}	Enable threshold	Voltage rising (2)		0.26		V
I_{PFC_OK}	Input bias current	V_{PFC_OK} = 0 to 2.5V		-0.1	-1	µA
V_{clamp}	Clamp voltage	I_{PFC_OK} = 1 mA	9	9.5		V
PWM_LATCH						
I_{leak}	Low level leakage current	V_{PWM_LATCH}=0			-1	µA
V_H	High level	I_{PWM_LATCH} = -0.5 mA	3.7			V
PWM_STOP						
I_{leak}	High level leakage current	V_{PWM_STOP} = 6V			1	µA
V_L	Low level	I_{PWM_STOP} = 0.5 mA			1	V
V_{clamp}	Clamp voltage	I_{PFC_OK} = 2 mA	9	9.5		V

Table 5. Electrical characteristics (continued)
($-25°C < T_J < +125°C$, V_{CC} = 12V, C_o = 1nF between pin GD and GND, C_{FF} =1µF between pin V_{FF} and GND; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Run function						
I_{RUN}	Input bias current	V_{RUN} = 0 to 3 V			-1	µA
V_{DIS}	Disable threshold	Voltage falling (2)	0.5	0.52	0.54	V
V_{EN}	Enable threshold	Voltage rising (2)	0.56	0.6	0.64	V
Start timer						
t_{START}	Start timer period		75	150	300	µs
Gate driver						
V_{OHdrop}	Dropout voltage	$I_{GDsource}$ = 20 mA		2	2.6	V
		$I_{GDsource}$ = 200 mA		2.5	3	V
V_{OLdrop}		I_{GDsink} = 200 mA		1	2	V
t_f	Current fall time			30	70	ns
t_r	Current rise time			40	80	ns
V_{Oclamp}	Output clamp voltage	$I_{GDsource}$ = 5mA; Vcc = 20V	10	12	15	V
	UVLO saturation	Vcc=0 to Vcc_{On}, I_{sink}=10mA			1.1	V

(1), (2) Parameters tracking each other

(3) The multiplier output is given by: $V_{CS} = K_M \cdot \frac{V_{MULT} \cdot (V_{COMP} - 2.5)}{V_{VFF}^2}$

(4) Parameters guaranteed by design, functionality tested in production.

5 Typical electrical performance

Figure 4. Supply current vs supply voltage

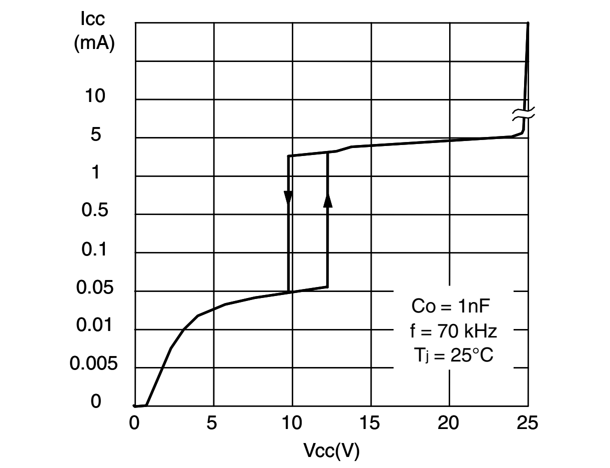


Figure 5. V_{CC} Zener voltage vs T_J

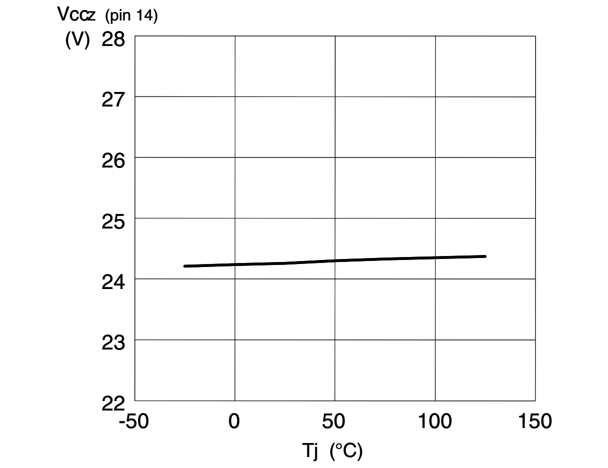


Figure 6. IC consumption vs T_J

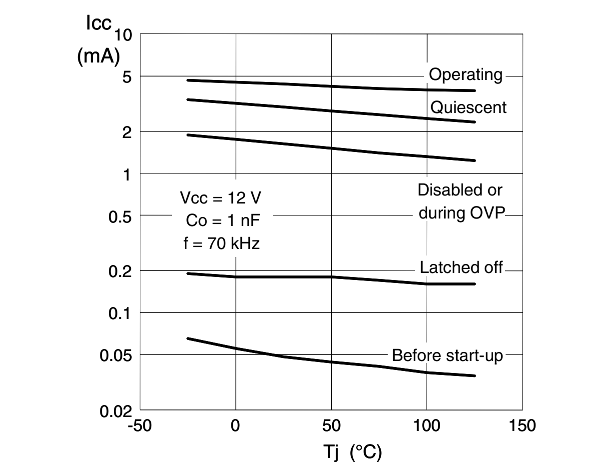


Figure 7. Feedback reference vs T_J

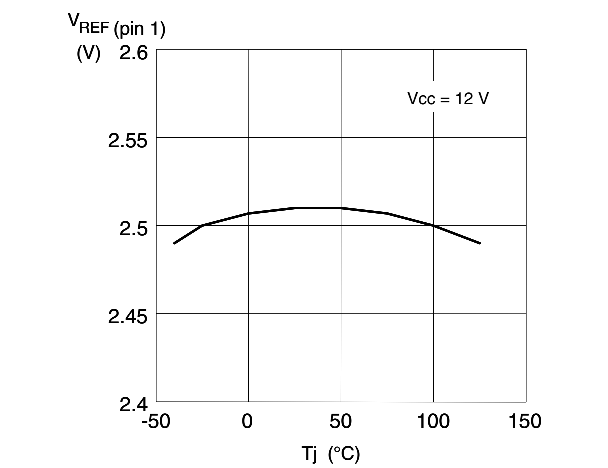


Figure 8. Start-up & UVLO vs T_J

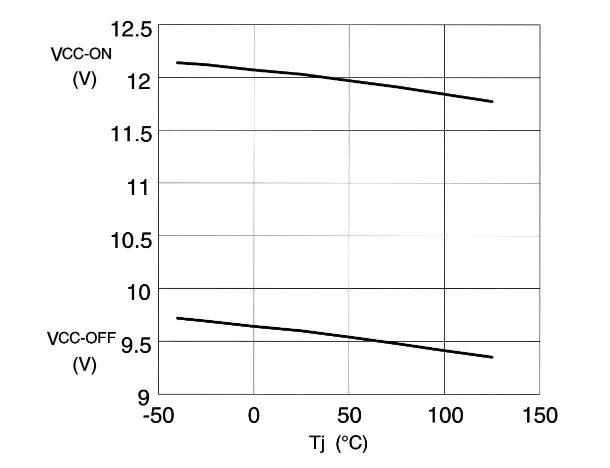


Figure 9. E/A output clamp levels vs T_J

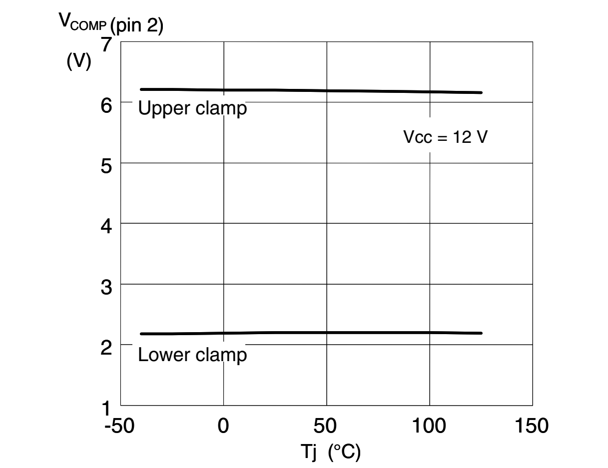


Figure 10. Static OVP level vs T_J

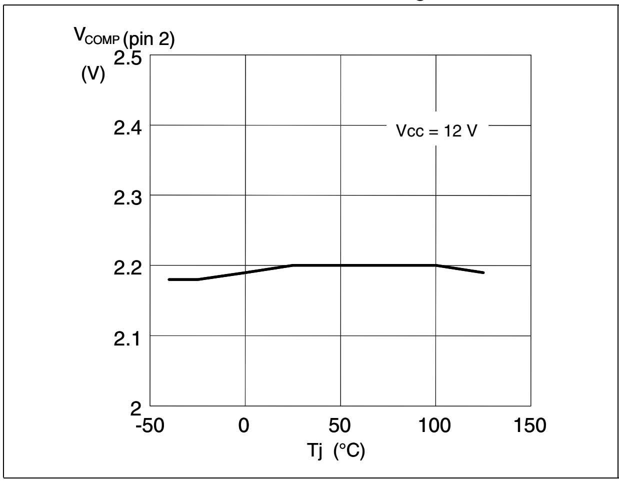


Figure 11. Vcs clamp vs T_J

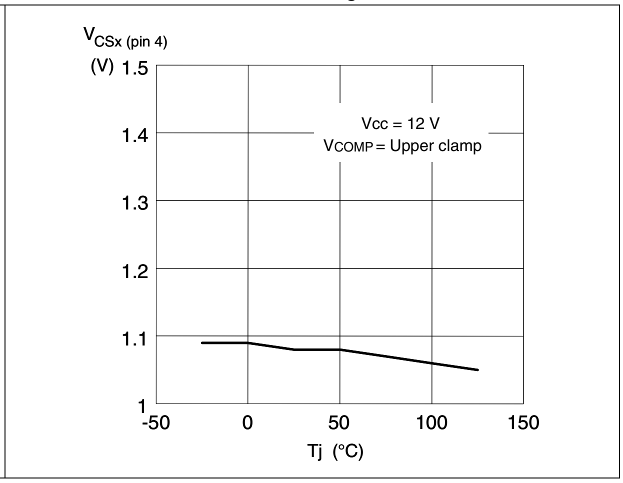


Figure 12. Dynamic OVP current vs T_J (normalized value)

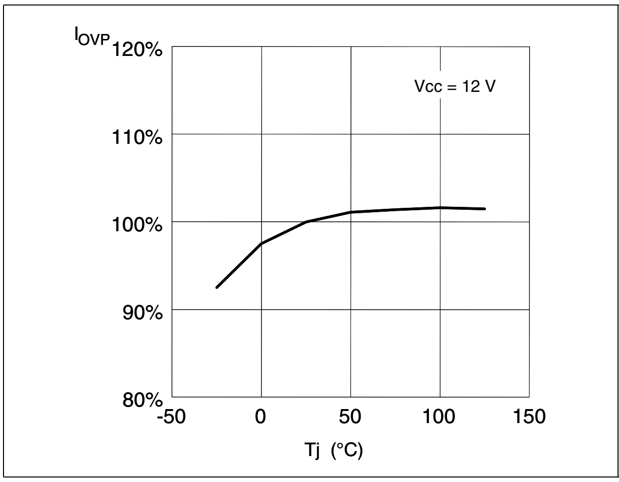


Figure 13. Current-sense offset vs mains voltage phase angle

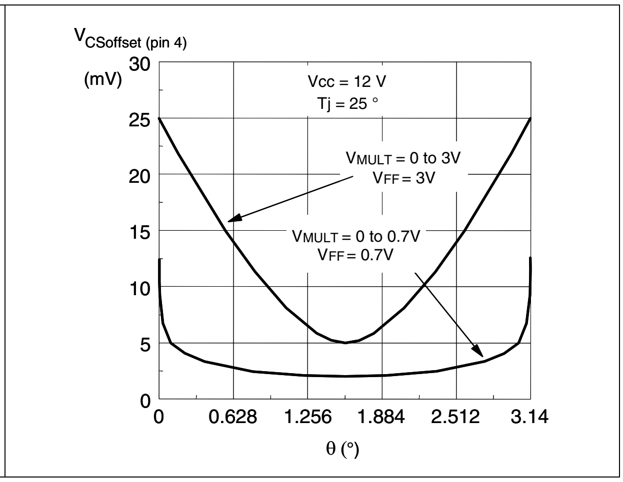


Figure 14. Delay-to-output vs T_J

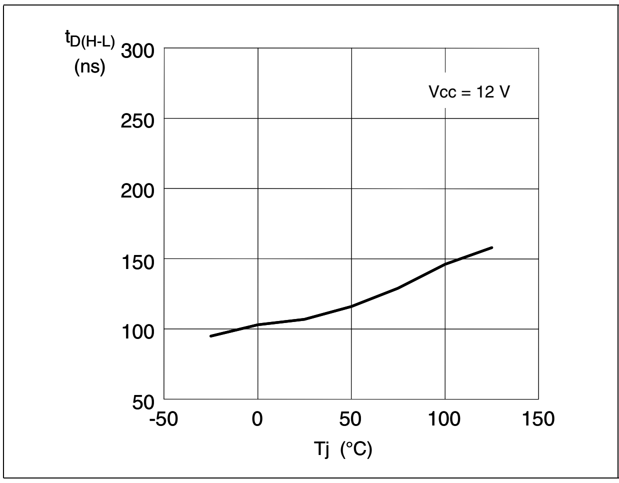


Figure 15. Ic latch-off level on current sense vs T_J (L6563 only)

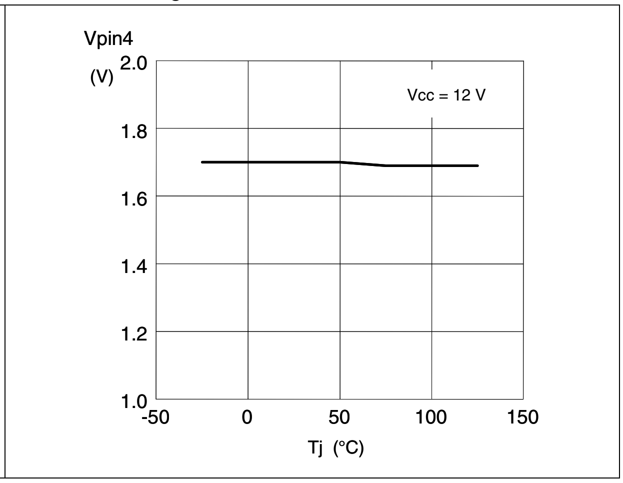


Figure 16. Multiplier characteristics @ V_{FF} = 1V

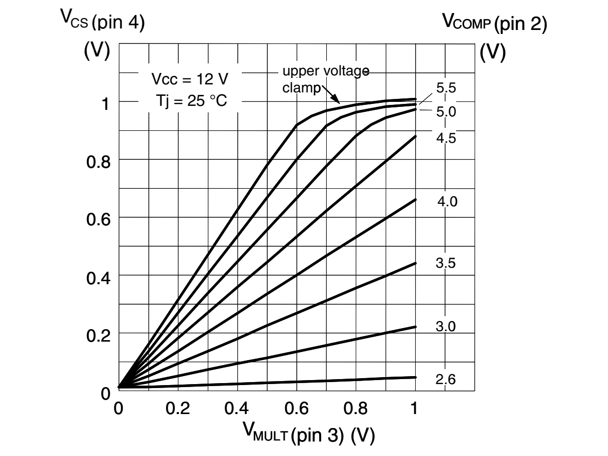


Figure 17. ZCD clamp levels vs T_J

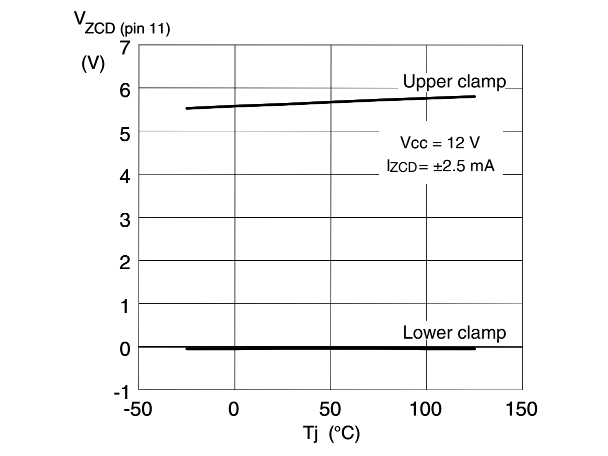


Figure 18. Multiplier characteristics @ V_{FF} = 3V

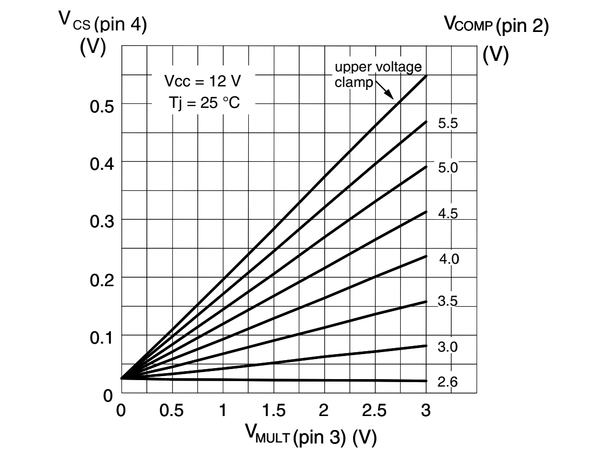


Figure 19. ZCD source capability vs T_J

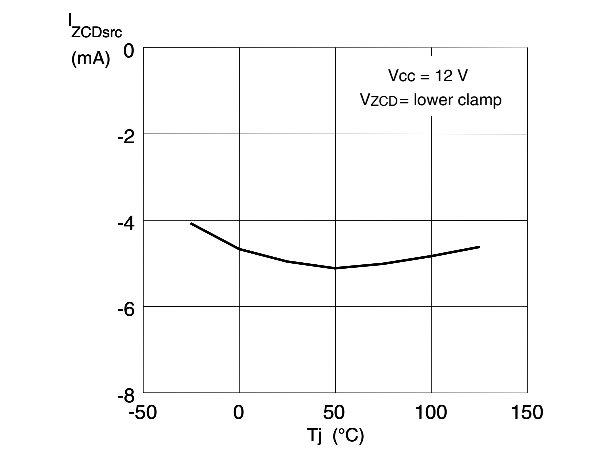


Figure 20. Multiplier gain vs T_J

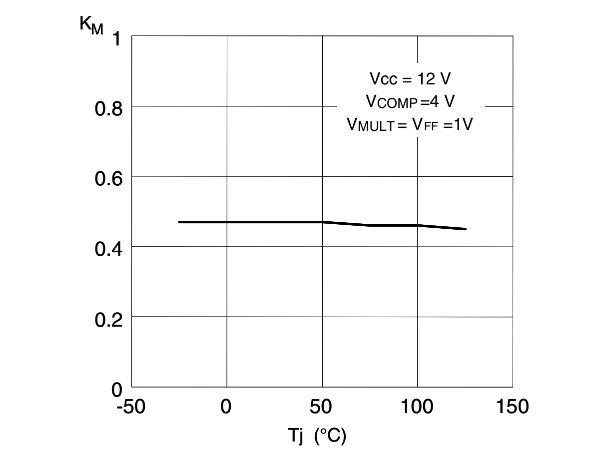


Figure 21. VFF & TBO dropouts vs T_J

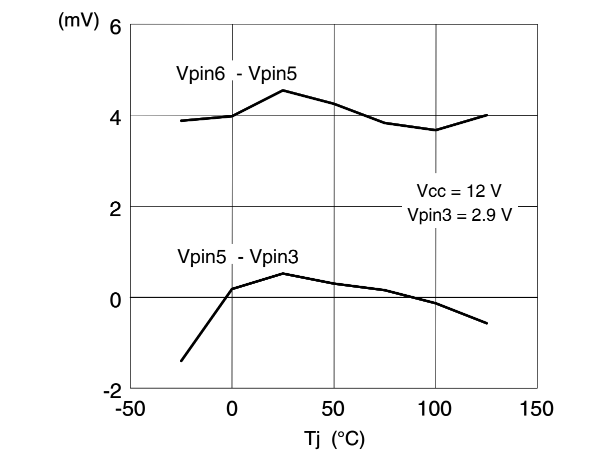


Figure 22. TBO current mismatch vs T_J

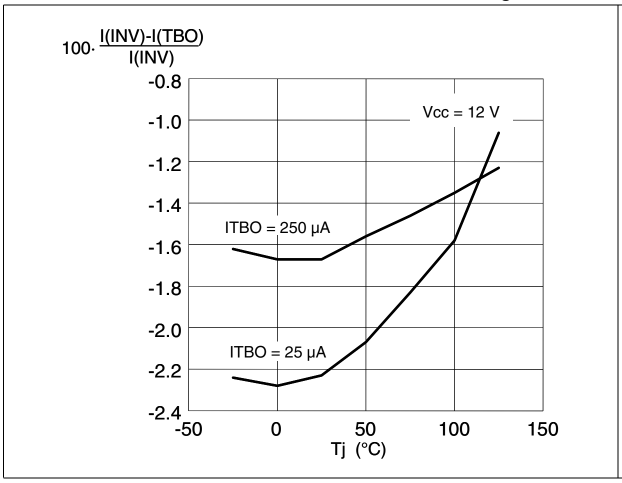


Figure 23. RUN thresholds vs T_J

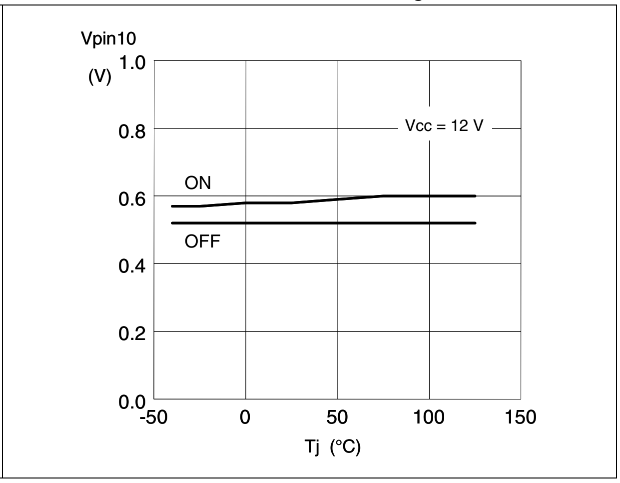


Figure 24. TBO-INV current mismatch vs TBO currents

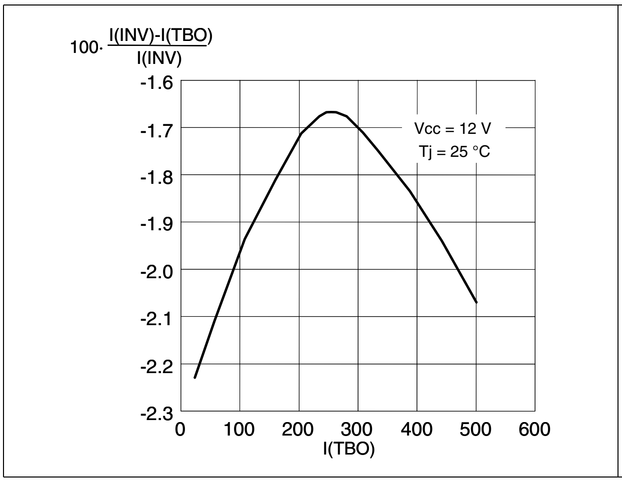


Figure 25. PWM_LATCH high saturation vs T_J

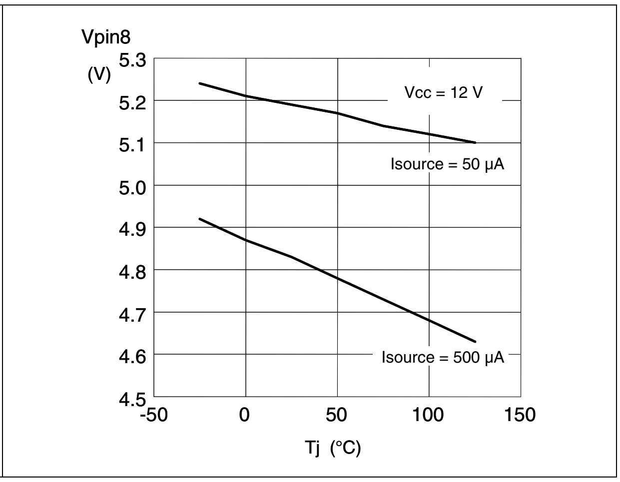


Figure 26. TBO clamp vs T_J

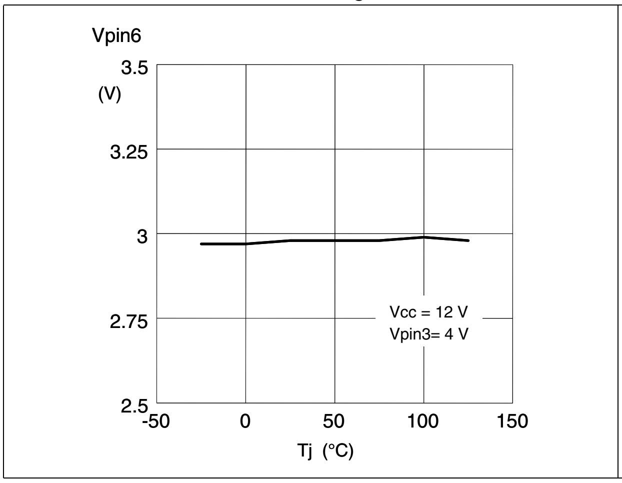


Figure 27. PWM_STOP low saturation vs T_J

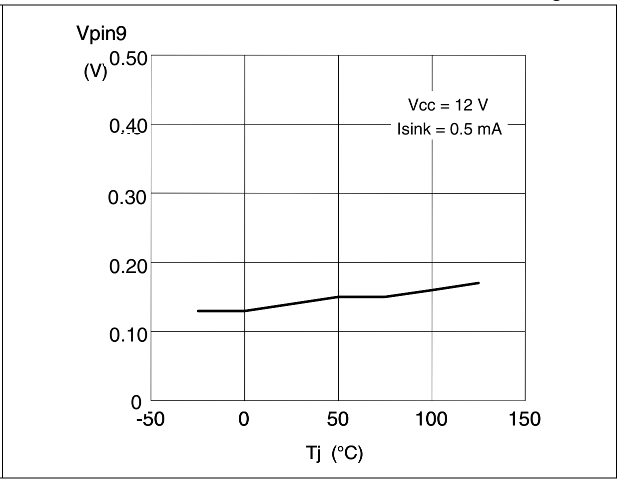


Figure 28. PFC_OK thresholds vs T_J

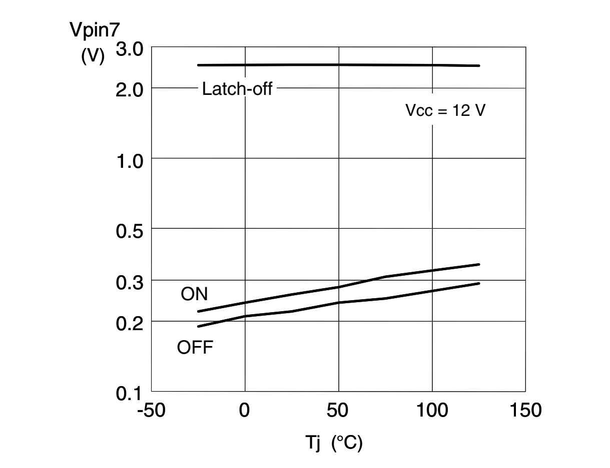


Figure 29. UVLO saturation vs T_J

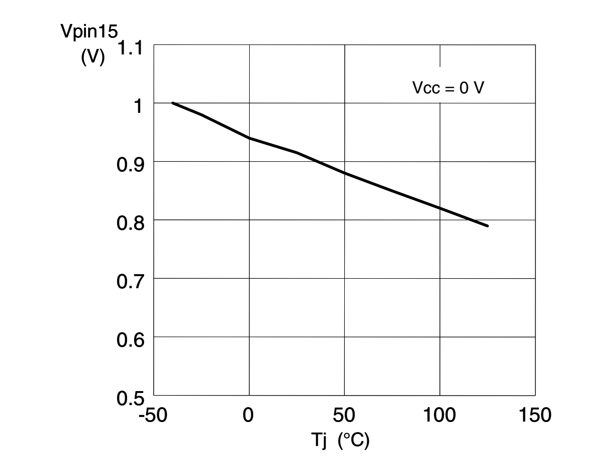


Figure 30. Start-up timer vs T_J

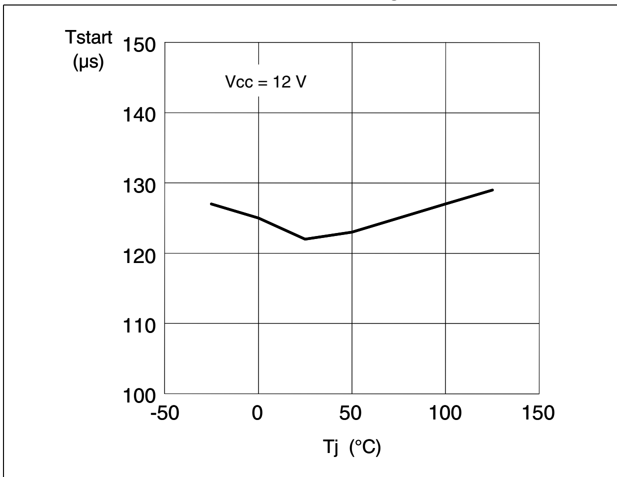


Figure 31. Gate-drive output low saturation

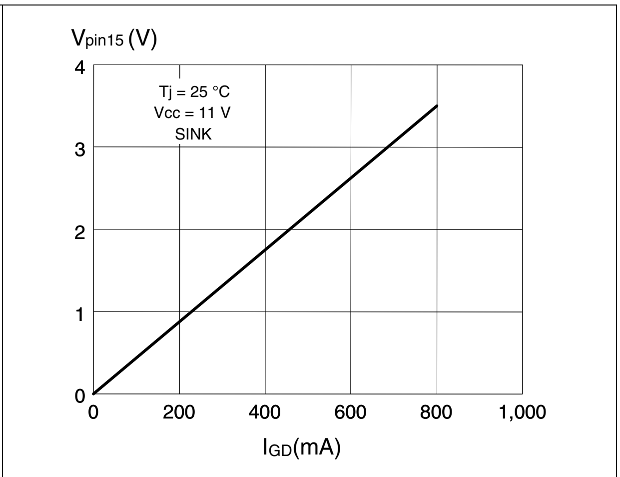


Figure 32. Gate-drive clamp vs T_J

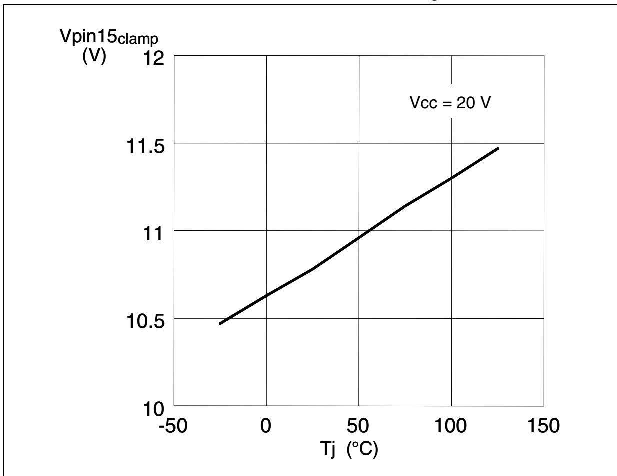
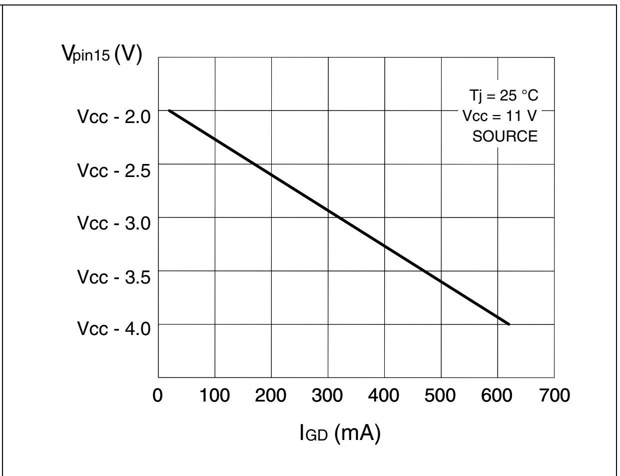


Figure 33. Gate-drive output high saturation



6 Application information

6.1 Overvoltage protection

Normally, the voltage control loop keeps the output voltage V_O of the PFC pre-regulator close to its nominal value, set by the ratio of the resistors R1 and R2 of the output divider. Neglecting the ripple components, under steady state conditions the current through R1 equals that through R2. Considering that the non-inverting input of the error amplifier is internally biased at 2.5V, the voltage at pin INV will be 2.5V as well, then:

Equation 1

$$I_{R2} = I_{R1} = \frac{2.5}{R2} = \frac{V_O - 2.5}{R1}$$

If the output voltage experiences an abrupt change ΔVo the voltage at pin INV is kept at 2.5V by the local feedback of the error amplifier, a network connected between pins INV and COMP that introduces a long time constant. Then the current through R2 remains equal to 2.5/R2 but that through R1 becomes:

Equation 2

$$I'_{R1} = \frac{V_O - 2.5 + \Delta V_O}{R1}$$

The difference current $\Delta I_{R1} = I'_{R1} - I'_{R1} = \Delta V_O/R1$ will flow through the compensation network and enter the error amplifier (pin COMP). This current is monitored inside the IC and when it reaches about 18 µA the output voltage of the multiplier is forced to decrease, thus reducing the energy drawn from the mains. If the current exceeds 20 µA, the OVP is triggered (Dynamic OVP), and the external power transistor is switched off until the current falls approximately below 5 µA. However, if the overvoltage persists (e.g. in case the load is completely disconnected), the error amplifier will eventually saturate low hence triggering an internal comparator (Static OVP) that will keep the external power switch turned off until the output voltage comes back close to the regulated value. The output overvoltage that is able to trigger the OVP function is then:

Equation 3

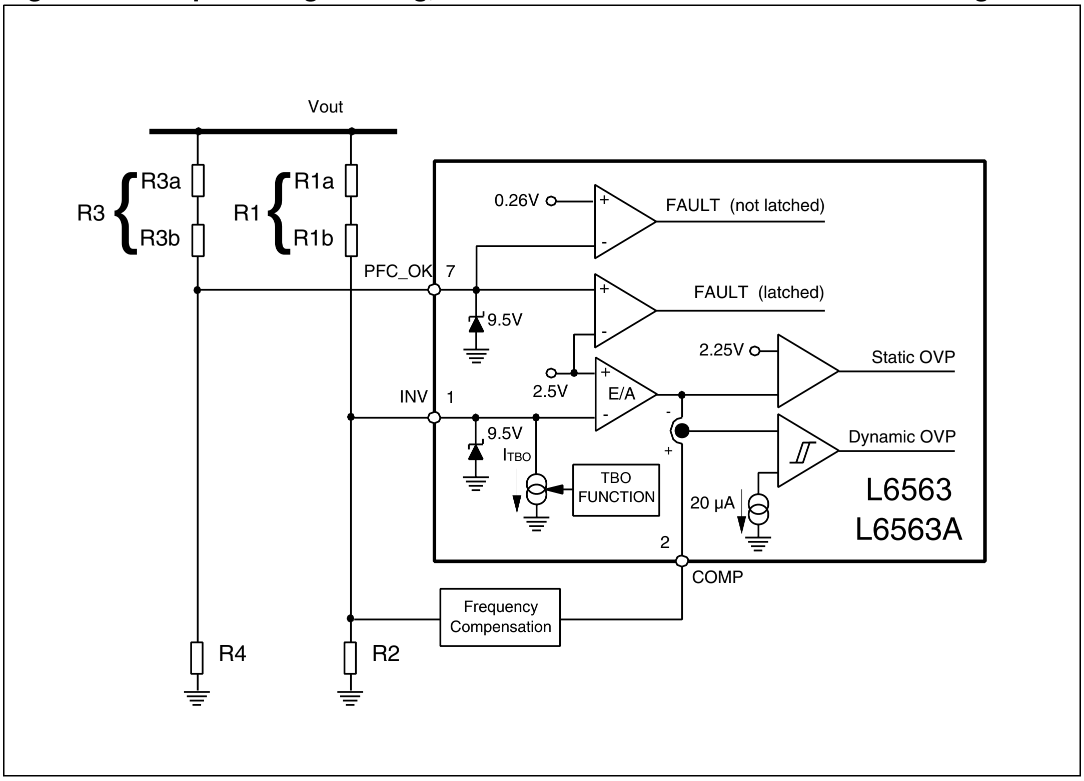
$$\Delta V_O = R1 \cdot 20 \cdot 10^{-6}$$

An important advantage of this technique is that the overvoltage level can be set independently of the regulated output voltage: the latter depends on the ratio of R1 to R2, the former on the individual value of R1. Another advantage is the precision: the tolerance of the detection current is 15%, which means 15% tolerance on the ΔV_O. Since it is usually much smaller than Vo, the tolerance on the absolute value will be proportionally reduced.

Example: V_O = 400V, ΔV_O = 40V.
Then: R1 = 40V/20µA = 2MΩ ; R2 = 2.5·2MΩ·/(400-2.5) = 12.58kΩ.
The tolerance on the OVP level due to the L6563/A will be 40·0.15 = 6 V, that is ± 1.36%.

When either OVP is activated the quiescent consumption is reduced to minimize the discharge of the Vcc capacitor.

Figure 34. Output voltage setting, OVP and FFP functions: internal block diagram



6.2 Feedback Failure Protection (FFP)

The OVP function above described is able to handle "normal" overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at start-up. It cannot handle the overvoltage generated, for instance, when the upper resistor of the output divider (R1) fails open: the voltage loop can no longer read the information on the output voltage and will force the PFC pre-regulator to work at maximum ON-time, causing the output voltage to rise with no control.

A pin of the device (PFC_OK) has been dedicated to provide an additional monitoring of the output voltage with a separate resistor divider (R3 high, R4 low, see *Figure 34*). This divider is selected so that the voltage at the pin reaches 2.5V if the output voltage exceeds a preset value, usually larger than the maximum Vo that can be expected, also including worst-case load/line transients.

Example: V_O = 400 V, Vox = 475V. Select: R3 = 3MΩ;
then: R4 = 3MΩ ·2.5/(475-2.5) = 15.87kΩ.

When this function is triggered, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 250 µA and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. At the same time the pin PWM_LATCH is asserted high. PWM_LATCH is an open source output able to deliver 3.7V min. with 0.5 mA load, intended for tripping a latched shutdown function of the PWM controller IC in the cascaded DC-DC converter, so that the entire unit is latched off. To restart the system it is necessary to recycle the input power, so that the Vcc voltages of both the L6563/A and the PWM controller go below their respective UVLO thresholds.

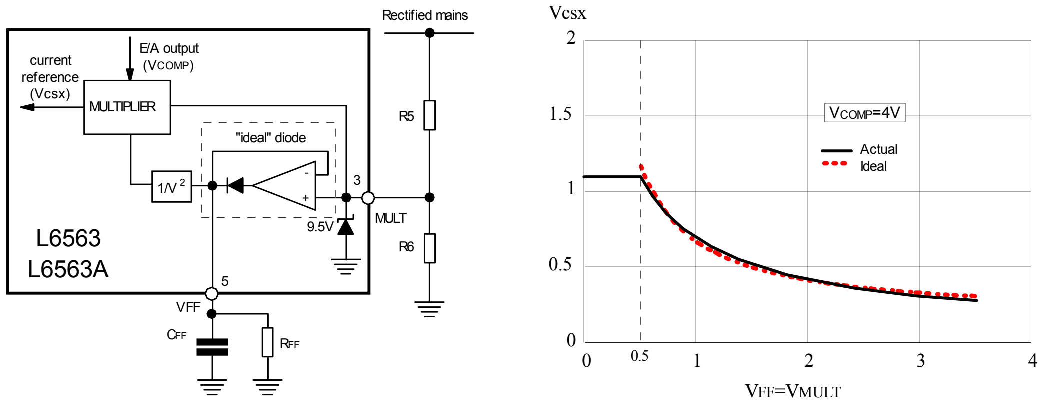
The PFC_OK pin doubles its function as a not-latched IC disable: a voltage below 0.2V will shut down the IC, reducing its consumption below 1 mA. In this case both PWM_STOP and PWM_LATCH keep their high impedance status. To restart the IC simply let the voltage at the pin go above 0.26 V.

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a PFC_OK pin floating will result in shutting down the IC and stopping the pre-regulator.

6.3 Voltage Feedforward

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. So does the crossover frequency f_c of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design.
For example, setting the gain of the error amplifier to get f_c = 20 Hz @ 264 Vac means having $f_c \cong$ 4 Hz @ 88 Vac, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.
Voltage Feedforward can compensate for the gain variation with the line voltage and allow overcoming all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (see *Figure 35*).

Figure 35. Voltage feedforward: squarer-divider ($1/V^2$) block diagram and transfer characteristic



In this way a change of the line voltage will cause an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier output will be halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain will be constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

Actually, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small the voltage generated will be affected by a considerable amount of ripple at twice the mains frequency that will cause distortion of the current reference (resulting in high THD and poor PF); if it is too large there will be a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off is required.

The device realizes Voltage Feedforward with a technique that makes use of just two external parts and that limits the feedforward time constant trade-off issue to only one direction. A capacitor C_{FF} and a resistor R_{FF} , both connected from the VFF (pin 5) pin to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (pin 3). R_{FF} provides a means to discharge C_{FF} when the line voltage decreases (see *Figure 35*). In this way, in case of sudden line voltage rise, C_{FF} will be rapidly charged through the low impedance of the internal diode and no appreciable overshoot will be visible at the pre-regulator's output; in case of line voltage drop C_{FF} will be discharged with the time constant $R_{FF} \cdot C_{FF}$, which can be in the hundred ms to achieve an acceptably low steady-state ripple and have low current distortion; consequently the output voltage can experience a considerable undershoot, like in systems with no feedforward compensation.

The twice-mains-frequency ($2 \cdot f_L$) ripple appearing across C_{FF} is triangular with a peak-to-peak amplitude that, with good approximation, is given by:

Equation 4

$$\Delta V_{FF} = \frac{2V_{MULTpk}}{1 + 4f_L R_{FF} C_{FF}}$$

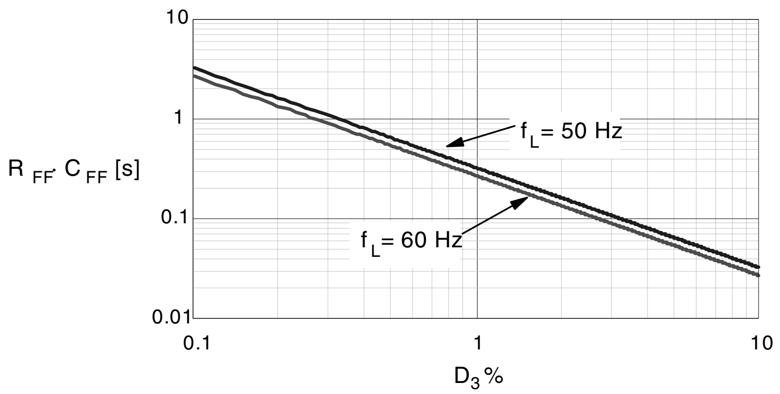
where f_L is the line frequency. The amount of 3rd harmonic distortion introduced by this ripple, related to the amplitude of its $2 \cdot f_L$ component, will be:

Equation 5

$$D_3\% = \frac{100}{2\pi f_L R_{FF} C_{FF}}$$

Figure 36 shows a diagram that helps choose the time constant $R_{FF} \cdot C_{FF}$ based on the amount of maximum desired 3rd harmonic distortion. Always connect R_{FF} and C_{FF} to the pin, the IC will not work properly if the pin is either left floating or connected directly to ground.

Figure 36. $R_{FF} \cdot C_{FF}$ as a function of 3rd harmonic distortion introduced in the input current



The dynamics of the voltage feedforward input is limited downwards at 0.5V (see *Figure 35*), that is the output of the multiplier will not increase any more if the voltage on the V_{FF} pin is below 0.5V. This helps to prevent excessive power flow when the line voltage is lower than the minimum specified value (brownout conditions).

6.4 THD optimizer circuit

The L6563/A is provided with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (Total Harmonic Distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge.

Figure 37 shows the internal block diagram of the THD optimizer circuit.

Figure 37. THD optimizer circuit

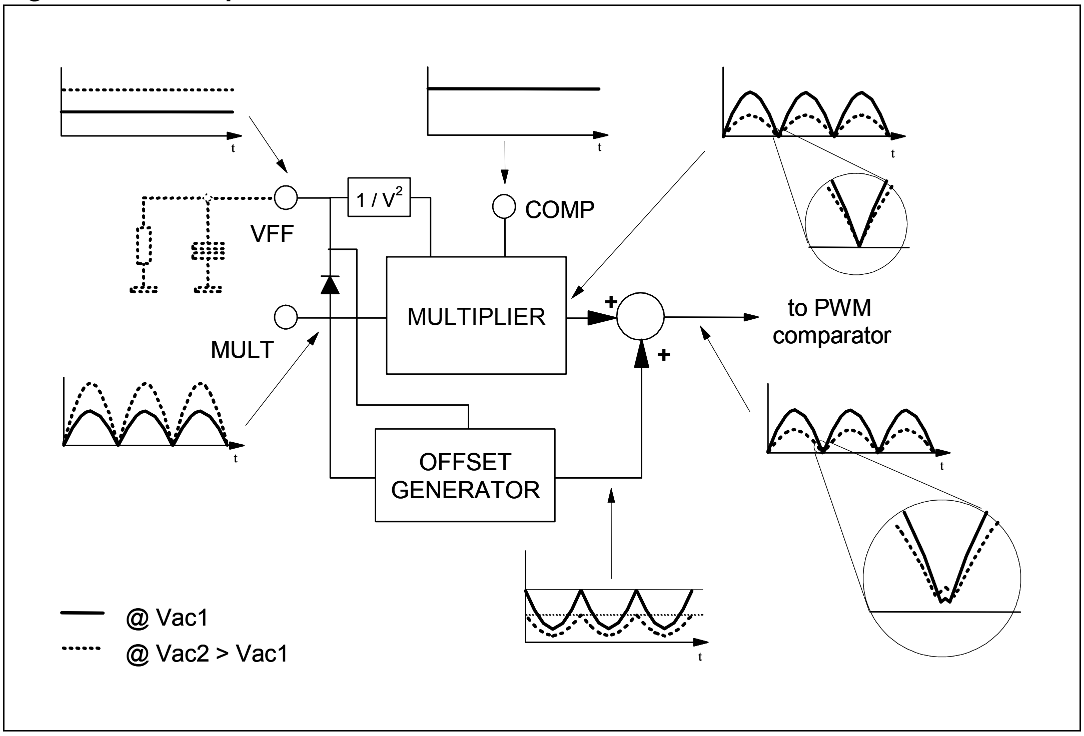
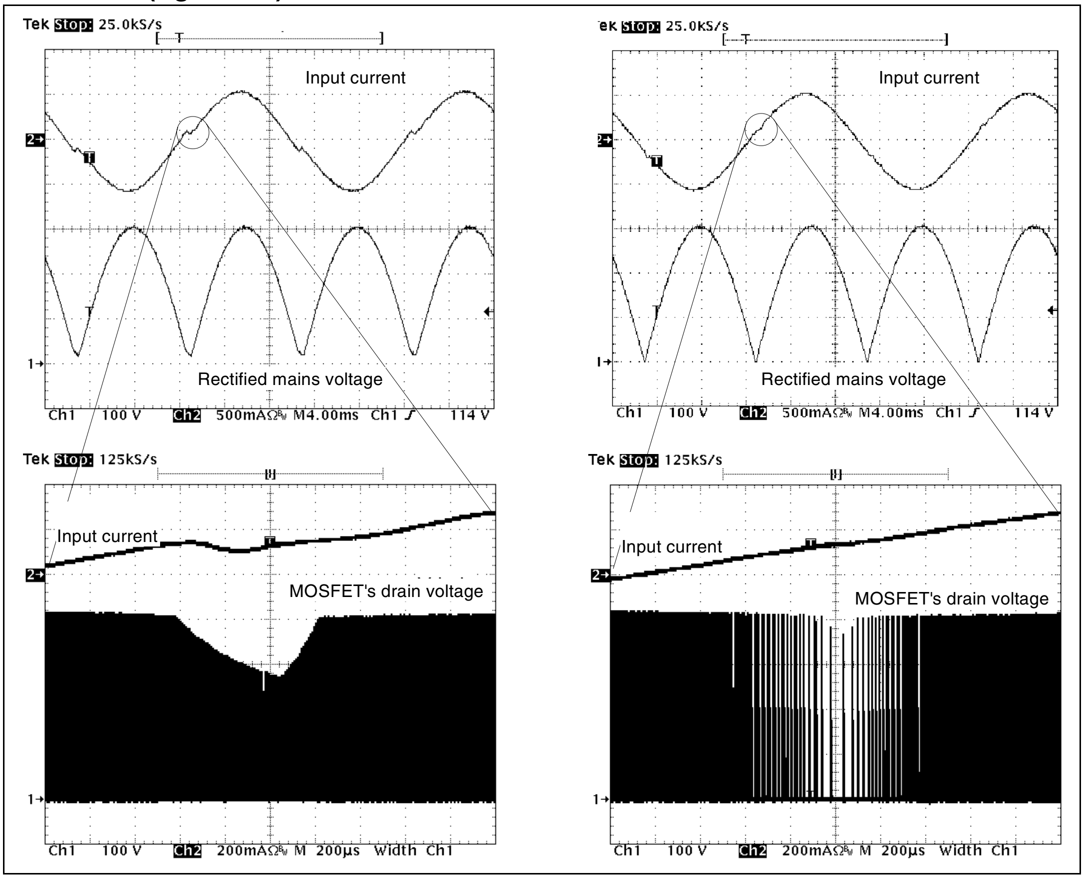


Figure 38. THD optimization: standard TM PFC controller (left side) and L6563/A (right side)



Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore the offset is modulated by the voltage on the V_{FF} pin (see *Section 6.3 on page 18* section) so as to have little offset at low line, where energy transfer at zero crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse.

The effect of the circuit is shown in *Figure 38*, where the key waveforms of a standard TM PFC controller are compared to those of this chip.

To take maximum benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus reducing the effectiveness of the optimizer circuit.

6.5 Tracking Boost function

In some applications it may be advantageous to regulate the output voltage of the PFC pre-regulator so that it tracks the RMS input voltage rather than at a fixed value like in conventional boost pre-regulators. This is commonly referred to as "tracking boost" or "follower boost" approach.

With this IC the function can be realized by connecting a resistor (R_T) between the TBO pin and ground. The TBO pin presents a DC level equal to the peak of the MULT pin voltage and is then representative of the mains RMS voltage. The resistor defines a current, equal to $V(TBO)/R_T$, that is internally 1:1 mirrored and sunk from pin INV (pin 1) input of the error amplifier. In this way, when the mains voltage increases the voltage at TBO pin will increase as well and so will do the current flowing through the resistor connected between TBO and GND. Then a larger current will be sunk by INV pin and the output voltage of the PFC pre-regulator will be forced to get higher. Obviously, the output voltage will move in the opposite direction if the input voltage decreases.

To avoid undesired output voltage rise should the mains voltage exceed the maximum specified value, the voltage at the TBO pin is clamped at 3V. By properly selecting the multiplier bias it is possible to set the maximum input voltage above which input-to-output tracking ends and the output voltage becomes constant. If this function is not used, leave the pin open: the device will regulate a fixed output voltage.

Starting from the following data:

- Vin_1 = minimum specified input RMS voltage;
- Vin_2 = maximum specified input RMS voltage;
- Vo_1 = regulated output voltage @ Vin = Vin_1;
- Vo_2 = regulated output voltage @ Vin = Vin_2;
- Vox = absolute maximum limit for the regulated output voltage;
- ΔVo = OVP threshold,

to set the output voltage at the desired values use the following design procedure:

1. Determine the input RMS voltage Vin_{clamp} that produces Vo = Vox:

Equation 6

$$Vin_{clamp} = \frac{Vox - Vo_1}{Vo_2 - Vo_1} \cdot Vin_2 - \frac{Vox - Vo_2}{Vo_2 - Vo_1} \cdot Vin_1$$

and choose a value Vin_x such that $Vin_2 = Vin_x < Vin_{clamp}$. This will result in a limitation of the output voltage range below Vox (it will equal Vox if one chooses $Vin_x = Vin_{clamp}$)

2. Determine the divider ratio of the MULT pin (pin 3) bias:

Equation 7

$$k = \frac{3}{\sqrt{2} \cdot Vin_x}$$

and check that at minimum mains voltage Vin_1 the peak voltage on pin 3 is greater than 0.65V.

3. Determine R1, the upper resistor of the output divider:

Equation 8

$$R1 = \frac{\Delta Vo}{20} \cdot 10^6$$

4. Calculate the lower resistor R_2 of the output divider and the adjustment resistor R_T:

Equation 9

$$R2 = 2.5 \cdot R1 \cdot \frac{Vin_2 - Vin_1}{(Vo_1 - 2.5) \cdot Vin_2 - (Vo_2 - 2.5) \cdot Vin_1}$$

$$R_T = \sqrt{2} \cdot k \cdot R1 \cdot \frac{Vin_2 - Vin_1}{Vo_2 - Vo_1}$$

5. Check that the maximum current sourced by the TBO pin (pin 6) does not exceed the maximum specified (0.25mA):

Equation 10

$$I_{TBOmax} = \frac{3}{R_T} \leq 0.25 \cdot 10^{-3}$$

In the following Mathcad® sheet, as an example, the calculation is shown for the circuit illustrated in *Figure 40. Figure 41* shows the internal block diagram of the tracking boost function.

Design data

$Vin_1 := 88V$ $Vo_1 := 200V$

$Vin_2 := 264V$ $Vo_2 := 385V$

$Vox := 400V$

$\Delta Vo := 40V$

Step 1

$$Vin_{clamp} := \frac{Vox - Vo_1}{Vo_2 - Vo_1} \cdot Vin_2 - \frac{Vox - Vo_2}{Vo_2 - Vo_1} \cdot Vin_1 \qquad Vin_{clamp} = 278.27V$$

choose: $Vin_x := 270V$

Step 2

$$k := \frac{3}{\sqrt{2} \cdot Vin_x} \qquad k = 7.857 \times 10^{-3}$$

Step 3

$$R1 := \frac{\Delta Vo}{20} \cdot 10^6 \qquad R1 = 2 \times 10^6\ \Omega$$