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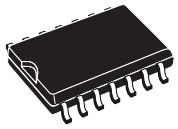
L6563S

Enhanced transition-mode PFC controller

Features

- Tracking boost function
- Fast “bidirectional” input voltage feedforward ($1/V^2$ correction)
- Interface for cascaded converter's PWM controller
- Remote ON/OFF control
- Accurate adjustable output overvoltage protection
- Protection against feedback loop disconnection (latched shutdown)
- Inductor saturation protection
- Low (≤ 100 µA) start-up current
- 6 mA max. operating bias current
- 1% (@ T_J = 25 °C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SO14 package



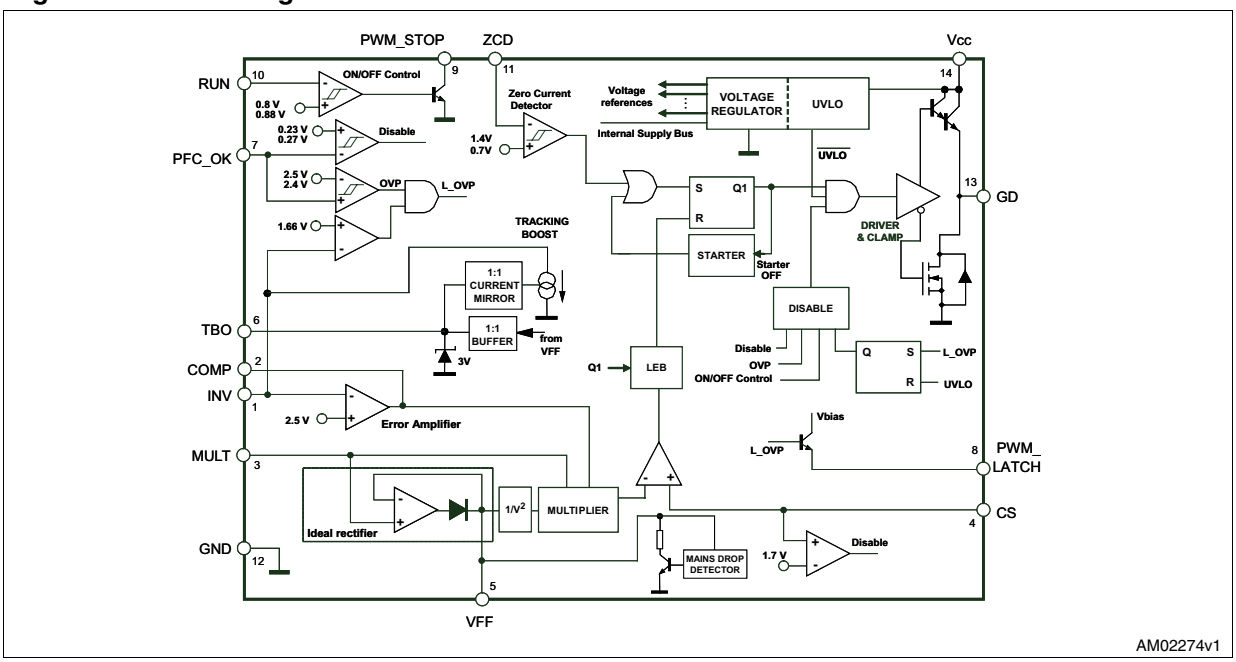
SO14

Applications

PFC pre-regulators for:

- High-end AC-DC adapter/charger
- Desktop PC, server, Web server
- IEC61000-3-2 or JEITA-MITI compliant SMPS, in excess of 400 W

Figure 1. Block diagram



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1 Description

The L6563S is a current-mode PFC controller operating in transition mode (TM). Coming with the same pin-out as its predecessor L6563, it offers improved performance and additional functions.

The highly linear multiplier, along with a special correction circuit that reduces crossover distortion of the mains current, allows wide-range-mains operation with an extremely low THD even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% @ T_J = 25 °C) internal voltage reference. Loop's stability is optimized by the voltage feedforward function ($1/V^2$ correction), which in this IC uses a proprietary technique that considerably improves line transient response as well in case of mains both drops and surges ("bidirectional").

Additionally, the IC provides the option for tracking boost operation, i.e. the output voltage is changed tracking the mains voltage.

The device includes disable functions suitable for remote ON/OFF control both in systems where the PFC pre-regulator works as a master and in those where it works as a slave. In addition to an overvoltage protection able to keep the output voltage under control during transient conditions, the IC is provided also with a protection against feedback loop failures or erroneous settings. Other on-board protection functions allow that brownout conditions and boost inductor saturation can be safely handled.

An interface with the PWM controller of the DC-DC converter supplied by the PFC pre-regulator is provided: the purpose is to stop the operation of the converter in case of anomalous conditions for the PFC stage (feedback loop failure, boost inductor's core saturation, etc.) and to disable the PFC stage in case of light load for the DC-DC converter, so as to make it easier to comply with energy saving norms (Blue Angel, EnergyStar, Energy2000, etc.).

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable for big MOSFET or IGBT drive. This, combined with the other features and the possibility to operate with ST's proprietary Fixed-Off-Time control, makes the device an excellent solution for SMPS up to 400 W that need to be compliant with EN61000-3-2 and JEITA-MITI standards.

2 Maximum ratings

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
Vcc	14	IC supply voltage (Icc = 20 mA)	self-limited	V
---	1, 3, 7	Max. pin voltage (I_{pin} =1 mA)	Self-limited	V
---	2, 4 to 6, 8, 10	Analog inputs and outputs	-0.3 to 8	V
V_{PWM_STOP}	9	Analog output	-0.3 to Vcc	V
I_{PWM_STOP}	9	Max. sink current	3	mA
I_{ZCD}	11	Zero current detector max. current	-10 (source) 10 (sink)	mA
VFF pin	5	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002 “human body model” Acceptance criteria: “normal performance”	+/- 1250	V
Other pins	1 to 4 6 to 14		+/- 2000	V

2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Max. thermal resistance, junction-to-ambient	120	°C/W
Ptot	Power dissipation @T_A = 50 °C	0.75	W
T_J	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

3 Pin connection

Figure 2. Pin connection

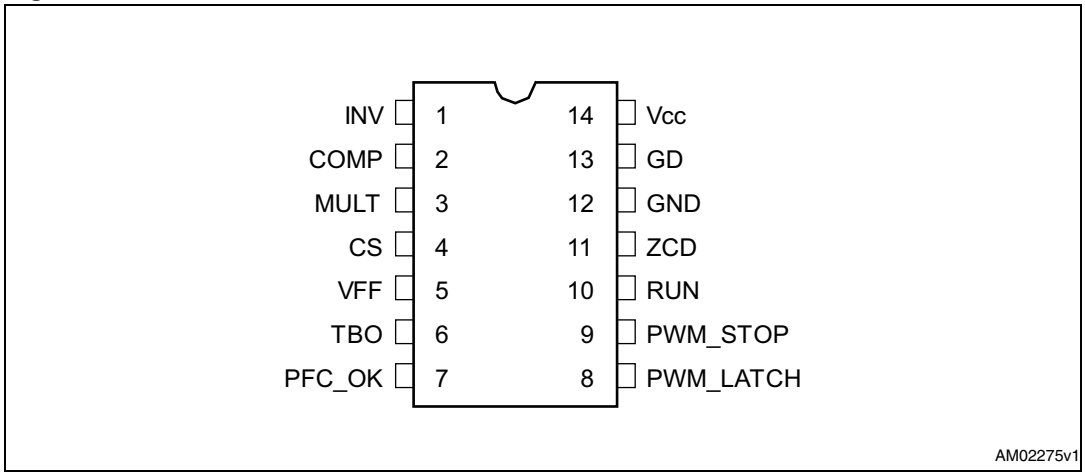


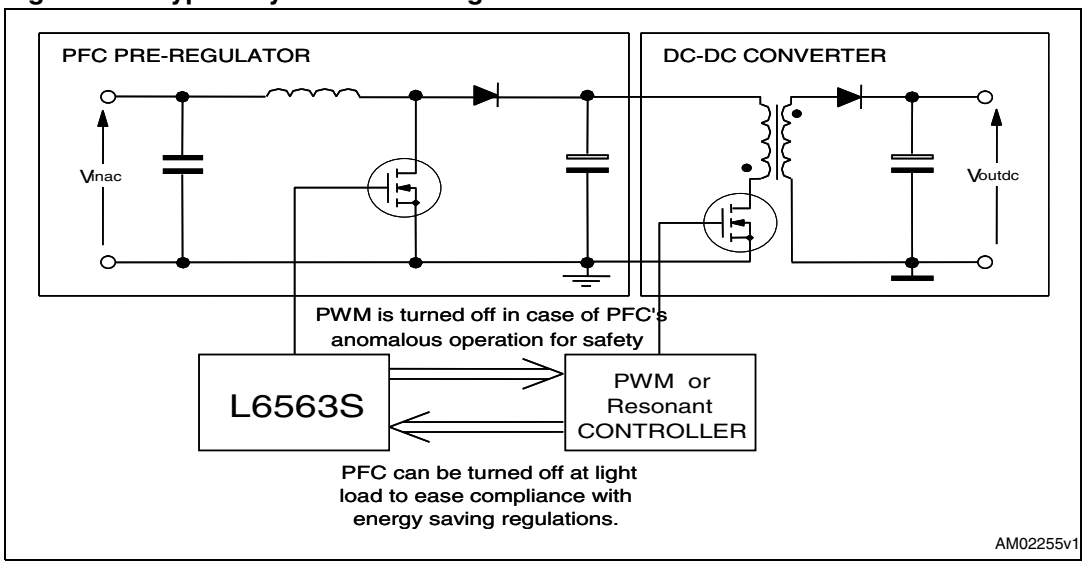
Table 3. Pin description

n°	Name	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. The pin normally features high impedance but, if the tracking boost function is used, an internal current generator programmed by TBO (pin 6) is activated. It sinks current from the pin to change the output voltage so that it tracks the mains voltage.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin 1) to achieve stability of the voltage control loop and ensure high power factor and low THD. To avoid uncontrolled rise of the output voltage at zero load, when the voltage on the pin falls below 2.4 V the gate driver output will be inhibited (burst-mode operation).
3	MULT	Mains input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop. The voltage on this pin is used also to derive the information on the RMS mains voltage.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET's turn-off. A second comparison level at 1.7 V detects abnormal currents (e.g. due to boost inductor saturation) and, on this occurrence, activates a safety procedure that temporarily stops the converter and limits the stress of the power components.
5	VFF	Second input to the multiplier for $1/V^2$ function. A capacitor and a parallel resistor must be connected from the pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage at this pin, a dc level equal to the peak voltage on pin MULT (3), compensates the control loop gain dependence on the mains voltage. Never connect the pin directly to GND but with a resistor ranging from 100 kΩ (minimum) to 2 MΩ (maximum).
6	TBO	Tracking boost function. This pin provides a buffered VFF voltage. A resistor connected between this pin and GND defines a current that is sunk from pin INV (#1). In this way, the output voltage is changed proportionally to the mains voltage (tracking boost). If this function is not used leave this pin open.

Table 3. Pin description (continued)

n°	Name	Function
7	PFC_OK	PFC pre-regulator output voltage monitoring/disable function. This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage on the pin exceeds 2.5 V the IC stops switching and restarts as the voltage on the pin falls below 2.4 V. However, if at the same time the voltage of the INV pin falls below 1.66V, a feedback failure is assumed. In this case the device is latched off and the pin PWM_LATCH (#8) is asserted high. Normal operation can be resumed only by cycling Vcc bringing its value lower than 6V before to move up the Turn on threshold. If the voltage on this pin is brought below 0.23 V the IC is shut down. To restart the IC the voltage on the pin must go above 0.27 V. This can be used as a remote on/off control input.
8	PWM_LATCH	Output pin for fault signaling. During normal operation this pin features high impedance. If a feedback failure is detected (PFC_OK > 2.5 V and INV< 1.66V) the pin is asserted high. Normally, this pin is used to stop the operation of the dc-dc converter supplied by the PFC pre-regulator by invoking a latched disable of its PWM controller. If not used, the pin will be left floating.
9	PWM_STOP	Output pin for fault signaling. During normal operation this pin features high impedance. If the IC is disabled by a voltage below 0.8 V on pin RUN (#10) the voltage on the pin is pulled to ground. Normally, this pin is used to temporarily stop the operation of the dc-dc converter supplied by the PFC pre-regulator by disabling its PWM controller. A typical usage of this function is brownout protection in systems where the PFC pre-regulator is the master stage. If not used, the pin will be left floating.
10	RUN	Remote ON/OFF control. A voltage below 0.8V shuts down (not latched) the IC and brings its consumption to a considerably lower level. PWM_STOP is asserted low. The IC restarts as the voltage at the pin goes above 0.88 V. Connect this pin to pin VFF (#5) either directly or through a resistor divider to use this function as brownout (AC mains undervoltage) protection.
11	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
12	GND	Ground. Current return for both the signal part of the IC and the gate driver.
13	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages.
14	Vcc	Supply voltage of both the signal part of the IC and the gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.

Figure 3. Typical system block diagram



4 Electrical characteristics

T_J = -25 to 125 °C, V_{CC} = 12 V, C_O = 1 nF between pin GD and GND, C_{FF} = 1 µF and R_{FF} = 1 MΩ between pin VFF and GND; unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
Vcc	Operating range	After turn-on	10.3		22.5	V
Vcc_{On}	Turn-on threshold	(1)	11	12	13	V
Vcc_{Off}	Turn-off threshold	(1)	8.7	9.5	10.3	V
$Vcc_{restart}$	Vcc for resuming from latch	OVP latched	5	6	7	V
Hys	Hysteresis		2.3		2.7	V
V_Z	Zener voltage	Icc = 20 mA	22.5	25	28	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, Vcc = 10 V		90	150	µA
I_q	Quiescent current	After turn-on, V_{MULT} = 1 V		4	5	mA
I_{CC}	Operating supply current	@ 70 kHz		5	6.0	mA
I_{qdis}	Idle state quiescent current	$V_{PFC_OK} > V_{PFC_OK_S}$ AND $V_{INV} < V_{PFC_OK} - V_{FFD}$		180	280	µA
		$V_{PFC_OK} < V_{PFC_OK_D}$ OR $V_{RUN} < V_{DIS}$		1.5	2.2	mA
I_q	Quiescent current	$V_{PFC_OK} > V_{PFC_OK_S}$ OR $V_{COMP} < 2.3$ V		2.2	3	mA
Multiplier input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 3 V		-0.2	-1	µA
V_{MULT}	Linear operation range		0 to 3			V
V_{CLAMP}	Internal clamp level	I_{MULT} = 1 mA	9	9.5		V
$\frac{\Delta Vcs}{\Delta V_{MULT}}$	Output max. slope	V_{MULT} =0 to 0.4 V, V_{VFF} = 0.8 V V_{COMP} = Upper clamp	2.2	2.34		V/V
K_M	Gain (2)	V_{MULT} = 1 V, V_{COMP} = 4 V	0.375	0.45	0.525	1/V
Error amplifier						
V_{INV}	Voltage feedback input threshold	T_J = 25 °C	2.475	2.5	2.525	V
		10.3 V < Vcc < 22.5 V (3)	2.455		2.545	
	Line regulation	Vcc = 10.3 V to 22.5 V		2	5	mV
I_{INV}	Input bias current	TBO open, V_{INV} = 0 to 4 V		-0.2	-1	µA
$V_{INVCLAMP}$	Internal clamp level	I_{INV} = 1 mA	8	9		V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Gv	Voltage gain	Open loop	60	80		dB
GB	Gain-bandwidth product			1		MHz
I_{COMP}	Source current	V_{COMP} = 4 V, V_{INV} = 2.4 V	2	4		mA
	Sink current	V_{COMP} = 4 V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5 mA	5.7	6.2	6.7	V
	Burst-mode voltage	(3)	2.3	2.4	2.5	
	Lower clamp voltage	I_{SINK} = 0.5 mA (3)	2.1	2.25	2.4	
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			1	µA
t_{LEB}	Leading edge blanking		100	150	250	ns
$td_{(H-L)}$	Delay to output		100	200	300	ns
$V_{CSclamp}$	Current sense reference clamp	V_{COMP} = Upper clamp, V_{MULT} =1 V V_{VFF} = 1 V	1.0	1.08	1.16	V
Vcs_{ofst}	Current sense offset	V_{MULT} = 0, V_{VFF} = 3 V		40	70	mV
		V_{MULT} = 3 V, V_{VFF} = 3 V		20		
Boost inductor saturation detector						
V_{CS_th}	Threshold on current sense	(3)	1.6	1.7	1.8	V
I_{INV}	E/A input pull-up current	After V_{CS} > V_{CS_th}, before restarting	5	10	13	µA
PFC_OK functions						
I_{PFC_OK}	Input bias current	V_{PFC_OK} = 0 to 2.6 V		-0.1	-1	µA
$V_{PFC_OK_C}$	Clamp voltage	I_{PFC_OK} = 1 mA	9	9.5		V
$V_{PFC_OK_S}$	OVP threshold	(1) voltage rising	2.435	2.5	2.565	V
$V_{PFC_OK_R}$	Restart threshold after OVP	(1) voltage falling	2.34	2.4	2.46	V
$V_{PFC_OK_D}$	Disable threshold	(1) voltage falling	0.12		0.35	V
$V_{PFC_OK_D}$	Disable threshold	(1) voltage falling T_J = 25 °C	0.17	0.23	0.29	V
$V_{PFC_OK_E}$	Enable threshold	(1) voltage rising	0.15		0.38	V
$V_{PFC_OK_E}$	Enable threshold	(1) voltage rising Tj = 25 °C	0.21	0.27	0.32	V
V_{FFD}	Feedback failure detection threshold (V_{INV} falling)	V_{PFC_OK} > $V_{PFC_OK_S}$	1.61	1.66	1.71	mV
Zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	5.0	5.7		V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 2.5 mA	-0.3	0	0.3	V
V_{ZCDA}	Arming voltage (positive-going edge)		1.1	1.4	1.9	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ZCDT}	Triggering voltage (negative-going edge)		0.5	0.7	0.9	V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 4.5 V			1	µA
I_{ZCDsrc}	Source current capability		-2.5	-4		mA
I_{ZCDsnk}	Sink current capability		2.5	5		mA
Tracking boost function						
ΔV	Dropout voltage V_{VFF}-V_{TBO}	I_{TBO} = 0.2 mA	-20		20	mV
I_{TBO}	Linear operation		0		0.2	mA
	I_{INV}-I_{TBO} current mismatch	I_{TBO} = 25 µA to 0.2mA	-5.5		+1.0	%
	I_{INV}-I_{TBO} current mismatch	I_{TBO} = 25 µA to 0.2mA T_J = 25 °C	-4.0		+0	%
$V_{TBOclamp}$	Clamp voltage	(3) V_{VFF} = 4 V	2.9	3	3.1	V
I_{TBO_Pull}	Pull-up current	V_{TBO} = 1 V V_{FF} = V_{MULT} = 0 V			2	µA
PWM_STOP						
Ileak	High level leakage current	V_{PWM_STOP} = Vcc			1	µA
V_L	Low level	I_{PWM_STOP} = 0.5 mA			1	V
RUN function						
I_{RUN}	Input bias current	V_{RUN} = 0 to 3 V			-1	µA
V_{DIS}	Disable threshold	(3) voltage falling	0.745	0.8	0.855	V
V_{EN}	Enable threshold	(3) voltage rising	0.845	0.88	0.915	V
Start-up timer						
t_{START_DEL}	Start-up delay	First cycle after wake-up	25	50	75	µs
t_{START}	Timer period		75	150	300	µs
		Restart after V_{CS} > V_{CS_th}	150	300	600	
Voltage feedforward						
V_{VFF}	Linear operation range		0.8		3	V
ΔV	Dropout V_{MULTpk}-V_{VFF}	Vcc < Vcc_{On}			800	mV
		Vcc > or = to Vcc_{On}			20	
ΔV_{VFF}	Line drop detection threshold	Below peak value	40	70	100	mV
ΔV_{VFF}	Line drop detection threshold	Below peak value T_J = 25 °C	50	70	90	mV
R_{DISCH}	Internal discharge resistor	T_J = 25 °C	7.5	10	12.5	kΩ
			5		20	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{VFF}	Linear operation range		0.8		3	V
PWM_LATCH						
Ileak	Low level leakage current	V_{PWM_LATCH} = 0			-1	µA
V_H	High level	I_{PWM_LATCH} = -0.5 mA	4.5			V
V_H	High level	I_{PWM_LATCH} = -0.25 mA Vcc = Vcc_{Off}	2.5			V
V_H	High level	I_{PWM_LATCH} = -0.25 mA Vcc = Vcc_{Off} T_J = 25 °C	2.8			V
Gate driver						
V_{OL}	Output low voltage	I_{sink} = 100 mA		0.6	1.2	V
V_{OH}	Output high voltage	I_{source} = 5 mA	9.8	10.3		V
I_{srcpk}	Peak source current		-0.6			A
I_{snkpk}	Peak sink current		0.8			A
t_f	Voltage fall time			30	60	ns
t_r	Voltage rise time			45	110	ns
V_{Oclamp}	Output clamp voltage	I_{source} = 5 mA; Vcc = 20 V	10	12	15	V
	UVLO saturation	Vcc= 0 to V_{CCon}, I_{sink} = 2 mA			1.1	V

1. Parameters tracking each other
2. The multiplier output is given by:

$$V_{CS} = V_{CS_Ofst} + K_M \cdot \frac{V_{MULT} \cdot (V_{COMP} - 2.5)}{V_{VFF}^2}$$

3. Parameters tracking each other

5 Typical electrical performance

Figure 4. IC consumption vs V_{CC}

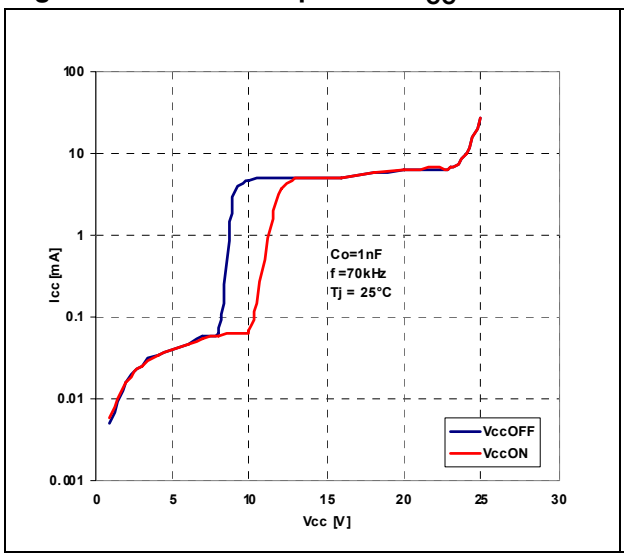


Figure 5. IC consumption vs T_J

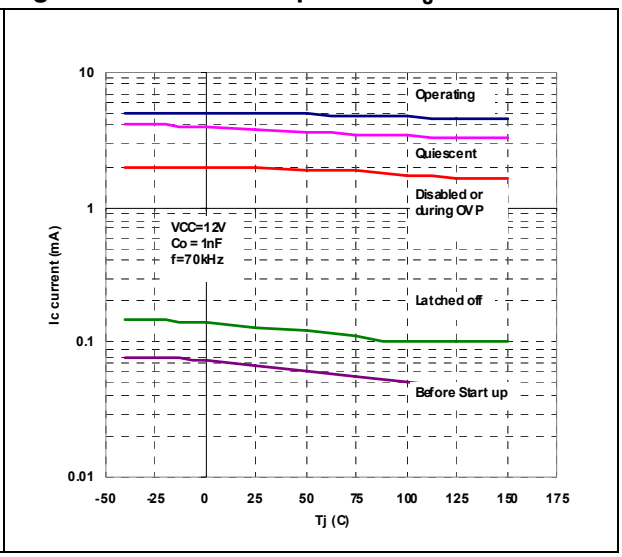


Figure 6. Vcc Zener voltage vs T_J

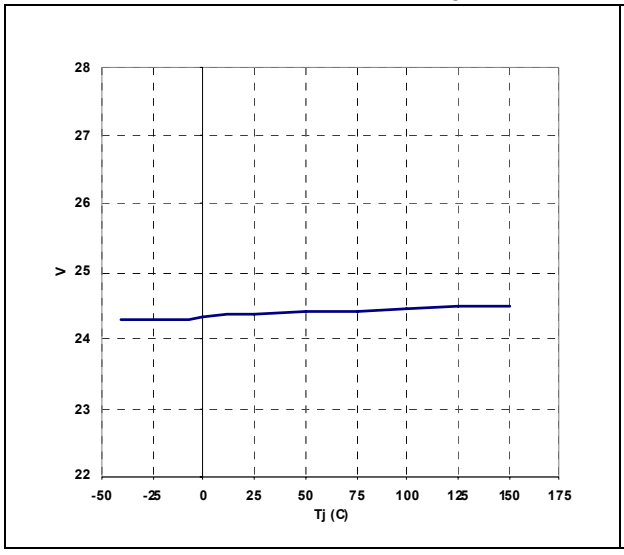


Figure 7. Start-up and UVLO vs T_J

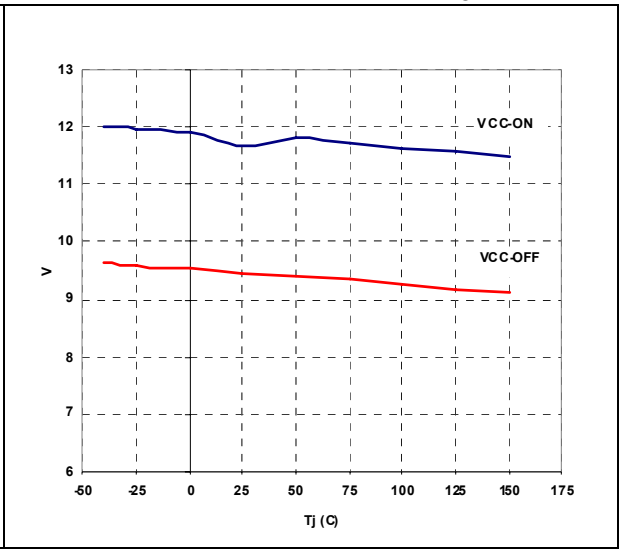


Figure 8. Feedback reference vs T_J

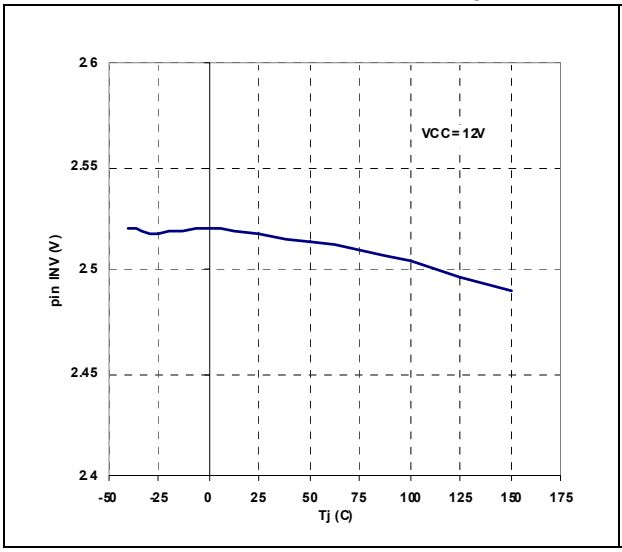


Figure 9. E/A output clamp levels vs T_J

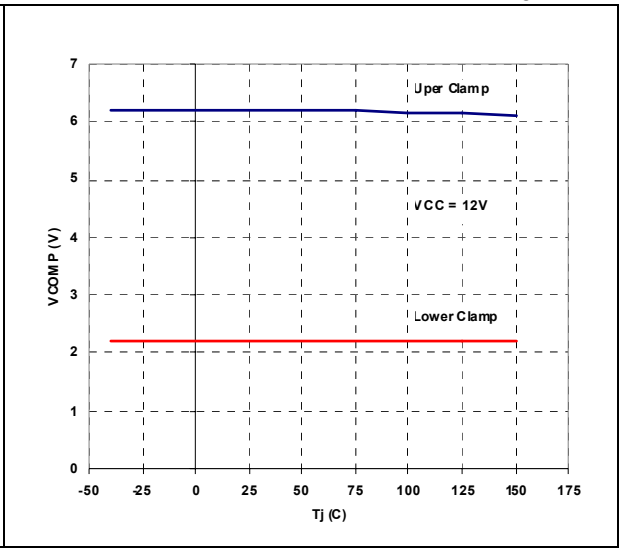


Figure 10. UVLO saturation vs T_J

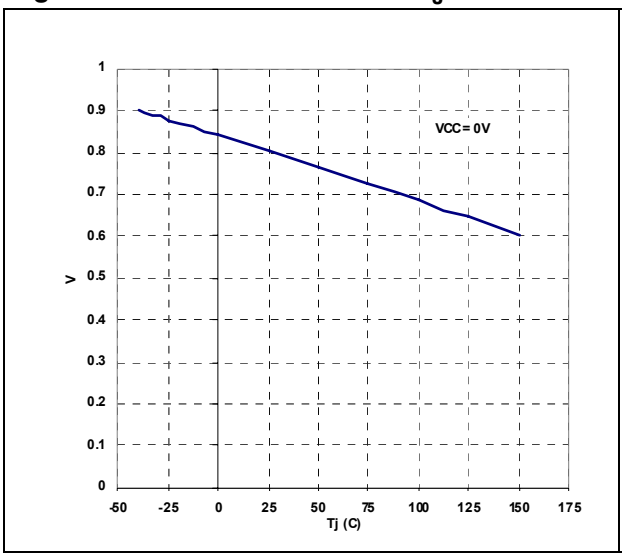


Figure 11. OVP levels vs T_J

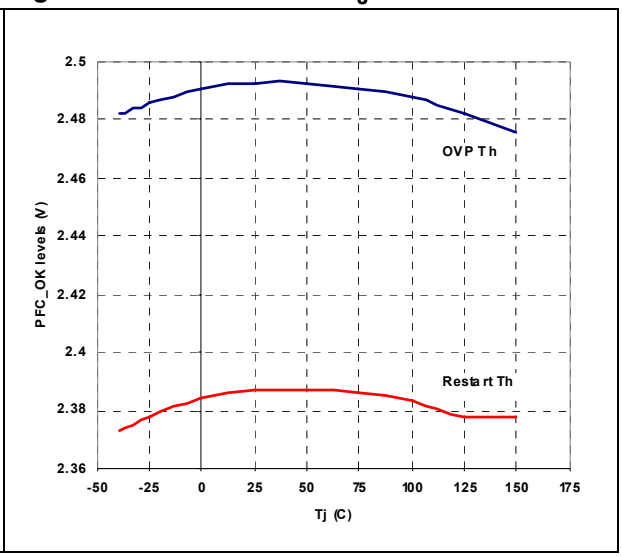


Figure 12. Inductor saturation threshold vs T_J

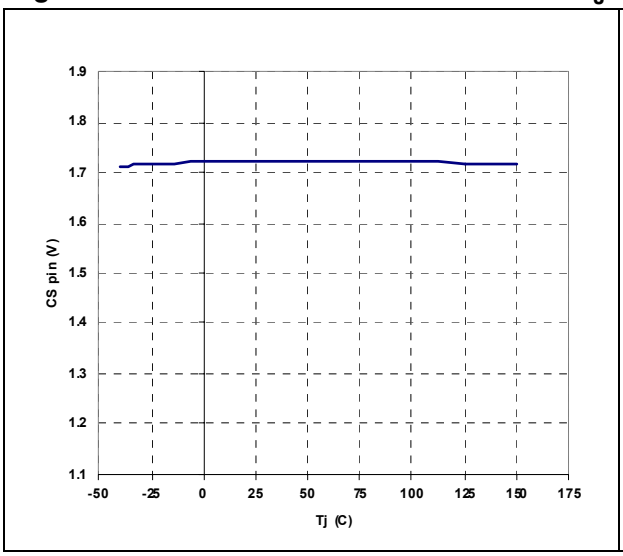


Figure 13. Vcs clamp vs T_J

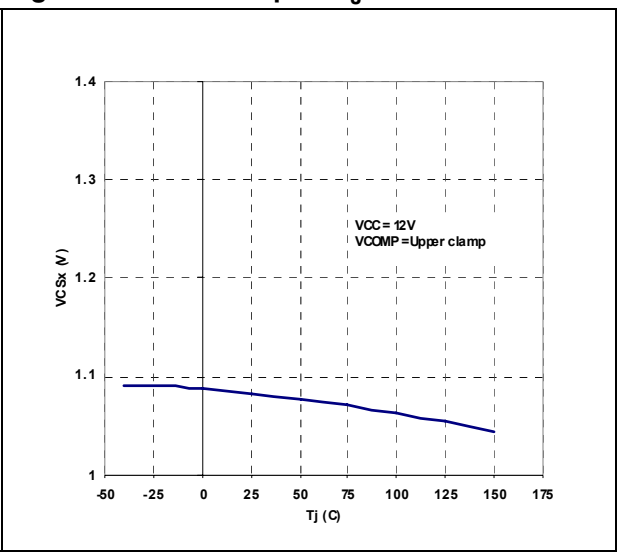


Figure 14. ZCD sink/source capability vs T_J

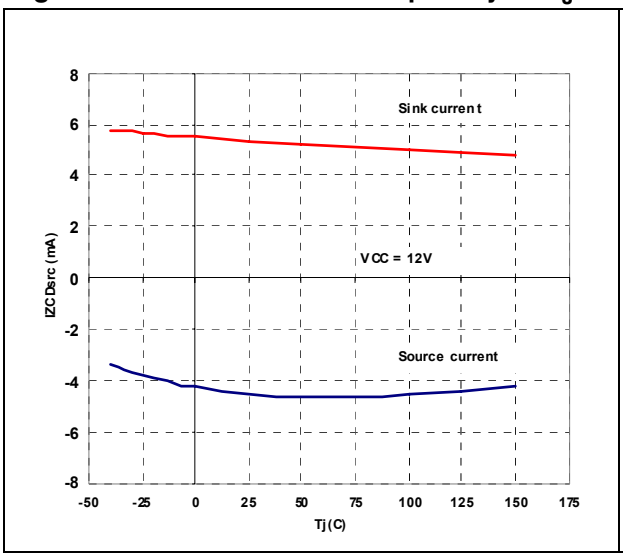


Figure 15. ZCD clamp level vs T_J

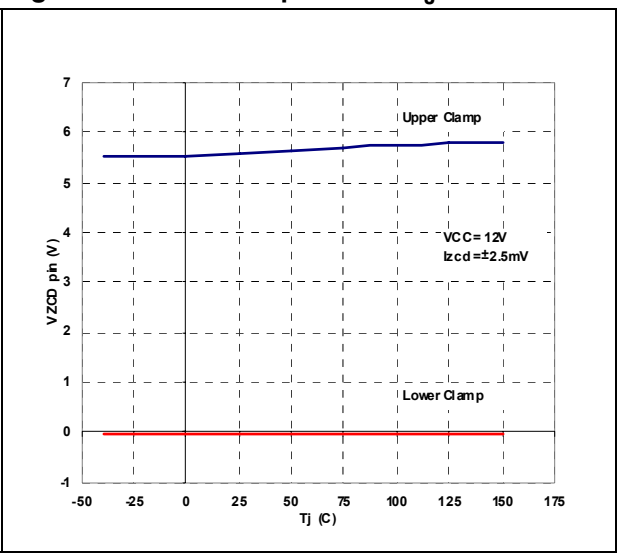


Figure 16. TBO clamp vs T_J

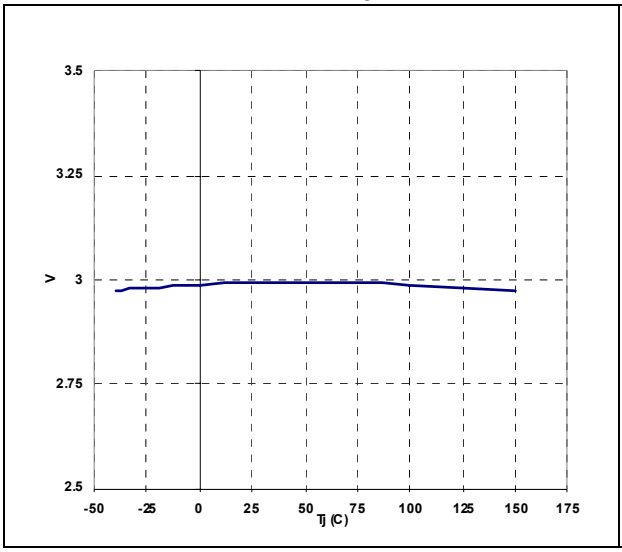


Figure 17. V_{VFF} - V_{TBO} dropout vs T_J

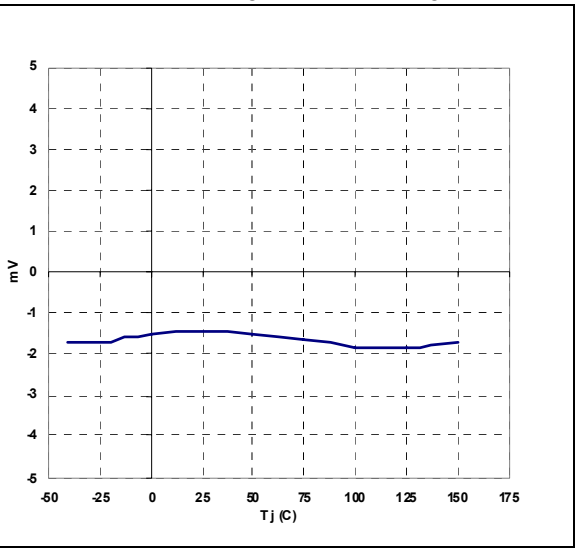


Figure 18. I_{INV} - I_{TBO} current mismatch vs T_J

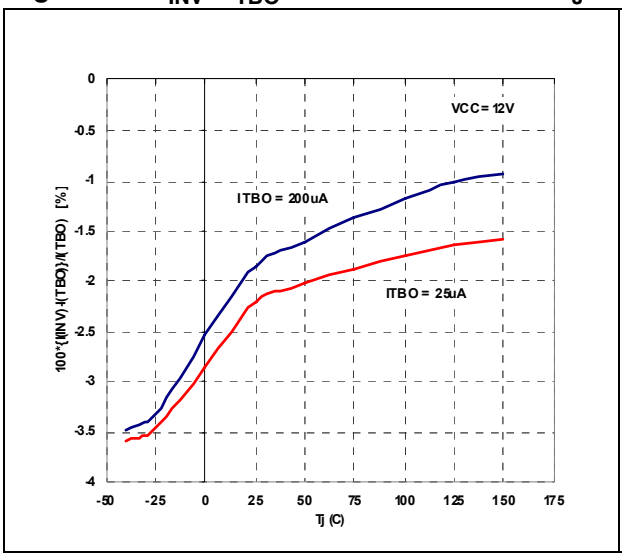


Figure 19. I_{INV} - I_{TBO} mismatch vs I_{TBO} current

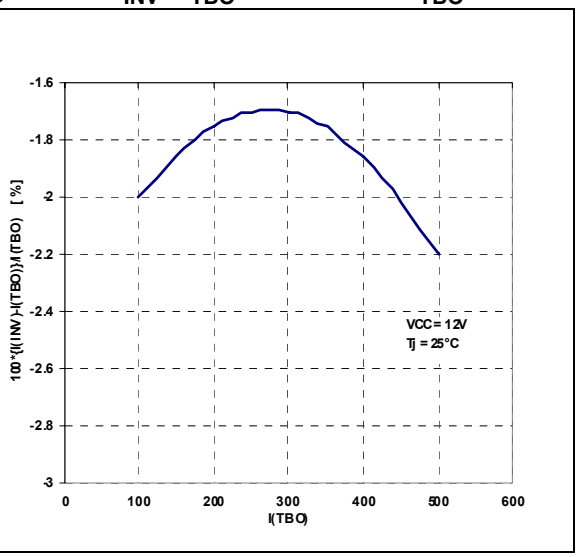


Figure 20. R discharge vs T_J

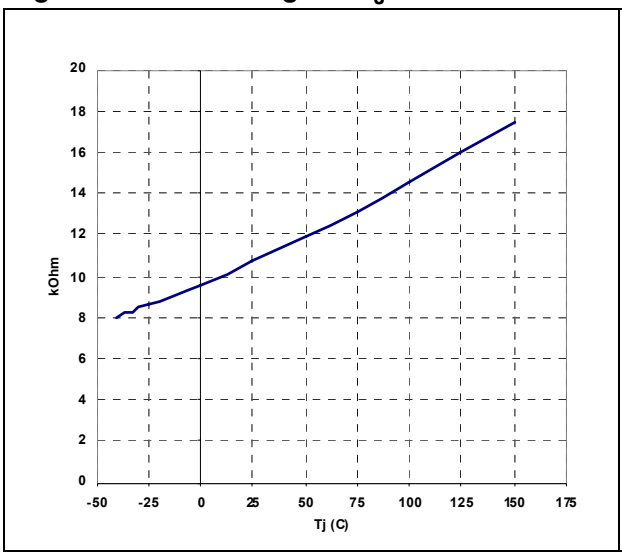


Figure 21. Line drop detection threshold vs T_J

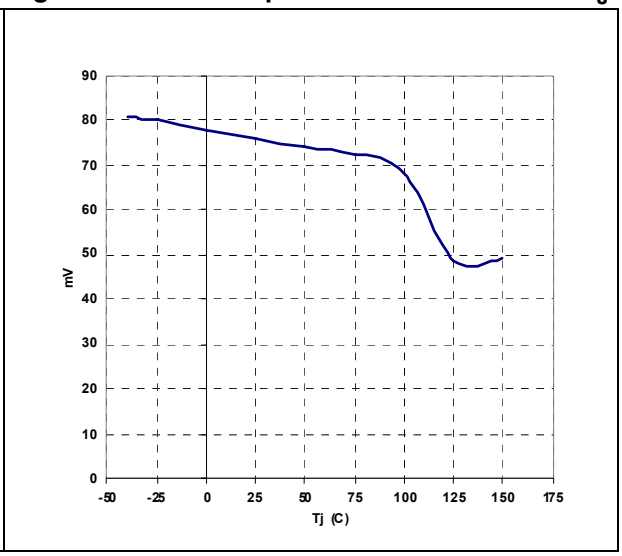


Figure 22. V_{MULTpk} - V_{VFF} dropout vs T_J

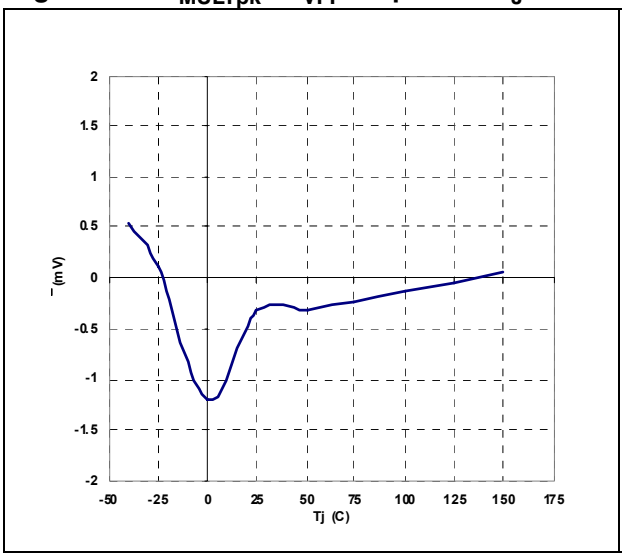


Figure 23. PFC_OK threshold vs T_J

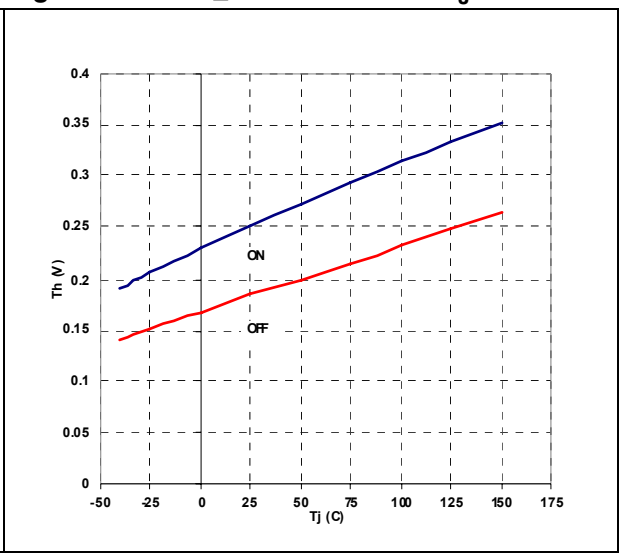


Figure 24. PFC_OK FFD threshold vs T_J

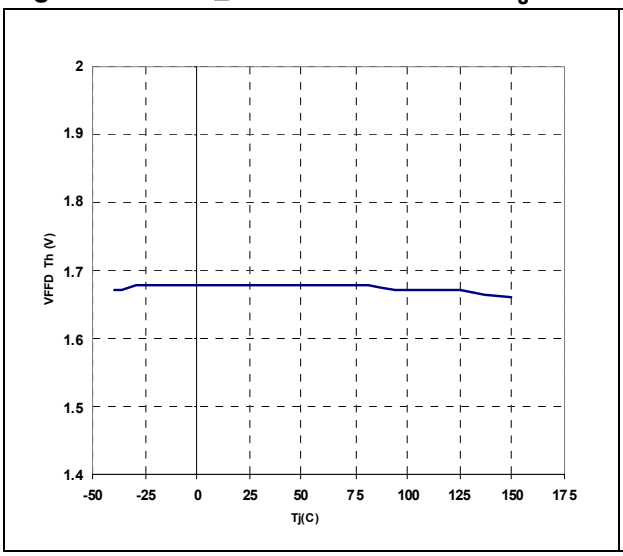


Figure 25. PWM_LATCH high saturation vs T_J

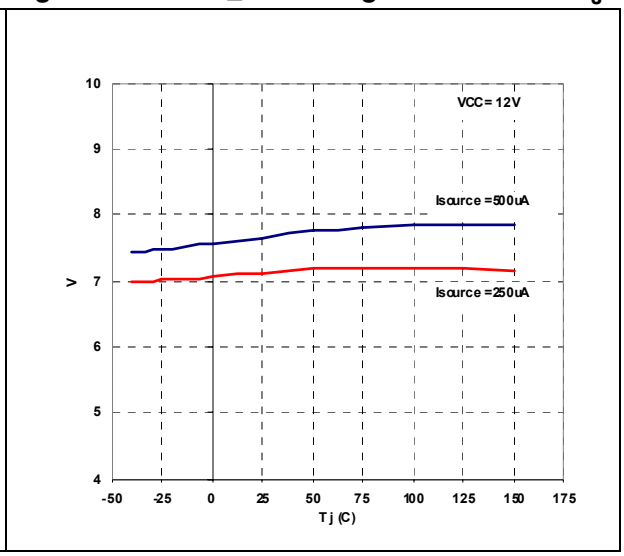


Figure 26. RUN threshold vs T_J

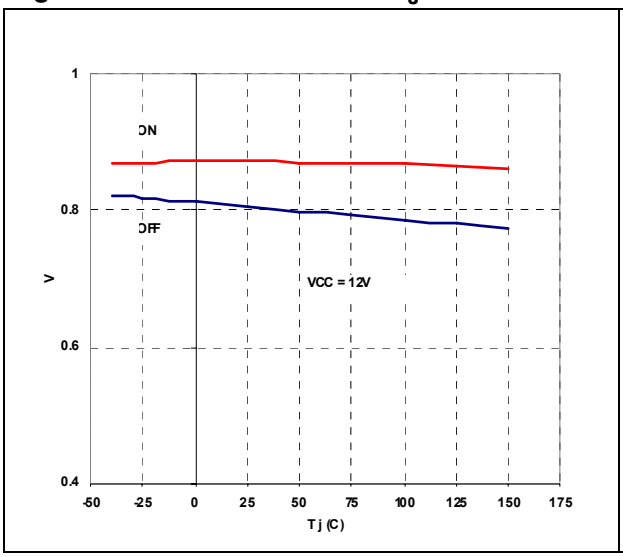


Figure 27. PWM_STOP low saturation vs T_J

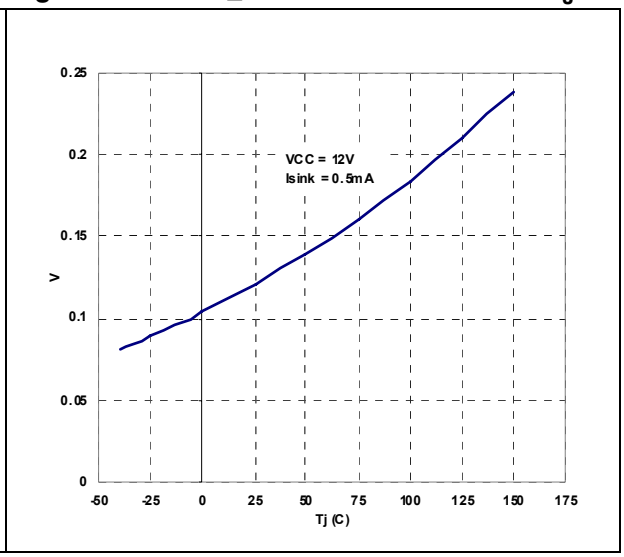


Figure 28. Multiplier characteristics @ V_{FF} = 1 V

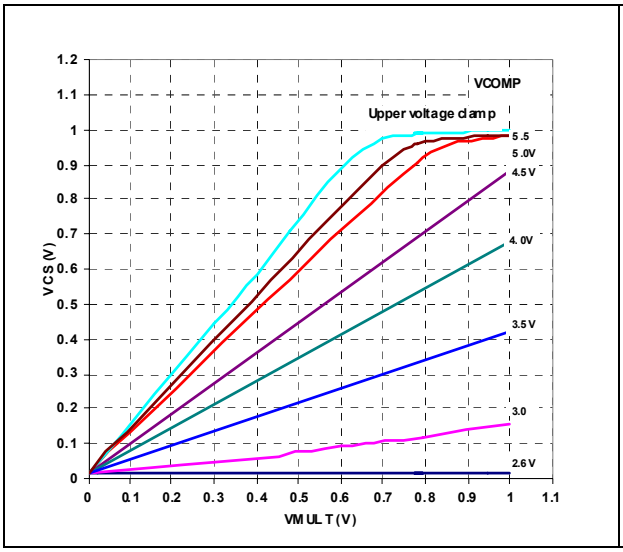


Figure 29. Multiplier characteristics @ V_{FF} = 3 V

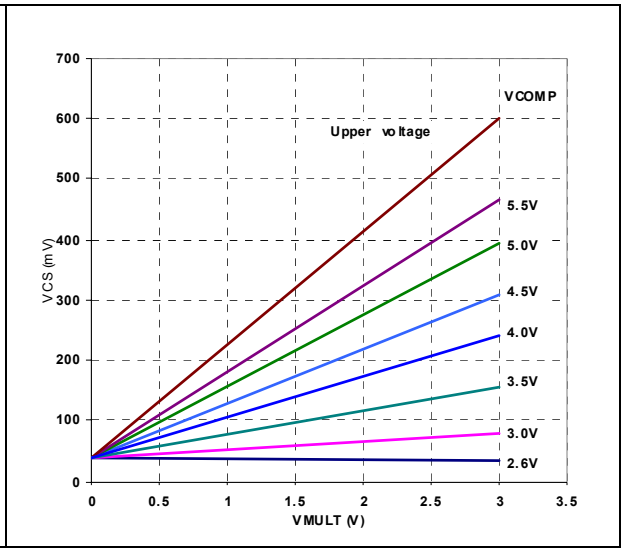


Figure 30. Multiplier gain vs T_J

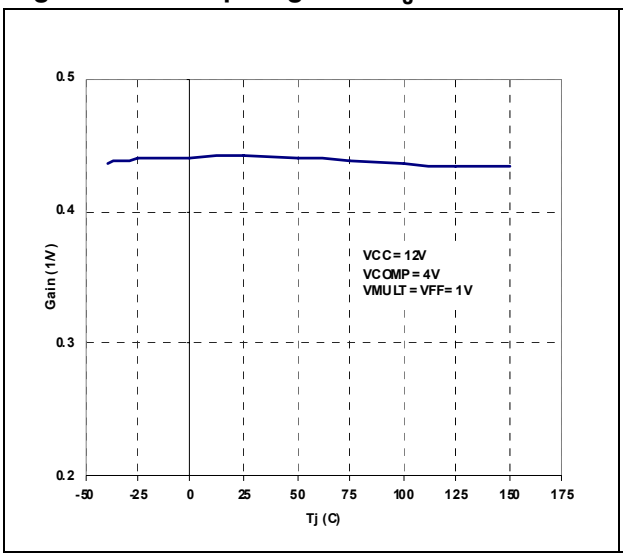


Figure 31. Gate drive clamp vs T_J

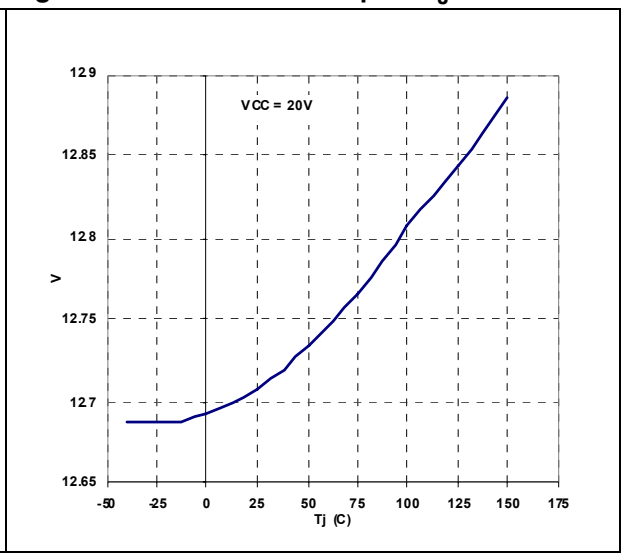


Figure 32. Gate drive output saturation vs T_J

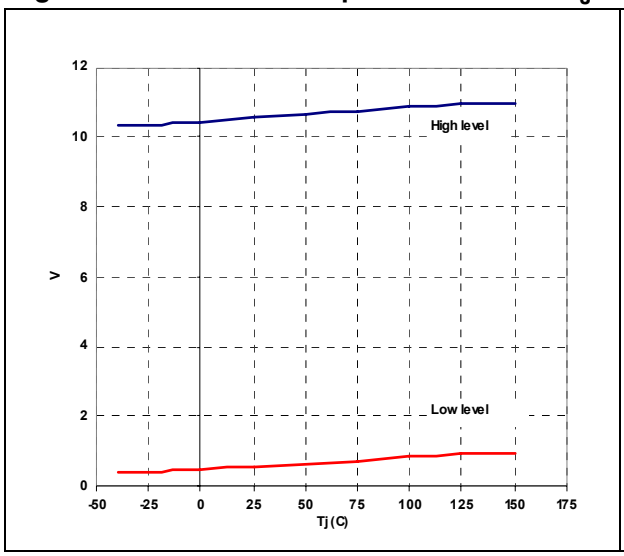


Figure 33. Delay to output vs T_J

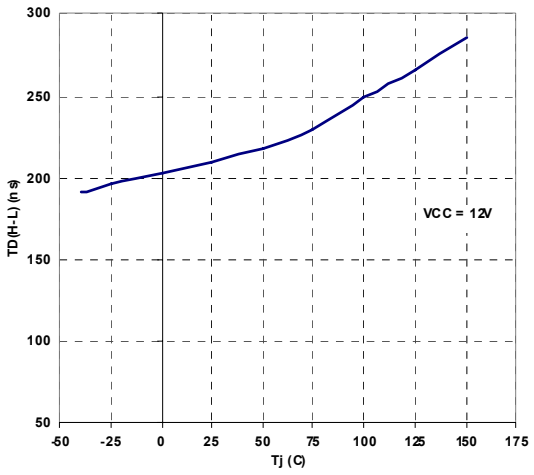
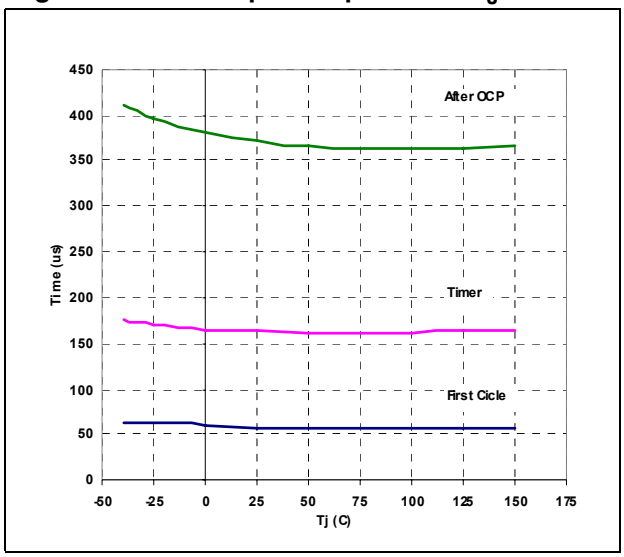


Figure 34. Start-up timer period vs T_J



6 Application information

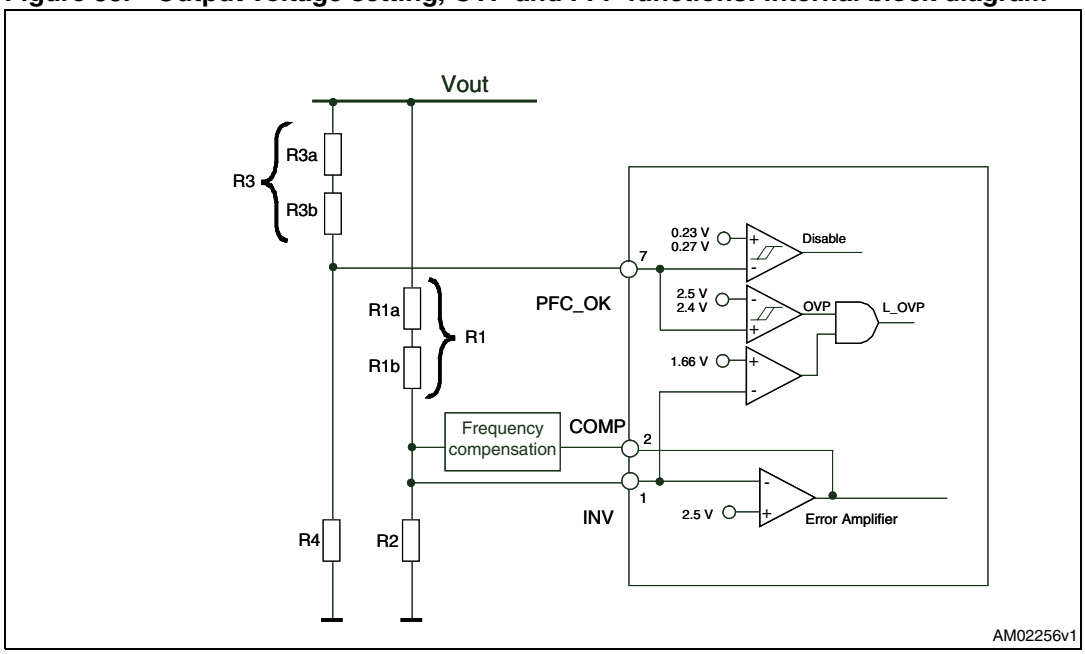
6.1 Overvoltage protection

Normally, the voltage control loop keeps the output voltage Vo of the PFC pre-regulator close to its nominal value, set by the ratio of the resistors R1 and R2 of the output divider. A pin of the device (PFC_OK) has been dedicated to monitor the output voltage with a separate resistor divider (R3 high, R4 low, see *Figure 35*). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value, usually larger than the maximum Vo that can be expected.

Example: V_O = 400 V, V_{OX} = 434 V. Select: R3 = 8.8 MΩ; then: R4 = 8.8 MΩ ·2.5/(434-2.5) = 51 kΩ.

When this function is triggered, the gate drive activity is immediately stopped until the voltage on the pin PFC_OK drops below 2.4 V. Notice that R1, R2, R3 and R4 can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the bias current of both INV and PFC_OK pins.

Figure 35. Output voltage setting, OVP and FFP functions: internal block diagram



6.2 Feedback failure protection (FFP)

The OVP function above described handles “normal” over voltage conditions, i.e. those resulting from an abrupt load/line change or occurring at start-up. In case the overvoltage is generated by a feedback disconnection, for instance when the upper resistor of the output divider (R1) fails open, an additional comparator detects the voltage at pin INV. If the voltage is lower than 1.66 V and the OVP is active, the FFP is triggered, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 180 µA and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. At the same time the pin PWM_LATCH is asserted high. PWM_LATCH is an open source output able to deliver 2.8 V minimum with 0.25 mA load, intended for tripping a latched shutdown function of the PWM controller IC in the cascaded dc-dc converter, so that the entire unit is latched off. To restart the system it is necessary to recycle the input power, so that the Vcc voltage of both the L6563S goes below 6V and that one of the PWM controller goes below its UVLO threshold.

The pin PFC_OK doubles its function as a not-latched IC disable: a voltage below 0.23V will shut down the IC, reducing its consumption below 2 mA. In this case both PWM_STOP and PWM_LATCH keep their high impedance status. To restart the IC simply let the voltage at the pin go above 0.27 V.

Note that these functions offer a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a PFC_OK pin floating will result in shutting down the IC and stopping the pre-regulator.

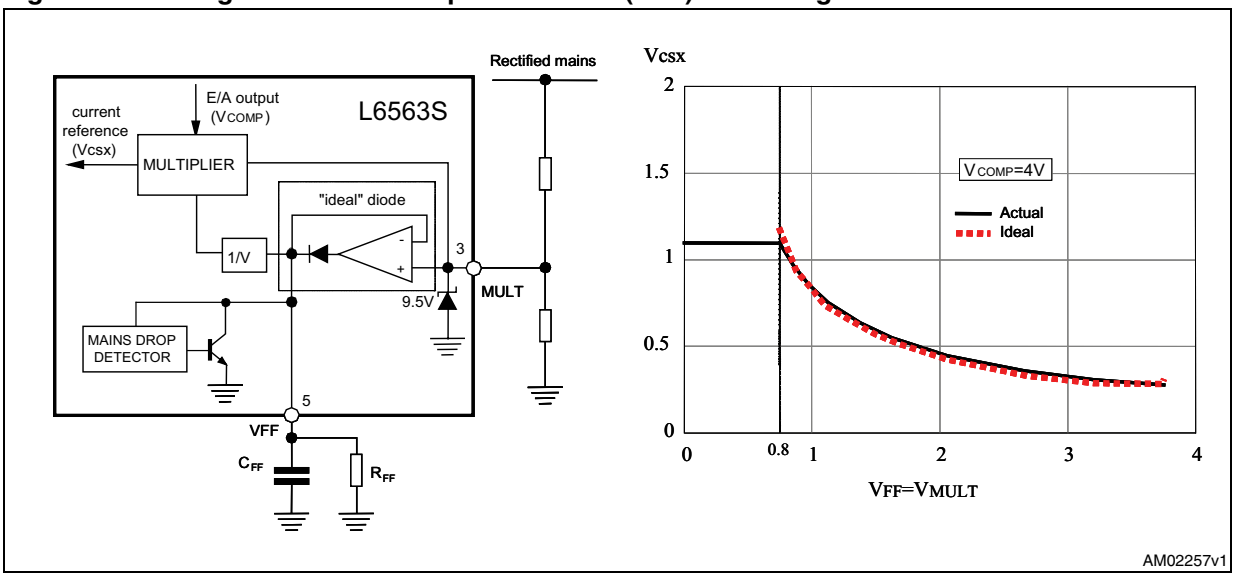
6.3 Voltage feedforward

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. So does the crossover frequency fc of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design.

For example, setting the gain of the error amplifier to get fc = 20 Hz @ 264 Vac means having fc 4 Hz @ 88 Vac, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage Feedforward can compensate for the gain variation with the line voltage and allow minimizing all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit (1/V2 corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (see *Figure 36*).

Figure 36. Voltage feedforward: squarer-divider (1/V^2) block diagram and transfer characteristic



In this way a change of the line voltage will cause an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier output will be halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain will be constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

Actually, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small the voltage generated will be affected by a considerable amount of ripple at twice the mains frequency that will cause distortion of the current reference (resulting in high THD and poor PF); if it is too large there will be a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off was required.

The L6563S realizes a NEW voltage feed forward that, with a technique that makes use of just two external parts, strongly minimizes this time constant trade-off issue whichever voltage change occurs on the mains, both surges and drops. A capacitor C_{FF} and a resistor RFF, both connected from the pin VFF (#5) to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (#3). In this way, in case of sudden line voltage rise, C_{FF} will be rapidly charged through the low impedance of the internal diode; in case of line voltage drop, an internal “mains drop” detector enables a low impedance switch which suddenly discharges CFF avoiding long settling time before reaching the new voltage level. The discharge of CFF is stopped as its voltage equals the voltage on pin MULT or if the voltage on pin RUN (in case it is connected to VFF) falls below 0.88 V, to prevent the “Brownout protection” function from being improperly activated (see “*Section 6.7 on page 31*).

As a result of the VFF pin functionality, an acceptably low steady-state ripple and low current distortion can be achieved with a limited undershoot or overshoot on the pre-regulator's output.