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L6701

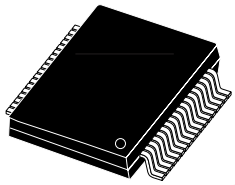
3 Phase Controller for VR10, VR9 and K8 CPUs

Features

- MULTI-DAC: VR9, VR10 AND K8 DAC SELECTABLE THROUGH SINGLE PIN
- 0.7% OUTPUT VOLTAGE ACCURACY
- ADJUSTABLE REFERENCE OFFSET
- HIGH CURRENT INTEGRATED DRIVERS
- DYNAMIC VID MANAGEMENT
- ACCURATE FULLY-DIFFERENTIAL LOAD-LINE CURRENT-SENSE ACROSS MAIN INDUCTORS MAKES BOM INDEPENDENT ON THE LAYOUT
- PRECISE CURRENT-SHARING AND OCP ACROSS LS MOSFETS
- CONSTANT OVER-CURRENT PROTECTION
- FEEDBACK DISCONNECTION PROTECTION
- PRELIMINARY OV PROTECTION
- OSCILLATOR INTERNALLY FIXED AT 100kHz (300kHz RIPPLE) EXT ADJUSTABLE
- SS_END / PGOOD SIGNAL
- INTEGRATED REMOTE-SENSE BUFFER
- PWSSO36 PACKAGE WITH EXPOSED PAD

Applications

- HIGH CURRENT VRM / VRD FOR DESKTOP / SERVER / WORKSTATION CPUs
- HIGH DENSITY DC / DC CONVERTERS



PowerSSO-36

Description

L6701 is an extremely simple, low cost solution to implement a three phase step-down controller with integrated high-current drivers in a compact PowerSSO-36 package with exposed pad.

The device embeds three selectable DACs: with a single pin it is possible to program the device to work in compatibility with VR9, VR10 or K8 applications managing D-VID with ±0.7% output voltage accuracy over line and temperature variations. Additional programmable offset can be added to the reference voltage with a single external resistor.

Fast protection against load over current let the system works in Constant Current mode until UVP. Preliminary OVP allows full load protection in case of startup with failed HS. Furthermore, feedback disconnection prevents from damaging the load in case of misconnections in the system board.

Combined use of DCR and $R_{DS(on)}$ current sensing assures precision in voltage positioning and safe current sharing and OCP per each phase.

Order codes

Part number	Package	Packing
L6701	PowerSSO-36	Tube
L6701TR	PowerSSO-36	Tape & Reel

Contents

1 Device Description

L6701 is multi-phase PWM controller with embedded high-current drivers that provides complete control logic and protections for a high-performance step-down DC-DC voltage regulator, optimized for advanced microprocessor power supply. Multi-phase buck is the simplest and most cost-effective topology employable to satisfy the increasing current demand of newer microprocessors and the modern high-current DC/DC converters and POLs requirements. It allows distributing equally load and power between the phases using smaller, cheaper and most common external power MOSFETs and inductors. Moreover, thanks to the equal phase-shift between each phase, the input and output capacitor count results in being reduced. Phase-interleaving causes in fact input rms current and output ripple voltage reduction and shows an effective output switching frequency increase: the 100kHz free-running frequency per phase, externally adjustable through a resistor, results multiplied on the output by the number of phases so reaching 300kHz in free-running.

L6701 includes multiple DACs, selectable through an apposite pin, allowing compatibility with both Intel VR9, VR10 and AMD Hammer specifications, also performing 5 VID transitions accordingly. In particular for Intel CPUs, it allows to automatically recognize the CPU with a single-wire connection, without any additional external component by proper connecting the selector pin to the proper CPU pin.

Precise voltage positioning (LL) is possible thanks to an accurate fully-differential current-sense across the main inductors still using only two pins for current-reading (pat. pend.): this makes any BOM insensitive to the board layout saving time in the design stage.

The device internally balance the current driven by each phase by sensing the voltage drop across the LS MOSFET $R_{DS(on)}$. OC protection is effective with a threshold for each phase causing the device to work in constant-current mode.

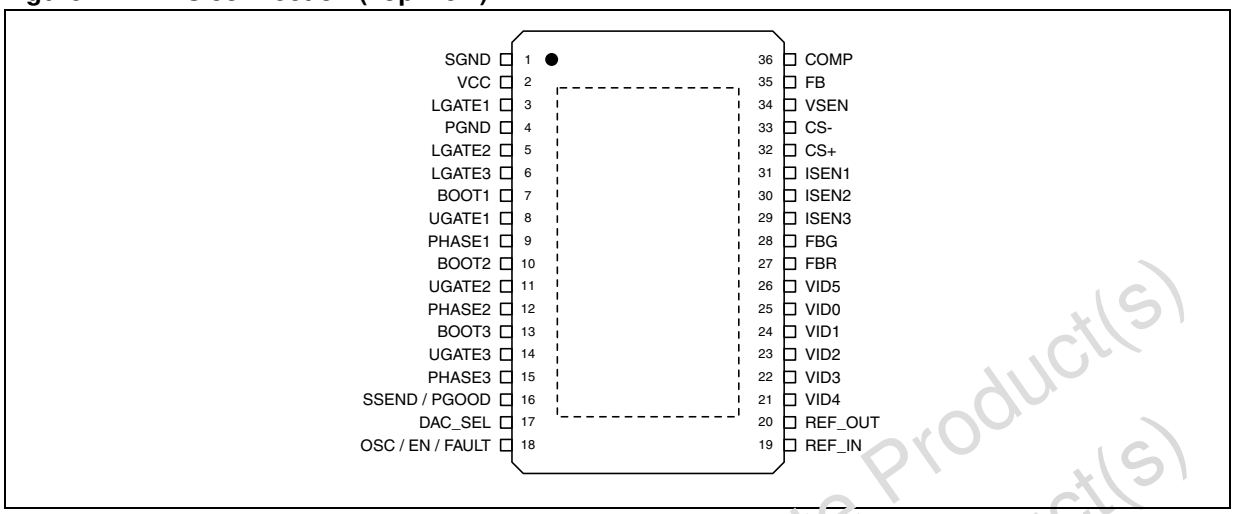
The controller provides output voltage protections to avoid any load damage due to failed components and/or feedback misconnections. Over-Voltage protects the load from dangerous over stress latching immediately the device by turning-on the lower driver and driving high the FAULT pin. Furthermore, preliminary-OVP protection also allows the device to protect the load from dangerous OVP when V_{CC} is not above the UVLO threshold. Under-Voltage protection causes the device to stop switching when set while Over-Current protection, with a threshold for each phase, causes the device to enter in constant current mode until the latched UVP.

L6701 implements soft-start increasing the reference up to the final value in 2048 clock cycles in closed loop regulation. Low-Side-Less feature allows the device to perform soft-start over pre-biased output avoiding dangerous current return through the main inductors as well as negative spike at the load side.

The compact PowerSSO-36 package with exposed thermal pad allows dissipating the power to drive the external MOSFET through the system board.

2 Pins description and connection diagrams

Figure 1. Pins connection (Top view)



2.1 Pin description

Table 1. Pins description

Pin n°	Name	Function
1	SGND	All the internal references are referred to this pin. Connect to the PCB Signal Ground.
2	VCC	Device Power Supply and LS driver supply. Operative voltage is 12V ±15%. Filter with at least 1µF MLCC vs. ground.
3	LGATE1	Channel 1 LS Driver Output. A small series resistor helps in reducing device-dissipated power.
4	PGND	LS Drivers return path. Connect to Power ground Plane.
5	LGATE2	Channel 2 LS Driver Output. A small series resistor helps in reducing device-dissipated power.
6	LGATE3	Channel 3 LS Driver Output. A small series resistor helps in reducing device-dissipated power.
7	BOOT1	Channel 1 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE1 and provide necessary Bootstrap diode. A small series resistor upstream the boot diode helps in reducing Boot capacitor overcharge.
8	UGATE1	Channel 1 HS driver output. A small series resistors helps in reducing device-dissipated power.
9	PHASE1	Channel 1 HS driver return path. It must be connected to the HS1 MOSFET source and provides return path for the HS driver of channel 1.

Table 1. Pins description (continued)

Pin n°	Name	Function
10	BOOT2	Channel 2 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE2 and provide necessary Bootstrap diode. A small series resistor upstream the boot diode helps in reducing Boot capacitor overcharge.
11	UGATE2	Channel 2 HS driver output. A small series resistors helps in reducing device-dissipated power.
12	PHASE2	Channel 2 HS driver return path. It must be connected to the HS2 MOSFET source and provides return path for the HS driver of channel 2.
13	BOOT3	Channel 3 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE3 and provide necessary Bootstrap diode. A small series resistor upstream the boot diode helps in reducing Boot capacitor overcharge.
14	UGATE3	Channel 3 HS driver output. A small series resistors helps in reducing device-dissipated power.
15	PHASE3	Channel 3 HS driver return path. It must be connected to the HS3 MOSFET source and provides return path for the HS driver of channel 3.
16	SSEND / PGOOD	*SSEND - Intel VR10 Mode*. Soft Start END Signal. Open Drain Output set free after SS has finished and pulled low when triggering any protection. Pull up to 5V (typ) or lower, if not used it can be left floating. *PGOOD - Intel VR9 & AMD Hammer Mode*. Open Drain Output set free after SS has finished and pulled low when VSEN is lower than the relative threshold. Pull up to 5V (typ) or lower, if not used it can be left floating.
17	DAC_SEL	*DAC SELection pin.* It allows programming the DAC table for the regulation. Internally pulled-up to 5V. Short to GND to program VR9 DAC, leave floating to program K8 DAC while connect to GND through 82kΩ to program VR10 DAC. Information about the selected DAC is latched before the system start-up. See *Section 7.1* for connections to enable CPU auto-detection.
18	OSC / EN / FAULT	*OSC*: It allows programming the switching frequency F_{SW} of each channel. Switching frequency can be increased according to the resistor connected from the pin vs. SGND with a gain of 4kHz/µA (see *Section 14*). Leaving the pin floating it programs a switching frequency of 100kHz per phase (300kHz on the load). *EN*: Forced low, the device stops operations with all MOSFETs OFF: all the protections are disabled except for *Preliminary Over Voltage*. When set low it resets the device from any latching condition. *FAULT*: The pin is forced high (5V) to signal an OVP / UVP FAULT: to recover from this condition, cycle VCC or the OSC pin. See *Section 13* for details.

Table 1. Pins description (continued)

Pin n°	Name	Function
19	REF_IN	Reference Input for the regulation. Connect directly or through a resistor to the REF_OUT pin. See *Section 10.3* for details. This pin is used as input for the protections.
20	REF_OUT	Reference Output. Connect directly or through a resistor to the REF_IN pin. See *Section 10.3* for details.
21 to 26	VID4 to VID0, VID5	Voltage IDentification Pins. Internally pulled up by 12.5µA to 5V, connect to SGND to program a '0' or leave floating to program a '1'. They allow programming output voltage as specified in *Table 5*, *Table 6* and *Table 7* according to DAC_SEL status.
27	FBR	Remote Buffer Non Inverting Input. Connect to the positive side of the load to perform remote sense. See *Section 16* for proper layout of this connection.
28	FBG	Remote Buffer Inverting Input. Connect to the negative side of the load to perform remote sense. See *Section 16* for proper layout of this connection.
29 to 31	ISEN3 to ISEN1	LS Current Sense Pins. These pins are used for current balance phase-to-phase as well as for the system OCP. Connect through a resistor R_{ISEN} to the relative PHASEx pin. See *Section 9* and *Section 13.6* for details.
32	CS+	Droop Current Sense non-inverting input. Connect through R_{PH}-C_{PH} network to the main inductors. Directly connect to output voltage when Droop function is not required. See *Section 10.1* and *Section 10.2* for details.
33	CS-	Droop Current Sense inverting input. Connect through resistor R_D to the main inductors common node. Leave floating when Droop Function is not required. See *Section 10.1* and *Section 10.2* for details. This pin also monitors the output for any feedback disconnection. See *Section 13.4* for details.
34	VSEN	Remote Buffer Output. It manages OVP and UVP protections and PGOOD (when applicable). See *Section 13* for details.
35	FB	Error Amplifier Inverting Input. Connect with a resistor R_{FB} vs. VSEN and with an R_F - C_F toward COMP.
36	COMP	Error Amplifier Output. Connect with an R_F - C_F vs. FB. The device cannot be disabled by pulling down this pin.
PAD	THERMAL PAD	Thermal pad connects the Silicon substrate and makes good thermal contact with the PCB to dissipate the power necessary to drive the external MOSFETs. Connect to the PGND plane with several VIAs to improve thermal conductivity.

3 Maximum Ratings

3.1 Absolute maximum ratings

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	to PGND	15	V
V_{BOOTx} - V_{PHASEx}	Boot Voltage	15	V
V_{UGATEx} - V_{PHASEx}		15	V
	LGATEx, PHASEx, to PGNDx	-0.3 to V_{CC} + 0.3	V
	VID0 to VID5	-0.3 to 5	V
	All other Pins to PGNDx	-0.3 to 7	V
V_{PHASEx}	Positive Peak Voltage; T<20ns @ 600kHz	26	V
	Negative Peak Voltage;	TBD	V

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance Junction to Ambient (Device soldered on 2s2p PC Board)	30	°C/W
R_{THJC}	Thermal Resistance Junction to Case	1	°C/W
T_{MAX}	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-40 to 150	°C
T_J	Junction Temperature Range	0 to 125	°C
P_{TOT}	Maximum Power Dissipation at 25°C (Device soldered on 2s2p PC Board)	3.3	W

4 Electrical specifications

4.1 Electrical characteristics

Table 4. Electrical Characteristics
(V_{CC} = 12V±15%, T_J = 0°C to 70°C unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply Current and Power-ON						
I_{CC}	VCC Supply current	HGATEx and LGATEx = OPEN BOOTx = 12V		17		mA
I_{BOOTx}	BOOTx Supply Current	HGATEx = OPEN; PHASEx to PGNDx; BOOTx = 12V		0.7		mA
$UVLO_{VCC}$	V_{CC} Turn-ON	V_{CC} Rising			9.2	V
	V_{CC} Turn-OFF	V_{CC} Falling	7			V
$UVLO_{OVP}$	Pre-OVP Turn-ON	V_{CC} Rising			3.8	V
	Pre-OVP Turn-OFF	V_{CC} Falling	3			V
Oscillator and Inhibit						
F_{SW}	Main Oscillator Accuracy	OSC = OPEN OSC = OPEN; T_J = 0°C to 125°C	90	100	110	kHz
OSC_{IL}	Disable Thresholds		0.5			V
d_{MAX}	Maximum Duty Cycle	OSC = OPEN; I_{ISENx} = 0µA		80		%
		OSC = OPEN; I_{ISENx} = 35µA		40		%
ΔV_{OSC}	PWMx Ramp Amplitude			3		V
FAULT	Voltage at Pin OSC	OVP Active		5		V
Reference and DAC						
V_{VID}	Output Voltage Accuracy	FBR = V_{OUT}; FBG = GND_{OUT}; VR10 and VR9 DACs; V_{OUT} > 1V	-0.7		0.7	%
		FBR = V_{OUT}; FBG = GND_{OUT}; K8 DAC; V_{OUT} > 1V	-1		1	%
I_{VID}	VID Pull-up Current			25		µA
VID_{IL}	VID Input Thresholds	VR9 and VR10 Mode; Input Low K8 Mode; Input Low			0.4 0.8	V V
VID_{IH}		VR9 and VR10 Mode; Input Low K8 Mode; Input Low	0.8 2			V V

Table 4. Electrical Characteristics (continued)
(V_{CC} = 12V±15%, T_J = 0°C to 70°C unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Error Amplifier and Remote Buffer						
A_0	EA DC Gain			80		dB
SR	Slew Rate	COMP = 10pF to SGND		15		V/µs
	RB DC Gain			1		V/V
CMRR	Remote Buffer Common Mode Rejection Ratio			40		dB
Differential Current Sensing and Offset						
I_{OCTH}	Over Current Threshold			35		µA
k_{IDROOP}	Droop Current Deviation	I_{DROOP} = 0 to 105µA; R_D=5.1kΩ	-3		3	µA
I_{OFFSET}	Offset Current		10	11.5	13	µA
Gate Drivers						
t_{RISE_UGATEx}	HS Rise Time	BOOTx - PHASEx = 10V; C_{UGATEx} to PHASEx = 3.3nF		15		ns
I_{UGATEx}	HS Source Current	BOOTx - PHASEx = 10V		1.5		A
R_{UGATEx}	HS Sink Resistance	BOOTx - PHASEx = 12V		2.5		Ω
t_{RISE_LGATEx}	LS Rise Time	VCC = 10V; C_{LGATEx} to PGNDx = 5.6nF		20		ns
I_{LGATEx}	LS Source Current	VCC = 10V		1.5		A
R_{LGATEx}	LS Sink Resistance	VCC = 12V		1.8		Ω
Protections						
OVP	Over Voltage Protection	VSEN Rising, VR10 and K8 Mode VSEN Rising, VR9 Mode	1.85 2.05	1.9 2.1	1.95 2.15	V V
Pre-OVP	Preliminary Over voltage Protection	FBR Rising, VR10 and K8 Mode FBR Rising, VR9 Mode	1.8 2.0	1.9 2.1	2.0 2.2	V V
		Hysteresis		300		mV
UVP	Under Voltage Protection	VSEN Falling; Below VID	-475	-400	-325	mV
PGOOD	PGOOD Threshold	K8 and VR9 Mode; VSEN Falling; Below VID	-280	-230	-180	mV
$V_{SSEND/PGOOD}$	SSEND / PGOOD Voltage Low	I = -4mA			0.4	V

5 Typical application circuit and block diagram

5.1 Application circuit

Figure 2. Typical application circuit

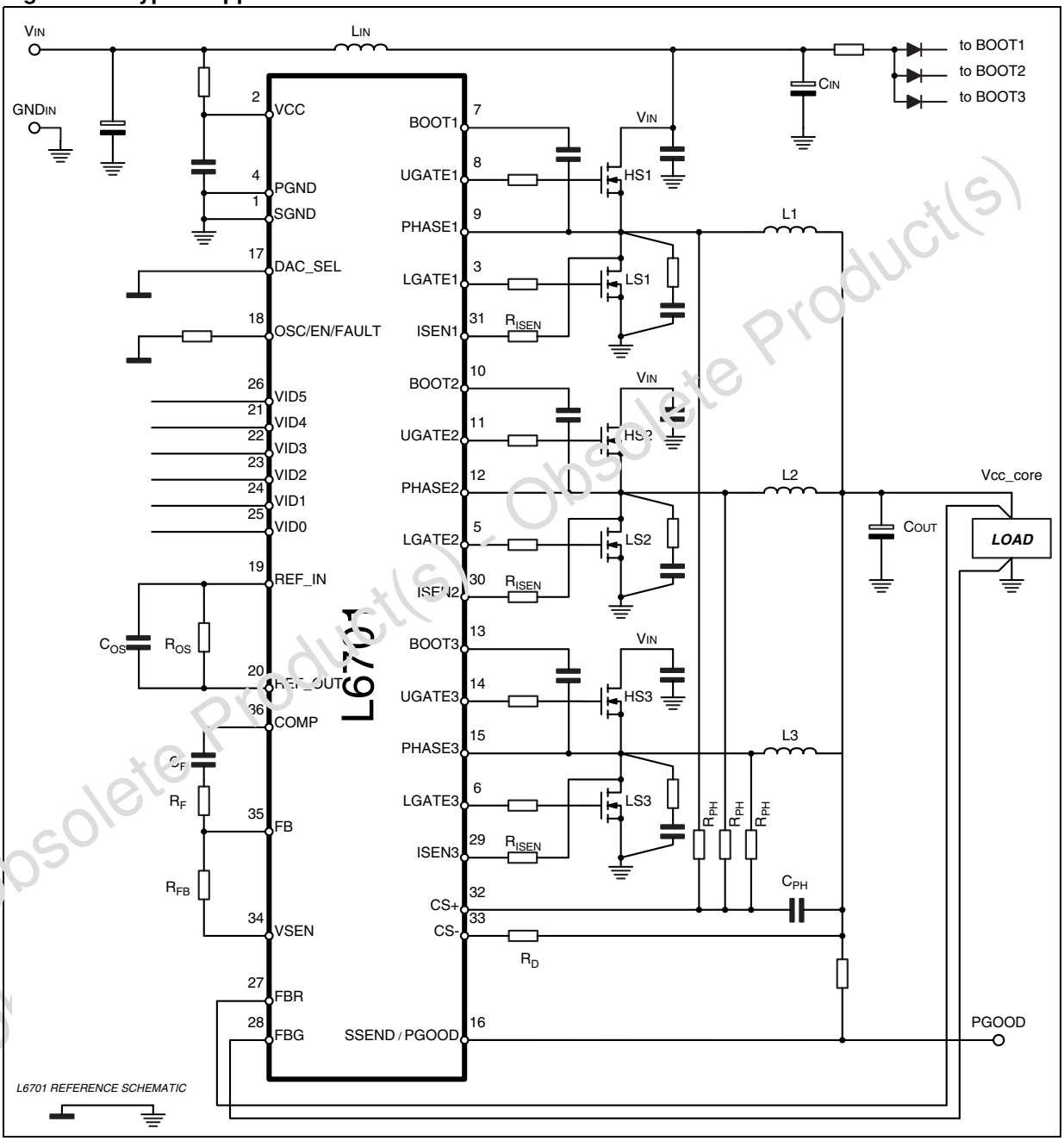
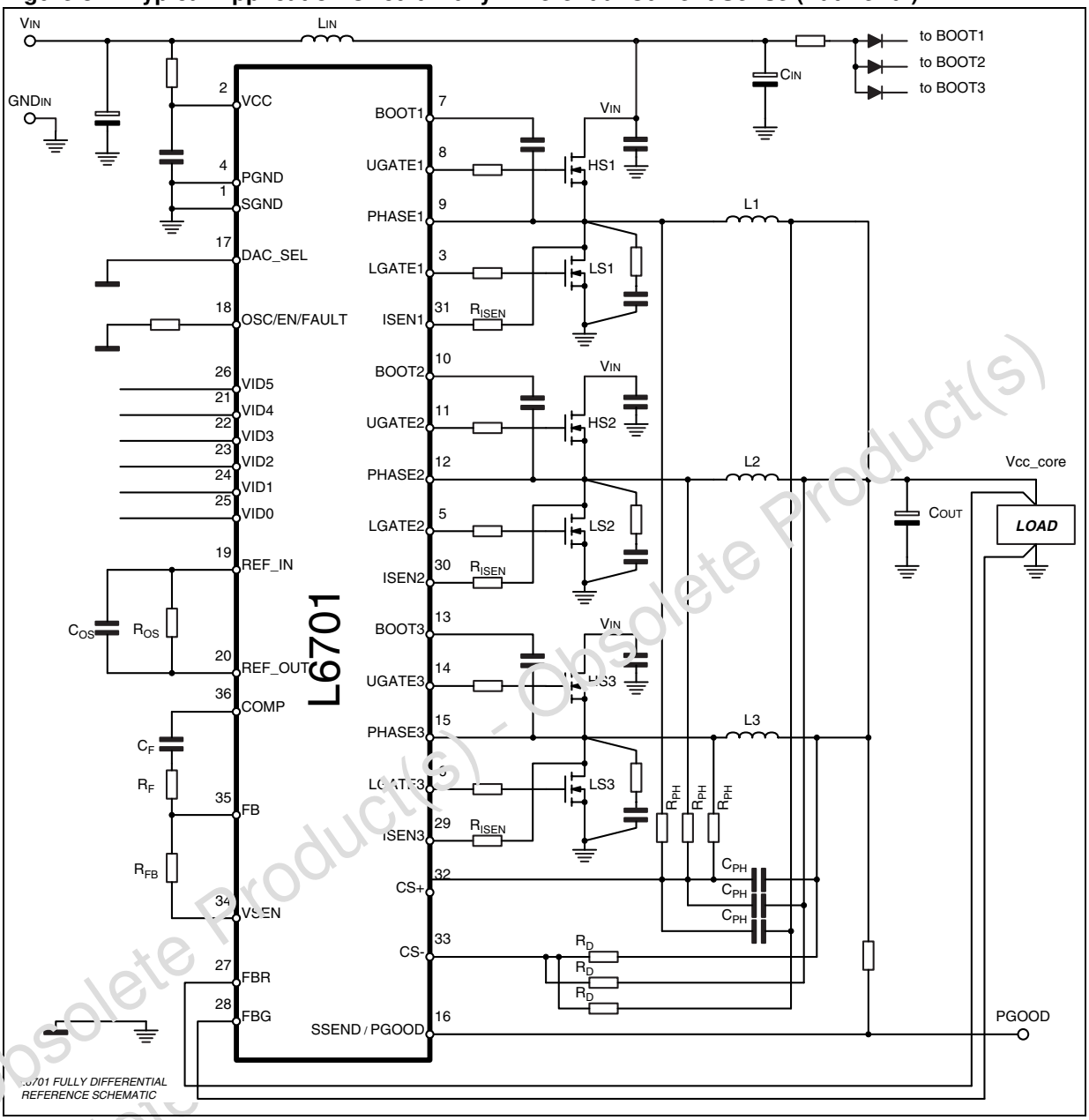
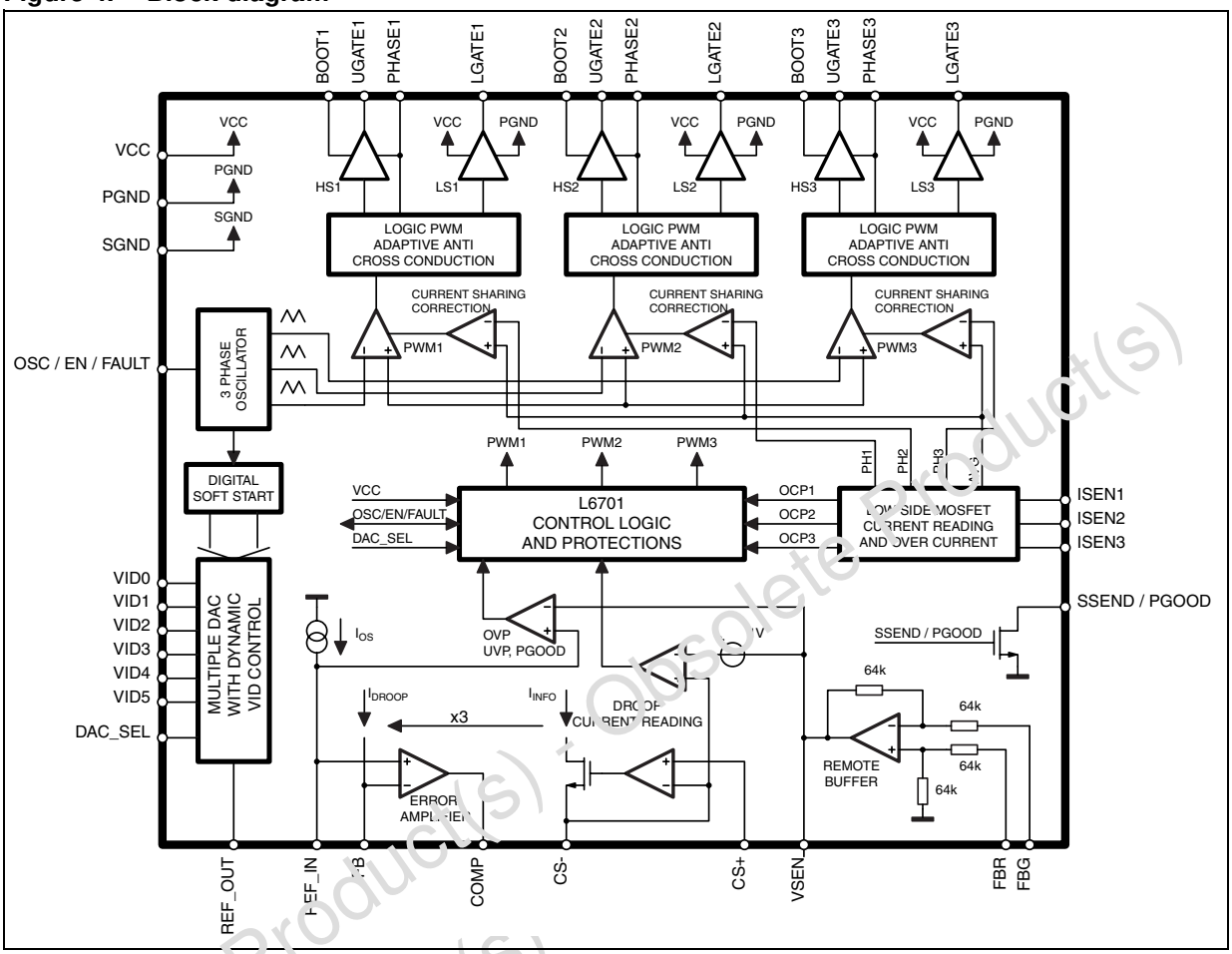


Figure 3. Typical Application Circuit: Fully Differential Current Sense (Pat.Pend.)



5.2 Block diagram

Figure 4. Block diagram



6 VID Tables

Table 5. Voltage IDentification (VID) for Intel VR10 DAC.

VID4	VID3	VID2	VID1	VID0	VID5	Output Voltage (1)	VID4	VID3	VID2	VID1	VID0	VID5	Output Voltage (1)
0	1	0	1	0	1	1.6000	1	1	0	1	0	1	1.2000
0	1	0	1	1	0	1.5875	1	1	0	1	1	0	1.1875
0	1	0	1	1	1	1.5750	1	1	0	1	1	1	1.1750
0	1	1	0	0	0	1.5625	1	1	1	0	0	0	1.1625
0	1	1	0	0	1	1.5500	1	1	1	0	0	1	1.1500
0	1	1	0	1	0	1.5375	1	1	1	0	1	0	1.1375
0	1	1	0	1	1	1.5250	1	1	1	0	1	1	1.1250
0	1	1	1	0	0	1.5125	1	1	1	1	0	0	1.1175
0	1	1	1	0	1	1.5000	1	1	1	1	0	1	1.1000
0	1	1	1	1	0	1.4875	1	1	1	1	1	0	OFF
0	1	1	1	1	1	1.4750	1	1	1	1	1	1	OFF
1	0	0	0	0	0	1.4625	0	0	0	0	0	0	1.0875
1	0	0	0	0	1	1.4500	0	0	0	0	0	1	1.0750
1	0	0	0	1	0	1.4375	0	0	0	0	1	0	1.0625
1	0	0	0	1	1	1.4250	0	0	0	0	1	1	1.0500
1	0	0	1	0	0	1.4125	0	0	0	1	0	0	1.0375
1	0	0	1	0	1	1.4000	0	0	0	1	0	1	1.0250
1	0	0	1	1	0	1.3875	0	0	0	1	1	0	1.0125
1	0	0	1	1	1	1.3750	0	0	0	1	1	1	1.0000
1	0	1	0	0	0	1.3625	0	0	1	0	0	0	0.9875
1	0	1	0	0	1	1.3500	0	0	1	0	0	1	0.9750
1	0	1	0	1	0	1.3375	0	0	1	0	1	0	0.9625
1	0	1	0	1	1	1.3250	0	0	1	0	1	1	0.9500
1	0	1	1	0	0	1.3125	0	0	1	1	0	0	0.9375
1	0	1	1	0	1	1.3000	0	0	1	1	0	1	0.9250
1	0	1	1	1	0	1.2875	0	0	1	1	1	0	0.9125
1	0	1	1	1	1	1.2750	0	0	1	1	1	1	0.9000
1	1	0	0	0	0	1.2625	0	1	0	0	0	0	0.8875
1	1	0	0	0	1	1.2500	0	1	0	0	0	1	0.8750
1	1	0	0	1	0	1.2375	0	1	0	0	1	0	0.8625

Table 5. Voltage IDentification (VID) for Intel VR10 DAC. (continued)

VID4	VID3	VID2	VID1	VID0	VID5	Output Voltage (1)	VID4	VID3	VID2	VID1	VID0	VID5	Output Voltage (1)
1	1	0	0	1	1	1.2250	0	1	0	0	1	1	0.8500
1	1	0	1	0	0	1.2125	0	1	0	1	0	0	0.8375

1. Since the VIDx pins program the maximum output voltage, according to VR10.x specifications, the device automatically regulates to a voltage 19mV lower avoiding the use of any external components to lower the output voltage. This improves the system tolerance performance since the reference already offset is trimmed in production within ±0.7%.

Table 6. Voltage IDentification (VID) for Intel VR9 DAC (VID5 doesn't care)

VID4	VID3	VID2	VID1	VID0	Output Voltage(1)	VID4	VID3	VID2	VID1	VID0	Output Voltage(1)
0	0	0	0	0	1.850	1	0	0	0	0	1.450
0	0	0	0	1	1.825	1	0	0	0	1	1.425
0	0	0	1	0	1.800	1	0	0	1	0	1.400
0	0	0	1	1	1.775	1	0	0	1	1	1.375
0	0	1	0	0	1.750	1	0	1	0	0	1.350
0	0	1	0	1	1.725	1	0	1	0	1	1.325
0	0	1	1	0	1.700	1	0	1	1	0	1.300
0	0	1	1	1	1.675	1	0	1	1	1	1.275
0	1	0	0	0	1.650	1	1	0	0	0	1.250
0	1	0	0	1	1.625	1	1	0	0	1	1.225
0	1	0	1	0	1.600	1	1	0	1	0	1.200
0	1	0	1	1	1.575	1	1	0	1	1	1.175
0	1	1	0	0	1.550	1	1	1	0	0	1.150
0	1	1	0	1	1.525	1	1	1	0	1	1.125
0	1	1	1	0	1.500	1	1	1	1	0	1.100
0	1	1	1	1	1.475	1	1	1	1	1	OFF

1. Since the VIDx pins program the maximum output voltage, the device automatically regulates to a voltage 19mV lower avoiding the use of any external components to lower the output voltage. This improves the system tolerance performance since the reference already offset is trimmed in production within ±0.7%.

Table 7. Voltage IDentification (VID) for AMD Hammer DAC

VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage
1	0	0	0	0	0	1.550	0	0	0	0	0	0	1.575
	0	0	0	0	1	1.525		0	0	0	0	1	1.550
	0	0	0	1	0	1.500		0	0	0	1	0	1.525
	0	0	0	1	1	1.475		0	0	0	1	1	1.500
	0	0	1	0	0	1.450		0	0	1	0	0	1.475
	0	0	1	0	1	1.425		0	0	1	0	1	1.450
	0	0	1	1	0	1.400		0	0	1	1	0	1.425
	0	0	1	1	1	1.375		0	0	1	1	1	1.400
	0	1	0	0	0	1.350		0	1	0	0	0	1.375
	0	1	0	0	1	1.325		0	1	0	0	1	1.350
	0	1	0	1	0	1.300		0	1	0	1	0	1.325
	0	1	0	1	1	1.275		0	1	0	1	1	1.300
	0	1	1	0	0	1.250		0	1	1	0	0	1.275
	0	1	1	0	1	1.225		0	1	1	0	1	1.250
	0	1	1	1	0	1.200		0	1	1	1	0	1.225
	0	1	1	1	1	1.175		0	1	1	1	1	1.200
	1	0	0	0	0	1.150		1	0	0	0	0	1.175
	1	0	0	0	1	1.125		1	0	0	0	1	1.150
	1	0	0	1	0	1.100		1	0	0	1	0	1.125
	1	0	0	1	1	1.075		1	0	0	1	1	1.100
	1	0	1	0	0	1.050		1	0	1	0	0	1.075
	1	0	1	0	1	1.025		1	0	1	0	1	1.050
	1	0	1	1	0	1.000		1	0	1	1	0	1.025
	1	0	1	1	1	0.975		1	0	1	1	1	1.000
	1	1	0	0	0	0.950		1	1	0	0	0	0.975
	1	1	0	0	1	0.925		1	1	0	0	1	0.950
	1	1	0	1	0	0.900		1	1	0	1	0	0.925
	1	1	0	1	1	0.875		1	1	0	1	1	0.900
	1	1	1	0	0	0.850		1	1	1	0	0	0.875
	1	1	1	0	1	0.825		1	1	1	0	1	0.850
	1	1	1	1	0	0.800		1	1	1	1	0	0.825
	1	1	1	1	1	OFF		1	1	1	1	1	OFF

7 Configuring the Device: DAC Selection

Multiple DACs need to be configured before the system start-up by programming the apposite pin DAC_SEL. The embedded DAC allows to regulate the output voltage with a tolerance of ±0.7% recovering from offsets and manufacturing variations. In case of selecting VR9 and VR10 Mode, the device automatically introduces a -19mV offset to the regulated voltage (see *Table 5* and *Table 6*) in order to avoid any external offset circuitry to worsen the guaranteed accuracy and, as a consequence, the calculated system TOB. In case of selecting the K8 DAC, VID5 gives the option to introduce +25mV offset to the regulation (See *Table 7*).

Output voltage is programmed through the VID pins: they are inputs of an internal DAC that is realized by means of a series of resistors providing a partition of the internal voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the voltage reference available on REF_OUT.

According to the selected DAC, the device also changes the protection thresholds as a consequence of different CPU specifications, see *Table 8* for details.

Table 8. L6701 Configuration

DAC_SEL	OPERATIVE MODE	OVP & Pre-OVP	UVP	PGOOD
OPEN	AMD K8 +25mV (Driven by VID5)	1.9V Fixed	-400mV	-230mV
82kΩ to GND	Intel VR10 -19mV	1.9V Fixed	-400mV	SSEND
GND	Intel VR9 -19mV	2.1V Fixed	-400mV	-230mV

7.1 Single-Wire CPU Automatic Detection

L6701 has been designed to automatically detect the Intel CPU connected by monitoring the DAC_SEL pin status at the start-up so modifying the DAC table accordingly (see *Table 8*). In fact, by directly connecting the DAC_SEL pin with #BOOTSEL pin of the CPU, the controller automatically recognize the different technology steps of the CPU so modifying the DAC table accordingly.

See CPU related documentation for further details about compatibility.

8 Driver Section

The integrated high-current drivers allow using different types of power MOS (also multiple MOS to reduce the equivalent $R_{DS(on)}$), maintaining fast switching transition.

The drivers for the high-side MOSFETs use BOOTx pins for supply and PHASEx pins for return. The drivers for the low-side MOSFETs use the VCC pin for supply and PGND pin for return.

The controller embodies a anti-shoot-through and adaptive dead-time control to minimize low side body diode conduction time maintaining good efficiency saving the use of Schottky diodes: when the high-side MOSFET turns off, the voltage on its source begins to fall; when the voltage reaches 2V, the low-side MOSFET gate drive is suddenly applied. When the low-side MOSFET turns off, the voltage at LGATEx pin is sensed. When it drops below 1V, the high-side MOSFET gate drive is suddenly applied. If the current flowing in the inductor is negative, the source of high-side MOSFET will never drop. To allow the low-side MOSFET to turn-on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET does not drop, the low side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Power conversion input is flexible: 5V, 12V bus or any bus that allows the conversion (See maximum duty cycle limitations) can be chosen freely.

8.1 Power Dissipation

L6701 embeds high current MOSFET drivers for both high side and low side MOSFETs: it is then important to consider the power that the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature. In addition, since the device has an exposed pad to better dissipate the power, the thermal resistance between junction and ambient consequent to the layout is also important: thermal pad need to be soldered to the PCB ground plane through several VIAs in order to facilitate the heat dissipation.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Device Power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow (assuming to supply HS and LS drivers with the same VCC of the device):

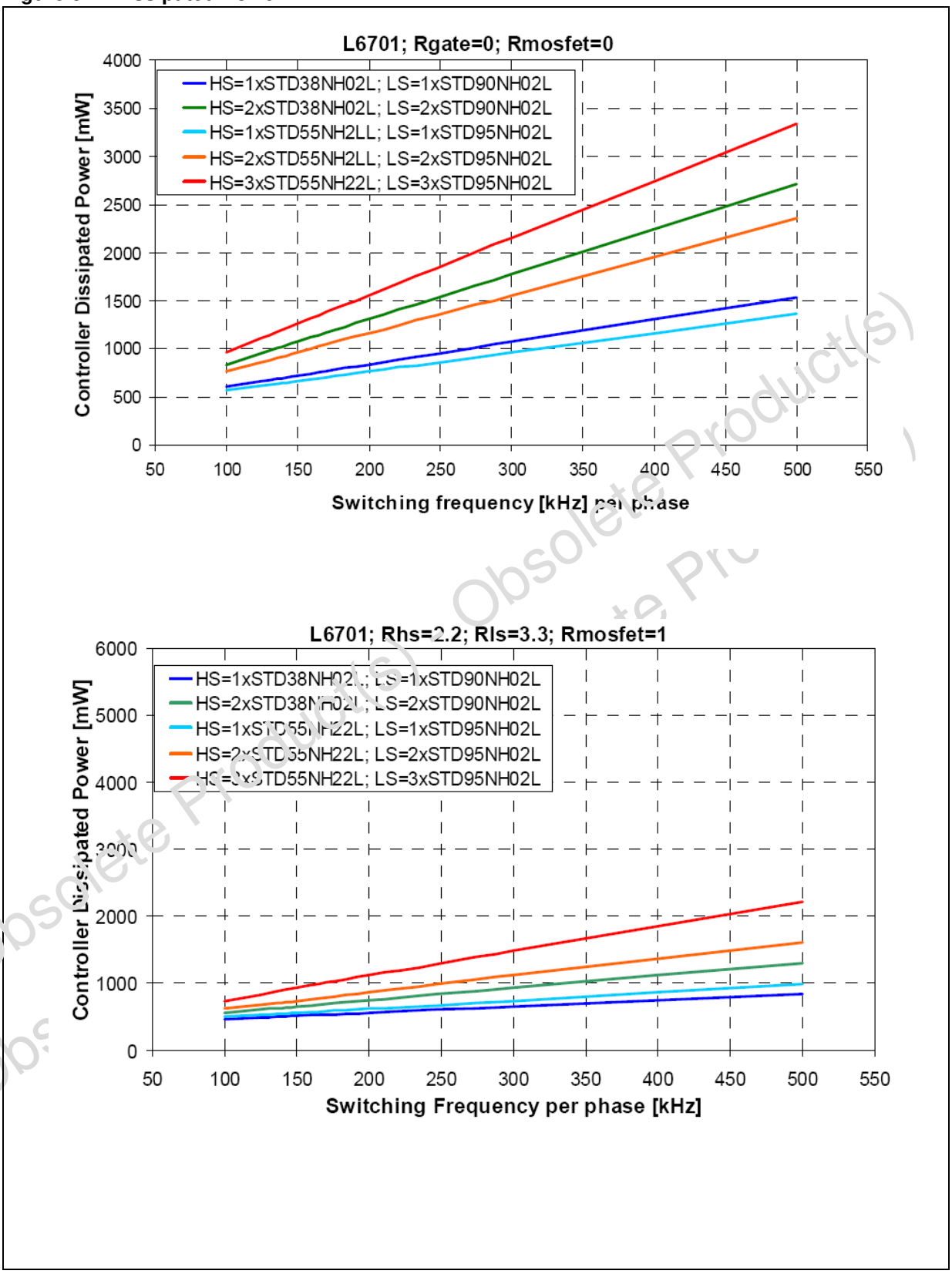
$$P_{DC} = V_{CC} \cdot (I_{CC} + 3 \cdot I_{CCDRx} + 3 \cdot I_{BOOTx})$$

- Drivers' power is the power needed by the driver to continuously switch on and off the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs (easy calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation. The total power dissipated to switch the MOSFETs results:

$$P_{SW} = 3 \cdot F_{SW} \cdot (Q_{GHS} \cdot V_{BOOT} + Q_{GLS} \cdot V_{CCDRx})$$

External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

Figure 5. Dissipated Power



9 Current Sharing Loop and Current Reading

9.1 Current Sharing Loop

L6701 embeds two separate Current Reading circuitries used to perform Current Sharing and OCP through ISENx pins and Voltage Positioning (Droop Function) through CS+ and CS- pins (See *Section 10*).

Current sharing control loop and connections are reported in *Figure 6*: the current read through the I_{SENx} pins is converted into a current I_{INFOx} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / 3$ is internally built into the device. The error between the read current I_{INFOx} and the reference I_{AVG} is then converted into a voltage that with a proper gain is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

9.2 Current Reading for Current Sharing

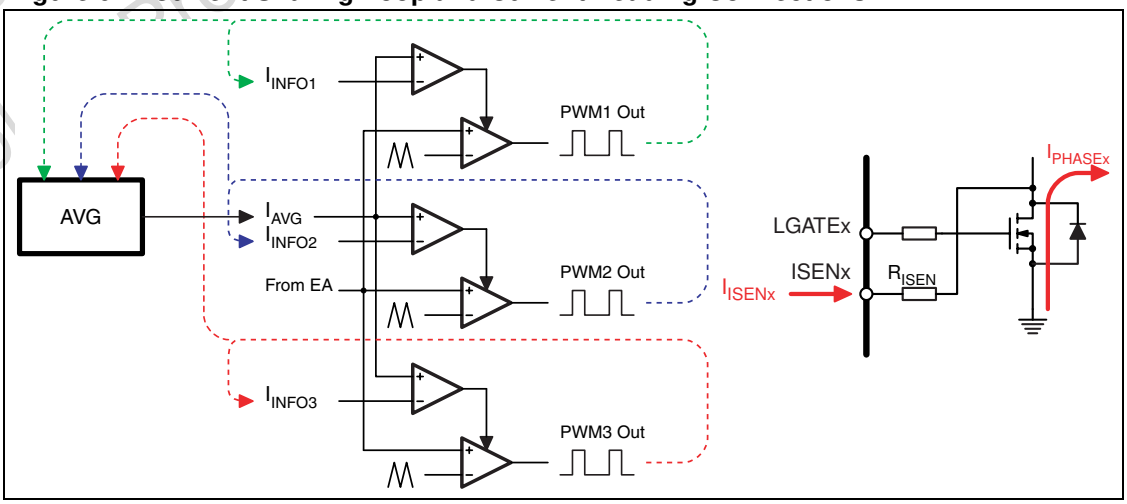
The current flowing trough each phase is read using the voltage drop across the low side MOSFETs $R_{DS(on)}$ or across a sense resistor in its series and it is internally converted into a current. The trans-conductance ratio is issued by the external resistor R_{ISEN} placed outside the chip between I_{SENx} and the reading point (usually the LS MOSFET Drain).

The current sense circuit tracks the current information for a time T_{TRACK} centered in the middle of the LS conduction time and holds the tracked information during the rest of the period. The current that flows from the I_{SENx} pin is the current information used by the device to perform current sharing and OCP and it is given by:

$$I_{ISENx} = \frac{R_{dsON}}{R_{ISEN}} \cdot I_{PHASEx} = I_{INFOx}$$

where $R_{DS(on)}$ is the ON resistance of the low side MOSFET and R_{ISEN} is the trans-conductance resistor connected between the ISENx pins and the LS Drain; I_{PHASEx} is the current carried by the relative phase and I_{INFOx} is the current information signal reproduced internally. R_{ISENx} is designed according to the Over Current Protection: see *Section 13.6* for details.

Figure 6. Current Sharing Loop and Current Reading Connections



10 Output Voltage Positioning

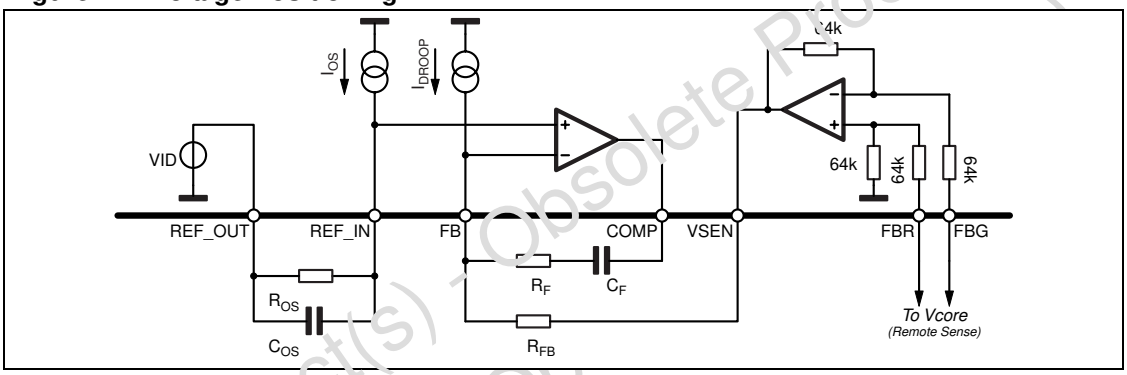
Output voltage positioning is performed by selecting the reference DAC and by programming the Droop Function and Offset to the reference (See *Figure 7*). The current (I_{DROOP}) sourced from the FB pin, directly proportional to the read current, causes the output voltage to vary according to the external R_{FB} resistor so implementing the desired load-line resistance. The current (I_{OS}) sourced from the REF_IN pin causes the reference voltage to be offset according to the resistance R_{FB} connected.

The output voltage is then driven by the following relationship:

$$V_{OUT} = VID + R_{OS} \cdot I_{OS} - R_{FB} \cdot I_{DROOP}$$

Both DROOP and OFFSET function can be disabled: see *Section 10.1* and *Section 10.3* for details.

Figure 7. Voltage Positioning



10.1 Load-Line (Droop Function - Optional)

This method "recovers" part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current: a static error proportional to the output current causes the output voltage to vary according to the sensed current.

Figure 8 shows the typical Current-Sense Circuit used to implement the Droop-Function in low-cost application (saves component count). The current flowing across the three inductors is read through the R_{PH} - C_{PH} filter across CS+ and CS- pins. R_D programs a trans-conductance gain and generates a current I_{CS} proportional to the average of the currents of the three phases. The current I_{CS} is then mirrored and, multiplied by three, sourced by the FB pin (I_{DROOP}). R_{FB} gives the final gain to program the desired load-line slope.

Considering the scheme reported on *Figure 8*, it is possible to observe that:

$$I_{CS} = \frac{I_{OUT}}{3} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R_{PH} \cdot C_{PH}/3} \cdot \frac{DCR}{R_D}$$

Time constant matching between the inductor (L / DCR) and the current reading filter ($R_{PH} \cdot C_{PH}/3$) is required to implement a real equivalent output impedance of the system so avoiding over and/or under shoot of the output voltage as a consequence of a load transient. It results:

$$\frac{L}{DCR} = \frac{R_{PH} \cdot C_{PH}}{3} \Rightarrow I_{CS} = \frac{I_{OUT}}{3} \cdot \frac{DCR}{R_D}$$

The device forces $I_{DROOP} = I_{CS}x3$, proportional to the read current, into the feedback resistor R_{FB} implementing the load regulation dependence. The output characteristic vs. load current is then given by (Offset disabled):

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_D} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

Where R_{LL} is the resulting load-line resistance implemented by the system.

The whole power supply can be then represented by a "real" voltage generator with an equivalent output resistance R_{LL} and a voltage value of VID.

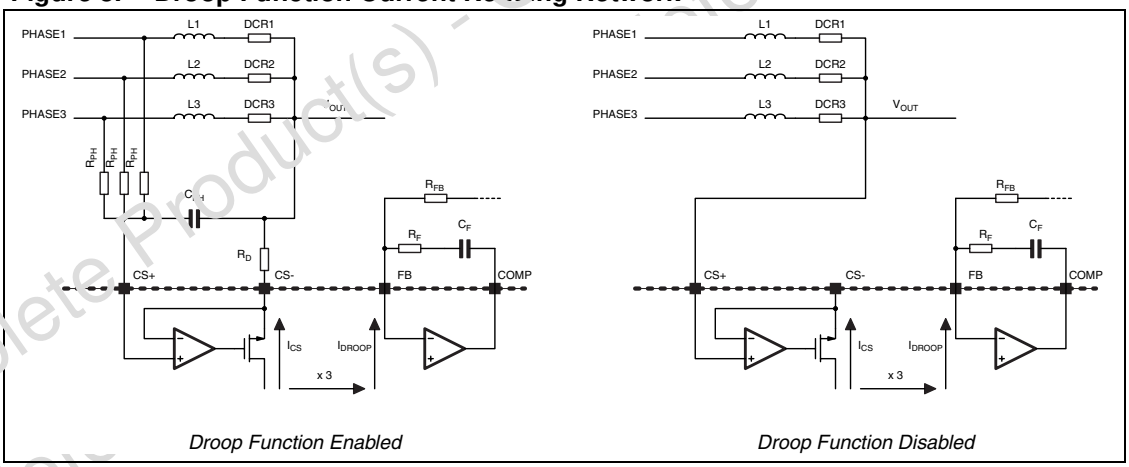
R_{FB} resistor can be then designed according to the R_{LL} specifications as follow:

$$R_{FB} = R_{LL} \cdot \frac{R_D}{DCR}$$

where R_D is typically designed to have I_{CS} = 35µA at the maximum output current (OCP).

Caution: Droop function is optional, in case it is not desired, the Current Sense circuit can be modified so that the device always read a null current (See *Figure 8*). To do this, it is enough to connect CS+ directly to the output voltage leaving CS- unconnected. The reaction will keep CS+ and CS- at the same voltage, always reading a null current and also assuring the FB disconnection protection to be effective.

Figure 8. Droop Function Current Reading Network



10.2 Fully-Differential Load-Line (Droop Function - Optional)

Fully-Differential current-reading for voltage-positioning allows the designer to save time in the application fine-tuning since the BOM so obtained becomes layout-independent. The patent-pending topology offered by L6701 allow implementing fully-differential current-sense still using only two current-sense pins (CS+ and CS-). *Figure 9* shows the typical Current-Sense Circuit used to implement the Fully-Differential Droop-Function. The current flowing across the three inductors is read through an R_{PH} - C_{PH} filter for each phase as well as an R_D is required for each phase to program the trans-conductance-gain. As previously mentioned, a current I_{CS} proportional to the average of the currents of the three phases is internally generated, mirrored

and, multiplied by three, sourced by the FB pin (I_{DROOP}). R_{FB} gives the final gain to program the desired load-line slope.

As before, the voltage positioning equations results (See *Figure 9*):

$$I_{CS} = I_{OUT} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R_{PH} \cdot C_{PH}} \cdot \frac{DCR}{R_D}$$

As a consequence:

$$\frac{L}{DCR} = R_{PH} \cdot C_{PH} \Rightarrow I_{CS} = I_{OUT} \cdot \frac{DCR}{R_D}$$

The device forces $I_{DROOP} = I_{CS}x3$, proportional to the read current, into the feedback resistor R_{FB} implementing the load regulation dependence. The output characteristic vs. load current is then given by (Offset disabled):

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - 3 \cdot R_{FB} \cdot \frac{DCR}{R_D} \cdot I_{OUT} = VID - R_{LLDIFF} \cdot I_{OUT}$$

Where R_{LLDIFF} is the resulting differential load-line resistance implemented by the system. The whole power supply can be then represented by a "real" voltage generator with an equivalent output resistance R_{LLDIFF} and a voltage value of VID.

R_{FB} resistor can be then designed according to the Load-Line (R_{LLDIFF}) specifications as follow:

$$R_{FB} = \frac{R_{LLDIFF}}{3} \cdot \frac{R_D}{DCR}$$

where R_D is typically designed to have I_{CS} = 35µA at the maximum output current (OCP).

Table 9 contains a quick-reference guide to design applications with typical and/or differential current sense.

Figure 9. Fully Differential Load-Line Current-Reading (pat. pend.)

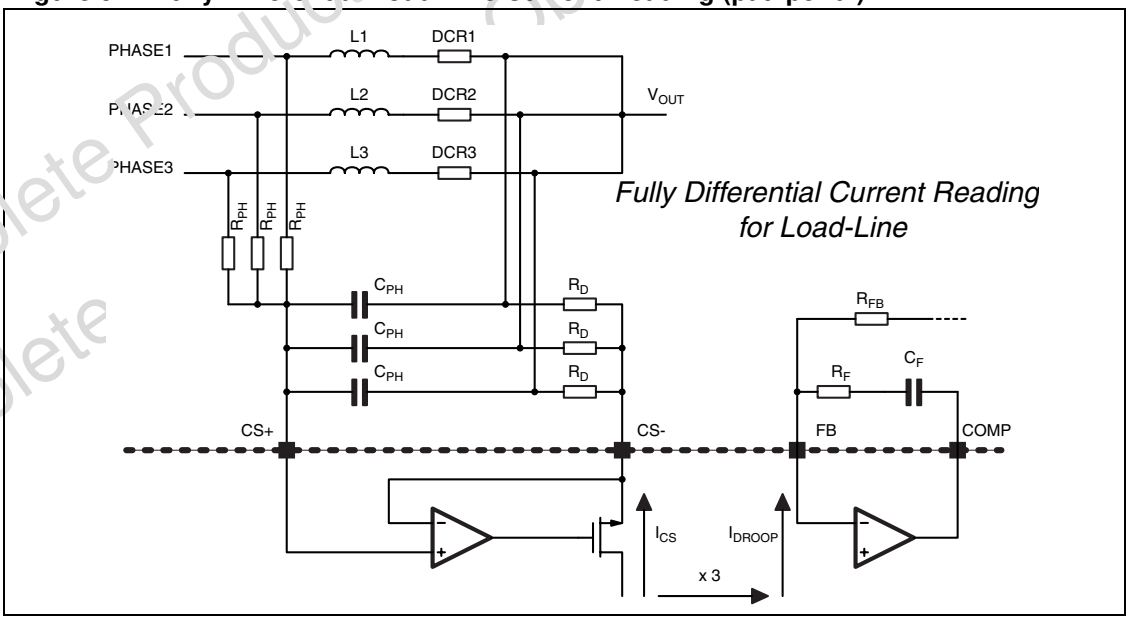


Table 9. Comparison between different load-line implementations.

	Fully-Differential LL	Non-Fully-Differential LL
Layout-insensitive BOM	Y	N
Time-Constant Matching	$\frac{L}{DCR} = R_{PH} \cdot C_{PH}$	$\frac{L}{DCR} = \frac{R_{PH} \cdot C_{PH}}{3}$
R_D Design (given OCP th.)	$R_D = OCP \cdot \frac{DCR}{35\mu}$	$R_D = \frac{OCP}{3} \cdot \frac{DCR}{35\mu}$
R_{FB} Design (given R_{LL})	$R_{FB} = \frac{R_{LL}}{3} \cdot \frac{R_D}{DCR}$	$R_{FB} = R_{LL} \cdot \frac{R_D}{DCR}$
R_{LL} (given R_D and R_{FB})	$R_{LL} = 3 \cdot \frac{DCR}{R_D} \cdot R_{FB}$	$R_{LL} = \frac{DCR}{R_D} \cdot R_{FB}$

10.3 Offset (Optional)

Positive offset can be added to the programmed reference by connecting a R_{OS} resistor between the REF_OUT and REF_IN pins. Referring to *Figure 7*, a constant current (I_{OS}=11.5µA) is sourced from the REF_IN pin as soon as the device is enabled, so programming a fixed voltage drop across R_{CS}: this voltage is directly added to the programmed reference giving the desired offset to the output voltage as follow:

$$V_{OS} = R_{OS} \cdot I_{OS}$$

Offset current is suddenly sourced from REF_IN pin as soon as the device implements Soft-Start: to avoid having steps during soft-start, the introduction of C_{OS} (in parallel to R_{OS}) is required. The resulting time constant need to be negligible with respect to the soft-start time as well as long enough to smooth the initial step. Typical values are in the range of few hundreds of nF.

Offset function can be easily disabled simply setting R_{OS} = 0.

Caution: Offset automatically given by the DAC selection differs from the offset implemented through the OFFSET pin: the built-in feature is trimmed in production and assures ±0.7% accuracy over load and line variations.

10.4 Remote Voltage Sense

L6701 embeds a Remote Sense Buffer to sense remotely the regulated voltage without any additional external components. In this way, the output voltage programmed is regulated between the remote buffer inputs compensating motherboard or connector losses. The device senses the output voltage remotely through the pins FBR and FBG (FBR is for the regulated voltage sense while FBG is for the ground sense) and reports this voltage internally at VSEN pin with unity gain eliminating the errors. Keeping the FBR and FBG traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

10.5 Maximum Duty Cycle limitation

To provide proper time for current-reading in order to equalize the current carried by each phase, the device implements a duty-cycle limitation. This limitation is not fixed but it is linearly variable with the current delivered to the load as follow:

$$T_{ON(max)} = \begin{cases} 0.80 \cdot T_{SW} & I_{ISENx} = 0\mu A \\ 0.40 \cdot T_{SW} & I_{ISENx} = 35\mu A \end{cases}$$

Duty Cycle limitation is variable with the delivered current to provide fast load transient response at light load as well as assuring robust over-current protection.

Figure 10 shows the maximum output voltage that the device is able to regulate considering the T_{ON} limitation imposed by the previous relationship. If the desired output characteristic crosses the limited-T_{ON} maximum output voltage, the output resulting voltage will start to drop after the cross-point. In this case, the output voltage starts to decrease following the resulting characteristic (dotted in *Figure 10*) until UVP is detected or anyway until I_{ISENx} = 35µA.

Figure 10. Maximum Duty Cycle limitation