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L6706

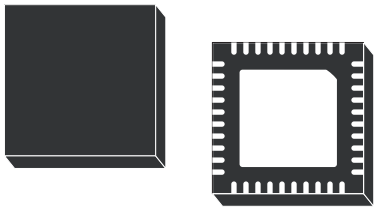
VR11.1 single phase controller with integrated driver

Features

- 8-bit programmable output up to 1.60000 V - Intel® VR11.1 DAC
- High current embedded driver
- High output voltage accuracy
- Programmable droop function
- Imon output
- Load transient boost LTB Technology™ to minimize the number of output capacitors
- Full differential current sense across inductor
- Differential remote voltage sensing
- Adjustable voltage offset
- LSLess startup to manage pre-biased output
- Feedback disconnection protection
- Preliminary overvoltage protection
- Programmable overcurrent protection
- Programmable overvoltage protection
- Adjustable switching frequency
- SSEND and OUTEN signal
- VFQFPN-40 6x6 mm package with exp. pad

Applications

- VTT and VAXG rails
- CPU power supply
- High density DC/DC converters



VFQFPN-40 6 x 6 mm

Description

The device implements a single phase step-down controller with integrated high current driver in a compact 6x6 mm body package with exposed pad.

The device embeds VR11.x DACs: the output voltage ranges up to 1.60000 V managing D-VID with high output voltage accuracy over line and temperature variations.

Imon capability guarantee full compatibility with VR11.1 enabling additional power saving technique.

Programmable droop function allows to supply all the latest Intel CPU rails.

Load transient boost LTB Technology™ reduces system cost by providing the fastest response to load transition.

The controller assures fast protection against load over current and under / over voltage. Feedback disconnection prevents from damaging the load in case of disconnections in the system board.

In case of over-current, the system works in constant current mode until UVP.

Table 1. Device summary

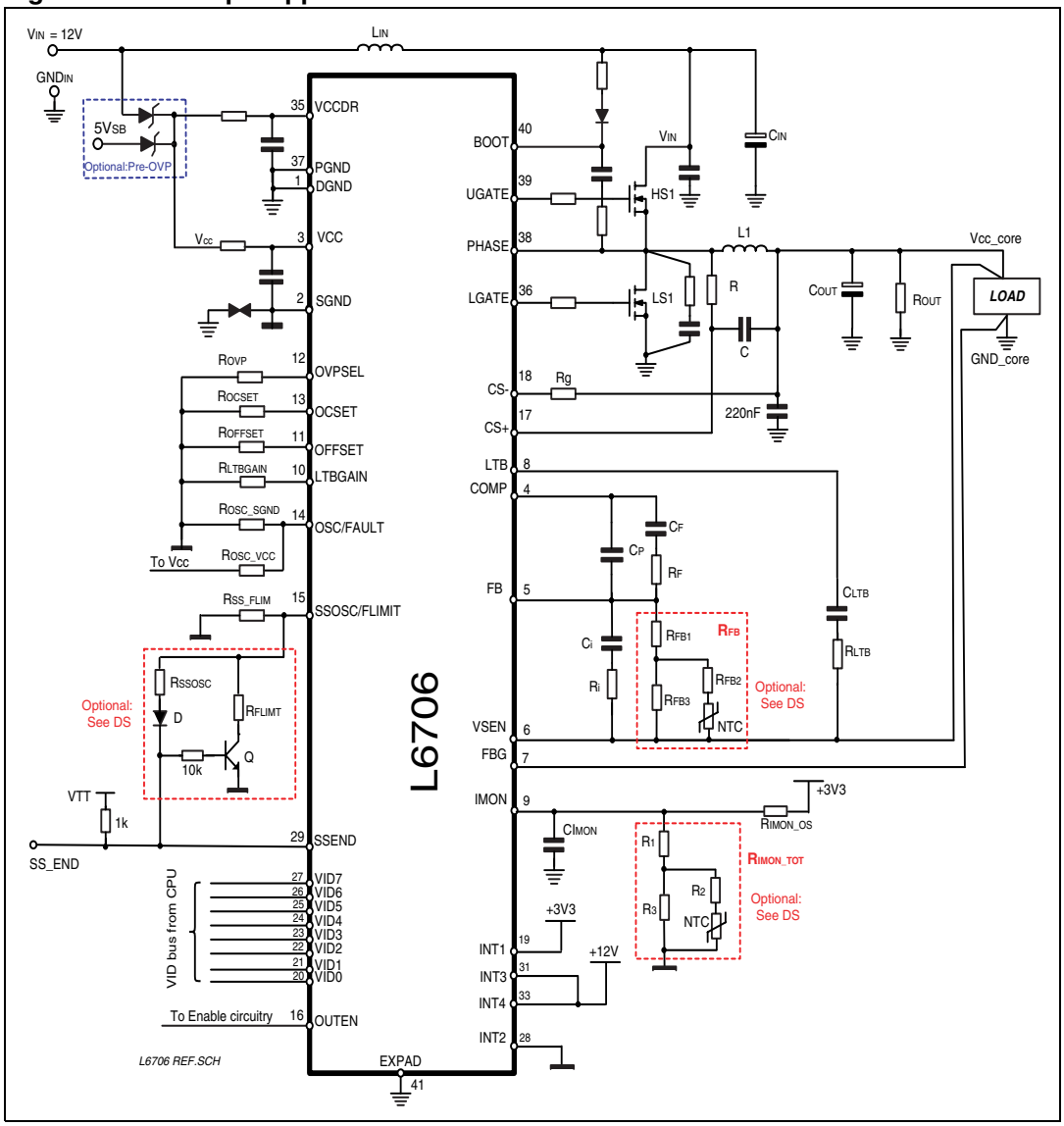
Order codes	Package	Packing
L6706	VFQFPN-40	Tray
L6706TR		Tape and reel

Contents

1 Principle application circuit and block diagram

1.1 Principle application circuit

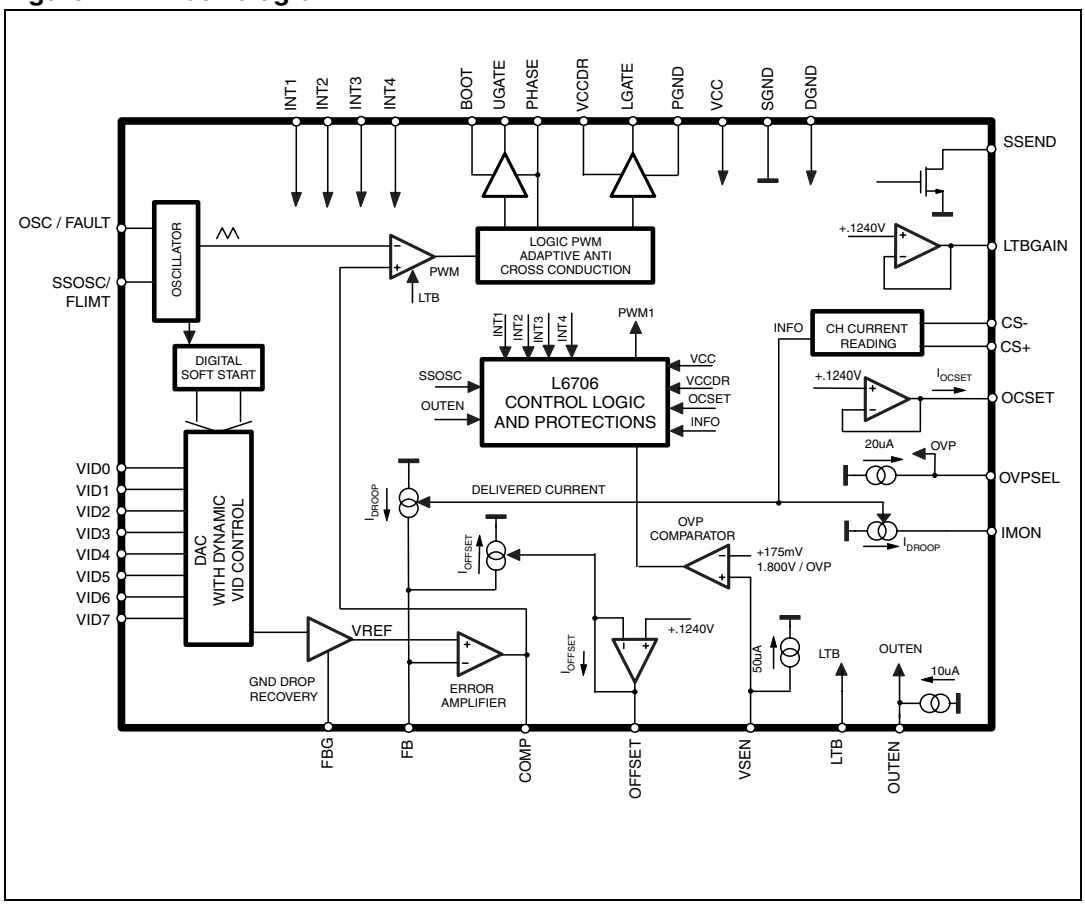
Figure 1. Principle application circuit [a]



a. Refer to the application note for the reference schematic.

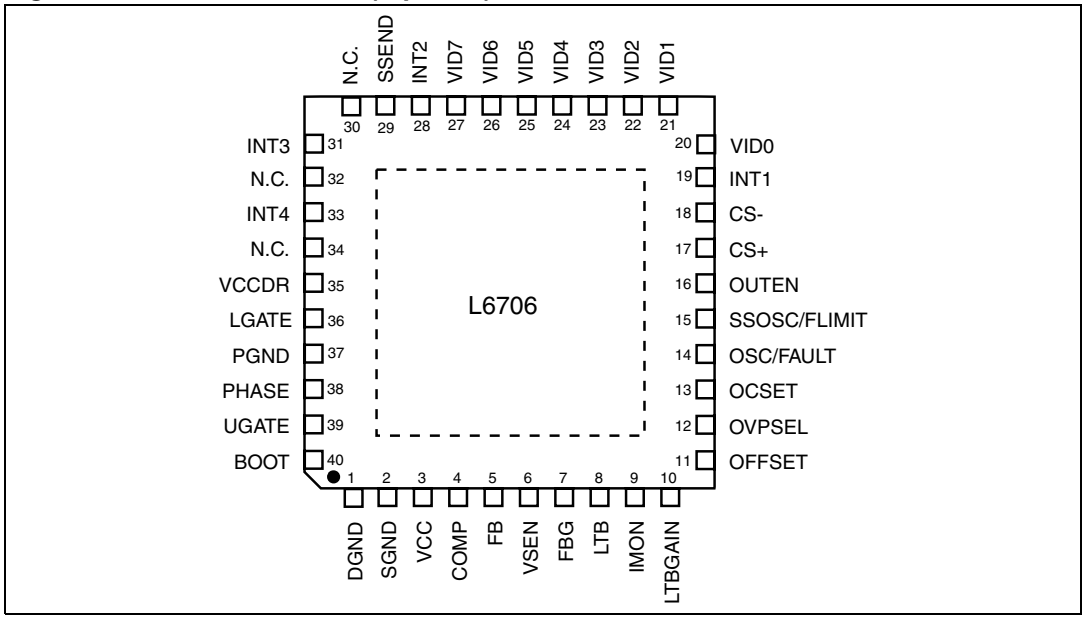
1.2 Block diagram

Figure 2. Block diagram



2 Pins description and connection diagrams

Figure 3. Pins connection (top view)



2.1 Pin description

Table 2. Pin description

N°	Name	Description
1	DGND	Digital GND. It must be connected to PGND (power ground).
2	SGND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
3	VCC	Device supply voltage pin. The operative supply voltage is 12 V ±15%. Filter with 1 x 1 µF MLCC capacitor vs. SGND.
4	COMP	Error amplifier output. Connect with an R_F - C_F//C_P vs. FB pin. The device cannot be disabled by pulling down this pin.
5	FB	Error amplifier inverting input pin. Connect with a resistor R_{FB} vs. VSEN and with an R_F - C_F//C_P vs. COMP pin. A current proportional to the load current is sourced from this pin in order to implement the droop effect. *See "Droop function" Section* for details.
6	VSEN	Output voltage monitor, manages OVP/UVP protections and FB disconnection. Connect to the positive side of the load to perform remote sense. *See "Layout guidelines" Section* for proper layout of this connection.
7	FBG	Connect to the negative side of the load to perform remote sense. *See "Layout guidelines" Section* for proper layout of this connection.

Table 2. Pin description (continued)

N°	Name	Description
8	LTB	Load transient boost pin. Internally fixed at 2 V, connecting a R_{LTB} - C_{LTB} vs. V_{OUT} allows to enable the load transient boost technology™: as soon as the device detects a transient load it turns on the PHASE. Short to SGND to disable the function. *See "Load transient boost technology" Section* for details.
9	IMON	Current monitor output pin. A current proportional to the load current is sourced from this pin. Connect through a resistor R_{MON} to SGND (or FBG) to implement a load indicator. The pin voltage is clamped to 1.1 V max.
10	LTBGAIN	Load transient boost technology™ gain pin. Internally fixed at 1.24 V, connecting a $R_{LTBGAIN}$ resistor vs SGND allows setting the GAIN of the LTB action. See *See "Load transient boost technology" Section* for details.
11	OFFSET	Offset programming pin. Internally fixed at 1.240 V, connecting a R_{OFFSET} resistor vs. SGND allows setting a current that is mirrored into FB pin in order to program a positive offset according to the selected R_{FB}. Short to SGND to disable the function. *See "Offset (optional)" Section* for details.
12	OVPSEL	Over voltage programming pin. Internally pulled up by 20 µA (min) to 3.3 V. Leave floating to use built-in protection thresholds (OVP_{TH}= VID + 175 mV typ). Connect to SGND through a R_{OVP} resistor and filter with 100 pF (max) to set the OVP threshold to a fixed voltage according to the R_{OVP} resistor. *See "Over voltage and programmable OVP" Section* for details.
13	OCSET	Over current setting, psi action pin. Connect to SGND through a R_{OCSET} resistor to set the OCP threshold. *See "Overcurrent protection" Section* for details.
14	OSC/ FAULT	Oscillator, fault pin. It allows programming the switching frequency F_{SW}. Frequency is programmed according to the resistor connected from the pin vs. SGND or VCC with a gain of 9.1 kHz/µA (see relevant section for details). Leaving the pin floating programs a switching frequency of 200 kHz. The pin is forced high (3.3 V typ) to signal an OVP/UVP fault: to recover from this condition, cycle VCC or the OUTEN pin. *See "Oscillator" Section* for details.
15	SSOSC/ FLIMIT	Soft-start oscillator pin. By connecting a resistor R_{SS} to GND, it allows programming the soft-start time. Soft-start time T_{SS} will proportionally change with a gain of 25 [µs / kΩ]. The same slope implemented to reach V_{BOOT} has to be considered also when the reference moves from V_{BOOT} to the programmed VID code. The pin is kept to a fixed 1.240 V. *See "Soft-start" Section* for details. It also allows to select maximum LTB frequency. *See "Load transient boost technology" Section*for details.

Table 2. Pin description (continued)

N°	Name	Description
16	OUTEN	Output enable pin. Internally pulled up by 10 µA (typ) to 3 V. Forced low, the device stops operations with all MOSFETs OFF: all the protections are disabled except for preliminary over voltage. Leave floating, the device starts-up implementing soft-start up to the selected VID code. Cycle this pin to recover latch from protections; filter with 1 nF (typ) vs. SGND.
17	CS+	Current sense positive input. Connect through an R-C filter to the phase-side of the output inductor. See *Section 20: Layout guidelines on page 43* for proper layout of this connection.
18	CS-	Current sense negative input. Connect through a Rg resistor to the output-side of the output inductor. See *Section 20: Layout guidelines on page 43* for proper layout of this connection.
19	INT1	Test mode pin. It must be left unconnected or connected to 3.3 V.
20 to 27	VID0 to VID7	Voltage identification pins. (not internally pulled up). Connect to SGND to program a '0' or connect to the external Pull-up resistor to program a '1'. They allow programming output voltage as specified in *Table 7.*
28	INT2	Test mode pin. It must be connected to SGND.
29	SSEND	Soft-start end signal. Open drain output sets free after SS has finished and pulled low when triggering any protection. Pull up to a voltage lower than 3.3 V, if not used it can be left floating.
30	N.C.	Not internally connected.
31	INT3	Test mode pin. It must be connected to 12 V.
32	N.C.	Not internally connected.
33	INT4	Test mode pin. It must be connected to 12 V.
34	N.C.	Not internally connected.
35	VCCDR	LS driver supply. VCDDR pin voltage has to be the same of VCC pin. Filter with 1 x 1 µF MLCC capacitor vs. PGND.
36	LGATE	LS driver output. A small series resistor helps in reducing device-dissipated power.
37	PGND	Power ground pin (LS drivers return path). Connect to power ground plane.
38	PHASE	HS driver return path. It must be connected to the HS MOSFET source and provides return path for the HS driver.

Table 2. Pin description (continued)

N°	Name	Description
39	UGATE	HS driver output. It must be connected to the HS MOSFET gate. A small series resistors helps in reducing device-dissipated power.
40	BOOT	HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE and provide necessary Bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge.
PAD	Thermal PAD	Exposed pad connects the silicon substrate. As a consequence it makes a good thermal contact with the PCB to dissipate the power necessary to drive the external MOSFETs. Connect it to the power ground plane using 4.3 x 4.3 mm square area on the PCB and with nine vias, to improve thermal conductivity.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (Device soldered on 2s2p PC board)	35	°C / W
R_{thJC}	Thermal resistance junction to case	1	°C / W
T_{MAX}	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-10 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}, V_{CCDR}	To PGND	15	V
V_{BOOT}- V_{PHASE}	Boot voltage	15	V
V_{UGATE}- V_{PHASE}		15	V
	LGATE to PGND	-0.3 to Vcc+0.3	V
	All other pins to PGND	-0.3 to 3.6	V
V_{PHASE}	Negative peak voltage to PGND; T < 400 ns VCC = VCCDR = 12 V	-8	V
	Positive voltage to PGND VCC = VCCDR = 12 V	26	V
	Positive peak voltage to PGND; T < 200 ns VCC = VCCDR = 12 V	30	V
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “normal performance”	+/- 1750	V

3.2 Electrical characteristics

V_{CC} = 12 V ± 15%, T_J = 0 °C to 70 °C unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	UGATE and LGATE open; VCC = VBOOT = 12 V		23	27	mA
I_{CCDR}	VCCDR supply current	LGATE = OPEN, VCCDR = 12 V		5	7	mA
I_{BOOT}	BOOT supply current	UGATE = OPEN, PHASE to PGND; VCC = BOOT = 12 V		2	3	mA
Power-on						
$UVLO_{VCC}$	VCC turn-ON	VCC rising; VCCDR = VCC		3.7	4.0	V
	VCC turn-OFF	VCC falling; VCCDR = VCC	3.3	3.5		V
Oscillator and inhibit						
F_{OSC}	Initial accuracy	OSC = OPEN OSC = OPEN; T_J = 0 to 125 °C	180 175	200 200	220 225	kHz kHz
TD_1	SS delay time		1	1.5		ms
TD_2	SS TD_2 time	R_{SSOSC} = 20 kΩ		500		µs
TD_3	SS TD_3 time		50	200		µs
OUTEN	Output enable	Rising thresholds voltage	0.80	0.85	0.90	V
		Hysteresis		100		mV
	Output pull-up current	OUTEN to SGND		10		µA
ΔVosc	Ramp amplitude			1.5		V
FAULT	Voltage at pin OSC/FAULT	OVP and UVP Active		3.3		V
Reference and DAC						
K_{VID}	Output voltage accuracy	VID = 1.000 V to VID = 1.600 V FB = VOUT; FBG = GNDOUT	-0.5	-	0.5	%
		VID = 0.800 V to VID = 1.000 V FB = VOUT; FBG = GNDOUT	-5	-	+5	mV
		VID = 0.500 V to VID = 0.800 V FB = VOUT; FBG = GNDOUT	-8	-	+8	mV
V_{BOOT}	Boot voltage			1.081		V
VID_{IH}	VID thresholds	Input low			0.35	V
VID_{IL}		Input high	0.8			V
Error amplifier						
A_0	EA DC gain			130		dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SR	EA slew-rate	COMP = 10 pF to SGND		25		V/µs
Differential current sensing and offset						
V_{OCSET}	OCSET pin voltage		1.120	1.260	1.400	mV
K_{IDROOP}	Droop current deviation from nominal value	Rg = 1 kΩ; I_{DROOP} = 25 µA;	-2	-	+2	µA
$K_{IOFFSET}$	Offset current accuracy	I_{OFFSET} = 50 µA to 250 µA	-5	-	5	%
I_{OFFSET}	OFFSET current range		0		250	µA
V_{OFFSET}	OFFSET pin bias	I_{OFFSET} = 0 to 250 µA		1.240		V
Gate drivers						
$t_{RISE\ UGATE}$	High side rise time	BOOT-PHASE = 12 V; C_{UGATE} to PHASE = 3.3 nF		20		ns
I_{UGATE}	High side source current	BOOT-PHASE = 12 V		1.5		A
R_{UGATE}	High side sink resistance	BOOT-PHASE = 12 V		1.8		Ω
$t_{RISE\ LGATE}$	Low side rise time	VCCDR = 12 V; C_{LGATE} to PGND = 5.6 nF		25		ns
I_{LGATE}	Low side source current	VCCDR = 12 V		2		A
R_{LGATE}	Low side sink resistance	VCCDR = 12 V		1.2		Ω
Protections						
OVP	Over voltage protection (VSEN rising)	Before V_{BOOT}		1.24	1.300	V
		Above VID (after TD_3)	150	175	200	mV
Programmable OVP	I_{OVP} current	OVP = SGND	20	22	24	µA
	Comparator offset voltage	OVP = 1.800 V	-20	0	20	mV
Pre-OVP	Preliminary over voltage protection	$UVLO_{OVP}$ < VCC < $UVLO_{VCC}$ VCC> $UVLO_{VCC}$ and OUTEN = SGND VSEN rising	1.750	1.800	1.850	V
		Hysteresis		350		mV
UVP	Under voltage threshold	VSEN falling; below VID	550	600	650	mV
V_{SSEND}	SS_END voltage low	I = -4 mA			0.4	V

4 Voltage identifications

Table 6. Voltage Identification (VID) mapping Intel VR11.x

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
800 mV	400 mV	200 mV	100 mV	50 mV	25 mV	12.5 mV	6.25 mV

Table 7. Voltage Identification (VID) Intel VR11.x(1)

HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)
0	0	OFF	4	0	1.21250	8	0	0.81250	C	0	0.41250
0	1	OFF	4	1	1.20625	8	1	0.80625	C	1	0.40625
0	2	1.60000	4	2	1.20000	8	2	0.80000	C	2	0.40000
0	3	1.59375	4	3	1.19375	8	3	0.79375	C	3	0.39375
0	4	1.58750	4	4	1.18750	8	4	0.78750	C	4	0.38750
0	5	1.58125	4	5	1.18125	8	5	0.78125	C	5	0.38125
0	6	1.57500	4	6	1.17500	8	6	0.77500	C	6	0.37500
0	7	1.56875	4	7	1.16875	8	7	0.76875	C	7	0.36875
0	8	1.56250	4	8	1.16250	8	8	0.76250	C	8	0.36250
0	9	1.55625	4	9	1.15625	8	9	0.75625	C	9	0.35625
0	A	1.55000	4	A	1.15000	8	A	0.75000	C	A	0.35000
0	B	1.54375	4	B	1.14375	8	B	0.74375	C	B	0.34375
0	C	1.53750	4	C	1.13750	8	C	0.73750	C	C	0.33750
0	D	1.53125	4	D	1.13125	8	D	0.73125	C	D	0.33125
0	E	1.52500	4	E	1.12500	8	E	0.72500	C	E	0.32500
0	F	1.51875	4	F	1.11875	8	F	0.71875	C	F	0.31875
1	0	1.51250	5	0	1.11250	9	0	0.71250	D	0	0.31250
1	1	1.50625	5	1	1.10625	9	1	0.70625	D	1	0.30625
1	2	1.50000	5	2	1.10000	9	2	0.70000	D	2	0.30000
1	3	1.49375	5	3	1.09375	9	3	0.69375	D	3	0.29375
1	4	1.48750	5	4	1.08750	9	4	0.68750	D	4	0.28750
1	5	1.48125	5	5	1.08125	9	5	0.68125	D	5	0.28125
1	6	1.47500	5	6	1.07500	9	6	0.67500	D	6	0.27500
1	7	1.46875	5	7	1.06875	9	7	0.66875	D	7	0.26875
1	8	1.46250	5	8	1.06250	9	8	0.66250	D	8	0.26250
1	9	1.45625	5	9	1.05625	9	9	0.65625	D	9	0.25625

Table 7. Voltage Identification (VID) Intel VR11.x[1] (continued)

HEX code		Output voltage [1]	HEX code		Output voltage [1]	HEX code		Output voltage [1]	HEX code		Output voltage [1]
1	A	1.45000	5	A	1.05000	9	A	0.65000	D	A	0.25000
1	B	1.44375	5	B	1.04375	9	B	0.64375	D	B	0.24375
1	C	1.43750	5	C	1.03750	9	C	0.63750	D	C	0.23750
1	D	1.43125	5	D	1.03125	9	D	0.63125	D	D	0.23125
1	E	1.42500	5	E	1.02500	9	E	0.62500	D	E	0.22500
1	F	1.41875	5	F	1.01875	9	F	0.61875	D	F	0.21875
2	0	1.41250	6	0	1.01250	A	0	0.61250	E	0	0.21250
2	1	1.40625	6	1	1.00625	A	1	0.60625	E	1	0.20625
2	2	1.40000	6	2	1.00000	A	2	0.60000	E	2	0.20000
2	3	1.39375	6	3	0.99375	A	3	0.59375	E	3	0.19375
2	4	1.38750	6	4	0.98750	A	4	0.58750	E	4	0.18750
2	5	1.38125	6	5	0.98125	A	5	0.58125	E	5	0.18125
2	6	1.37500	6	6	0.97500	A	6	0.57500	E	6	0.17500
2	7	1.36875	6	7	0.96875	A	7	0.56875	E	7	0.16875
2	8	1.36250	6	8	0.96250	A	8	0.56250	E	8	0.16250
2	9	1.35625	6	9	0.95625	A	9	0.55625	E	9	0.15625
2	A	1.35000	6	A	0.95000	A	A	0.55000	E	A	0.15000
2	B	1.34375	6	B	0.94375	A	B	0.54375	E	B	0.14375
2	C	1.33750	6	C	0.93750	A	C	0.53750	E	C	0.13750
2	D	1.33125	6	D	0.93125	A	D	0.53125	E	D	0.13125
2	E	1.32500	6	E	0.92500	A	E	0.52500	E	E	0.12500
2	F	1.31875	6	F	0.91875	A	F	0.51875	E	F	0.11875
3	0	1.31250	7	0	0.91250	B	0	0.51250	F	0	0.11250
3	1	1.30625	7	1	0.90625	B	1	0.50625	F	1	0.10625
3	2	1.30000	7	2	0.90000	B	2	0.50000	F	2	0.10000
3	3	1.29375	7	3	0.89375	B	3	0.49375	F	3	0.09375
3	4	1.28750	7	4	0.88750	B	4	0.48750	F	4	0.08750
3	5	1.28125	7	5	0.88125	B	5	0.48125	F	5	0.08125
3	6	1.27500	7	6	0.87500	B	6	0.47500	F	6	0.07500
3	7	1.26875	7	7	0.86875	B	7	0.46875	F	7	0.06875
3	8	1.26250	7	8	0.86250	B	8	0.46250	F	8	0.06250
3	9	1.25625	7	9	0.85625	B	9	0.45625	F	9	0.05625
3	A	1.25000	7	A	0.85000	B	A	0.45000	F	A	0.05000
3	B	1.24375	7	B	0.84375	B	B	0.44375	F	B	0.04375

Table 7. Voltage Identification (VID) Intel VR11.x[1] (continued)

HEX code		Output voltage [1]	HEX code		Output voltage [1]	HEX code		Output voltage [1]	HEX code		Output voltage [1]
3	C	1.23750	7	C	0.83750	B	C	0.43750	F	C	0.03750
3	D	1.23125	7	D	0.83125	B	D	0.43125	F	D	0.03125
3	E	1.22500	7	E	0.82500	B	E	0.42500	F	E	OFF
3	F	1.21875	7	F	0.81875	B	F	0.41875	F	F	OFF

1. According to INTEL specs, the device automatically regulates output voltage 19 mV lower to avoid any external offset to modify the built-in 0.5% accuracy improving TOB performances. Output regulated voltage is than what extracted from the table lowered by 19 mV.

5 Device description

L6706 is single phase PWM controller with embedded high current drivers providing complete control logic and protections for a high performance step-down DC-DC voltage regulator optimized for advanced microprocessor power supply.

L6706 is a dual-edge asynchronous PWM controller featuring load transient boost LTB Technology™: the device turns on the phase as soon as a load transient is detected allowing to minimize system cost by providing the fastest response to load transition. Load transition is detected (through LTB pin) measuring the derivate dV/dt of the output voltage and the dV/dt can be easily programmed extending the system design flexibility. Moreover, load transient boost (LTB) Technology™ gain can be easily modified in order to keep under control the output voltage ring back.

LTB Technology™ can be disabled and in this condition the device works as a dual-edge asynchronous PWM.

L6706 permits easy system design by allowing current reading across inductor in fully differential mode. Also a sense resistor in series to the inductor can be considered to improve reading precision.

The controller allows compatibility with both Intel VR11.0 and VR11.1 processors specifications, also performing D-VID transitions accordingly.

The device is VR11.1 compatible implementing IMON signal.

Low-side-less startup allows soft-start over pre-biased output avoiding dangerous current return through the main inductor as well as negative spike at the load side.

L6706 provides a programmable over-voltage protection to protect the load from dangerous over stress, latching immediately by turning ON the lower driver and driving high the OSC/FAULT pin. Furthermore, preliminary OVP protection also allows the device to protect load from dangerous OVP when VCC is not above the UVLO threshold or OUTEN is low. The overcurrent protection is externally adjustable through a single resistor. The device keeps constant the peak of the inductor current ripple working in constant current mode until the latched UVP.

A compact 6 x 6 mm body VFQFPN-40 package with exposed thermal pad allows dissipating the power to drive the external MOSFET through the system board.

6 DAC and current reading

L6706 embeds VRD11.x DAC *(see Table 7)* that allows to regulate the output voltage with a tolerance of ±0.5% recovering from offsets and manufacturing variations.

The device automatically introduces a -19 mV (both VRD11.x) offset to the regulated voltage in order to avoid any external offset circuitry to worsen the guaranteed accuracy and, as a consequence, the calculated system TOB.

Output voltage is programmed through the VID pins: they are inputs of an internal DAC that is realized by means of a series of resistors providing a partition of the internal voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the voltage reference (i.e. the set-point of the error amplifier, V_{REF}).

L6706 embeds a flexible, fully-differential current sense circuitry that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows placing sensing element in different locations without affecting the measurement's accuracy.

Reading current across the inductor DCR, the current flowing trough phase is read using the voltage drop across the output inductor or across a sense resistor in its series and internally converted into a current. The trans-conductance ratio is issued by the external resistor Rg placed outside the chip between CS- pin toward the reading points.

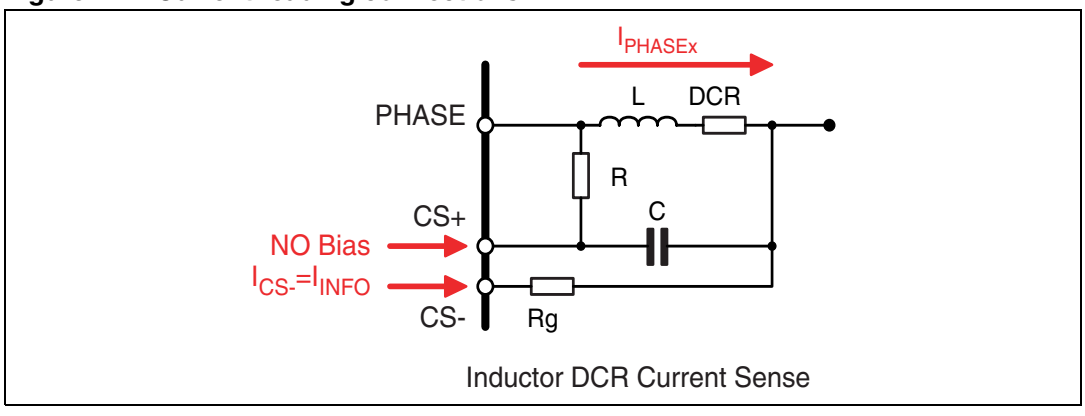
The current sense circuit always tracks the current information, no bias current is sourced from the CS+ pin: this pin is used as a reference keeping the CS- pin to this voltage. To correctly reproduce the inductor current an R-C filtering network must be introduced in parallel to the sensing element.

The current that flows from the CS- pin is then given by the following equation (see *Figure 4*):

$$I_{CS-} = \frac{DCR}{Rg} \cdot \frac{1 + s \cdot L/(DCR)}{1 + s \cdot R \cdot C} \cdot I_{PHASE}$$

Where I_{PHASE} is the current carried by the relative phase.

Figure 4. Current reading connections



Considering now to match the time constant between the inductor and the R-C filter applied (Time constant mismatches cause the introduction of poles into the current reading network

causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance), it results:

$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad I_{CS-} = \frac{DCR}{Rg} \cdot I_{PHASE} = I_{INFO} \Rightarrow \quad I_{INFO} = \frac{DCR}{Rg} \cdot I_{PHASE}$$

Where I_{INFO} is the current information reproduced internally.

The Rg trans-conductance resistor has to be selected using the following formula, in order to guarantee the correct functionality of internal current reading circuitry:

$$Rg = \frac{DCR^{MAX}}{20\mu A} \cdot I_{OUT}MAX$$

Where I_{OUT}^{MAX} is the maximum output current, DCR^{MAX} the maximum inductor DCR.

7 Differential remote voltage sensing

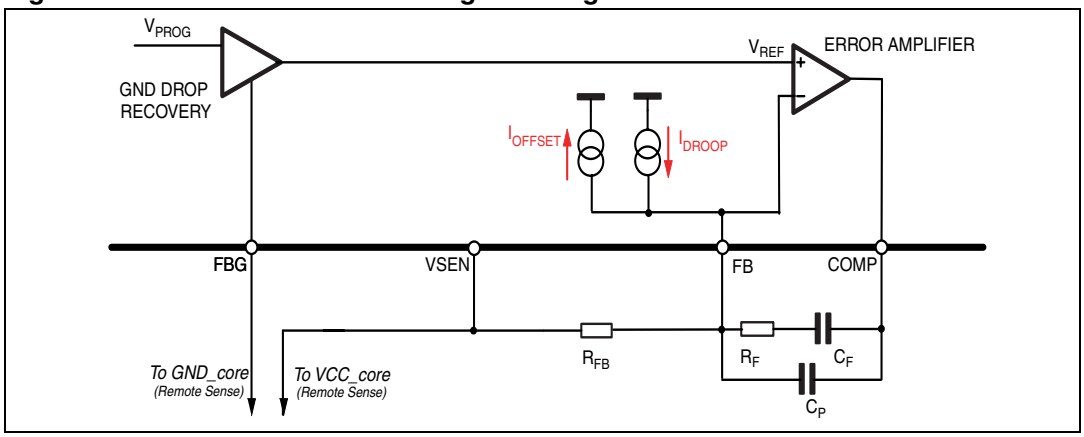
The output voltage is sensed in fully-differential mode between the FB and FBG pin.

The FB pin has to be connected through a resistor to the regulation point while the FBG pin has to be connected directly to the remote sense ground point.

In this way, the output voltage programmed is regulated between the remote sense point compensating motherboard or connector losses.

Keeping the FB and FBG traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Figure 5. Differential remote voltage sensing connections



8 Voltage positioning

Output voltage positioning is performed by selecting the internal reference value through VID pins and by programming the droop function and offset to the reference (see *Figure 6 on page 20*). The currents sourced/sunk from FB pin cause the output voltage to vary according to the external R_{FB}.

The output voltage is then driven by the following relationship:

$$V_{OUT}(I_{OUT}) = V_{PROG} - R_{FB} \cdot [I_{DROOP}(I_{OUT}) - I_{OFFSET}]$$

where:

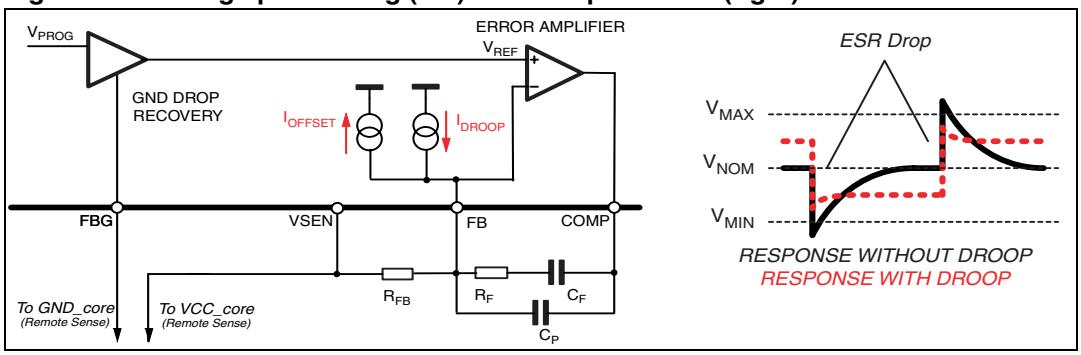
$$V_{PROG} = VID - 19mV$$

$$I_{DROOP}(I_{OUT}) = \frac{DCR}{Rg} \cdot I_{OUT}$$

$$I_{OFFSET} = \frac{1.240V}{R_{OFFSET}}$$

OFFSET function can be disabled shorting to SGND the OFFSET pin.

Figure 6. Voltage positioning (left) and droop function (right)



8.1 Offset (optional)

The OFFSET pin allows programming a positive offset (V_{OS}) for the output voltage by connecting a resistor R_{OFFSET} vs. SGND as shown in *Figure 7*; this offset has to be considered in addition to the one already introduced during the production stage (V_{PROG} = VID-19 mV).

OFFSET function can be disabled shorting to SGND the OFFSET pin.

The OFFSET pin is internally fixed at 1.240 V (*Table 5*) a current is programmed by connecting the resistor R_{OFFSET} between the pin and SGND: this current is mirrored and then properly sunk from the FB pin as shown in *Figure 7*. Output voltage is then programmed as follow:

$$V_{OUT}(I_{OUT}) = V_{PROG} - R_{FB} \cdot \left[I_{DROOP}(I_{OUT}) - \frac{1.240V}{R_{OFFSET}} \right]$$

where:

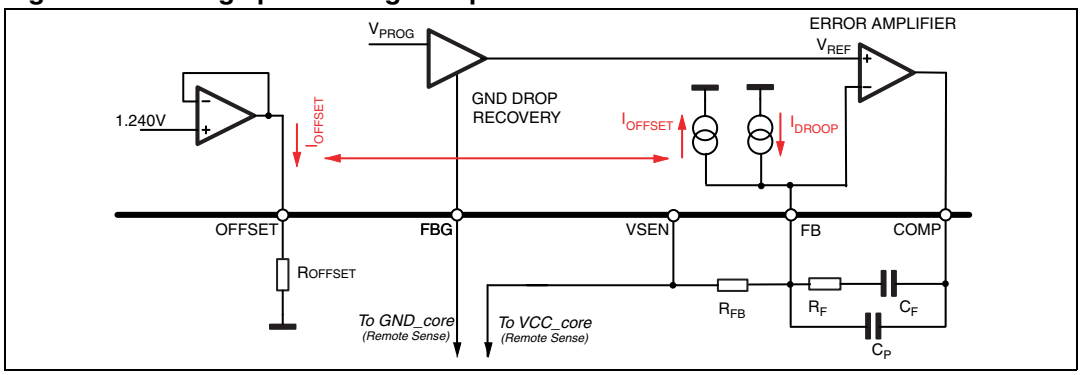
$$V_{OS} = R_{FB} \cdot \frac{1.240V}{R_{OFFSET}}$$

Offset resistor can be designed by considering the following relationship (RFB is fixed by the Droop effect):

$$R_{OFFSET} = R_{FB} \cdot \frac{1.240V}{V_{OS}}$$

Offset automatically given by the DAC selection differs from the offset implemented through the OFFSET pin: the built-in feature is trimmed in production and assures ±0.5% error over load and line variations

Figure 7. Voltage positioning with positive offset



8.2 Droop function

This method “recovers” part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current: a static error proportional to the output current causes the output voltage to vary according to the sensed current.

As shown in *Figure 6*, the ESR drop is present in any case, but using the droop function the total deviation of the output voltage is minimized. Moreover, more and more high-performance CPUs require precise load-line regulation to perform in the proper way. DROOP function is not then required only to optimize the output filter, but also becomes a requirement of the load.

The device forces a current I_{DROOP}, proportional to the read current, into the feedback R_{FB} resistor implementing the load regulation dependence. Since I_{DROOP} depends on the current information, the output characteristic vs. load current is then given by (neglecting the OFFSET voltage term):

$$V_{OUT} = V_{PROG} - R_{FB} \cdot I_{DROOP} = V_{REF} - R_{FB} \cdot \frac{DCR}{Rg} \cdot I_{OUT} = V_{PROG} - R_{DROOP} \cdot I_{OUT}$$

Where DCR is the inductor parasitic resistance (or sense resistor when used) and I_{OUT} is the output current of the system. The whole power supply can be then represented by a

"real" voltage generator with an equivalent output resistance R_{DROOP} and a voltage value of V_{PROG}. R_{FB} resistor can be also designed according to the R_{DROOP} specifications as follow:

$$R_{FB} = R_{DROOP} \cdot \frac{Rg}{DCR}$$

9 Droop thermal compensation

Current sense element (DCR inductor) has a non-negligible temperature variation. As a consequence, the sensed current is subjected to a measurement error that causes the regulated output voltage to vary accordingly (when droop function is implemented).

To recover from this temperature related error, NTC resistor can be added into feedback compensation network, as shown in *Figure 8.*

The output voltage is then driven by the following relationship (neglecting the OFFSET voltage term):

$$V_{OUT} = V_{PROG} - (R_{FB} \cdot I_{DROOP})$$

where R_{FB} is the equivalent feedback resistor and it depends on the temperature through NTC resistor.

Considering the relationships between I_{DROOP} and the I_{OUT}, the output voltage results:

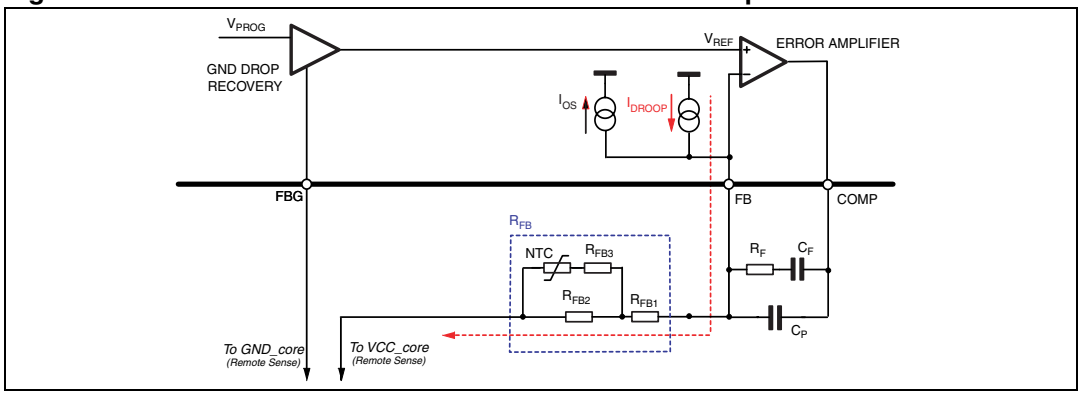
$$V_{OUT}[(T,I_{OUT})] = V_{PROG} - \left(R_{FB}[T] \cdot \frac{DCR[T]}{Rg} \cdot I_{OUT}\right)$$

where T is the temperature.

If the inductor temperature increases the DCR inductor increases and NTC resistor decreases. As a consequence the equivalent R_{FB} resistor decreases keeping constant the output voltage respect to temperature variation.

NTC resistor must be placed as close as possible to the sense element (phase inductor).

Figure 8. NTC connections for DC load line thermal compensation



10 Output current monitoring (IMON)

The device sources from IMON pin a current proportional to the load current (the sourced current is a copy of droop current).

Connect IMON pin through a R_{IMON} resistor to remote ground (GND Core) to implement a load indicator, as shown in *Figure 9*.

As INTEL VR11.1 specification required, on the IMON voltage as to be added a small positive offset to avoid under-estimation of the output load (due to elements accuracy).

The voltage across IMON pin is given by the following formula:

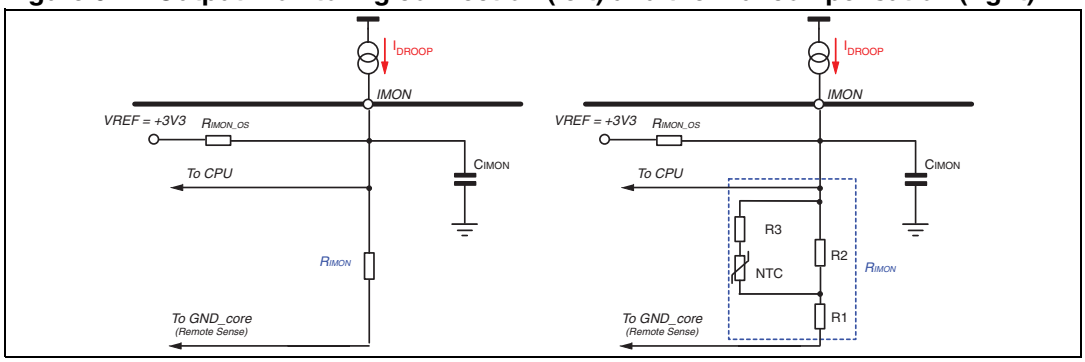
$$V_{MONITORING} = \frac{R_{IMON} \cdot R_{OS}}{R_{IMON} + R_{OS}} \cdot I_{DROOP} + V_{REF} \cdot \frac{R_{IMON}}{R_{IMON} + R_{OS}}$$

where:

$$I_{DROOP} = \frac{DCR}{Rg} \cdot I_{OUT}$$

The IMON pin voltage is clamped to 1.100 V max to preserve the CPU from excessive voltages as INTEL VR11.1 specification required.

Figure 9. Output monitoring connection (left) and thermal compensation (right)



Current sense element (DCR inductor) has a non-negligible temperature variation. As a consequence, the sensed current is subjected to a measurement error that causes the monitoring voltage to vary accordingly.

To recover from this temperature related error, NTC resistor can be added into monitoring network, as shown in *Figure 9.*

The monitoring voltage is then driven by the following relationship (neglecting the offset term for simplicity):

$$V_{MONITORING} = \frac{R_{IMON} \cdot R_{OS}}{R_{IMON} + R_{OS}} \cdot I_{DROOP} = \frac{R_{IMON} \cdot R_{OS}}{R_{IMON} + R_{OS}} \cdot \frac{DCR}{Rg} \cdot I_{OUT}$$

where now the R_{IMON} is the equivalent monitoring resistor and it depends on the temperature through NTC resistor.

Considering the relationships between I_{DROOP} and the I_{OUT}, the voltage results:

$$V_{MONITORING}[(T,I_{OUT})] = \frac{R_{IMON}[T] \cdot R_{OS}}{R_{IMON}[T] + R_{OS}} \cdot \frac{DCR[T]}{Rg} \cdot I_{OUT}$$

where T is the temperature.

If the inductor temperature increases the DCR inductor increases and NTC resistor decreases. As a consequence the equivalent R_{IMON} resistor decreases keeping constant the monitoring voltage respect to temperature variation. NTC resistor must be placed as close as possible to the sense element (phase inductor).